MIC5219

500 mA Peak Output LDO Regulator

Features

- 500 mA Output Current Capability
  - SOT23-5 Package - 500 mA Peak
  - 2 mm x 2 mm x 0.9 mm VDFN Package - 500 mA Continuous
  - 2 mm x 2 mm x 0.6 mm Thin DFN Package - 500 mA Continuous
  - MSOP-8 Package - 500 mA Continuous
- Low 500 mV Maximum Dropout Voltage at Full Load
- Extremely Tight Load and Line Regulation
- Tiny SOT-23-5 and Power MSOP-8 Package
- Ultra-Low Noise Output
- Low Temperature Coefficient
- Current and Thermal Limiting
- Reversed-Battery Protection
- CMOS/TTL-Compatible Enable/Shutdown Control
- Near-Zero Shutdown Current

Applications

- Laptop, Notebook, and Palmtop Computers
- Cellular Telephones and Battery-Powered Equipment
- Consumer and Personal Electronics
- PC Card V_{CC} and V_{PP} Regulation and Switching
- SMPS Post-Regulator/DC-to-DC Modules
- High-Efficiency Linear Power Supplies

General Description

The MIC5219 is an efficient linear voltage regulator with high peak output current capability, very low dropout voltage, and better than 1% output voltage accuracy. Dropout is typically 10 mV at light loads and less than 500 mV at full load.

The MIC5219 is designed to provide a peak output current for start-up conditions where higher inrush current is demanded. It features a 500 mA peak output rating. Continuous output current is limited only by package and layout.

The MIC5219 can be enabled or shut down by a CMOS- or TTL-compatible signal. When disabled, power consumption drops nearly to zero. Dropout ground current is minimized to help prolong battery life. Other key features include reversed-battery protection, current limiting, overtemperature shutdown, and low noise performance with an ultra-low noise option.

The MIC5219 is available in adjustable or fixed output voltages in the space-saving 6-pin (2 mm × 2 mm) VDFN, 6-pin (2 mm × 2 mm) Thin DFN, SOT23-5, and 8-pin power MSOP packages. For higher power requirements see the MIC5209 or MIC5237.

MIC5219

500 毫安峰值输出低压差线性稳压器

特性

- 500毫安输出电流能力 - SOT23-5
  封装 - 500毫安峰值输出 - 2毫米×2
  毫米×0.9毫米VDFN封装 - 500毫安连续输出
  - 2毫米×2毫米×0.6毫米超薄DFN封装 - 500毫安连续输出
  - MSOP-8封装 - 500毫安连续输出
- 满载时最大压降电压低至500毫伏
- 极其严格的负载稳压和线路稳压
- 微型SOT-23-5及功率型MSOP-8封装
- 超低噪声输出
- 低温度系数
- 电流及热量限制保护
- 反向电池保护功能
- CMOS/TTL兼容的使能/关断控制
- 近零关断电流

应用领域

- 笔记本电脑、手提电脑及掌上电脑
- 蜂窝电话及电池供电设备
- 消费类及个人电子产品
- PC卡 V_{CC}与 V_{PP}稳压及开关
- 开关电源后稳压器/DC-DC模块
- 高效线性电源

产品概述

MIC5219是一款高效线性稳压器，具备高峰值输出电流能力、极低压降电压及优于1%的输出电压精度。在轻载条件下，压降电压典型值为10 mV，满载时小于500 mV。

MIC5219专为启动时提供峰值输出电流设计，以满足较高涌入电流需求。其峰值输出电流额定值为500毫安。连续输出电流仅受封装和电路布局限制。

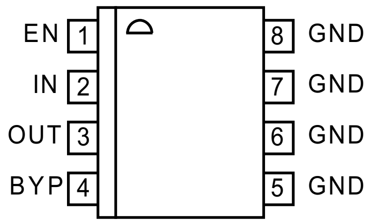
MIC5219可通过兼容CMOS或TTL的信号实现使能或关闭，关闭时功耗几乎为零。降低地电流以延长电池寿命。

其他主要特性包括反向电池保护、电流限制、过温关断以及低噪声性能，并提供超低噪声选项。

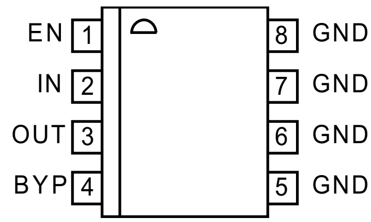
MIC5219 提供可调或固定输出电压，封装形式包括节省空间的6引脚（2 mm × 2 mm）VDFN、6引脚（2 mm × 2 mm）薄型DFN、SOT23-5及8引脚功率MSOP封装。如需更高功率，请参见 MIC5209 或 MIC5237。

Package Types

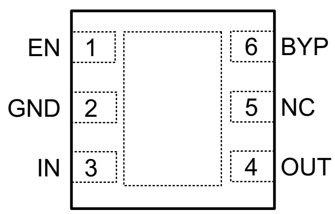
MIC5219-x.xYMM
MSOP-8 (MM)
Fixed Voltages
(Top View)



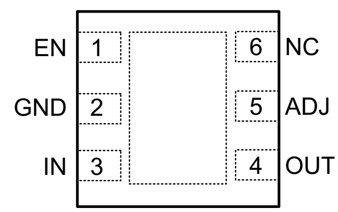
MIC5219YMM
MSOP-8 (MM)
Adjustable Voltages
(Top View)



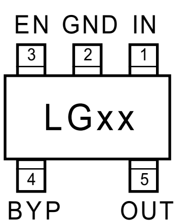
MIC5219-x.xYML
6-Pin VDFN (ML)
(Top View)



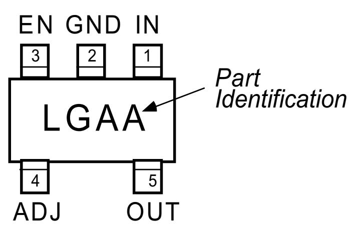
MIC5219YMT
6-Pin TDFN (MT)
(Top View)



MIC5219-x.xYM5
SOT23-5 (M5)
Fixed Voltages
(Top View)

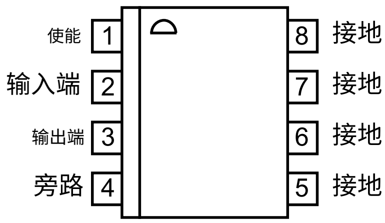


MIC5219YM5
SOT23-5 (M5)
Adjustable Voltage
(Top View)

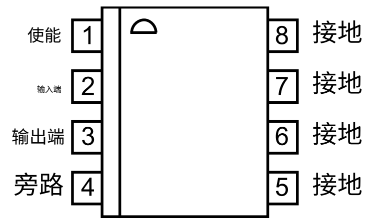


封装类型

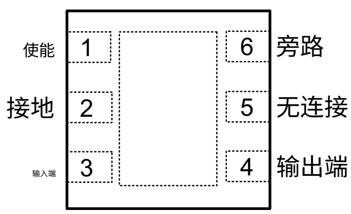
MIC5219-x.xYMM
MSOP-8 (MM)
固定电压
（顶视图）



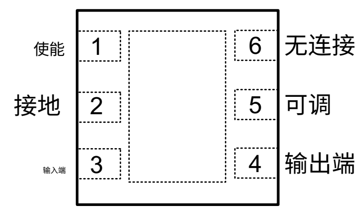
MIC5219YMM
MSOP-8 (MM)
可调电压
（顶视图）



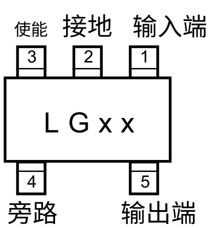
MIC5219-x.xYML
6引脚 VDFN (ML)
（顶视图）



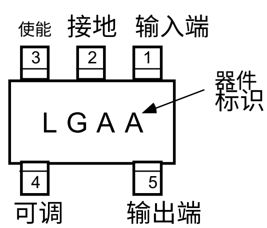
MIC5219YMT
6引脚 TDFN (MT)
（顶视图）



MIC5219-x.xYM5
SOT23-5 (M5)
固定电压
（顶视图）

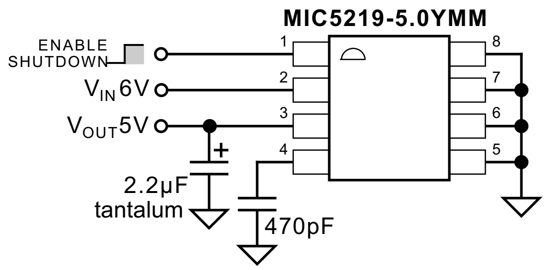


MIC5219YM5
SOT23-5 (M5)
可调电压
（顶视图）

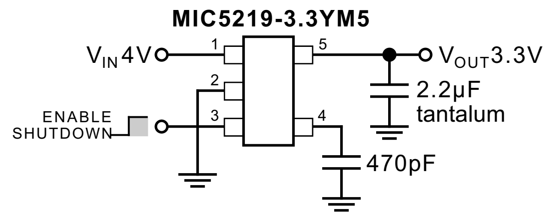


Typical Application Circuits

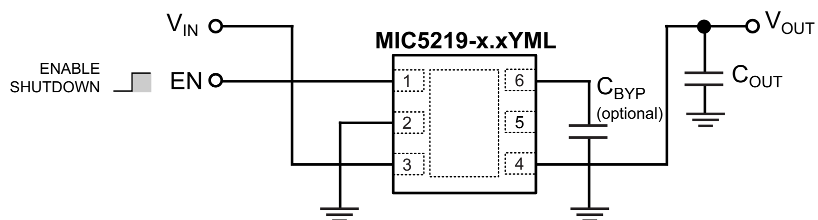
MIC5219
5V Ultra-Low Noise Regulator



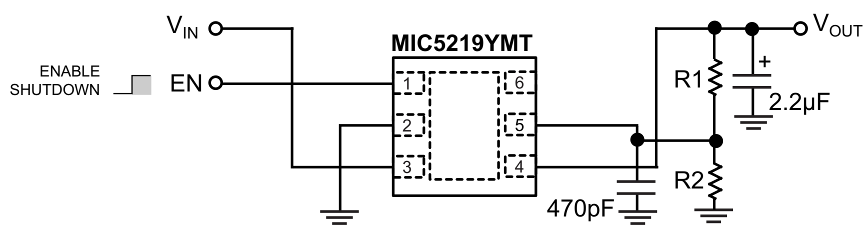
MIC5219
3.3V Ultra-Low Noise Regulator



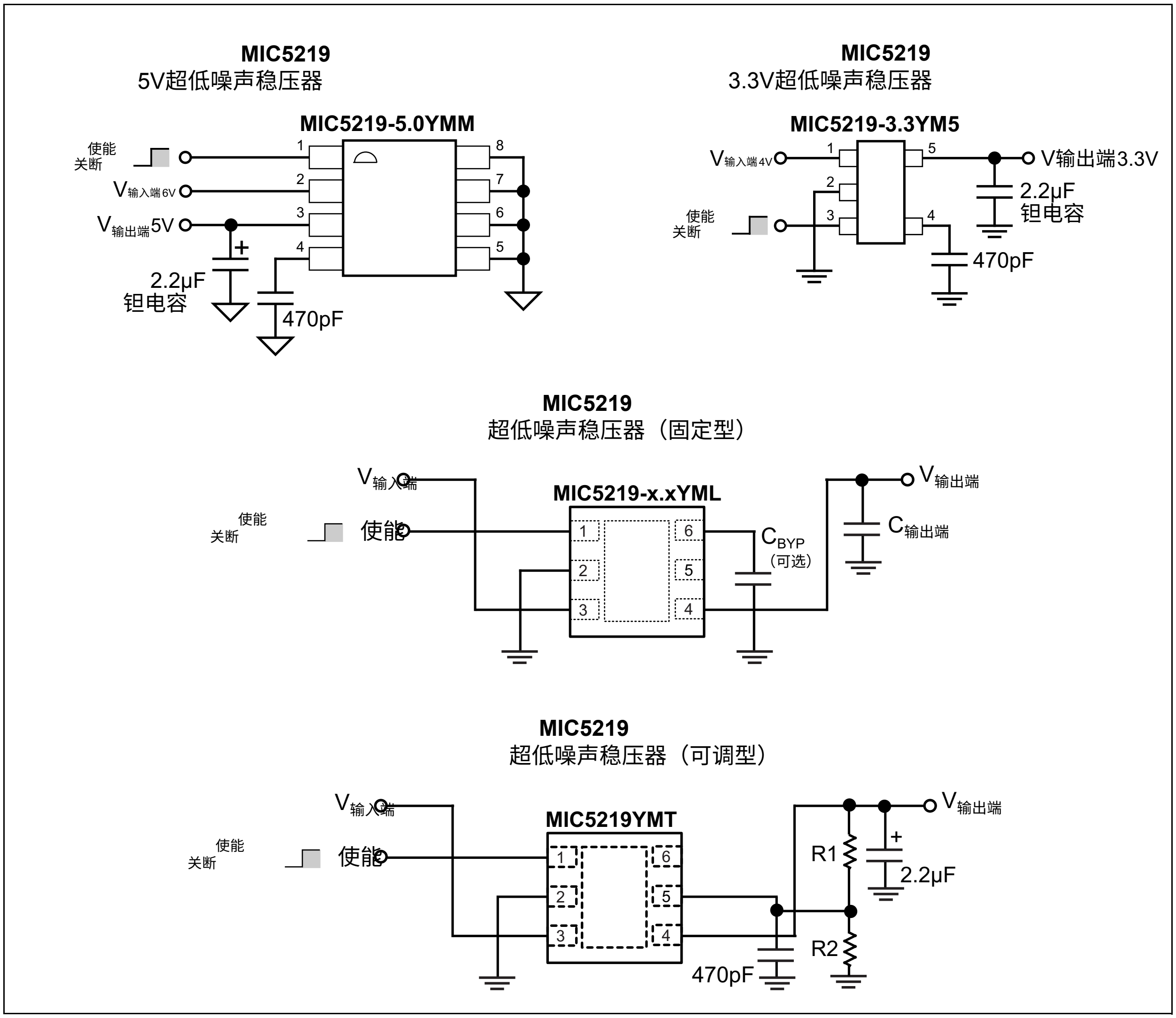
MIC5219
Ultra-Low Noise Regulator (Fixed)



MIC5219
Ultra-Low Noise Regulator (Adjustable)

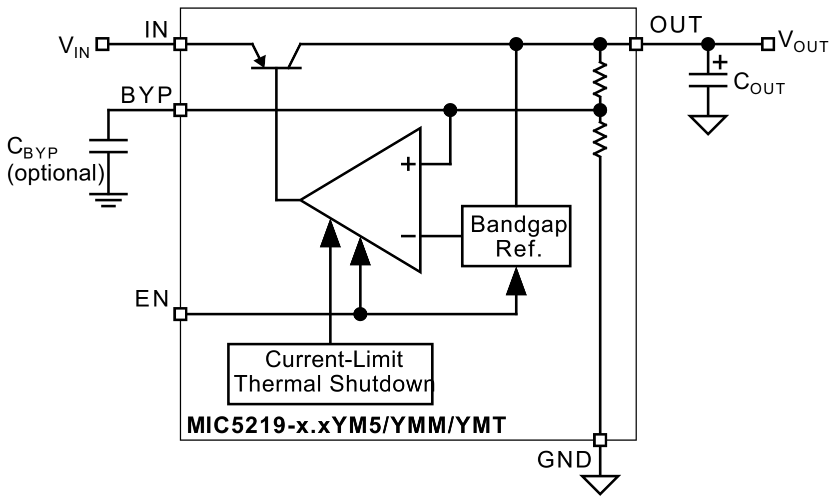


典型应用电路

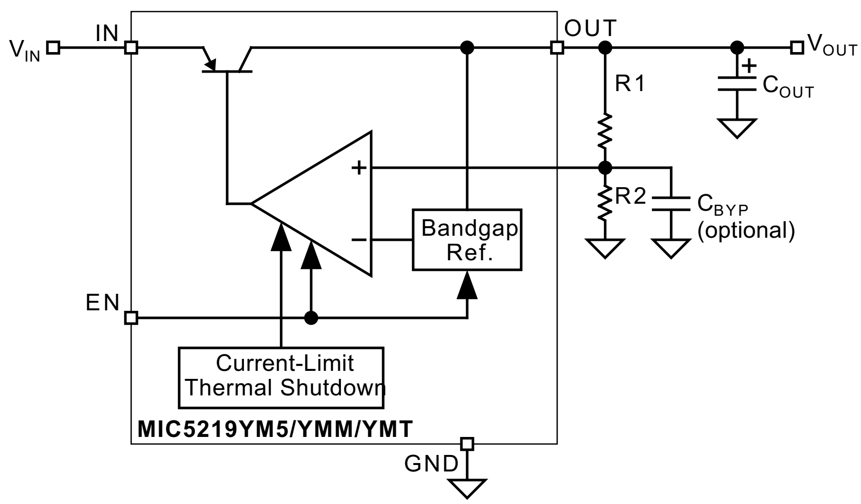

MIC5219
5V超低噪声稳压器
MIC5219-5.0YMM
使能
关断
V输入端6V
V输出端5V
2.2μF
钽电容
470pF
MIC5219
3.3V超低噪声稳压器
MIC5219-3.3YM5
V输入端4V
V输出端3.3V
2.2μF
钽电容
使能
关断
470pF
MIC5219
超低噪声稳压器（固定型）
MIC5219-x.xYML
V输入端
使能
关断
使能
CBYP
（可选）
V输出端
C输出端
MIC5219
超低噪声稳压器（可调型）
MIC5219YMT
V输入端
使能
关断
使能
V输出端
R1
R2
2.2μF
470pF

Block Diagrams

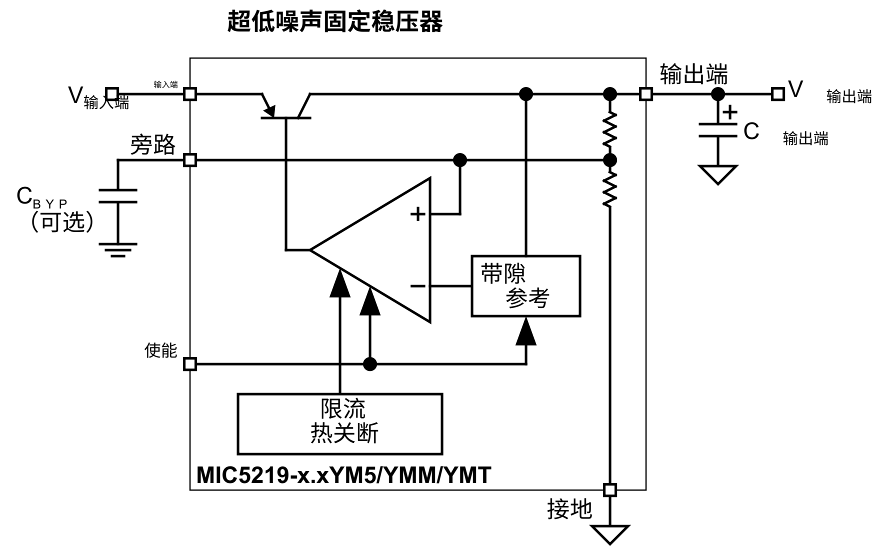
Ultra-Low Noise Fixed Regulator

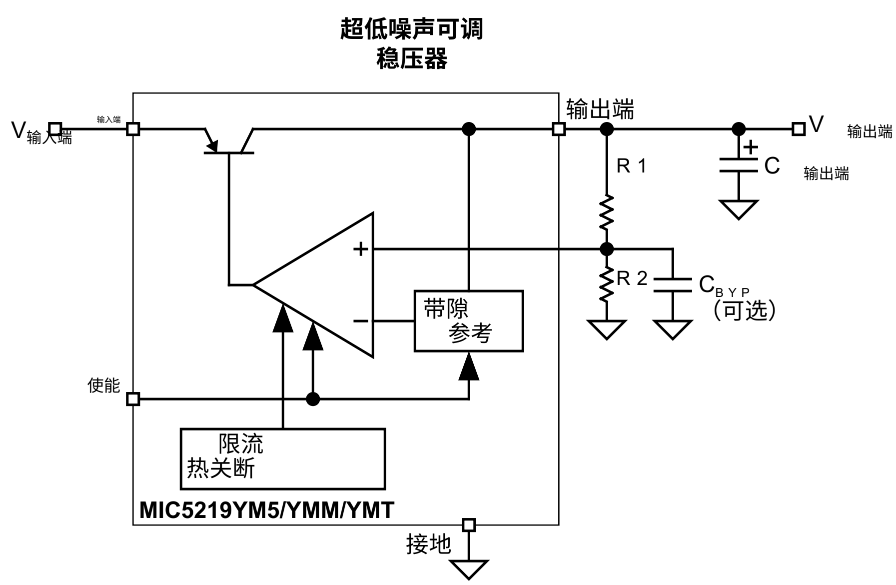


Ultra-Low Noise Adjustable Regulator



框图


超低噪声固定稳压器
V输入端
输入端
旁路
C BYP
（可选）
使能
带隙
参考
限流
热关断
MIC5219-x.xYM5/YMM/YMT
输出端
V 输出端
C 输出端
接地


超低噪声可调
稳压器
V输入端
输入端
使能
带隙
参考
限流
热关断
MIC5219YM5/YMM/YMT
输出端
V 输出端
C 输出端
R 1
R 2
C BYP
（可选）
接地

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Input Voltage (V_{IN}) .... –20V to +20V
Power Dissipation (P_D) .... Internally Limited

Operating Ratings ††

Supply Input Voltage (V_{IN}) .... +2.5V to +12V
Enable Input Voltage (V_{EN}) .... 0V to V_{IN}

† Notice: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its operating ratings. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D(MAX)} = (T_{J(MAX)} – T_A) \div \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. See Table 4-1 and the Thermal Considerations section for details.

†† Notice: The device is not guaranteed to function outside its operating rating.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, $V_{IN} = V_{OUT} + 1.0V$; $C_{OUT} = 4.7\ \mu F$, $I_{OUT} = 100\ \mu A$; $T_J = +25°C$, **bold** values indicate $–40°C \le T_J \le +125°C$.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Voltage	V_{OUT}	–1	—	1	%	Variation from Nominal V_{OUT}
		–2	—	**2**	%	
Output Voltage Temperature Coefficient	$\Delta V_{OUT}/\Delta T$	—	**40**	—	ppm/°C	Note 1
Line Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.009	0.05	%/V	$V_{IN} = V_{OUT}$ + 1V to 12V
		—	—	**0.1**		
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.05	0.5	%	I_{OUT} = 100 µA to 500 mA, Note 2
		—	—	**0.7**		

Note 1: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

2: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range from 100 µA to 500 mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

3: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential.

4: Ground pin current is the regulator quiescent current plus pass transistor base current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

5: V_{EN} is the voltage externally applied to devices with the EN (enable) input pin.

6: Thermal regulation is defined as the change in output voltage at a time "t" after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 500 mA load pulse at V_{IN} = 12V for t = 10 ms.

7: C_{BYP} is an optional, external bypass capacitor connected to devices with a BYP (bypass) or ADJ (adjust) pin.

1.0 电气特性

绝对最大额定值 †

电源输入电压 (V_{IN}) .... –20V 至 +20V
功率耗散 (P_D) ....内部限制

工作额定值 ††

电源输入电压 (V_{IN}) .... +2.5V 至 +12V
使能输入电压 (V_{EN}) ....0V 至 V_{IN}

† 注意：绝对最大额定值表示超过该范围可能导致器件损坏。当器件在工作额定值范围外运行时，电气规格不适用。最大允许功率耗散取决于最大结温 TJ(MAX)、结-环境热阻 θJA 及环境温度 TA。 任意环境温度下的最大允许功率耗散计算公式为：PD(MAX)= (TJ(MAX) – TA) ÷ θJA。 超过最大允许功率耗散将导致芯片温度过高，稳压器将进入热关断。详情请参见表4-1及热设计注意事项章节。

†† 注意：器件在其工作范围之外不保证正常工作。

电气特性

电气特性：除非另有说明，V_{IN}= V_{OUT}+ 1.0V；C_{OUT}= 4.7 µF，I_{OUT}= 100 µA；
T_J= +25°C，粗体数值表示 –40°C ≤ TJ ≤ +125°C。

参数	符号	最小值	典型值	最大值	单位	条件
输出电压	$V_{输出端}$	–1	—	1	%	相对于标称输出电压的偏差
		–2	—	**2**	%	
输出电压 温度系数	$\Delta V_{OUT}/\Delta T$	—	**40**	—	ppm/°C	注释 1
线性稳压	$\Delta V_{OUT}/V_{OUT}$	—	0.009	0.05	%/V	V_{IN} = V_{OUT} + 1V 至 12V
		—	—	**0.1**		
负载稳压	$\Delta V_{OUT}/V_{OUT}$	—	0.05	0.5	%	I_{OUT} = 100 µA 至 500 毫安，注释 2
		—	—	**0.7**		

注释 **1**：输出电压温度系数定义为最坏情况下的电压变化量除以总温度范围。

注释 **2**：稳压性能在恒定结温条件下通过低占空比脉冲测试测量。器件在100 µA至500毫安负载范围内测试负载稳压。输出电压因热效应产生的变化由热调节规格涵盖。

注释 **3**：压降电压定义为输入与输出电压差，在该差值下输出电压比1V差值时的额定值低2%。

注释 **4**：地引脚电流为稳压器静态电流与通断晶体管基极电流之和。从电源汲取的总电流等于负载电流与地引脚电流之和。

5: V_{EN} 是外部施加到带有EN（使能）输入引脚的器件上的电压。

6: 热调节定义为在施加功率耗散变化后，时间“t”时刻输出电压的变化，排除负载和线路稳压的影响。规格基于 V_{IN}= 12V，负载脉冲为500毫安，持续时间t = 10毫秒。

7: C_{BYP}是连接到带有BYP（旁路）或ADJ（可调）引脚器件的可选外部旁路电容。

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, $V_{IN} = V_{OUT} + 1.0V$; $C_{OUT} = 4.7\ \mu F$, $I_{OUT} = 100\ \mu A$; $T_J = +25°C$, **bold** values indicate $-40°C \le T_J \le +125°C$.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Dropout Voltage (Note 3)	$V_{IN} - V_{OUT}$	—	10	60	mV	I_{OUT} = 100 µA
		—	—	**80**		
		—	115	175	mV	I_{OUT} = 50 mA
		—	—	**250**		
		—	175	300	mV	I_{OUT} = 150 mA
		—	—	**400**		
		—	350	500	mV	I_{OUT} = 500 mA
		—	—	**600**		
Ground Pin Current (Note 4, 5)	I_{GND}	—	80	130	µA	$V_{EN} \ge 3.0V$, I_{OUT} = 100 µA
		—	—	**170**		
		—	350	650	µA	$V_{EN} \ge 3.0V$, I_{OUT} = 50 mA
		—	—	**900**		
		—	1.8	2.5	mA	$V_{EN} \ge 3.0V$, I_{OUT} = 150 mA
		—	—	**3.0**		
		—	12	20	mA	$V_{EN} \ge 3.0V$, I_{OUT} = 500 mA
		—	—	**25**		
Ground Pin Quiescent Current (Note 4)		—	0.05	3	µA	$V_{EN} \le 0.4V$
		—	0.10	**8**	µA	$V_{EN} \le 0.18V$
Ripple Rejection	PSRR	—	75	—	dB	f = 120 Hz
Current Limit	I_{LIMIT}	—	700	**1000**	mA	V_{OUT} = 0V
Thermal Regulation (Note 3)	$\Delta V_{OUT}/\Delta P_D$	—	**0.05**	—	%/W	Note 6
Output Noise (Note 7)	e_{no}	—	500	—	nV/√ Hz	I_{OUT} = 50 mA, C_{OUT} = 2.2 µF, C_{BYP} = 0
		—	300	—	nV/√ Hz	I_{OUT} = 50 mA, C_{OUT} = 2.2 µF, C_{BYP} = 470 pF

Note 1: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

2: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range from 100 µA to 500 mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

3: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential.

4: Ground pin current is the regulator quiescent current plus pass transistor base current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

5: V_{EN} is the voltage externally applied to devices with the EN (enable) input pin.

6: Thermal regulation is defined as the change in output voltage at a time “t” after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 500 mA load pulse at V_{IN} = 12V for t = 10 ms.

7: C_{BYP} is an optional, external bypass capacitor connected to devices with a BYP (bypass) or ADJ (adjust) pin.

电气特性（续）

电气特性：除非另有说明，V_{IN}= V_{OUT}+ 1.0V； C_{OUT}= 4.7 μF， I_{OUT}= 100 μA；
T_J= +25°C，粗体数值表示 –40°C ≤ TJ ≤ +125°C。

参数	符号	最小值	典型值	最大值	单位	条件
压降电压（注3）	$V_{IN} - V_{OUT}$	—	10	60	毫伏	I_{OUT} = 100 μA
		—	—	**80**		
		—	115	175	毫伏	I_{OUT} = 50毫安
		—	—	**250**		
		—	175	300	毫伏	I_{OUT} = 150毫安
		—	—	**400**		
		—	350	500	毫伏	I_{OUT} = 500毫安
		—	—	**600**		
地引脚电流（注4，注5）	I_{GND}	—	80	130	μA	V_{EN} ≥ 3.0V, I_{OUT} = 100 μA
		—	—	**170**		
		—	350	650	μA	V_{EN} ≥ 3.0V, I_{OUT} = 50 毫安
		—	—	**900**		
		—	1.8	2.5	毫安	V_{EN} ≥ 3.0V, I_{OUT} = 150 毫安
		—	—	**3.0**		
		—	12	20	毫安	V_{EN} ≥ 3.0V, I_{OUT} = 500 毫安
		—	—	**25**		
地引脚静态电流（注4）		—	0.05	3	μA	V_{EN} ≤ 0.4V
		—	0.10	**8**	μA	V_{EN} ≤ 0.18V
纹波抑制	PSRR	—	75	—	dB	f = 120 Hz
电流限制	I_{LIMIT}	—	700	**1000**	毫安	V_{OUT} = 0V
热调节（注3）	$\Delta V_{输出端}/\Delta P_D$	—	**0.05**	—	%/W	注6
输出噪声（注7）	e_{no}	—	500	—	nV/√ Hz	I输出端= 50 毫安，C输出端= 2.2 μF，C旁路= 0
		—	300	—	nV/√ Hz	I输出端= 50 毫安，C输出端 = 2.2 μF, C旁路= 470 pF

注释 **1**：输出电压温度系数定义为最坏情况下的电压变化量除以总温度范围。

注释 **2**：稳压性能在恒定结温条件下通过低占空比脉冲测试测量。器件在100 μA至500毫安负载范围内测试负载稳压。输出电压因热效应产生的变化由热调节规格涵盖。

注释 **3**：压降电压定义为输入与输出电压差，在该差值下输出电压比1V差值时的额定值低2%。

注释 **4**：地引脚电流为稳压器静态电流与通断晶体管基极电流之和。从电源汲取的总电流等于负载电流与地引脚电流之和。

5: V_{EN} 是外部施加到带有EN（使能）输入引脚的器件上的电压。

6: 热调节定义为在施加功率耗散变化后，时间“t”时刻输出电压的变化，排除负载和线路稳压的影响。规格基于 V_{IN}= 12V，负载脉冲为500毫安，持续时间t = 10毫秒。

7: C_{BYP}是连接到带有BYP（旁路）或ADJ（可调）引脚器件的可选外部旁路电容。

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, $V_{IN} = V_{OUT} + 1.0V$; $C_{OUT} = 4.7\ \mu F$, $I_{OUT} = 100\ \mu A$; $T_J = +25°C$, **bold** values indicate $-40°C \le T_J \le +125°C$.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
ENABLE Input						
Enable Input Logic-Low Voltage	V_{ENL}	—	—	0.4	V	V_{EN} = logic low (regulator shutdown)
		—	—	**0.18**		
		2.0	—	—	V	V_{EN} = logic high (regulator enabled)
Enable Input Current	I_{ENL}	—	0.01	–1	µA	$V_{ENL} \le 0.4V$
		—	**0.01**	**–2**		$V_{ENL} \le 0.18V$
	I_{ENH}	2	5	20	µA	$V_{ENH} \ge 2.0V$
		—	—	**25**		

Note 1: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

2: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range from 100 µA to 500 mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

3: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential.

4: Ground pin current is the regulator quiescent current plus pass transistor base current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

5: V_{EN} is the voltage externally applied to devices with the EN (enable) input pin.

6: Thermal regulation is defined as the change in output voltage at a time “t” after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 500 mA load pulse at V_{IN} = 12V for t = 10 ms.

7: C_{BYP} is an optional, external bypass capacitor connected to devices with a BYP (bypass) or ADJ (adjust) pin.

电气特性（续）

电气特性：除非另有说明，V_{IN}= V_{OUT}+ 1.0V；C_{OUT}= 4.7 μF，I_{OUT}= 100 μA；T_J= +25°C，粗体数值表示 –40°C ≤ TJ ≤ +125°C。

参数	符号	最小值	典型值	最大值	单位	条件
使能输入						
使能输入逻辑低电平电压	V_{ENL}	—	—	0.4	V	V_{EN} = 逻辑低（稳压器关闭）
		—	—	**0.18**		
		2.0	—	—	V	V_{EN} = 逻辑高（稳压器使能）
使能输入电流	I_{ENL}	—	0.01	–1	μA	V_{ENL} ≤ 0.4V
		—	**0.01**	**–2**		V_{ENL} ≤ 0.18V
	I_{ENH}	2	5	20	μA	V_{ENH} ≥ 2.0V
		—	—	**25**		

注释 **1**：输出电压温度系数定义为最坏情况下的电压变化量除以总温度范围。

注释 **2**：稳压性能在恒定结温条件件下通过低占空比脉冲测试测量。器件在100 μA至500毫安负载范围内测试负载稳压。输出电压因热效应产生的变化由热调节规格涵盖。

注释 **3**：压降电压定义为输入与输出电压差，在该差值下输出电压比1V差值时的额定值低2%。

注释 **4**：地引脚电流为稳压器静态电流与通断晶体管基极电流之和。从电源汲取的总电流等于负载电流与地引脚电流之和。

5: V_{EN} 是外部施加到带有EN（使能）输入引脚的器件上的电压。

6: 热调节定义为在施加功率耗散变化后，时间“t”时刻输出电压的变化，排除负载和线路稳压的影响。规格基于 V_{IN}= 12V，负载脉冲为500毫安，持续时间t = 10毫秒。

7: C_{BYP}是连接到带有BYP（旁路）或ADJ（可调）引脚器件的可选外部旁路电容。

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_A	–40	—	+125	°C	—
Maximum Junction Temperature Range	T_J	–40	—	+125	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	260	—	°C	Soldering, 5 sec.
Package Thermal Resistances						
Thermal Resistance, MSOP-8Ld	θ_{JA}	—	160	—	°C/W	Minimum footprint area.
Thermal Resistance, SOT23-5Ld	θ_{JA}	—	220	—	°C/W	Minimum footprint area.
Thermal Resistance, VDFN-6Ld	θ_{JA}	—	90	—	°C/W	Minimum footprint area.
Thermal Resistance, TDFN-6Ld	θ_{JA}	—	90	—	°C/W	Minimum footprint area.

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

温度规格（注1）

参数	符号	最小值	典型值	最大值	单位	条件
温度范围						
工作环境温度范围	T_A	–40	—	+125	°C	—
最大结温范围	T_J	–40	—	+125	°C	—
储存温度范围	T_S	–65	—	+150	°C	—
引脚温度	—	—	260	—	°C	焊接，5秒
封装热阻						
热阻，MSOP-8Ld封装	θ_{JA}	—	160	—	°C/W	最小占地面积。
热阻，SOT23-5Ld封装	θ_{JA}	—	220	—	°C/W	最小占地面积。
热阻，VDFN-6Ld封装	θ_{JA}	—	90	—	°C/W	最小占地面积。
热阻，TDFN-6Ld封装	θ_{JA}	—	90	—	°C/W	最小占地面积。

注**1**：最大允许功率耗散取决于环境温度、最大允许结温及结到空气的热阻（即T_A、T_J、θ_{JA}）。超过最大允许功率耗散将导致器件工作结温超过最大+**1**25°C额定值。持续结温高于+**1**25°C会影响器件的可靠性。

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

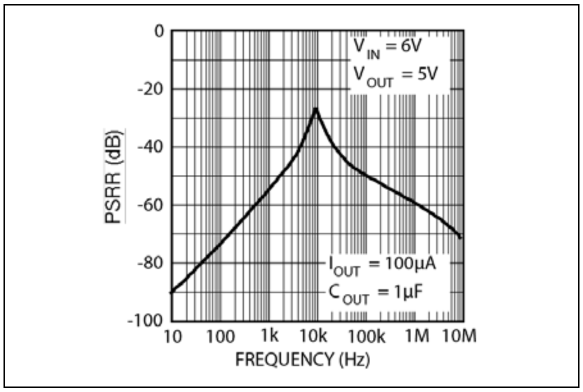


FIGURE 2-1: *Power Supply Rejection Ratio.*

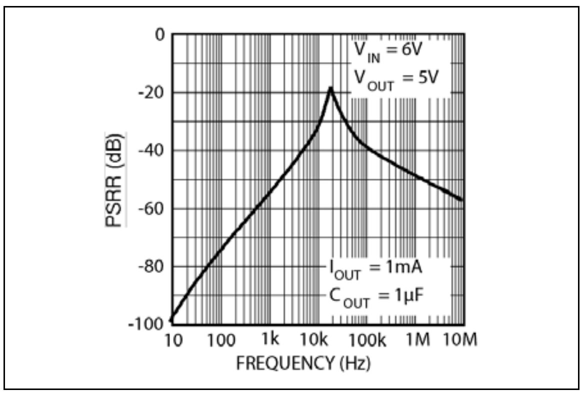


FIGURE 2-2: *Power Supply Rejection Ratio.*

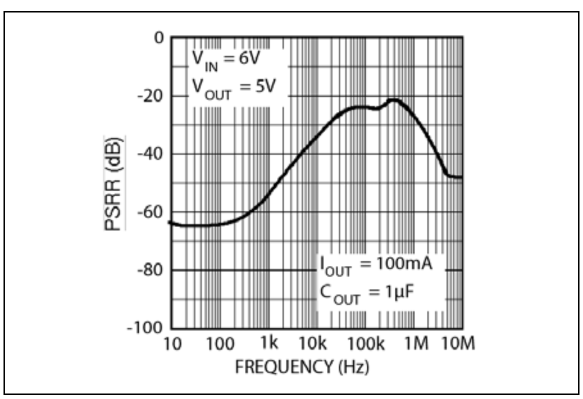


FIGURE 2-3: *Power Supply Rejection Ratio.*

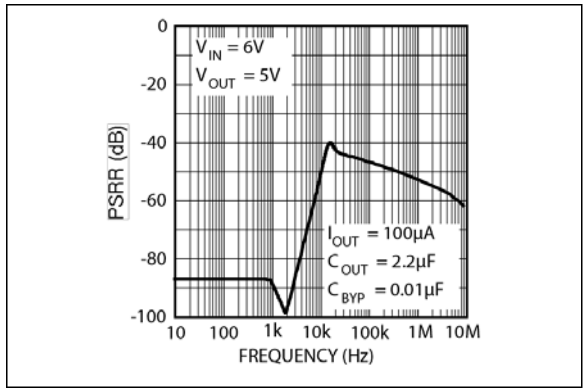


FIGURE 2-4: *Power Supply Rejection Ratio.*

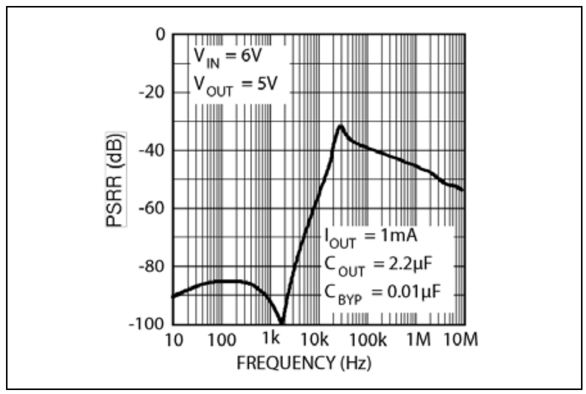


FIGURE 2-5: *Power Supply Rejection Ratio.*

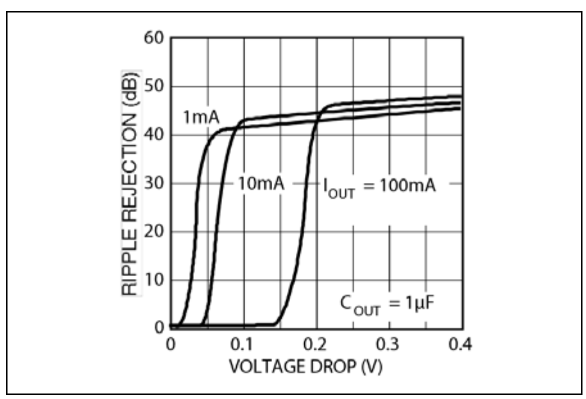


FIGURE 2-6: *Power Supply Ripple Rejection vs. Voltage Drop.*

2.0 典型性能曲线

注意：以下图表和表格基于有限样本的统计汇总，仅供参考。此处列出的性能参数未经测试或保证。部分图表或表格中的数据可能超出规定的工作范围（例如超出规定的电源范围），因此不在保证范围内。

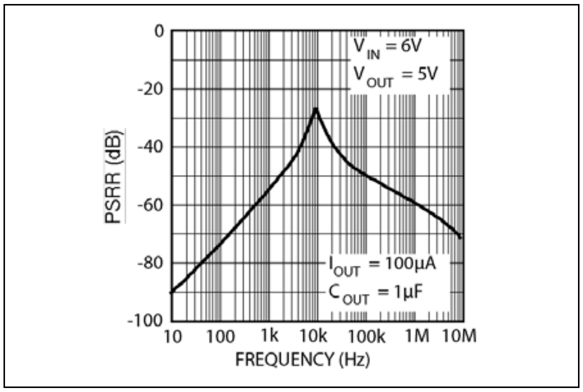


图2-1： 电源抑制比比率。

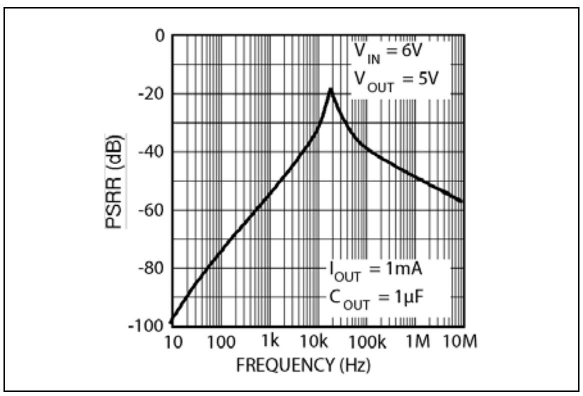


图2-2： 电源抑制比比率。

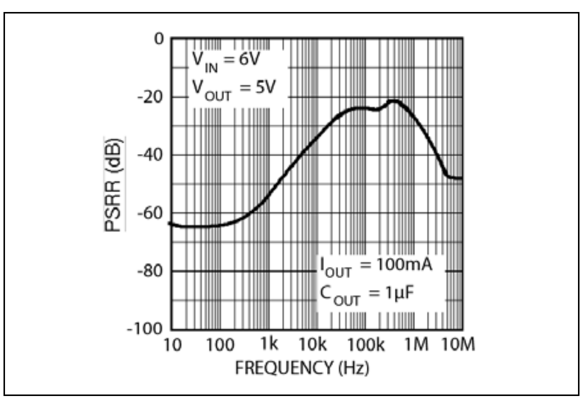


图2-3： 电源抑制比比率。

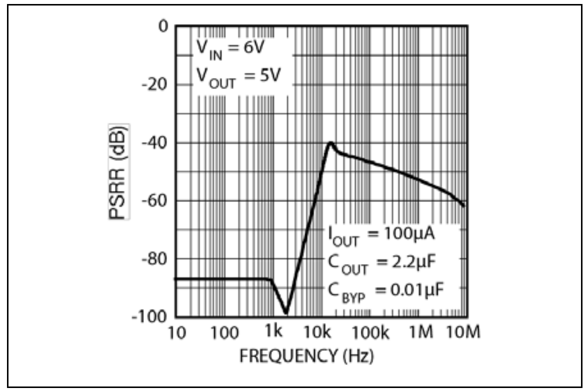


图2-4： 电源抑制比比率。

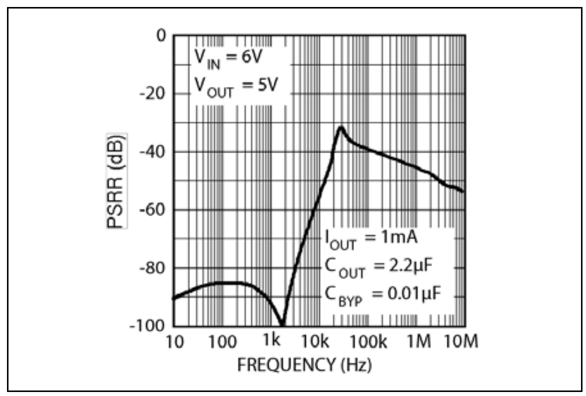


图 2-5： 电源抑制比比率。

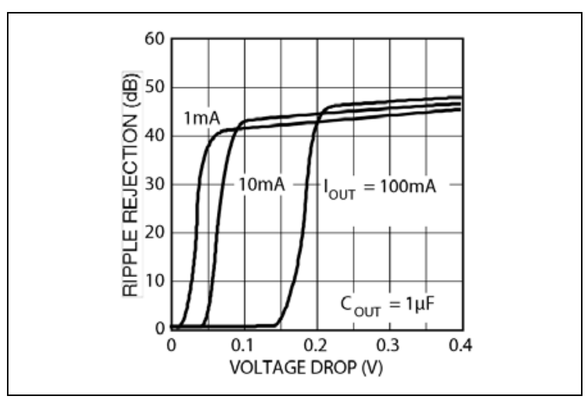


图 2-6： 电源纹波抑制与压降电压的关系

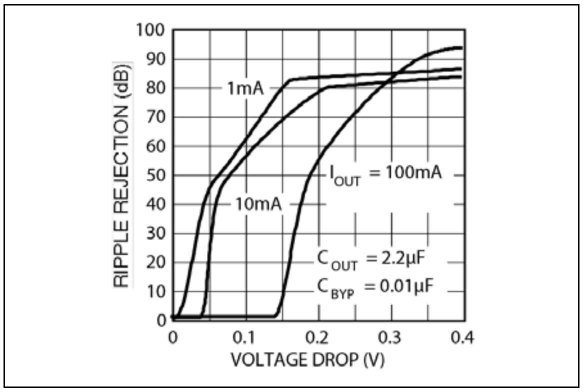


FIGURE 2-7: *Power Supply Ripple Rejection vs. Voltage Drop.*

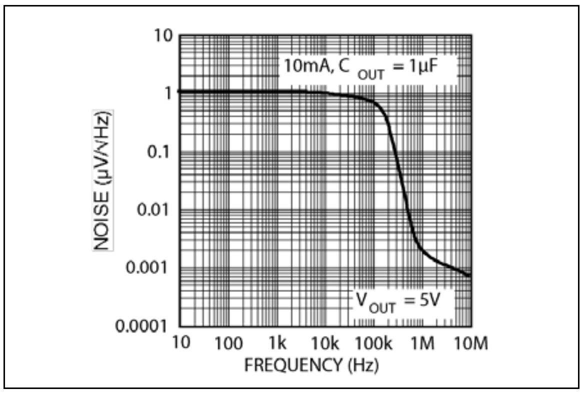


FIGURE 2-8: *Noise Performance.*

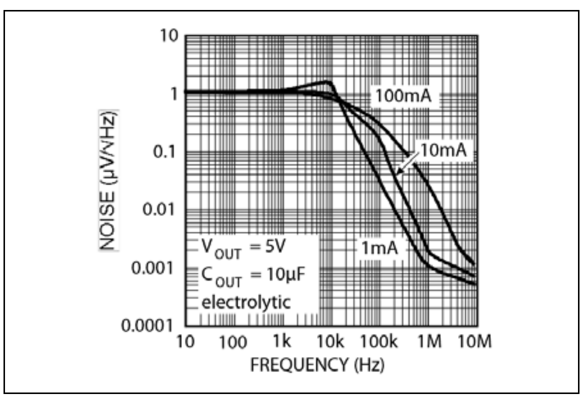


FIGURE 2-9: *Noise Performance.*

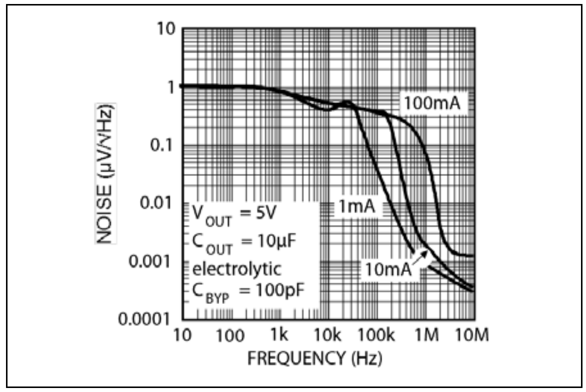


FIGURE 2-10: *Noise Performance.*

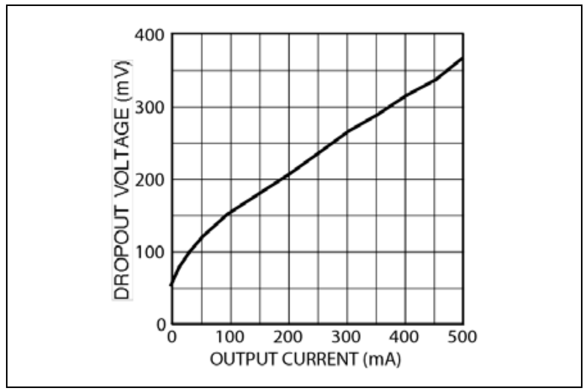


FIGURE 2-11: *Dropout Voltage vs. Output Current.*

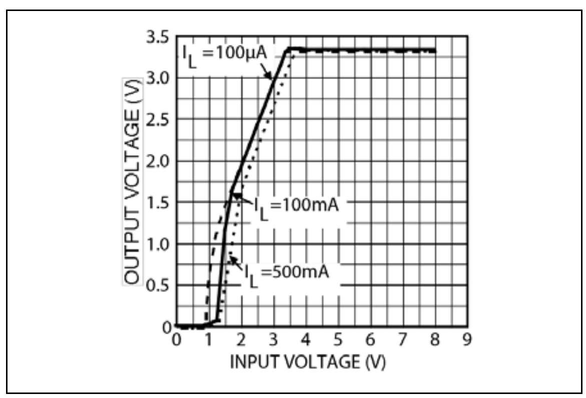


FIGURE 2-12: *Dropout Characteristics.*

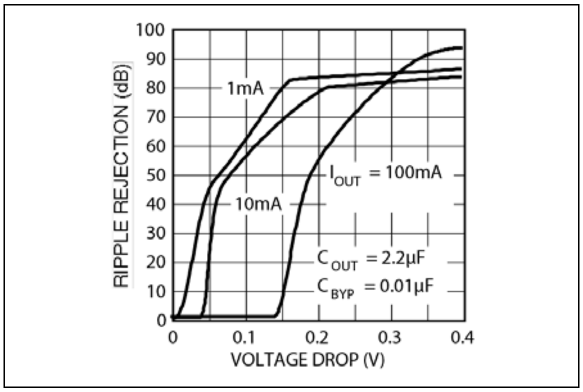


图 *2-7*： 电源纹波抑制与压降电压的关系

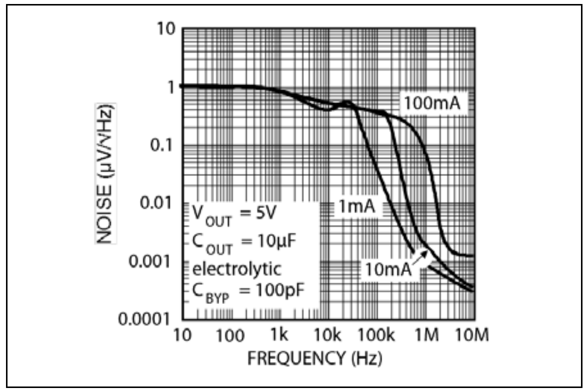


图 *2-10*： 噪声性能

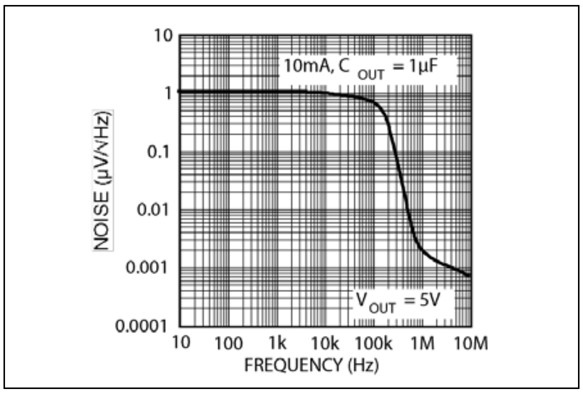


图 *2-8*： 噪声性能

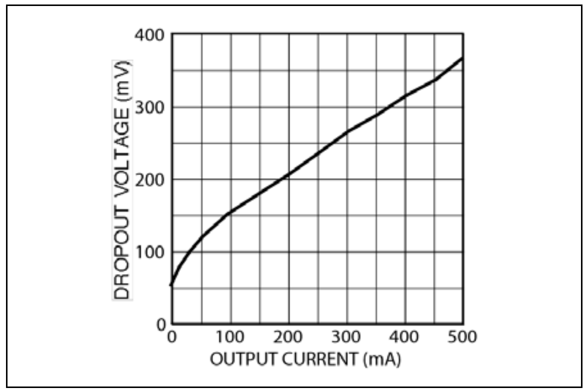


图 *2-11*： 压降电压与输出电流的关系

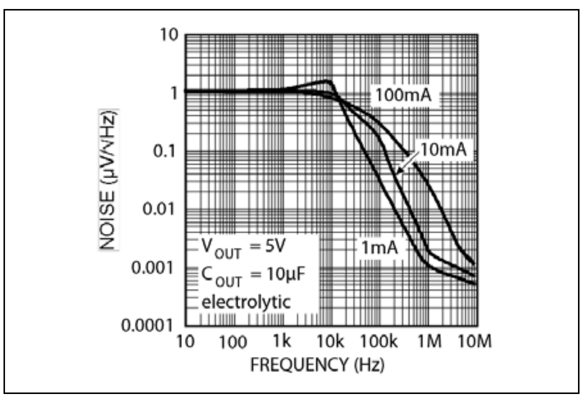


图 *2-9*： 噪声性能

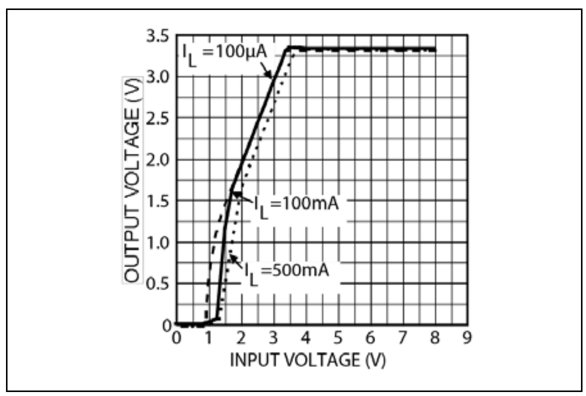


图 *2-12*： 压降特性

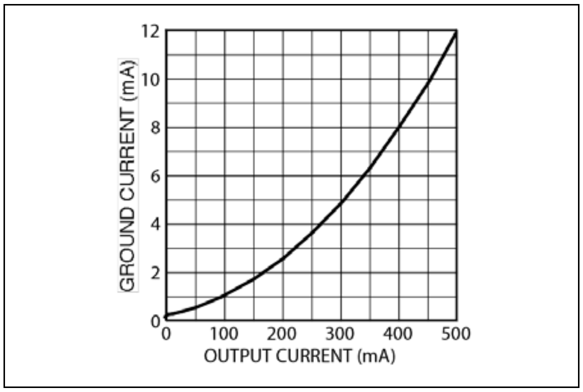


FIGURE 2-13: *Ground Current vs. Output Current*.

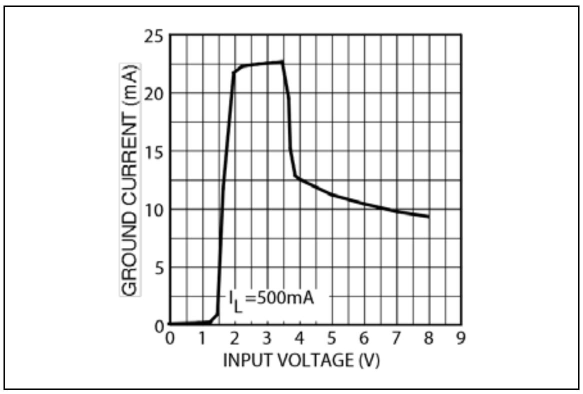


FIGURE 2-14: *Ground Current vs. Supply Voltage*.

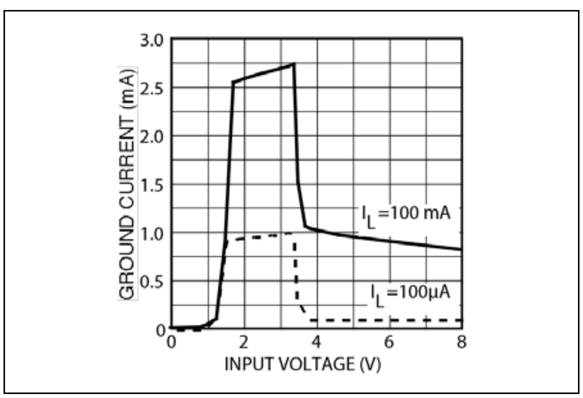


FIGURE 2-15: *Ground Current vs. Supply Voltage*.

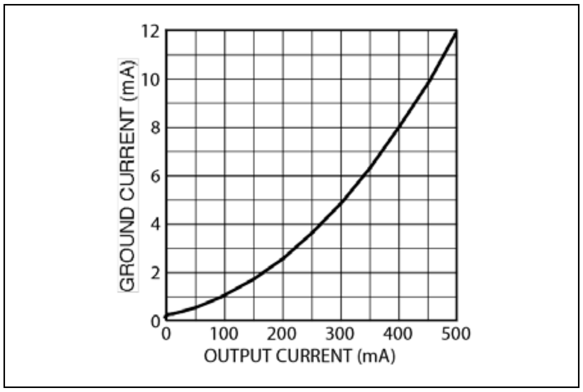


图 *2-13*： 地电流与输出端电流
电流。

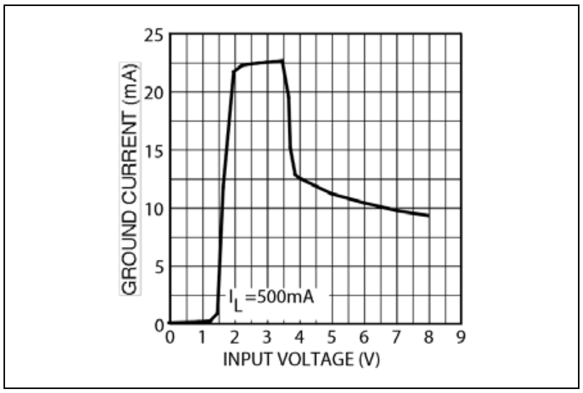


图 *2-14*： 地电流与电源电压
电压。

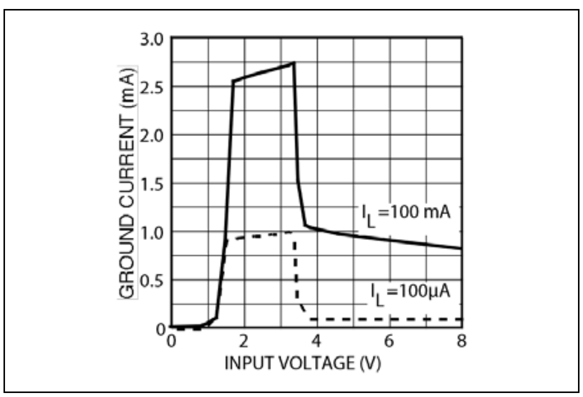


图 *2-15*： 地电流与电源电压
电压。

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number VDFN-6 TDFN-6	Pin Number MSOP-8	Pin Number SOT23-5	Pin Name	Description
3	2	1	IN	Supply input.
2	5 - 8	2	GND	Ground: MSOP-8 pins 5 through 8 are internally connected.
4	3	5	OUT	Regulator output.
1	1	3	EN	Enable (input): CMOS-compatible control input. Logic-high = enable; logic-low or open = shutdown.
6	4 (FIXED)	4 (FIXED)	BYP	Reference bypass: Connect an external 470 pF capacitor to GND to reduce output noise. May be left open.
5 (NC)	4 (ADJ)	4 (ADJ)	ADJ	Adjust (input): Feedback input. Connect to resistive voltage-divider network.
EP	—	—	GND	Ground: Internally connected to the exposed pad. Connect externally to GND pin.

3.0 引脚说明

引脚说明详见表 3-1。

表 3-1：引脚功能表

引脚编号 VDFN-6 TDFN-6	引脚编号 MSOP-8	引脚编号 SOT23-5	引脚名称	功能描述
3	2	1	输入端	电源输入端。
2	5 - 8	2	接地	接地：MSOP-8 的第 5 至第 8 引脚内部相连。
4	3	5	输出端	稳压器输出端。
1	1	3	使能	使能（输入）： CMOS兼容的控制输入。 逻辑高电平 = 使能；逻辑低电平或开路 = 关断。
6	4（固定）	4（固定）	旁路	参考旁路：连接一个外部470 pF电容至地，以降低输出噪声。可不连接。
5（无连接）	4（可调）	4（可调）	可调	调节（输入）： 反馈输入端。连接至分压电阻网络。
裸片散热片	—	—	接地	地：内部连接至裸片散热片，外部连接至地引脚。

4.0 APPLICATION INFORMATION

The MIC5219 is designed for 150 mA to 200 mA output current applications where a high-current spike (500 mA) is needed for short, start-up conditions. Basic application of the device will be discussed initially followed by a more detailed discussion of higher current applications.

4.1 Enable/Shutdown

Forcing EN (enable/shutdown) high (>2V) enables the regulator. EN is compatible with CMOS logic. If the enable/shutdown feature is not required, connect EN to IN (supply input). See Figure 4-5.

4.2 Input Capacitor

A 1 µF capacitor should be placed from IN to GND if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

4.3 Output Capacitor

An output capacitor is required between OUT and GND to prevent oscillation. The minimum size of the output capacitor is dependent upon whether a reference bypass capacitor is used. 1 µF minimum is recommended when C_{BYP} is not used (see Figure 4-5). 2.2 µF minimum is recommended when C_{BYP} is 470 pF (see Figure 4-6). For applications <3V, the output capacitor should be increased to 22 µF minimum to reduce start-up overshoot. Larger values improve the regulator's transient response. The output capacitor value may be increased without limit.

The output capacitor should have an ESR (equivalent series resistance) of about 1Ω or less and a resonant frequency above 1 MHz. Ultra-low ESR capacitors could cause oscillation and/or under-damped transient response. Most tantalum or aluminum electrolytic capacitors are adequate; film types will work, but are more expensive. Many aluminum electrolytics have electrolytes that freeze at about –30°C, so solid tantalums are recommended for operation below –25°C.

At lower values of output current, less output capacitance is needed for stability. The capacitor can be reduced to 0.47 µF for current below 10 mA, or 0.33 µF for currents below 1 mA.

4.4 No-Load Stability

The MIC5219 will remain stable and in regulation with no load (other than the internal voltage divider) unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications.

4.5 Reference Bypass Capacitor

BYP is connected to the internal voltage reference. A 470 pF capacitor (C_{BYP}) connected from BYP to GND quiets this reference, providing a significant reduction in output noise (ultra-low noise performance). C_{BYP} reduces the regulator phase margin; when using C_{BYP}, output capacitors of 2.2 µF or greater are generally required to maintain stability.

The start-up speed of the MIC5219 is inversely proportional to the size of the reference bypass capacitor. Applications requiring a slow ramp-up of output voltage should consider larger values of C_{BYP}. Likewise, if rapid turn-on is necessary, consider omitting C_{BYP}.

4.6 Thermal Considerations

The MIC5219 is designed to provide 200 mA of continuous current in two very small profile packages. Maximum power dissipation can be calculated based on the output current and the voltage drop across the part. To determine the maximum power dissipation of the package, use the thermal resistance, junction-to-ambient, of the device and the following basic equation.

EQUATION 4-1:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

$T_{J(MAX)}$ is the maximum junction temperature of the die, +125°C, and T_A is the ambient operating temperature. θ_{JA} is layout-dependent; Table 4-1 shows examples of thermal resistance, junction-to-ambient, for the MIC5219.

TABLE 4-1: MIC5219 THERMAL RESISTANCE

Package	θ_{JA} Rec. Min. Footprint	θ_{JA} 1" Square 2 oz. Copper	θ_{JC}
MSOP-8	160°C/W	70°C/W	30°C/W
SOT23-5	220°C/W	170°C/W	130°C/W
2x2 VDFN	90°C/W	—	—
2x2TDFN	90°C/W	—	—

4.0 应用信息

MIC5219设计用于150毫安至200毫安输出电流的应用场合，其中短时间启动时需要500毫安的高电流峰值。首先讨论器件的基本应用，随后详细介绍更高电流的应用。

4.1 使能/关断

将EN（使能/关断）端强制为高电平（>2V）即可使稳压器工作。EN端兼容CMOS逻辑。若不需要使能/关断功能，请将EN端连接至IN端（电源输入）。详见图4-5。

4.2 输入电容

当输入端与交流滤波电容之间的导线长度超过10英寸，或输入端使用电池时，应在IN与GND之间放置一个1 μF的电容。

4.3 输出电容

输出端与GND之间必须连接输出电容以防止振荡。输出电容的最小容量取决于是否使用参考旁路电容。未使用C_{BYP}时，建议最小容量为1 μF（见图4-5）。

当C_{BYP}为470 pF时，建议最小容量为2.2 μF（见图4-6）。对于低于3V的应用，输出电容应至少增加到22 μF，以减少启动时的过冲。更大的电容值能够提升稳压器的瞬态响应性能。输出电容的容量可以无限制地增加。

输出电容的等效串联电阻（ESR）应约为1Ω或更低，且谐振频率应高于1 MHz。超低ESR电容可能引起振荡或欠阻尼的瞬态响应。大多数钽电容或铝电解电容均适用；薄膜电容也可使用，但成本较高。许多铝电解电容的电解液在约–30°C时会冻结，因此建议在–25°C以下环境中使用固体钽电容。

在较低输出电流条件下，所需的输出电容容量较小以保证稳定性。当输出电流低于10毫安时，电容可减小至0.47 μF；低于1毫安时，可减小至0.33 μF。

4.4 无负载稳压稳定性

MIC5219在无负载（除内部分压器外）情况下仍能保持稳定和稳压，这一点区别于许多其他稳压器。这在CMOS RAM保持供电应用中尤为重要。

4.5 参考旁路电容

BYP端连接至内部电压参考。一个470 pF的电容（C_{BYP}）连接在BYP与GND之间，可稳定该参考，显著降低输出噪声，实现超低噪声性能。C_{BYP}会降低稳压器的相位裕度；使用C_{BYP}时，通常需要2.2 μF或更大容量的输出电容以确保稳定。

MIC5219的启动速度与参考旁路电容的大小成反比。需要输出电压缓慢上升的应用应考虑使用较大容量的C_{BYP}；反之，若需快速启动，则可考虑省略C_{BYP}。

4.6 热量考虑

MIC5219设计用于在两种极小型封装中提供200毫安的连续输出电流。
最大功率耗散可根据输出电流及器件上的电压降计算得出。要确定封装的最大功率耗散，请使用器件的结-环境热阻及以下基本公式。

公式 4-1：

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

$T_{J(MAX)}$为芯片的最大结温，+125°C，T_A 为环境工作温度。θ_{JA}取决于布局；表4-1列出了MIC5219的结-环境热阻示例。

表4-1：MIC5219热阻

封装	θ_{JA} 推荐最小焊盘尺寸	θ_{JA} 1英寸平方 2盎司铜层	θ_{JC}
MSOP-8	160°C/W	70°C/W	30°C/W
SOT23-5	220°C/W	170°C/W	130°C/W
2x2 VDFN	90°C/W	—	—
2x2TDFN	90°C/W	—	—

The actual power dissipation of the regulator circuit can be determined using one simple equation.

EQUATION 4-2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

Substituting $P_{D(MAX)}$ for P_D and solving for the operating conditions that are critical to the application will give the maximum operating conditions for the regulator circuit. For example, if we are operating the MIC5219-3.3YM5 at room temperature, with a minimum footprint layout, we can determine the maximum input voltage for a set output current.

EQUATION 4-3:

$$P_{D(MAX)} = \frac{125°C - 25°C}{220°C/W} = 455mW$$

The thermal resistance, junction-to-ambient, for the minimum footprint is 220°C/W, taken from Table 4-1. The maximum power dissipation number cannot be exceeded for proper operation of the device. Using the output voltage of 3.3V, and an output current of 150 mA, we can determine the maximum input voltage. Ground current, maximum of 3 mA for 150 mA of output current, can be taken from the Electrical Characteristics section of the data sheet.

EQUATION 4-4:

$$455mW = (V_{IN} - 3.3V) \times 150mA + V_{IN} \times 3mA$$

$$455mW = 150mA \times V_{IN} + 3mA \times V_{IN} - 495mW$$

$$950mW = 153mA \times V_{IN}$$

$$V_{IN(MAX)} = 6.2V_{MAX}$$

Therefore, a 3.3V application at 150 mA of output current can accept a maximum input voltage of 6.2V in a SOT23-5 package. For a full discussion of heat sinking and thermal effects on voltage regulators, refer to the “Regulator Thermals” section of Microchip’s Designing with Low-Dropout Voltage Regulators handbook.

4.7 Peak Current Applications

The MIC5219 is designed for applications where high start-up currents are demanded from space constrained regulators. This device will deliver 500 mA start-up current from a SOT23-5 or MSOP-8 package, allowing high power from a very low profile device. The MIC5219 can subsequently provide output current that is only limited by the thermal characteristics of the device. You can obtain higher continuous currents from the device with the proper design. This is easily proved with some thermal calculations.

If we look at a specific example, it may be easier to follow. The MIC5219 can be used to provide up to 500 mA continuous output current. First, calculate the maximum power dissipation of the device, as was done in the Thermal Considerations section. Worst case thermal resistance (θ_{JA} = 220°C/W for the MIC5219-x.xYM5), will be used for this example.

EQUATION 4-5:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Assuming a 25°C room temperature, we have a maximum power dissipation value calculated in Equation 4-6.

EQUATION 4-6:

$$P_{D(MAX)} = \frac{125°C - 25°C}{220°C/W} = 455mW$$

Then we can determine the maximum input voltage for a 5 volt regulator operating at 500 mA, using worst case ground current.

稳压器电路的实际功率耗散可通过一个简单的方程计算得出。

方程 4-2：

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

将 $P_{D(MAX)}$ 代入 P_D 并求解对应用至关重要的工作条件，即可获得稳压器电路的最大工作参数。例如，在室温下采用最小占地面积布局运行 MIC5219-3.3YM5 时，可以确定设定输出电流下的最大输入电压。

方程 4-3：

$$P_{D(MAX)} = \frac{125°C - 25°C}{220°C/W} = 455mW$$

最小占地面积的结-环境热阻为220°C/W，数据取自表4-1。
为确保器件正常工作，最大功率耗散不得超过该数值。在输出电压为3.3V、输出电流为150毫安的条件下，可以确定最大输入电压。

地电流在输出电流为150毫安时最大为3毫安，相关数据可见于数据手册的电气特性部分。

方程 4-4：

$$455mW = (V_{IN} - 3.3V) \times 150mA + V_{IN} \times 3mA$$

$$455mW = 150mA \times V_{IN} + 3mA \times V_{IN} - 495mW$$

$$950mW = 153mA \times V_{IN}$$

$$V_{IN(MAX)} = 6.2V_{MAX}$$

因此，在SOT23-5封装中，3.3V、150毫安输出电流的应用可接受的最大输入电压为6.2V。 有关散热和热效应对稳压器的详细讨论，请参阅Microchip《低压差线性稳压器设计》手册中的"稳压器热特性"章节。

4.7 峰值电流应用

MIC5219设计用于对空间受限的稳压器要求高启动电流的场合。该器件可从SOT23-5或MSOP-8封装中提供500毫安启动电流，使得低外形器件能够输出高功率。MIC5219随后可提供仅受器件热特性限制的输出电流。通过合理设计，可以从器件获得更高的连续输出电流。这可以通过一些热计算轻松验证。

如果我们以一个具体例子说明，理解起来会更容易。MIC5219可用于提供高达500毫安的连续输出电流。首先，计算器件的最大功率耗散，如“热考虑”章节所示。本例将采用最坏情况热阻（θ_{JA} = 220°C/W，适用于MIC5219-x.xYM5）进行计算。

方程 4-5：

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

假设环境温度为 25°C，最大功率耗散值如方程 4-6 所示计算。

方程 4-6：

$$P_{D(MAX)} = \frac{125°C - 25°C}{220°C/W} = 455mW$$

然后，我们可以利用最坏情况下的地电流，确定在 500 毫安输出电流下，5 伏稳压器的最大输入电压。

EQUATION 4-7:

$$P_{D(MAX)} = 455mW = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

Where:

I_{OUT} = 500 mA
V_{OUT} = 5V
I_{GND} = 20 mA

$$455mW = (V_{IN} - 5V) \times 500mA + V_{IN} \times 20mA$$

$$2.995W = 520mA \times V_{IN}$$

$$V_{IN(MAX)} = \frac{2.995W}{520mA} = 5.683V$$

Therefore, to be able to obtain a constant 500 mA output current from the MIC5219-5.0YM5 at room temperature, you need extremely tight input-output voltage differential, barely above the maximum dropout voltage for that current rating.

You can run the part from larger supply voltages if the proper precautions are taken. Varying the duty cycle using the enable pin can increase the power dissipation of the device by maintaining a lower average power figure. This is ideal for applications where high current is only needed in short bursts. Figure 4-1 shows the safe operating regions for the MIC5219-x.xYM5 at three different ambient temperatures and at different output currents. The data used to determine this figure assumed a minimum footprint PCB design for minimum heat sinking. Figure 4-2 incorporates the same factors as the first figure, but assumes a much better heat sink. A 1" square copper trace on the PC board reduces the thermal resistance of the device. This improved thermal resistance improves power dissipation and allows for a larger safe operating region.

Figure 4-3 and Figure 4-4 show safe operating regions for the MIC5219-x.xYMM, the power MSOP package part. These graphs show three typical operating regions at different temperatures. The lower the temperature, the larger the operating region. The graphs were obtained in a similar way to the graphs for the MIC5219-x.xYM5, taking all factors into consideration and using two different board layouts, minimum footprint and 1" square copper PC board heat sink. For further discussion of PC board heat sink characteristics, refer to Application Hint 17, Designing PC Board Heat Sinks.

The information used to determine the safe operating regions can be obtained in a similar manner such as determining typical power dissipation, already discussed. Determining the maximum power dissipation based on the layout is the first step, this is done in the same manner as in the previous two sections. Then, a larger power dissipation number multiplied by a set maximum duty cycle would give that maximum power dissipation number for the layout. This is best shown through an example. If the application calls for 5V at 500 mA for short pulses, but the only supply voltage available is 8V, then the duty cycle has to be adjusted to determine an average power that does not exceed the maximum power dissipation for the layout.

EQUATION 4-8:

$$Av\dot{g}P_D = \left(\frac{\%DC}{100}\right)(V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

$$455mW = \left(\frac{\%DC}{100}\right)(8V - 5V) \times 500mA + 8V \times 20mA$$

$$455mW = \left(\frac{\%DC}{100}\right) \times 1.66W$$

$$0.274 = \frac{\%DC}{100}$$

$$\%DC = 27.4\%(\text{Duty Cycle Max.})$$

With an output current of 500 mA and a three volt drop across the MIC5219-xxYMM, the maximum duty cycle is 27.4%.

Applications also call for a set nominal current output with a greater amount of current needed for short durations. This is a tricky situation, but it is easily remedied. Calculate the average power dissipation for each current section, then add the two numbers giving the total power dissipation for the regulator. For example, if the regulator is operating normally at 50 mA, but for 12.5% of the time it operates at 500 mA output, the total power dissipation of the part can be easily determined. First, calculate the power dissipation of the device at 50 mA. We will use the MIC5219-3.3YM5 with 5V input voltage as our example.

EQUATION 4-9:

$$P_D \times 50mA = (5V - 3.3V) \times 50mA + 5V \times 650\mu A$$

$$P_D \times 50mA = 88.25mW$$

方程 4-7：

$$P_{D(MAX)} = 455\text{毫瓦} = (V_{IN} - V_{OUT}) \times I_{\text{输出端}} + V_{IN} \times I_{GND}$$

其中：

I输出端 = 500 毫安

V输出端 = 5V

I接地 = 20 毫安

$$455\,mW = (V_{IN} - 5V) \times 500\,mA + V_{IN} \times 20\,mA$$

$$2.995\,W = 520\,mA \times V_{IN}$$

$$V_{IN(MAX)} = \frac{2.995\text{瓦}}{520\text{毫安}} = 5.683\text{伏}$$

因此，为了在室温下从 MIC5219-5.0YM5 获得恒定的 500 毫安输出电流，输入与输出电压差必须非常严格，几乎仅略高于该电流等级的最大压降电压。

如果采取适当的预防措施，可以使用更高电压的电源驱动该器件。通过使能引脚调节占空比，可以通过保持较低的平均功率来增加器件的功率耗散。这非常适合仅在短时间内需要大电流的应用。图4-1显示了MIC5219-x.xYM5在三种不同环境温度及不同输出电流下的安全工作区域。绘制该图所用数据基于最小占地面积的PCB设计，以实现最小散热。图4-2考虑了与图4-1相同的因素，但假设采用了更优的散热器。

PCB上一块1英寸见方的铜迹线降低了器件的热阻。这种热阻的改善提升了功率耗散能力，扩大了安全工作区域。

图4-3和图4-4显示了MIC5219-x.xYMM功率MSOP封装器件的安全工作区域。这些图表展示了不同温度下的三个典型工作区域。温度越低，工作区域越大。这些图表的获取方法与MIC5219-x.xYM5的图表类似，综合考虑所有因素，并采用了两种不同的电路板布局：最小占地面积布局和1英寸平方铜制PCB散热片布局。有关PCB散热片特性的详细讨论，请参阅应用提示17——设计PCB散热片。

用于确定安全工作区域的信息可以通过类似方法获得，例如前文已讨论的典型功率耗散的确定。基于布局确定最大功率耗散是第一步，这一步与前两个部分的方法相同。然后，将较大的功率耗散数值乘以设定的最大占空比，即可得到该布局的最大功率耗散值。通过一个例子可以更好地说明这一点。如果应用要求在短脉冲中提供5V、500毫安的输出电流，而唯一可用的电源电压为8V，则必须调整占空比，以确定不超过布局最大功率耗散的平均功率。

公式 4-8：

$$\text{平均}P_D = \left(\frac{\%\text{占空比}}{100}\right)(V_{\text{输入}} - V_{\text{输出端}}) \times I_{OUT} + V_{IN} \times I_{GND}$$

$$455\text{毫瓦} = \left(\frac{\%\text{占空比}}{100}\right)(8V - 5V) \times 500\,mA + 8V \times 20\,mA$$

$$455\text{毫瓦} = \left(\frac{\%\text{占空比}}{100}\right) \times 1.66\,W$$

$$0.274 = \frac{\%\text{占空比}}{100}$$

$$\%\text{占空比}\text{最大}27.4\%$$

当输出电流为500毫安且MIC5219-xxYMM上的压降为3伏时，最大占空比为27.4%。

某些应用要求设定一个标称电流输出，同时在短时间内需要更大的电流。这虽然是一个棘手的问题，但可以轻松解决。计算每个电流阶段的平均功率耗散，然后将两者相加，得到稳压器的总功率耗散。例如，若稳压器正常工作时输出电流为50毫安，但有12.5%的时间输出电流为500毫安，则可以轻松计算出器件的总功率耗散。首先，计算器件在50毫安时的功率耗散。我们以输入电压为5V的MIC5219-3.3YM5为例。

公式 4-9：

$$P_D \times 50\,mA = (5V - 3.3\,V) \times 50\,mA + 5V \times 650\,\mu A$$

$$P_D \times 50\,mA = 88.25\text{毫瓦}$$

However, this is continuous power dissipation, the actual on-time for the device at 50 mA is (100% – 12.5%) or 87.5% of the time, or 87.5% duty cycle. Therefore, P_D must be multiplied by the duty cycle to obtain the actual average power dissipation at 50 mA.

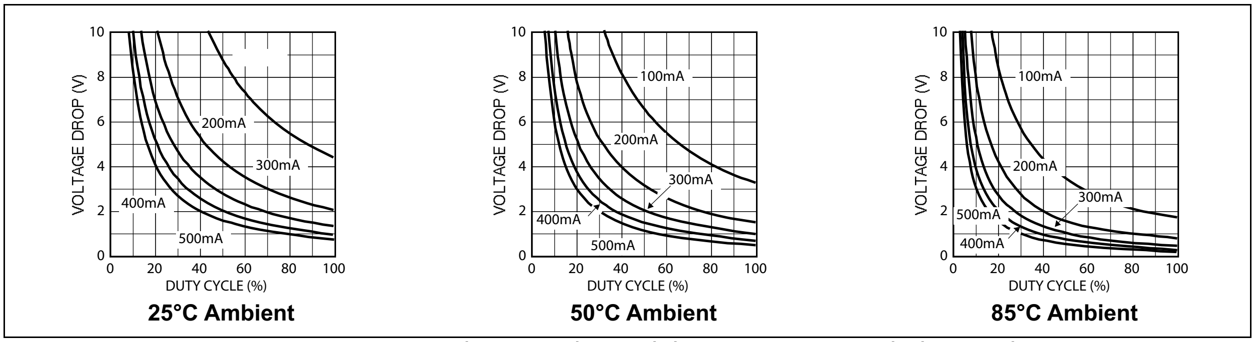


FIGURE 4-1: *MIC5219-x.xYM5 (SOT23-5) on Minimum Recommended Footprint.*

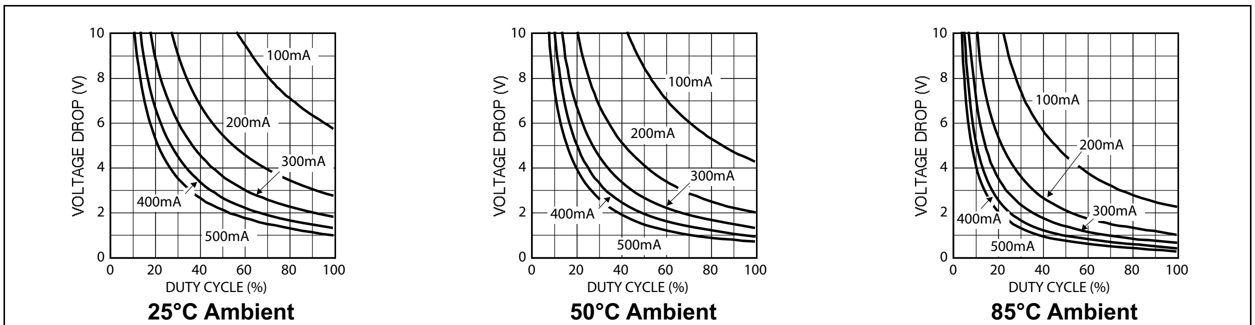


FIGURE 4-2: *MIC5219-x.xYM5 (SOT23-5) on 1-Inch² Copper Cladding.*

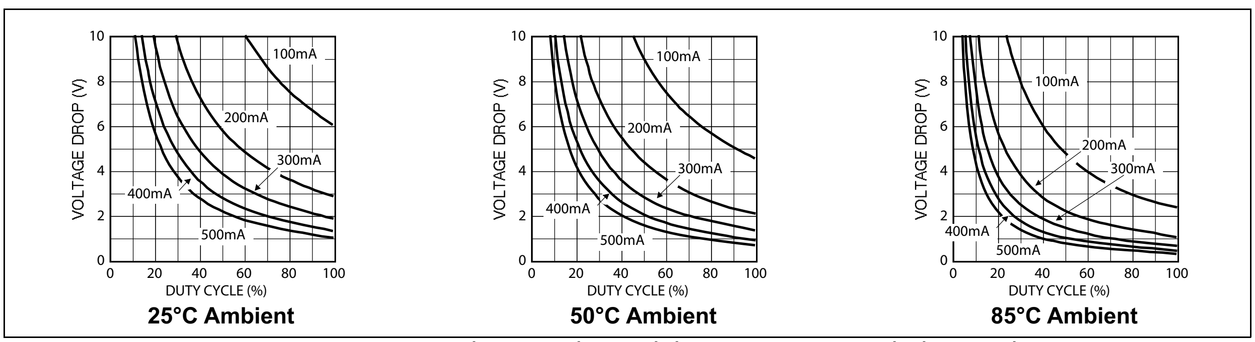


FIGURE 4-3: *MIC5219-x.xYMM (MSOP-8) on Minimum Recommended Footprint.*

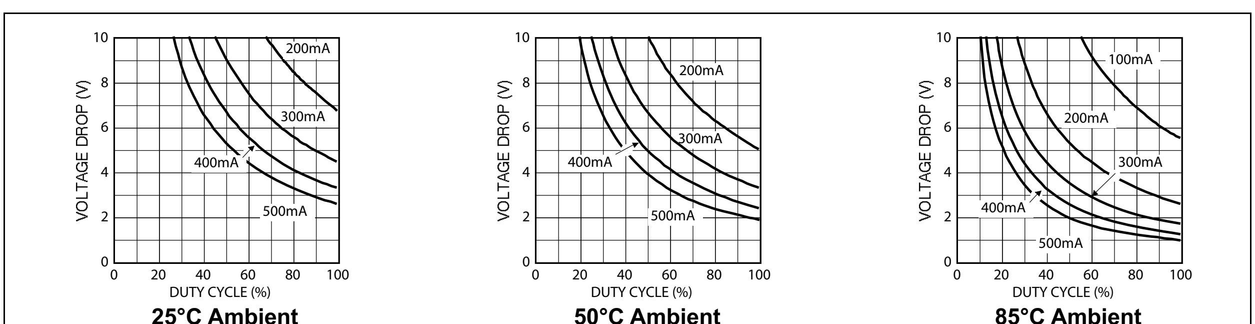


FIGURE 4-4: *MIC5219-x.xYMM (MSOP-8) on 1-Inch² Copper Cladding.*

然而，这是连续功率耗散，器件在50毫安时的实际导通时间为（100% – 12.5%），即87.5%的时间，或87.5%的占空比。因此，P_D必须乘以占空比，才能得到50毫安时的实际平均功率耗散。

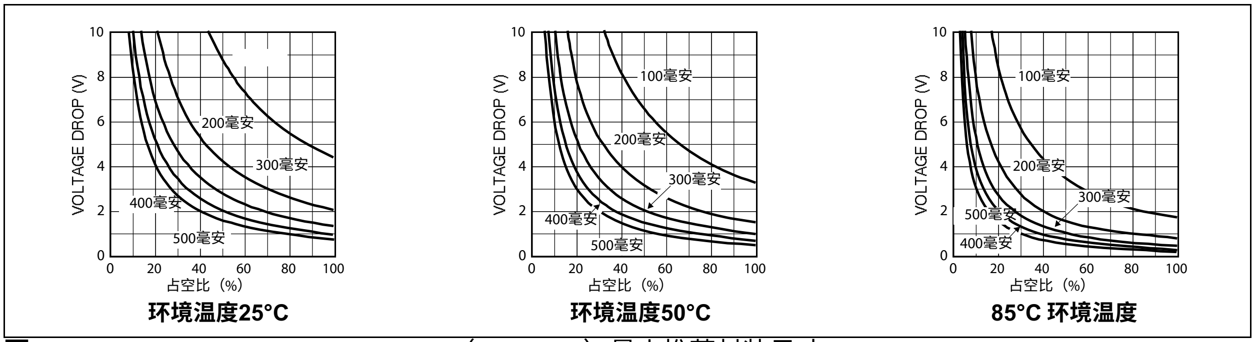


图*4-1*： *MIC5219-x.xYM5*（*SOT23-5*）最小推荐封装尺寸。

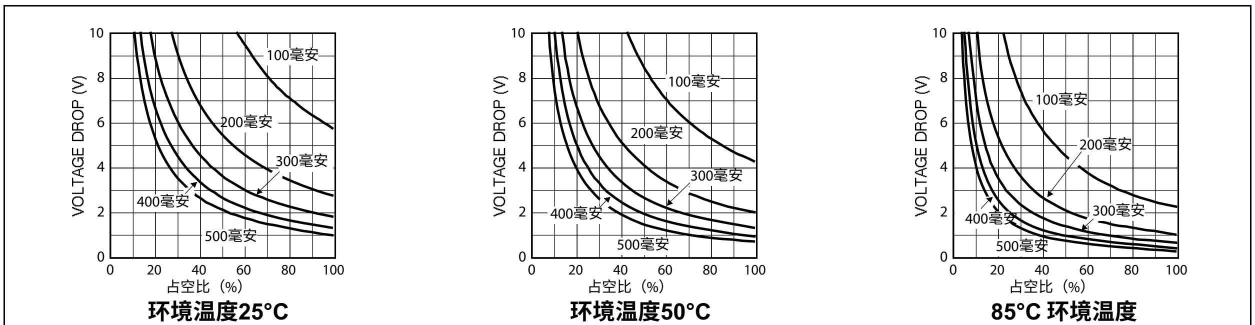


图*4-2*： *MIC5219-x.xYM5*（*SOT23-5*）*1*平方英寸铜覆层。

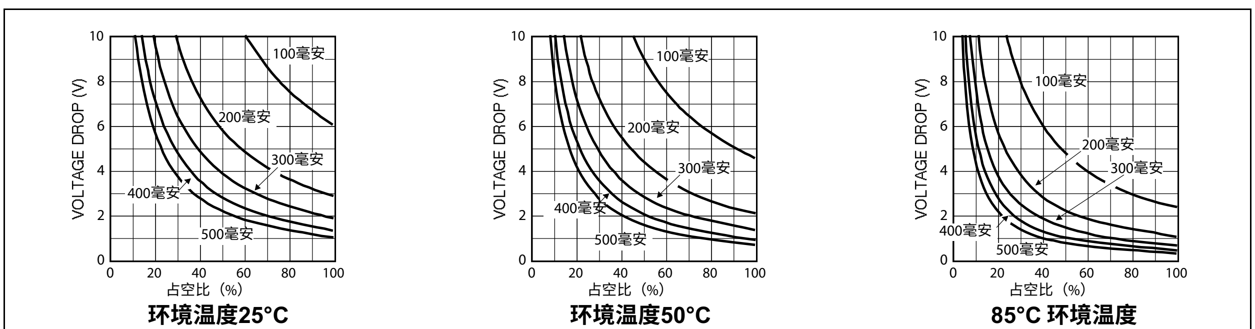


图*4-3*： *MIC5219-x.xYMM*（*MSOP-8*）最小推荐封装尺寸。

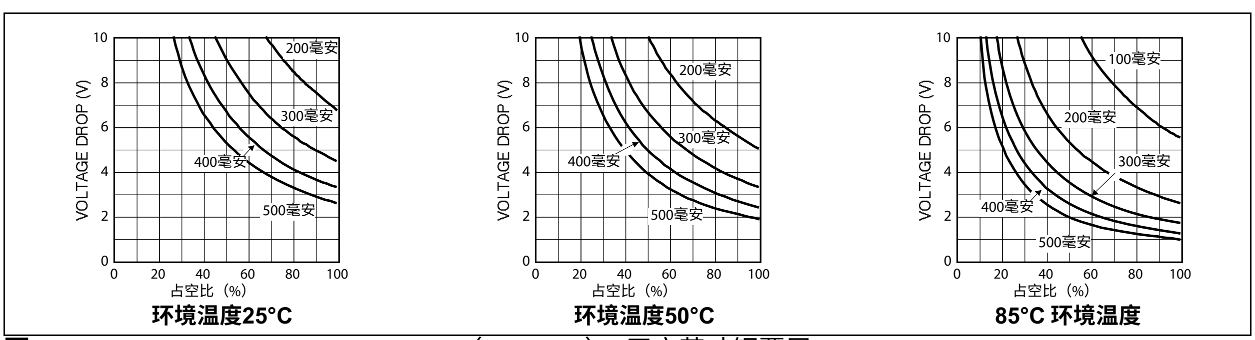


图*4-4*： *MIC5219-x.xYMM*（*MSOP-8*）*1*平方英寸铜覆层。

EQUATION 4-10:

$$P_D \times 50mA = 0.875 \times 88.25mW$$

$$P_D \times 50mA = 77.22mW$$

The power dissipation at 500 mA must also be calculated.

EQUATION 4-11:

$$P_D \times 500mA = (5V - 3.3V) \times 500mA + 5V \times 20mA$$

$$P_D \times 500mA = 950mW$$

This number must be multiplied by the duty cycle at which it would be operating: 12.5%.

EQUATION 4-12:

$$P_D = 0.125 \times 950mW$$

$$P_D = 118.75mW$$

The total power dissipation of the device under these conditions is the sum of the two power dissipation figures.

EQUATION 4-13:

$$P_{D(TOTAL)} = P_D \times 50mA + P_D \times 500mA$$

$$P_{D(TOTAL)} = 77.22mW + 118.75mW$$

$$P_{D(TOTAL)} = 196mW$$

The total power dissipation of the regulator is less than the maximum power dissipation of the SOT23-5 package at room temperature, on a minimum footprint board and therefore would operate properly.

Multilayer boards with a ground plane, wide traces near the pads, and large supply-bus lines will have better thermal conductivity.

For additional heat sink characteristics, please refer to Application Hint 17, Designing P.C. Board Heat Sinks. For a full discussion of heat sinking and thermal effects on voltage regulators, refer to "Regulator Thermals" section of Microchip's Designing with Low-Dropout Voltage Regulators handbook.

4.8 Fixed Regulator Circuits

Figure 4-5 shows a basic MIC5219-x.xYMX fixed-voltage regulator circuit. A 1µF minimum output capacitor is required for basic fixed-voltage applications.

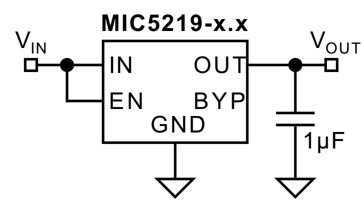


FIGURE 4-5: *Low-Noise Fixed Voltage Regulator.*

Figure 4-6 includes the optional 470 pF noise bypass capacitor between BYP and GND to reduce output noise. Note that the minimum value of C_{OUT} must be increased when the bypass capacitor is used.

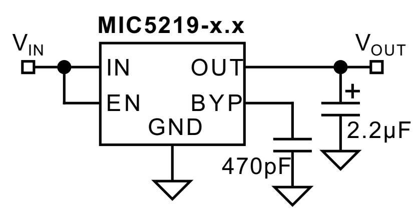


FIGURE 4-6: *Ultra-Low Noise Fixed Voltage Regulator.*

4.9 Adjustable Regulator Circuits

Figure 4-7 shows the basic circuit for the MIC5219 adjustable regulator. The output voltage is configured by selecting values for R1 and R2 using the following formula.

EQUATION 4-14:

$$V_{OUT} = 1.242V \times \left(\frac{R2}{R1} + 1\right)$$

This equation is correct due to the configuration of the bandgap reference. The bandgap voltage is relative to the output, as seen in the block diagram. Traditional regulators normally have the reference voltage relative to ground and have a different V_{OUT} equation.

公式 4-10：

$$P_D \times 50mA = 0.875 \times 88.25\,mW$$

$$P_D \times 50mA = 77.22\text{毫瓦}$$

还需计算500毫安时的功率耗散。

公式 4-11：

$$P_D \times 500mA = (5V - 3.3V) \times 500mA + 5V \times 20mA$$

$$P_D \times 500mA = 950\text{毫瓦}$$

该数值需乘以其工作时的占空比：12.5%。

公式 4-12：

$$P_D = 0.125 \times 950mW$$

$$P_D = 118.75\text{毫瓦}$$

在这些条件下，器件的总功率耗散为两个功率耗散数值之和。

公式 4-13：

$$P_{D(设计)} = P_D \times 50mA + P_D \times 500mA$$

$$P_{D(设计)} = 77.22\text{毫瓦} + 118.75\text{毫瓦}$$

$$P_{D(设计)} = 196\text{毫瓦}$$

稳压器的总功率耗散低于SOT23-5封装在室温、最小占地面积电路板上的最大功率耗散，因此能够正常工作。

采用接地平面、多层电路板、焊盘附近宽走线及大电源总线的电路板，热传导性能更佳。

有关额外散热器特性，请参阅应用提示17“设计印刷电路板散热器”。有关散热及热效应对稳压器的全面讨论，请参阅Microchip《低压差线性稳压器设计》手册中的“稳压器热学”章节。

4.8 固定稳压器电路

图4-5 展示了一个基本的MIC5219-x.xYMX固定电压稳压器电路。基本固定电压应用至少需要1μF的输出电容。

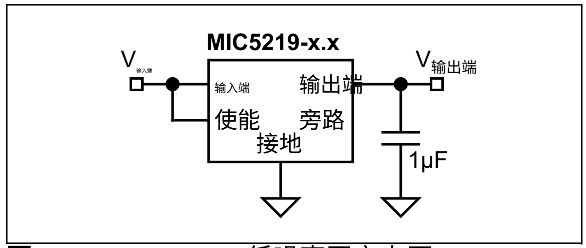


图4-5： 低噪声固定电压稳压器

图4-6中包含了可选的470 pF噪声旁路电容，连接于BYP与GND之间，以降低输出噪声。注意，使用旁路电容时，必须增加C_{OUT}的最小值。

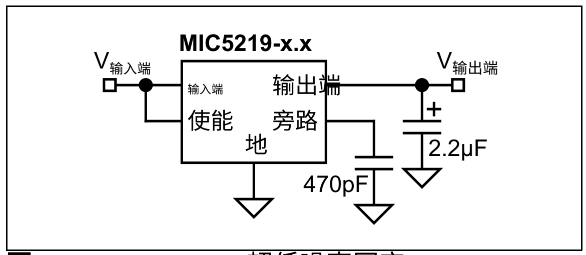


图4-6： 超低噪声固定电压稳压器

4.9 可调稳压器电路

图4-7展示了MIC5219可调稳压器的基本电路。输出电压通过选择R1和R2的阻值，并使用以下公式进行设定。

公式4-14：

$$V_{OUT} = 1.242\text{伏特}\left(\frac{R2}{R1} + 1\right)$$

由于带隙基准的配置，该方程是正确的。带隙电压相对于输出端，如框图所示。传统稳压器通常将参考电压相对于地，且具有不同的V_{OUT}方程。

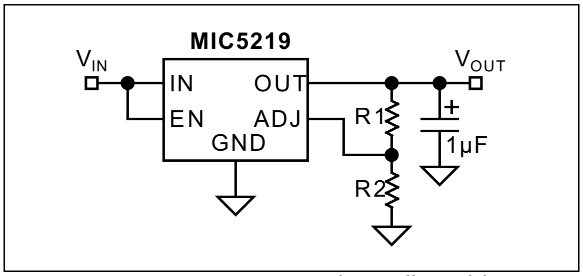


FIGURE 4-7: Low-Noise Adjustable Voltage Regulator.

Although ADJ is a high-impedance input, for best performance, R2 should not exceed 470 kΩ.

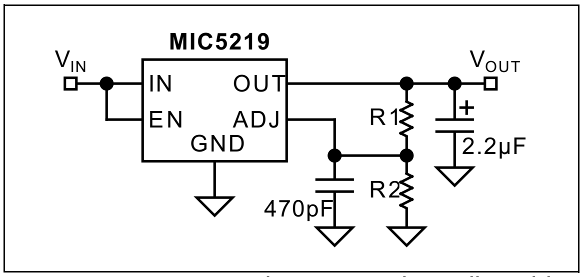


FIGURE 4-8: Ultra-Low Noise Adjustable Application.

Figure 4-8 includes the optional 470 pF bypass capacitor from ADJ to GND to reduce output noise.

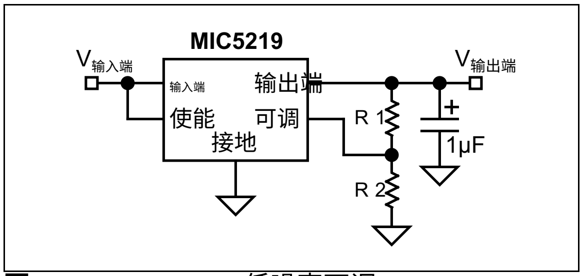


图4-7： 低噪声可调电压稳压器。

虽然ADJ为高阻抗输入，但为获得最佳性能，R2不应超过470 kΩ。

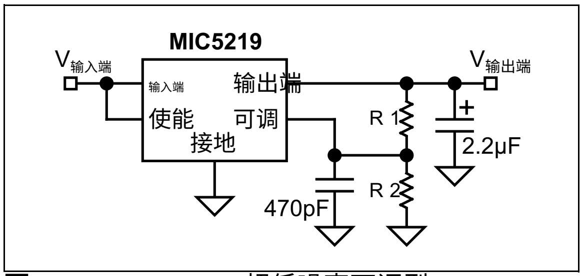
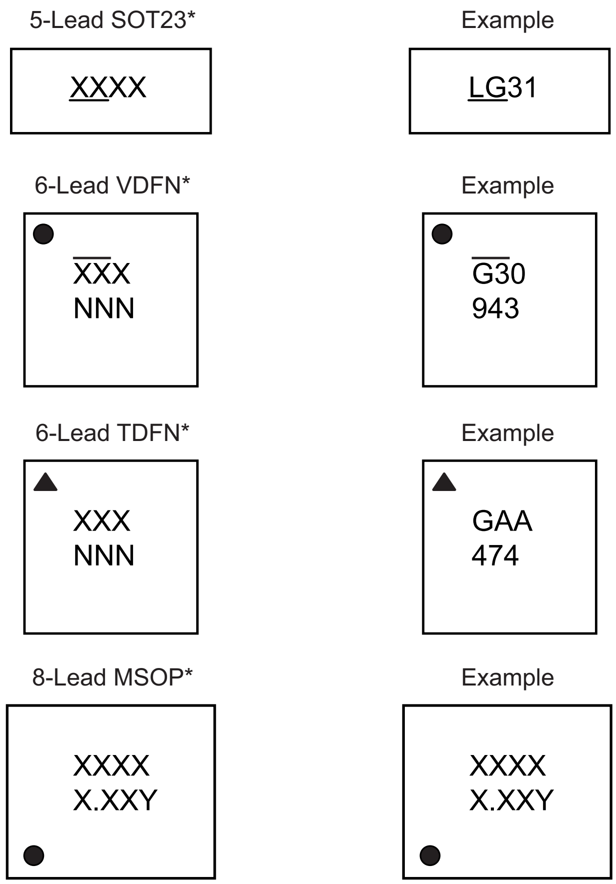


图 4-8： 超低噪声可调型应用示例。

图 4-8 包含从 ADJ 到 GND 的可选 470 pF 旁路电容，用于降低输出噪声。

5.0 PACKAGING INFORMATION

5.1 Package Marking Information



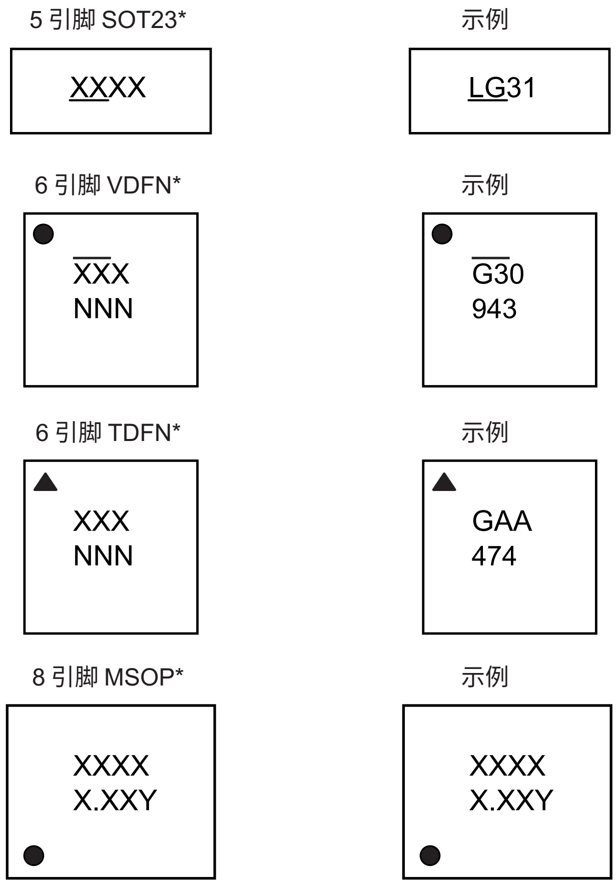
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).	

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

5.0 包装信息

5.1 封装标识信息



图例：	XX...X	产品代码或客户专用信息
	Y	年份代码（公历年份最后一位数字）
	YY	年份代码（公历年份最后两位数字）
	WW	周代码（1月1日所在周为第‘01’周）
	NNN	字母数字追溯代码
	(e3)	无铅JEDEC®哑光锡（Sn）标识
	*	该封装为无铅。无铅JEDEC标识（）可见于该封装的外包装上。
	●、▲、▼ 引脚1标记以点、向上三角或向下三角（△标记）表示。	

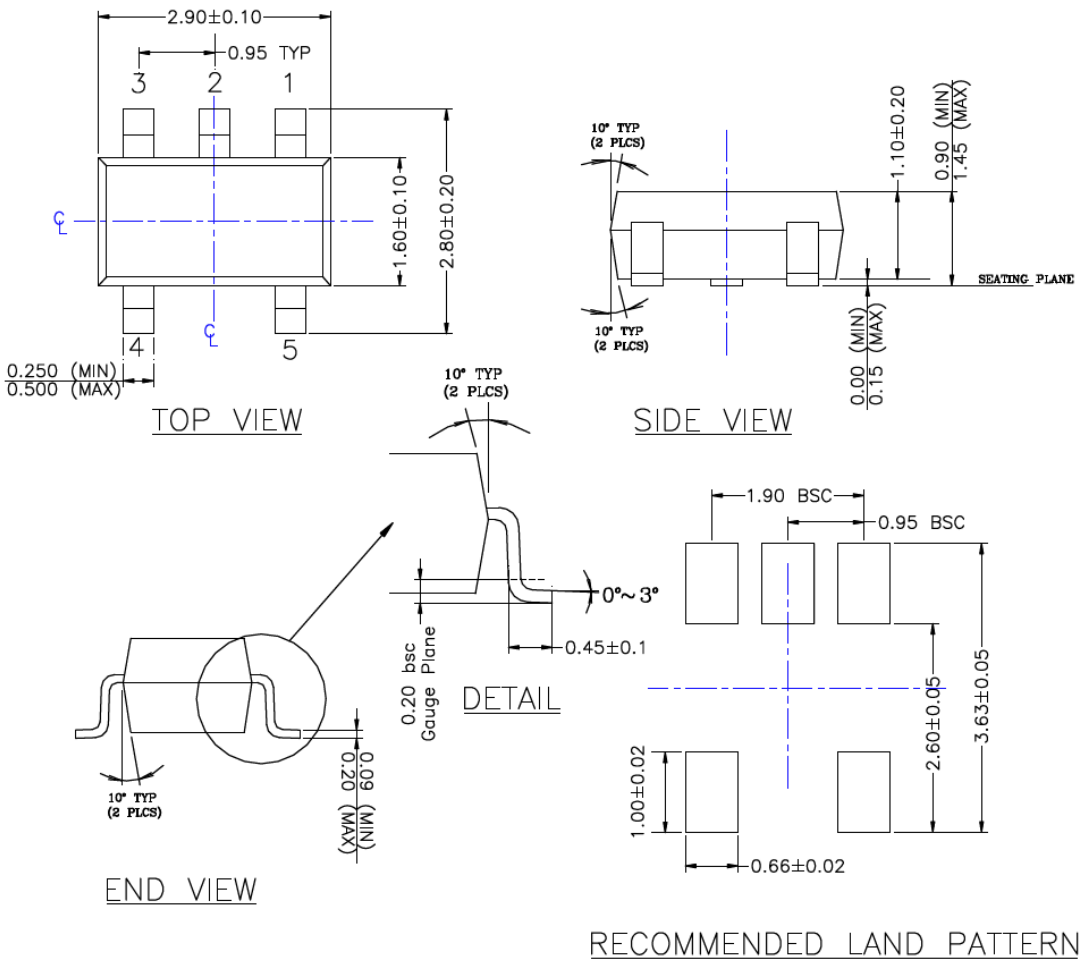
注意：若完整的Microchip零件编号无法标注于一行，将转至下一行，从而限制客户专用信息的可用字符数。封装可能包含或不包含公司标志。

下划线（_）和/或上划线（¯）符号可能不按比例显示。

5-Lead SOT23 Package Outline and Recommended Land Pattern

TITLE
5 LEAD SOT23 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOT23-5LD-PL-1	UNIT	MM



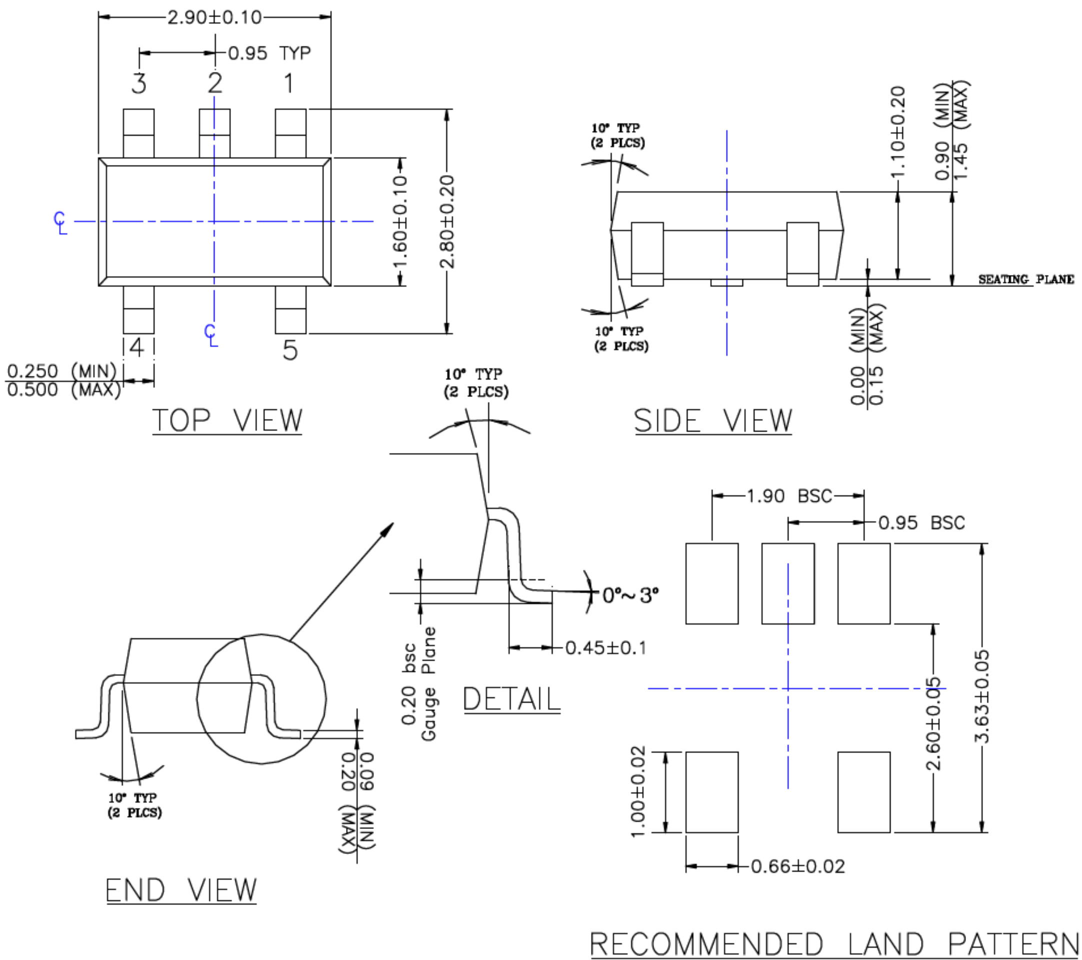
NOTE:
1. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & BURR.
2. PACKAGE OUTLINE INCLUSIVE OF SOLER PLATING.
3. DIMENSION AND TOLERANCE PER ANSI Y14.5M, 1982.
4. FOOT LENGTH MEASUREMENT BASED ON GAUGE PLANE METHOD.
5. DIE FACES UP FOR MOLD, AND FACES DOWN FOR TRIM/FORM.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

5引脚 SOT23 封装轮廓及推荐焊盘图

TITLE
5 LEAD SOT23 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOT23-5LD-PL-1	UNIT	MM



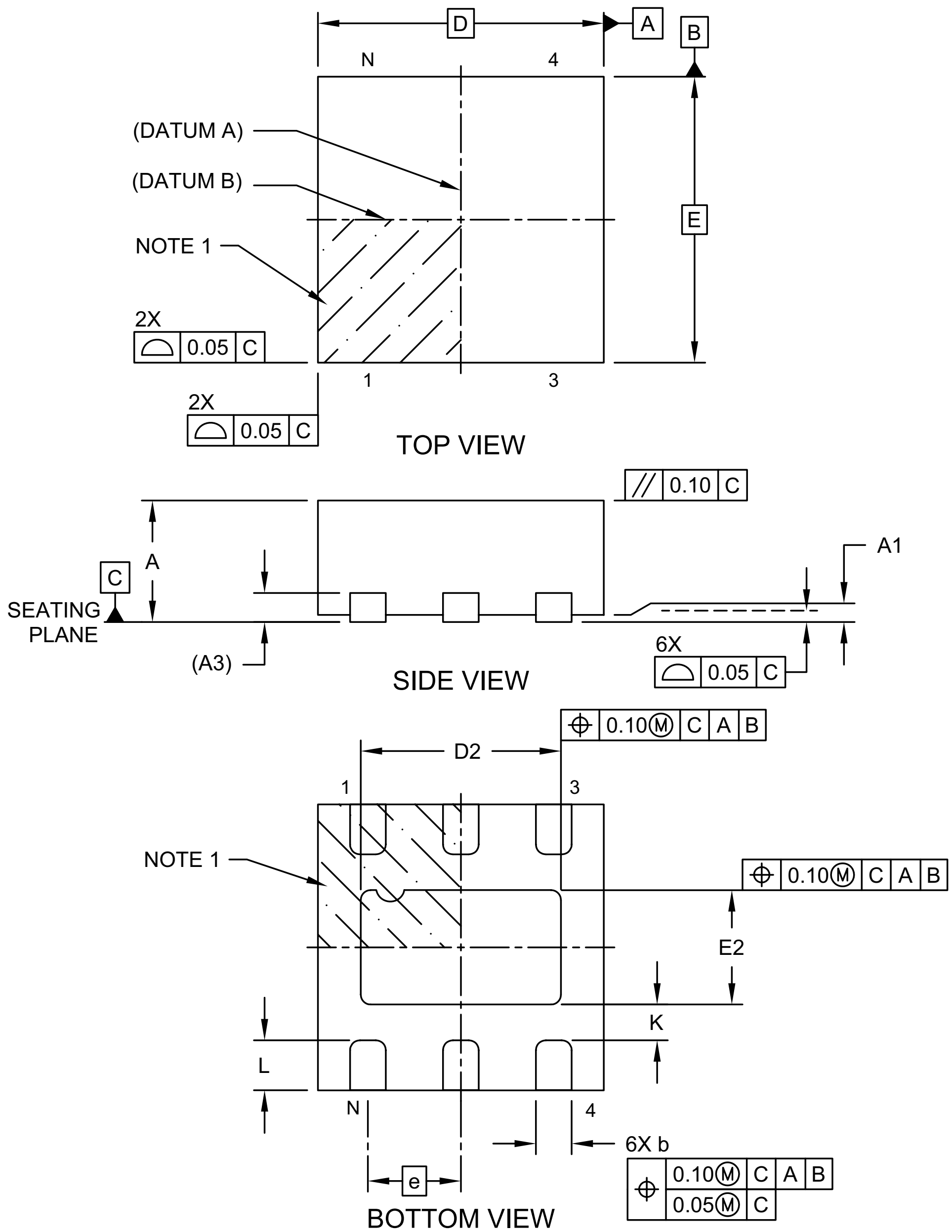
NOTE:
1. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & BURR.
2. PACKAGE OUTLINE INCLUSIVE OF SOLER PLATING.
3. DIMENSION AND TOLERANCE PER ANSI Y14.5M, 1982.
4. FOOT LENGTH MEASUREMENT BASED ON GAUGE PLANE METHOD.
5. DIE FACES UP FOR MOLD, AND FACES DOWN FOR TRIM/FORM.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

注：有关最新封装图纸，请参阅位于 http://www.microchip.com/packaging 的 Microchip封装规范。

6-Lead VDFN 2 mm x 2 mm Package Outline and Recommended Land Pattern

6-Lead Very Thin Plastic Dual Flat, No Lead Package (JDA) - 2x2 mm Body [VDFN] Micrel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

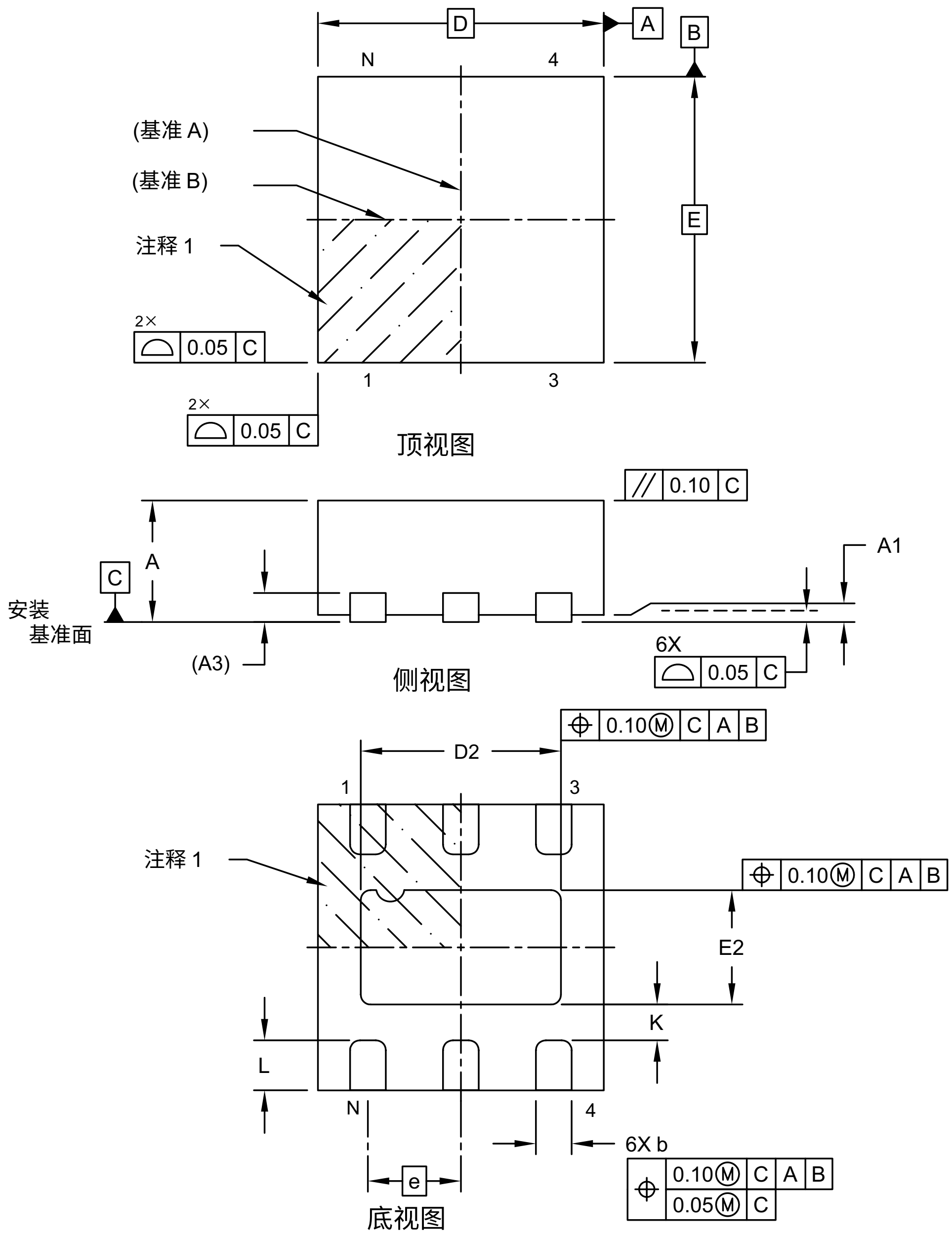


Microchip Technology Drawing C04-1016A Sheet 1 of 2

6引脚 VDFN 2 mm x 2 mm 封装轮廓及推荐焊盘图

6引脚超薄塑料无引脚双扁平封装（JDA）- 2×2 毫米封装 [VDFN]
Micrel 传统封装

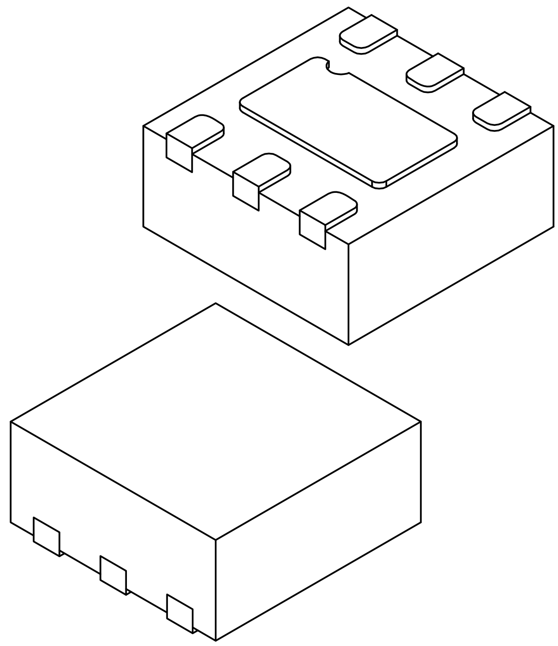
注意：	有关最新封装图纸，请参阅位于 http://www.microchip.com/packaging 的 Microchip封装规范。



Microchip Technology 图纸 C04-1016A 第1页，共2页

6-Lead Very Thin Plastic Dual Flat, No Lead Package (JDA) - 2x2 mm Body [VDFN] Micrel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.75	0.80	0.85
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

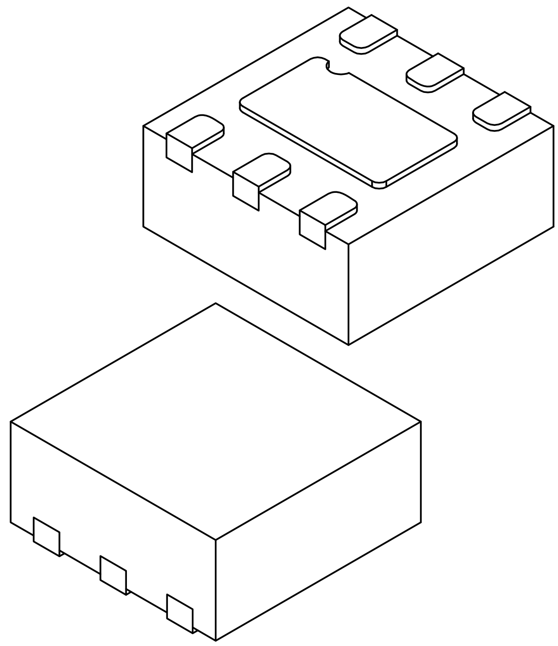
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1016A Sheet 2 of 2

6引脚超薄塑料无引脚双扁平封装（JDA）- 2×2 毫米封装 [VDFN] Micrel传统封装

注意： 有关最新封装图纸，请参阅位于 http://www.microchip.com/packaging 的 Microchip封装规范。



	单位	毫米		
尺寸极限		最小值	标称值	最大值
引脚数量	N	6		
间距	e	0.65 BSC		
整体高度	A	0.80	0.85	0.90
支撑高度	A1	0.00	0.02	0.05
端子厚度	A3	0.203 REF		
整体长度	D	2.00 BSC		
裸露焊盘长度	D2	1.35	1.40	1.45
整体宽度	E	2.00 BSC		
露出焊盘宽度	E2	0.75	0.80	0.85
端子宽度	b	0.20	0.25	0.30
端子长度	L	0.30	0.35	0.40
引脚至裸露焊盘距离	K	0.20	-	-

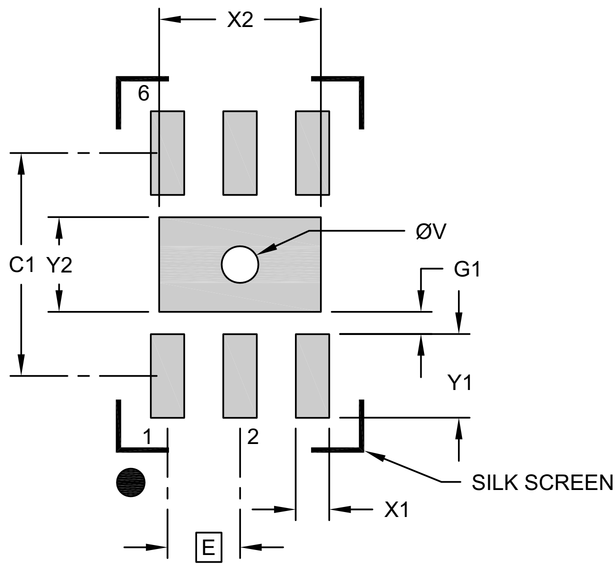
注：

1. 引脚1的视觉标记可能有所不同，但必须位于阴影区域内。
2. 封装采用锯切分离工艺
3. 尺寸和公差依据ASME Y14.5M标准
   BSC：基本尺寸。理论上显示的精确值，不含公差。
   REF：参考尺寸，通常无公差，仅供参考。

Microchip Technology 图纸 C04-1016A 第2页，共2页

6-Lead Very Thin Plastic Dual Flat, No Lead Package (JDA) - 2x2 mm Body [VDFN] Micrel Legacy Package

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			0.85
Optional Center Pad Length	Y2			1.45
Contact Pad Spacing	C1		2.00	
Contact Pad Width (X6)	X1			0.30
Contact Pad Length (X6)	Y1			0.75
Contact Pad to Center Pad (X6)	G1	0.20		
Thermal Via Diameter	V	0.27	0.30	0.33

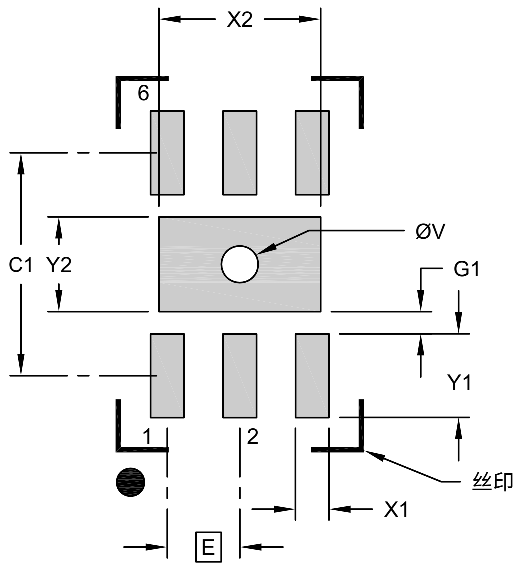
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-21016A

6引脚超薄塑料无引脚双扁平封装（JDA）- 2×2 毫米封装 [VDFN]
Micrel传统封装

注意： 有关最新封装图纸，请参阅位于 http://www.microchip.com/packaging 的 Microchip封装规范。



推荐焊盘布局

		单位	毫米	
尺寸极限		最小值	标称值	最大值
引脚间距	E		0.65 BSC	
可选中心焊盘宽度	X2			0.85
可选中心焊盘长度	Y2			1.45
接触焊盘间距	C1		2.00	
接触焊盘宽度（X6）	X1			0.30
引脚焊盘长度（X6）	Y1			0.75
接触焊盘至中心焊盘距离（X6）	G1	0.20		
散热通孔直径	V	0.27	0.30	0.33

注：

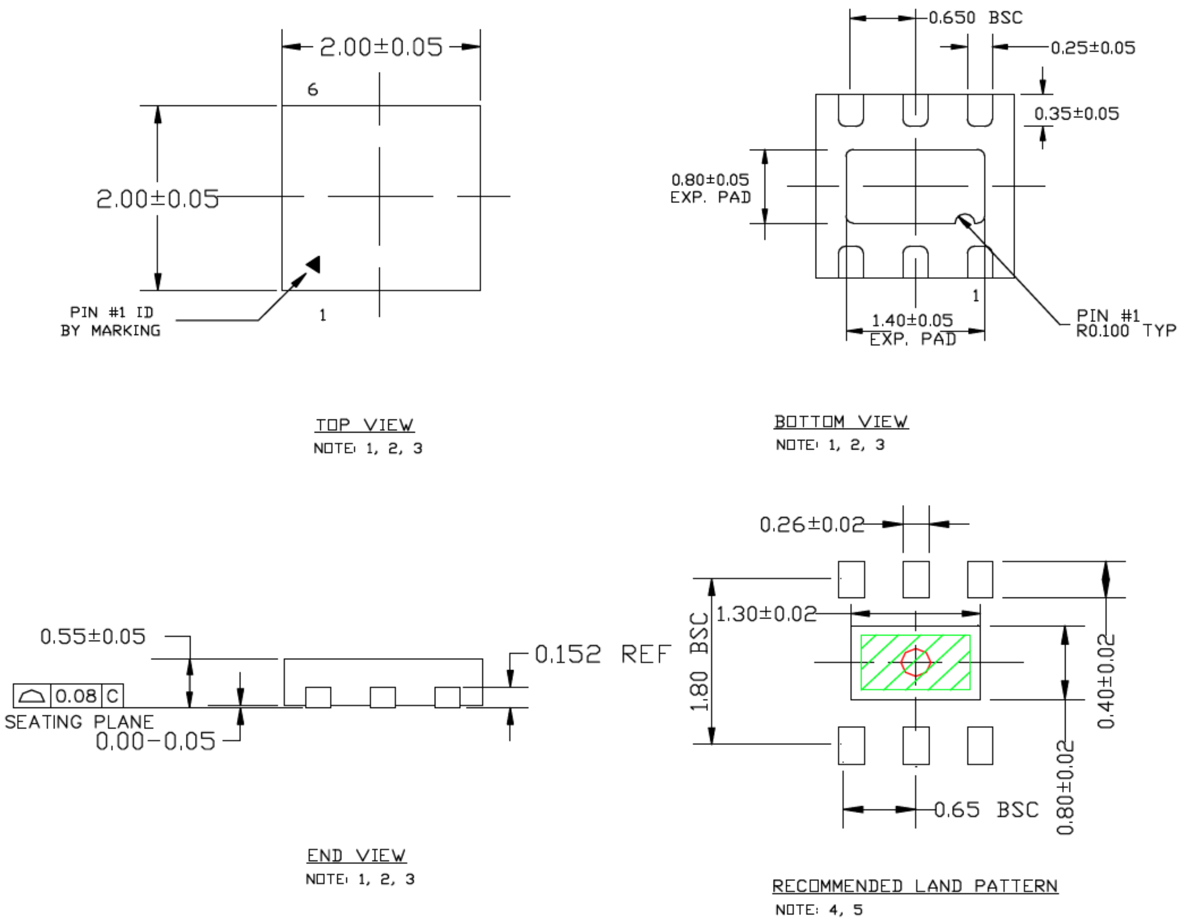
1. 尺寸和公差依据ASME Y14.5M标准
   BSC：基本尺寸。理论上显示的精确值，不含公差。
2. 为获得最佳焊接效果，如使用散热通孔，应进行填充或覆盖，以避免回流焊过程中焊料流失

Microchip Technology 图纸 C04-21016A

6-Lead 2 mm x 2 mm TDFN Package Outline and Recommended Land Pattern

TITLE
6 LEAD TDFN 2x2mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN (0.65mm lead pitch)

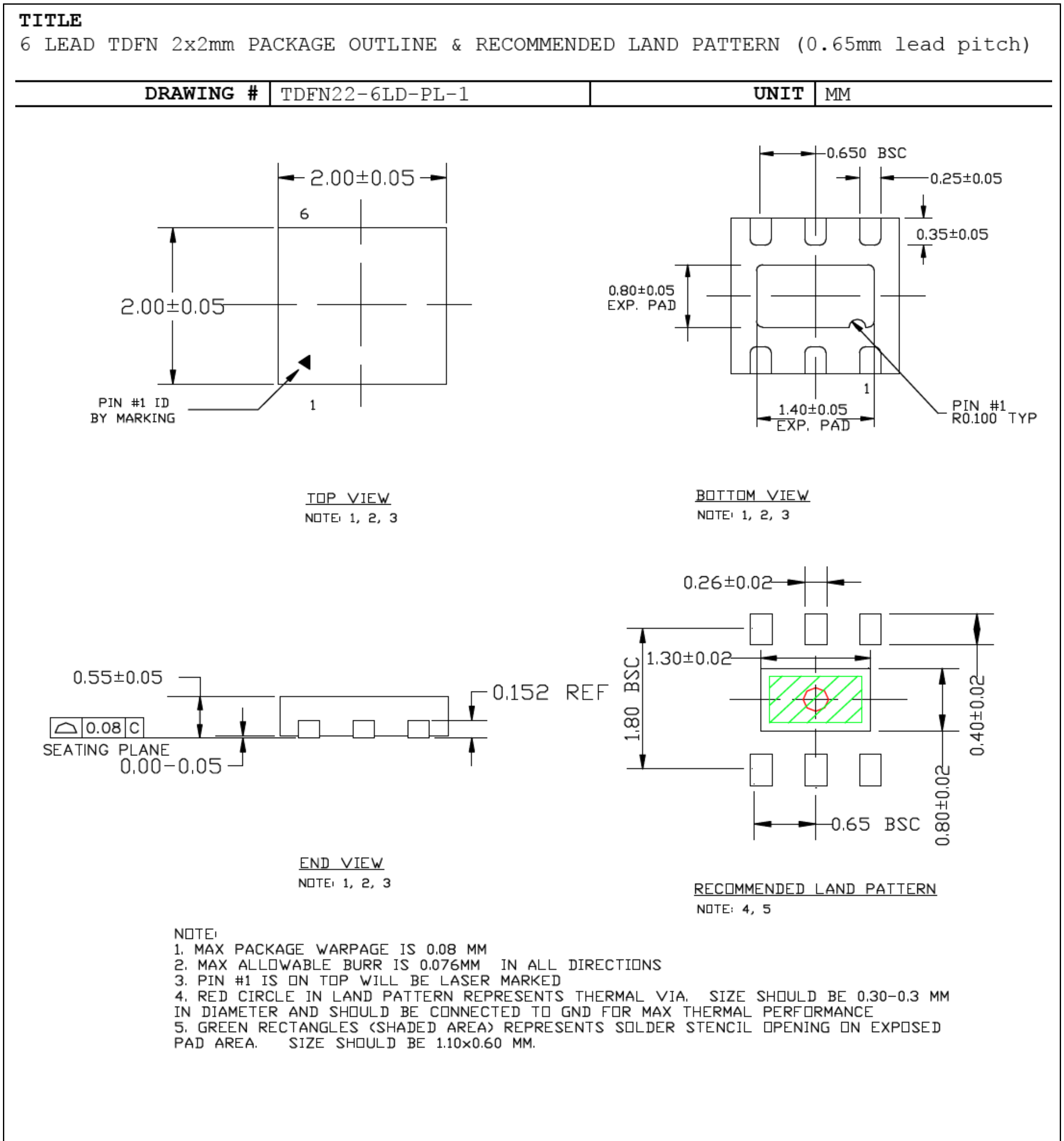
DRAWING #	TDFN22-6LD-PL-1	UNIT	MM



NOTE:
1. MAX PACKAGE WARPAGE IS 0.08 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN REPRESENTS THERMAL VIA. SIZE SHOULD BE 0.30-0.3 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) REPRESENTS SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 1.10x0.60 MM.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

6引脚 2 mm × 2 mm TDFN 封装轮廓及推荐焊盘布局

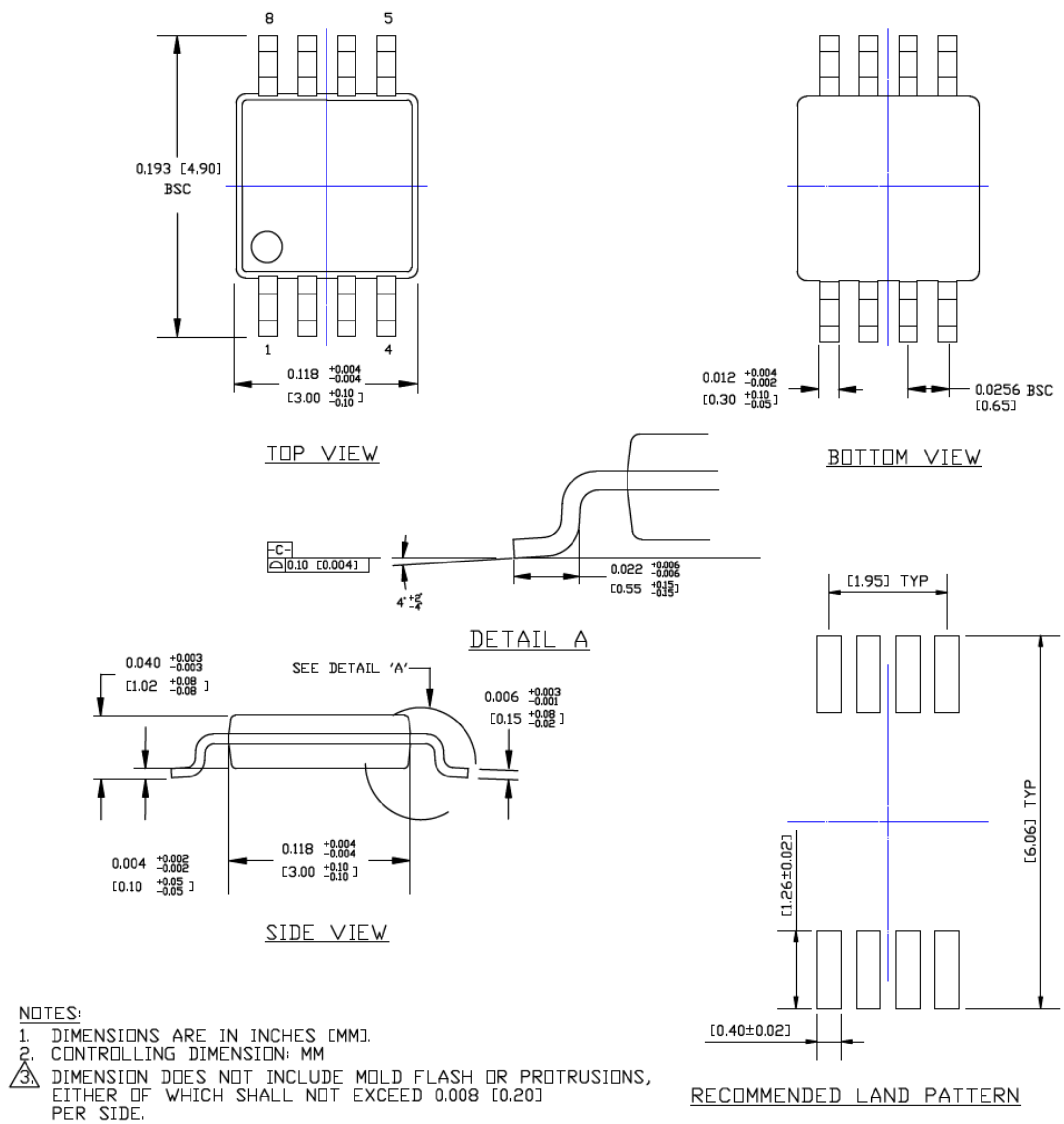


注：有关最新封装图纸，请参阅位于 http://www.microchip.com/packaging 的 Microchip封装规范。

8-Lead MSOP Package Outline and Recommended Land Pattern

TITLE
8 LEAD MSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	MSOP-8LD-PL-1	**UNIT**	INCH [MM]

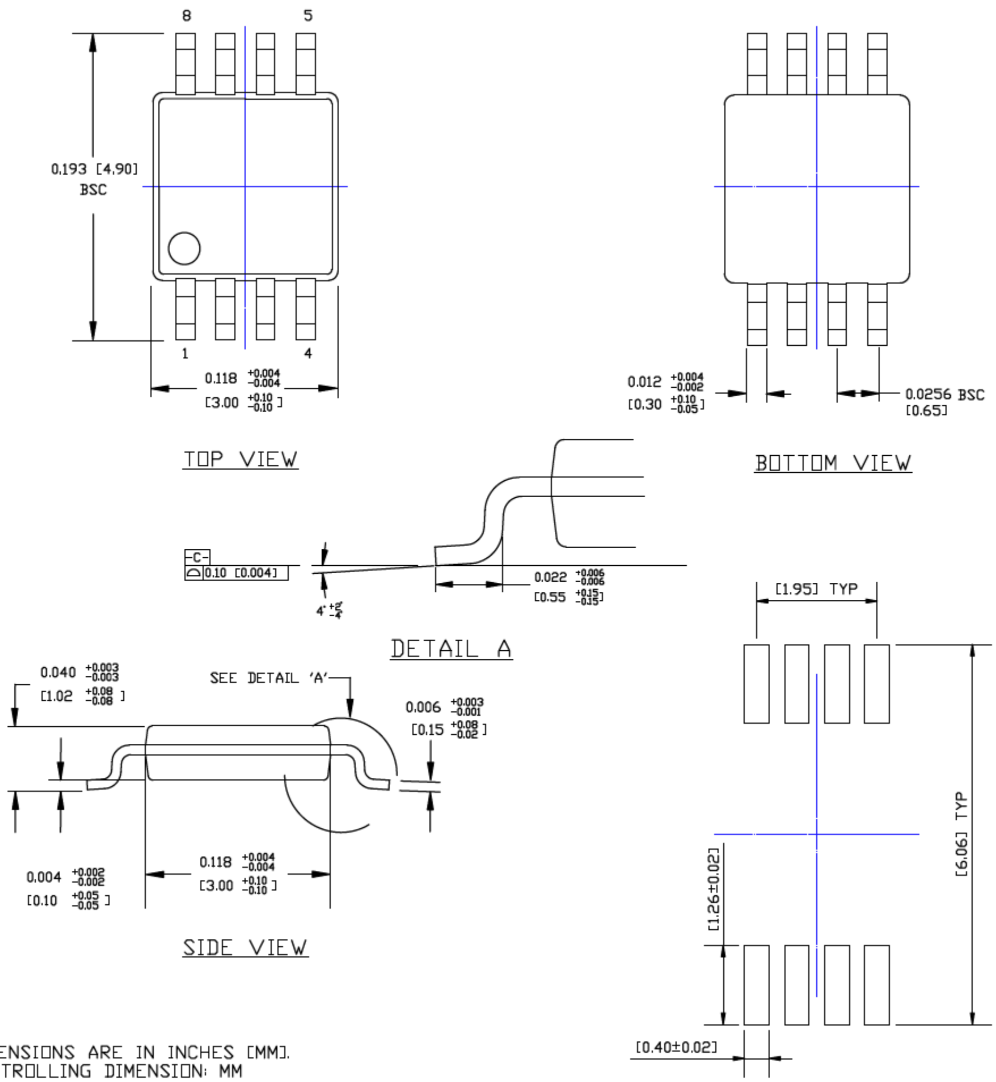


Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

8引脚 MSOP 封装轮廓及推荐焊盘布局

TITLE
8 LEAD MSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	MSOP-8LD-PL-1	UNIT	INCH [MM]



NOTES:
1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.20] PER SIDE.

注：有关最新封装图纸，请参阅位于 http://www.microchip.com/packaging 的 Microchip封装规范。

NOTES:

注释：

APPENDIX A: REVISION HISTORY

Revision A (May 2018)

- Converted Micrel document MIC5219 to Microchip data sheet DS20006021A.
- Minor text changes throughout.

附录A：修订历史

修订版A（2018年5月）

- 将Micrel文档MIC5219转换为Microchip数据手册DS20006021A。
- 全文进行了小幅文字修改。

NOTES:

注释：

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	X.X	X	XX	-XX
Part No.	Voltage	Junction Temp. Range	Package	Media Type

Device:	MIC5219: 500 mA Peak Output LDO Regulator
Voltage:	2.5 = 2.5V (SOT23, MSOP Packages) 2.6 = 2.6V (SOT23 Package) 2.7 = 2.7V (SOT23 Package) 2.8 = 2.8V (VDFN Package) 2.85 = 2.85V (SOT23, MSOP Packages) 2.9 = 2.9V (SOT23 Package) 3.0 = 3.0V (SOT23, MSOP, VDFN Packages) 3.1 = 3.1V (SOT23 Package) 3.3 = 3.3V (SOT23, MSOP, VDFN Packages) 3.6 = 3.6V (SOT23, MSOP Packages) 5.0 = 5.0V (SOT23, MSOP, TDFN Packages) <blank> = ADJ (SOT23, MSOP, TDFN Packages)
Junction Temperature Range:	Y = –40°C to +125°C
Package:	M5 = 5-Lead SOT23 ML = 6-Lead 2 mm x 2 mm x 0.9 mm VDFN MT = 6-Lead 2 mm x 2 mm x 0.6 mm TDFN MM = 8-Lead MSOP
Media Type:	TR = 3,000/Reel (SOT23) TX = 3,000/Reel (SOT23 Reverse Pin 1 orientation) TR = 2,500/Reel (MSOP) TR = 5,000/Reel (VDFN and TDFN) <blank>= 100/Tube (MSOP)

Note: Other voltage options available. Contact your Microchip Sales Office.

Examples:

a) 5-Lead SOT23, 500 mA Peak Output Current Capability, Adjustable & Fixed Output Voltages, 3,000/Reel.

Catalog P/N	Output Voltage	Marking Code
MIC5219-2.5YM5-TR	2.5V	LG25
MIC5219-2.6YM5-TR	2.6V	LG26
MIC5219-2.7YM5-TR	2.7V	LG27
MIC5219-2.8YM5-TR	2.8V	LG28
MIC5219-2.85YM5-TR	2.85V	LG2J
MIC5219-2.9YM5-TR	2.9V	LG29
MIC5219-3.0YM5-TR	3.0V	LG30
MIC5219-3.1YM5-TR	3.1V	LG31
MIC5219-3.3YM5-TR	3.3V	LG33
MIC5219-3.6YM5-TR	3.6V	LG36
MIC5219-5.0YM5-TR	5.0V	LG50
MIC5219YM5-TR	Adjustable	

b) 6-Lead VDFN, 500 mA Continuous Output Current Capability, Adjustable & Fixed Output Voltages, 5,000/Reel

Catalog P/N	Output Voltage	Marking Code
MIC5219-2.8YML-TR	2.8V	G28
MIC5219-3.0YML-TR	3.0V	G30
MIC5219-3.3YML-TR	3.3V	G33
MIC5219-3.6YML-TR	3.6V	G36

c) 6-Lead TDFN, 500 mA Continuous Output Current Capability, Adjustable & Fixed Output Voltages, 5,000/Reel

Catalog P/N	Output Voltage	Marking Code
MIC5219-5.0YMT-TR	5.0V	G50
MIC5219YMT-TR	Adjustable	GAA

d) 8-Lead MSOP, 500 mA Continuous Output Current Capability, Adjustable & Fixed Output Voltages, 100/Tube or 2,500/Reel

CPN Bulk	Qty	CPN T/R	Qty
MIC5219-2.5YMM	100/Tube	MIC5219-2.5YMM-TR	2,500/Reel
MIC5219-2.85YMM	100/Tube	MIC5219-2.85YMM-TR	2,500/Reel
MIC5219-3.0YMM	100/Tube	MIC5219-3.0YMM-TR	2,500/Reel
MIC5219-3.3YMM	100/Tube	MIC5219-3.3YMM-TR	2,500/Reel
MIC5219-3.6YMM	100/Tube	MIC5219-3.6YMM-TR	2,500/Reel
MIC5219-5.0YMM	100/Tube	MIC5219-5.0YMM-TR	2,500/Reel
MIC5219YMM	100/Tube	MIC5219YMM-TR	2,500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

产品识别系统

如需订购或获取价格、交货等信息，请联系您当地的Microchip代表或销售办事处。

器件	X.X	X	XX	-XX
零件编号	电压	结温范围	封装	介质类型

器件： MIC5219: 500 毫安峰值输出低压差线性稳压器

电压：
2.5 = 2.5V（SOT23，MSOP封装）
2.6 = 2.6V（SOT23封装）
2.7 = 2.7 V（SOT23 封装）
2.8 = 2.8 V（VDFN 封装）
2.85 = 2.85 V（SOT23，MSOP 封装）
2.9 = 2.9 V（SOT23 封装）
3.0 = 3.0 V（SOT23，MSOP，VDFN 封装）
3.1 = 3.1 V（SOT23 封装）
3.3 = 3.3 V（SOT23，MSOP，VDFN 封装）
3.6 = 3.6 V（SOT23，MSOP 封装）
5.0 = 5.0 V（SOT23，MSOP，TDFN 封装）
<blank> = 可调（SOT23，MSOP，TDFN 封装）

结温范围： Y = –40°C 至 +125°C

封装：
M5 = 5 引脚 SOT23
ML = 6 引脚 2 mm × 2 mm × 0.9 mm VDFN
MT = 6 引脚 2 mm × 2 mm × 0.6 mm TDFN
MM = 8 引脚 MSOP

介质类型：
TR = 3,000/卷 (SOT23)
TX = 3,000/卷 (SOT23 反向引脚1方向)
TR = 2,500/卷 (MSOP)
TR = 5,000/卷 (VDFN 和 TDFN)
<空白> = 100/管 (MSOP)

注：提供其他电压选项。请联系Microchip销售办公室。

示例：

a) 5引脚SOT23封装，500毫安峰值输出电流能力，可调及固定输出电压，3,000/卷。

目录料号	输出电压	标记代码
MIC5219-2.5YM5-TR	2.5V	LG25
MIC5219-2.6YM5-TR	2.6V	LG26
MIC5219-2.7YM5-TR	2.7V	LG27
MIC5219-2.8YM5-TR	2.8V	LG28
MIC5219-2.85YM5-TR	2.85V	LG2J
MIC5219-2.9YM5-TR	2.9V	LG29
MIC5219-3.0YM5-TR	3.0V	LG30
MIC5219-3.1YM5-TR	3.1V	LG31
MIC5219-3.3YM5-TR	3.3V	LG33
MIC5219-3.6YM5-TR	3.6V	LG36
MIC5219-5.0YM5-TR	5.0V	LG50
MIC5219YM5-TR	可调	

b) 6引脚 VDFN 封装，500 毫安连续输出电流能力，可调和固定输出电压，5,000/卷 目录料号

	输出电压	标记代码
MIC5219-2.8YML-TR	2.8V	G28
MIC5219-3.0YML-TR	3.0V	G30
MIC5219-3.3YML-TR	3.3V	G33
MIC5219-3.6YML-TR	3.6V	G36

c) 6引脚TDFN封装，500毫安连续输出电流能力，支持可调及固定输出电压，5,000/卷，目录料号

	输出电压	标记代码
MIC5219-5.0YMT-TR	5.0V	G50
MIC5219YMT-TR	可调	GAA

d) 8引脚MSOP封装，500毫安连续输出电流能力，支持可调及固定输出电压，100/管或2,500/卷，

CPN 散装	数量	CPN 卷带包装	数量
MIC5219-2.5YMM	100/管	MIC5219-2.5YMM-TR	2,500/卷
MIC5219-2.85YMM	100只/管	MIC5219-2.85YMM-TR	2,500只/卷
MIC5219-3.0YMM	100只/管	MIC5219-3.0YMM-TR	2,500只/卷
MIC5219-3.3YMM	100只/管	MIC5219-3.3YMM-TR	2,500只/卷
MIC5219-3.6YMM	100只/管	MIC5219-3.6YMM-TR	2,500只/卷
MIC5219-5.0YMM	100只/管	MIC5219-5.0YMM-TR	2,500只/卷
MIC5219YMM	100只/管	MIC5219YMM-TR	2,500只/卷

注1：带盘卷装标识仅出现在目录零件编号描述中。该标识用于订购，不印刷在器件封装上。请向Microchip销售办公室确认带盘卷装选项的封装可用性。

NOTES:

注释：

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电话：886-3-577-8366

台湾 - 高雄
电话：886-7-213-7830

台湾 - 台北
电话：886-2-2508-8600

泰国 - 曼谷
电话：66-2-694-1351

越南 - 胡志明市
电话：84-28-5448-2100

欧洲

奥地利 - 韦尔斯
电话：43-7242-2244-39
传真：43-7242-2244-393

丹麦 - 哥本哈根
电话：45-4450-2828
传真：45-4485-2829

芬兰 - 埃斯波
电话：358-9-4520-820

法国 - 巴黎
电话：33-1-69-53-63-20
传真：33-1-69-30-90-79

德国 - 加兴
电话：49-8931-9700

德国 - 哈恩
电话：49-2129-3766400

德国 - 海尔布隆
电话：49-7131-67-3636

德国 - 卡尔斯鲁厄
电话：49-721-625370

德国 - 慕尼黑
电话：49-89-627-144-0
传真：49-89-627-144-44

德国 - 罗森海姆
电话：49-8031-354-560

以色列 - 拉阿纳纳
电话：972-9-744-7705

意大利 - 米兰
电话：39-0331-742611
传真：39-0331-466781

意大利 - 帕多瓦
电话：39-049-7625286

荷兰 - 德鲁嫩
电话：31-416-690399
传真：31-416-690340

挪威 - 特隆赫姆
电话：47-7289-7561

波兰 - 华沙
电话：48-22-3325737

罗马尼亚 - 布加勒斯特
电话：40-21-407-87-50

西班牙 - 马德里
电话：34-91-708-08-90
传真：34-91-708-08-91

瑞典 - 哥德堡
电话：46-31-704-60-40

瑞典 - 斯德哥尔摩
电话：46-8-5090-4654

英国・沃金厄姆
电话：44-118-921-5800
传真：44-118-921-5820

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