MAX17048/MAX17049 3µA 1-Cell/2-Cell Fuel Gauge with ModelGauge

General Description

The MAX17048/MAX17049 ICs are tiny, micropower current fuel gauges for lithium-ion (Li+) batteries in handheld and portable equipment. The MAX17048 operates with a single lithium cell and the MAX17049 with two lithium cells in series.

The ICs use the sophisticated Li+ battery-modeling algorithm ModelGauge™ to track the battery relative state-of-charge (SOC) continuously over widely varying charge and discharge conditions. The ModelGauge algorithm eliminates current-sense resistor and battery-learn cycles required in traditional fuel gauges. Temperature compensation is implemented using the system microcontroller.

The ICs automatically detect when the battery enters a low-current state and enters low-power 3µA hibernate mode, while still providing accurate fuel gauging. The ICs automatically exit hibernate mode when the system returns to active state.

On battery insertion, the ICs debounce initial voltage measurements to improve the initial SOC estimate, thus allowing them to be located on system side. SOC, voltage, and rate information is accessed using the I²C interface. The ICs are available in a tiny 0.9mm x 1.7mm, 8-bump wafer-level package (WLP), or a 2mm x 2mm, 8-pin TDFN package.

Applications

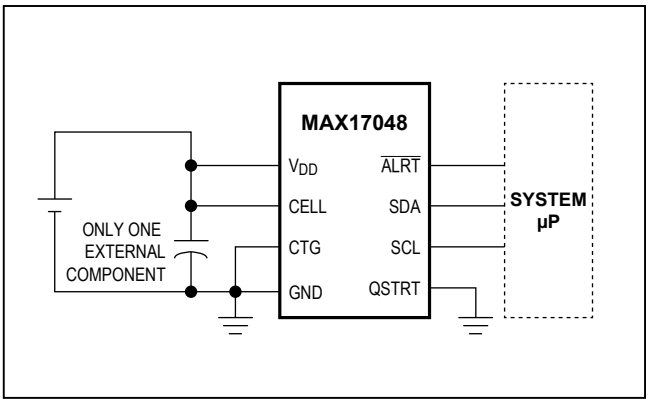
- Smartphones, Tablets
- Smartwatches, Wearables
- Bluetooth Headsets
- Health and Fitness Monitors
- Digital Still, Video, and Action Cameras
- Medical Devices
- Handheld Computers and Terminals
- Wireless Speakers
- Home and Building Automation, Sensors

***Ordering Information* appears at end of data sheet.**

Features and Benefits

- MAX17048: 1 Cell, MAX17049: 2 Cells
- Precision ±7.5mV/Cell Voltage Measurement
- ModelGauge Algorithm
  - Provides Accurate State-of-Charge
  - Compensates for Temperature/Load Variation
  - Does Not Accumulate Errors, Unlike Coulomb Counters
  - Eliminates Learning
  - Eliminates Current-Sense Resistor
- Ultra-Low Quiescent Current
  - 3µA Hibernate, 23µA Active
  - Fuel Gauges in Hibernate Mode
  - Automatically Enters and Exits Hibernate Mode
- Reports Charge and Discharge Rate
- Battery-Insertion Debounce
  - Best of 16 Samples to Estimate Initial SOC
- Programmable Reset for Battery Swap
  - 2.28V to 3.48V Range
- Configurable Alert Indicator
  - Low SOC
  - 1% Change in SOC
  - Battery Undervoltage/Overvoltage
  - VRESET Alert
- I²C Interface
- 8-Bit OTP ID Register (Contact Factory)

Simple Fuel-Gauge Circuit Diagram



19-6171; Rev 7; 11/16

maxim integrated™

MAX17048/MAX17049　　3µA 1节电池/2节电池电量计，内置ModelGauge

概述

MAX17048/MAX17049 集成电路是用于手持及便携设备中锂离子（Li+）电池的微功率电流燃料计。MAX17048适用于单节锂电池，MAX17049 适用于两节串联锂电池。

该集成电路采用先进的锂电池建模算法 ModelGauge™，能够在广泛变化的充放电条件下持续跟踪电池的相对电池荷电状态（SOC）。 ModelGauge 算法消除了传统燃料计中对电流感应电阻和电池学习周期的需求。温度补偿由系统微控制器实现。

集成电路能自动检测电池进入低电流状态，并进入低功耗3µA休眠模式，同时仍能提供准确的燃料计量。当系统恢复活动状态时，集成电路会自动退出休眠模式。

电池插入时，集成电路对初始电压测量进行消抖处理，以提升初始SOC估算的准确性，从而支持其安装于系统侧。通过I²C接口访问SOC、电压及速率信息。该集成电路提供尺寸为0.9mm × 1.7mm的8凸点晶圆级封装（WLP），或尺寸为2mm × 2mm的

8引脚TDFN封装。

应用领域

- 智能手机、平板电脑
- 智能手表、可穿戴设备
- 蓝牙耳机
- 健康与健身监测设备
- 数码静态相机、摄像机及运动相机
- 医疗设备
- 手持计算机及终端设备
- 无线扬声器
- 家居及建筑自动化、传感器

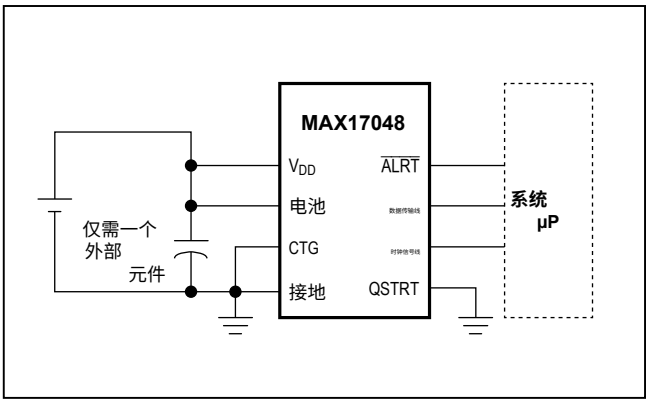
订购信息详见数据手册末尾。

ModelGauge 是 *Maxim Integrated Products, Inc.* 的注册商标。

特性与优势

- MAX17048：单节电池，MAX17049：双节电池
- 精确±7.5mV/节电池电压测量
- ModelGauge算法
  - 提供准确的电池荷电状态
  - 补偿温度和负载变化
  - 不累积误差，区别于库仑计数器
  - 无需学习过程
  - 无需电流检测电阻
- 超低静态电流
  - 3µA休眠电流，23µA工作电流
  - 休眠模式下的电量计
  - 自动进入和退出休眠模式
- 报告充放电速率
- 电池插入防抖动
  - 从16个样本中选取最佳值以估算初始电池荷电状态
- 支持电池更换的可编程复位
  - 电压范围2.28V至3.48V
- 可配置的警报指示
  - 低电池荷电状态警报
  - 电池荷电状态变化1%警报
  - 电池欠压/过压警报
  - VRESET 警报
- I²C 接口
- 8位 OTP ID 寄存器（请联系工厂）

简易电量计电路图



Absolute Maximum Ratings

CELL to GND .....-0.3V to +12V
All Other Pins to GND .....-0.3V to +6V
Continuous Sink Current, SDA, $\overline{ALRT}$ 20mA
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (TDFN only) (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = 2.5V to 4.5V, T_A= -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 2)	2.5		4.5	V
Fuel-Gauge SOC Reset (VRESET Register)	V_{RST}	Configuration range, in 40mV steps	2.28		3.48	V
		Trimmed at 3V	2.85	3.0	3.15	V
Data I/O Pins	SCL, SDA, $\overline{ALRT}$	(Note 2)	-0.3		+5.5	V
Supply Current	I_{DD0}	Sleep mode, $T_A \le +50°C$		0.5	2	µA
		Hibernate mode, reset comparator disabled (VRESET.Dis = 1)		3	5	
		Hibernate mode, reset comparator enabled (VRESET.Dis = 0)		4		
	I_{DD1}	Active mode		23	40	
Time Base Accuracy	t_{ERR}	Active, hibernate modes (Note 3)	-3.5	±1	+3.5	%
ADC Sample Period		Active mode		250		ms
		Hibernate mode		45		s
Voltage Error	V_{ERR}	V_{CELL} = 3.6V, T_A = +25°C (Note 4)	-7.5		+7.5	mV/cell
			-20		+20	
Voltage-Measurement Resolution				1.25		mV/cell
Voltage-Measurement Range		MAX17048: V_{DD} pin	2.5		5	V
		MAX17049: CELL pin	5		10	
SDA, SCL, QSTRT Input Logic-High	V_{IH}		1.4			V
SDA, SCL, QSTRT Input Logic-Low	V_{IL}				0.5	V
SDA, $\overline{ALRT}$ Output Logic-Low	V_{OL}	I_{OL} = 4mA			0.4	V
SDA, SCL Bus Low-Detection Current	I_{PD}	$V_{SDA} = V_{SCL}$ = 0.4V (Note 5)		0.2	0.4	µA
Bus Low-Detection Timeout	t_{SLEEP}	(Note 6)	1.75		2.5	s

绝对最大额定值

电池端至接地..... 0.3V 至 +12V
所有其他引脚至接地..... -...0.3V 至 +6V
连续吸收电流，SDA， $\overline{ALRT}$..... .....20mA
工作温度范围..... -.....40°C 至 +85°C
存储温度范围..... -.....55°C 至 +125°C
引脚温度（仅限TDFN封装）（焊接，10秒）..... ....+300°C
焊接温度（回流焊）..... .....+260°C

超过"绝对最大额定值"中列出的应力可能导致器件永久损坏。这些仅为应力额定值，不代表器件在这些或规格操作部分未涵盖的任何其他条件下均能正常工作。长时间暴露于绝对最大额定值条件可能影响器件可靠性。

电气特性

(V_{DD} = 2.5V 至 4.5V，T_A = -20°C 至 +70°C，除非另有说明。典型值在 T_A = +25°C。）（注1）

参数	符号	条件	最小值	典型值	最大值	单位
电源电压	V_{DD}	（注2）	2.5		4.5	V
燃料计SOC复位（VRESET寄存器）	V_{RST}	配置范围，步进为40mV	2.28		3.48	V
		在3V时校准	2.85	3.0	3.15	V
数据输入/输出引脚	时钟信号线，数据传输线 $\overline{ALRT}$	（注2）	-0.3		+5.5	V
电源电流	I_{DD0}	睡眠模式，环境温度T_A≤ +50°C		0.5	2	µA
		休眠模式，复位比较器禁用（VRESET.Dis= 1）		3	5	
		休眠模式，复位比较器已启用 (VRESET.Dis= 0)		4		
	I_{DD1}	活动模式		23	40	
时间基准精度	t_{ERR}	活动模式与休眠模式（注3）	-3.5	±1	+3.5	%
ADC采样周期		活动模式		250		毫秒
		休眠模式		45		秒
电压误差	V_{ERR}	VCELL = 3.6V, T_A = +25°C（注4）	-7.5		+7.5	毫伏/单体电池
			-20		+20	
电压测量分辨率				1.25		毫伏/单体电池
电压测量范围		MAX17048: V_{DD} 引脚	2.5		5	V
		MAX17049：CELL引脚	5		10	
SDA、SCL、QSTRT 输入逻辑高	V_{IH}		1.4			V
SDA、SCL、QSTRT 输入逻辑低	V_{IL}				0.5	V
SDA、 $\overline{ALRT}$输出逻辑低	V_{OL}	I_{OL} = 4mA			0.4	V
SDA、SCL 总线低电平检测电流	I_{PD}	VSDA = V_{SCL} = 0.4V（注5）		0.2	0.4	µA
总线低电平检测超时	t_{SLEEP}	（注6）	1.75		2.5	秒

Electrical Characteristics (I²C INTERFACE)

(2.5V < V_{DD} < 4.5V, T_A = -20°C to +70°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 7)	0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
START Condition (Repeated) Hold Time	$t_{HD:STA}$	(Note 8)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 9, 10)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 9)	100			ns
Rise Time of Both SDA and SCL Signals	t_R		20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F		20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 11)	0		50	ns
Capacitive Load for Each Bus Line	C_B	(Note 12)			400	pF
SCL, SDA Input Capacitance	$C_{B,IN}$				60	pF

Note 1: Specifications are 100% tested at T_A = +25°C. Limits over the operating range are guaranteed by design and characterization.
Note 2: All voltages are referenced to GND.
Note 3: Test is performed on unmounted/unsoldered parts.
Note 4: The voltage is trimmed and verified with 16x averaging.
Note 5: This current is always present.
Note 6: The IC enters shutdown mode after SCL < V_{IL} and SDA < V_{IL} for longer than 2.5s.
Note 7: Timing must be fast enough to prevent the IC from entering sleep mode due to bus low for period > t_{SLEEP}.
Note 8: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 9: The maximum $t_{HD:DAT}$ has to be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 10: This device internally provides a hold time of at least 100ns for the SDA signal (referred to the $V_{IH,MIN}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 11: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instance.
Note 12: C_B is total capacitance of one bus line in pF.

电气特性（I²C 接口）

(2.5V < V_{DD} < 4.5V，环境温度 T_A = -20°C 至 +70°C，除非另有说明。)（注 1）

参数	符号	条件	最小值	典型值	最大值	单位
SCL时钟频率	f_{SCL}	（注7）	0		400	kHz
STOP与START条件之间的总线空闲时间	t_{BUF}		1.3			μs
启动条件（重复）保持时间	$t_{HD:STA}$	（注8）	0.6			μs
SCL时钟低电平周期	t_{LOW}		1.3			μs
SCL时钟高电平周期	t_{HIGH}		0.6			μs
重复启动条件的建立时间	$t_{SU:STA}$		0.6			μs
数据保持时间	$t_{HD:DAT}$	（注9，10）	0		0.9	μs
数据建立时间	$t_{SU:DAT}$	（注9）	100			纳秒
SDA和SCL信号的上升时间	t_R		20 + 0.1CB		300	纳秒
SDA和SCL信号的下降时间	t_F		20 + 0.1CB		300	纳秒
停止条件的建立时间	$t_{SU:STO}$		0.6			μs
输入滤波器抑制的尖峰脉冲宽度	t_{SP}	(注 11)	0		50	纳秒
每条总线的电容负载线	C_B	(注 12)			400	pF
SCL、SDA 输入电容	$C_{B,IN}$				60	pF

注 **1**：规格在环境温度 TA= +25°C 时进行 **1**00% 测试。工作范围内的极限值通过设计和特性验证予以保证。

注 **2**：所有电压均以接地为参考。
注 **3**：测试在未安装或未焊接的器件上进行。
注 **4**：电压经过修整，并通过 16 倍平均进行验证。
注 **5**：该电流始终存在。
注 **6**：当 SCL < VIL且 SDA < VIL持续超过 2.5 秒时，IC 进入关断模式。
注 **7**：时序必须足够快，以防止因总线低电平持续时间超过 **t**SLEEP而导致 IC 进入睡眠模式。
注 **8**：fSCL必须满足最小时钟低电平时间加上上升和下降时间。
注**9**：仅当设备不延长SCL信号的低电平周期（t_{LOW}）时，才需满足最大$t_{HD:DAT}$。注**10**：该设备内部为SDA信号（相对于SCL信号的$V_{IH,MI}$**N**）提供至少**100**ns的保持时间，以跨越SCL下降沿的不确定区域。

注**11**：SDA和SCL上的滤波器抑制输入缓冲器处的噪声脉冲，并延迟采样时刻。
注**12**： C_B为单条总线线的总电容，单位为pF。

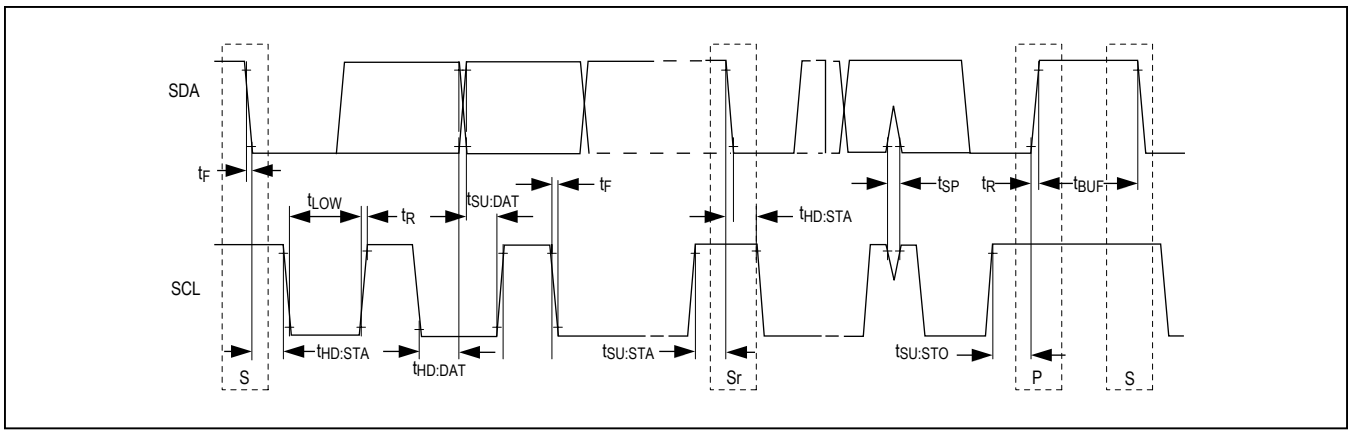
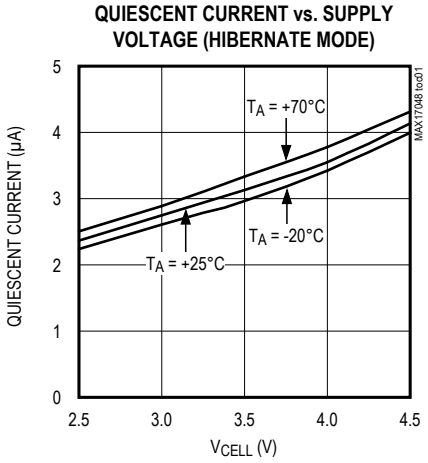
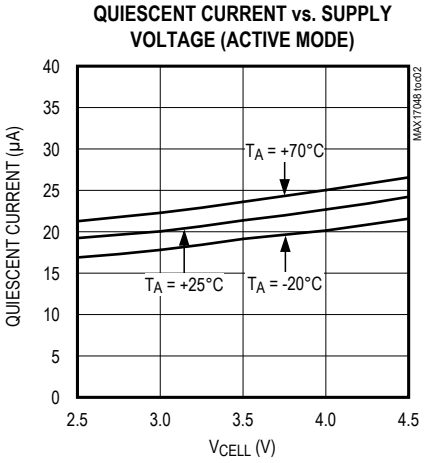


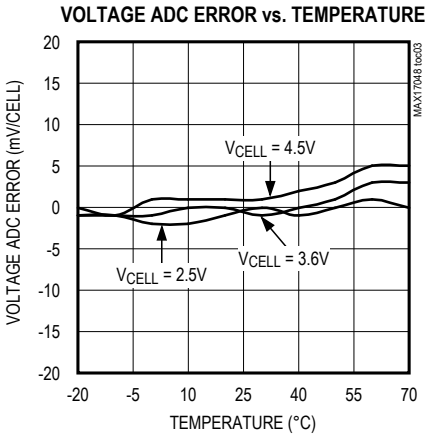
Figure 1. I²C Bus Timing Diagram

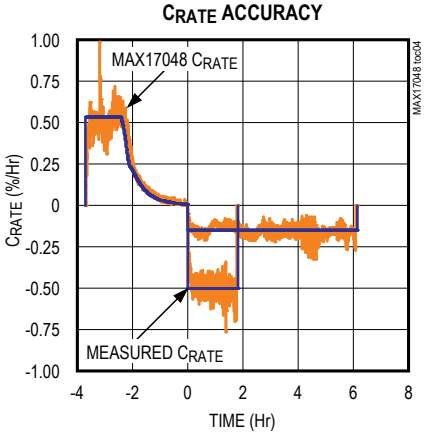
Typical Operating Characteristics

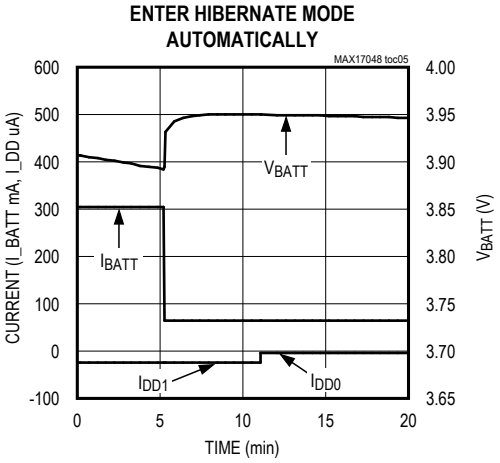
(T_A = +25°C, battery is Sanyo UF504553F, unless otherwise noted.)











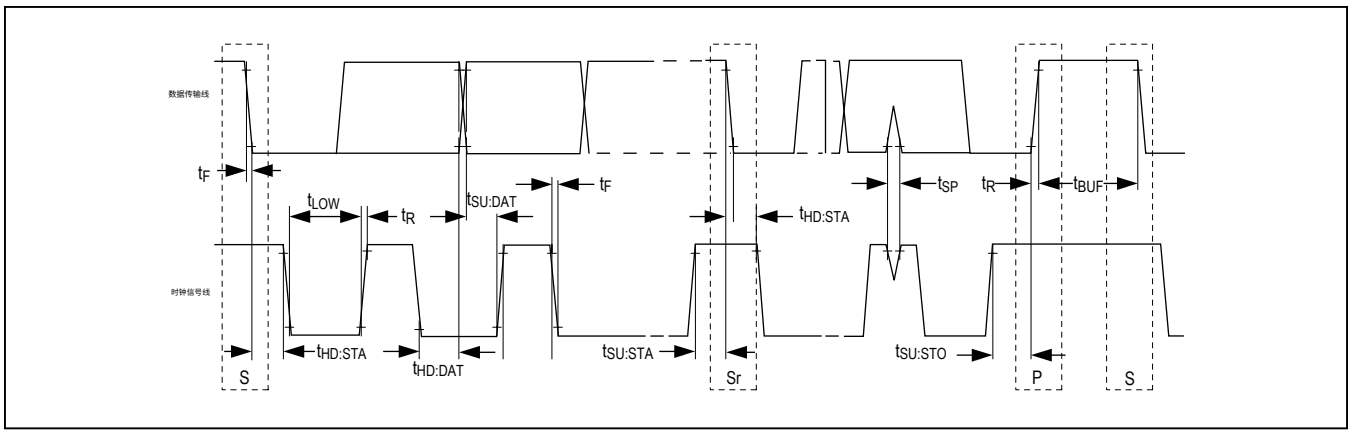
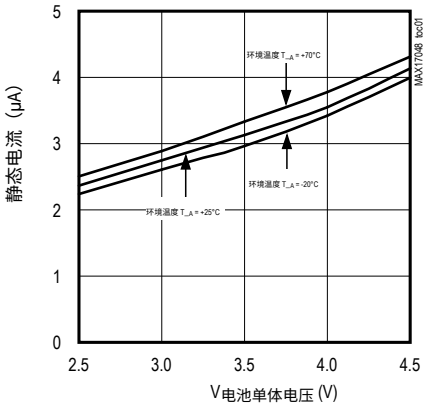


图 *1. I²C* 总线时序图

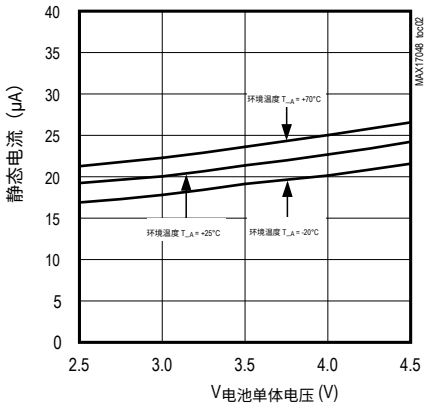
典型工作特性

(T_A = +25°C，电池型号为 Sanyo UF504553F，除非另有说明。)

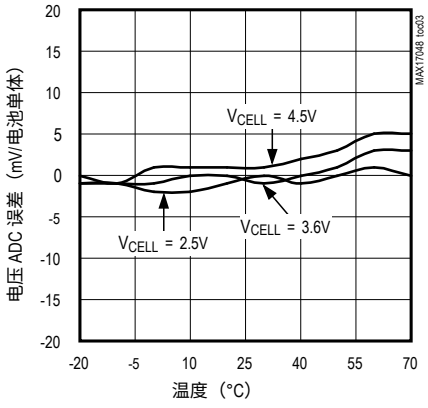
静态电流与电源电压关系（休眠模式）



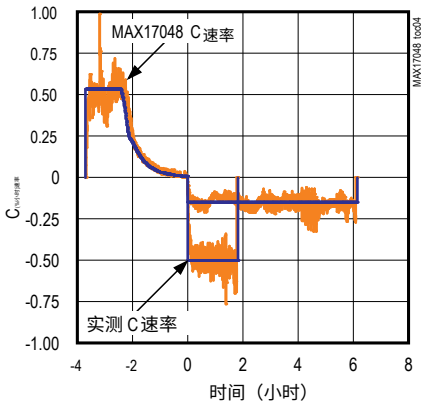
静态电流与电源电压关系（活动模式）



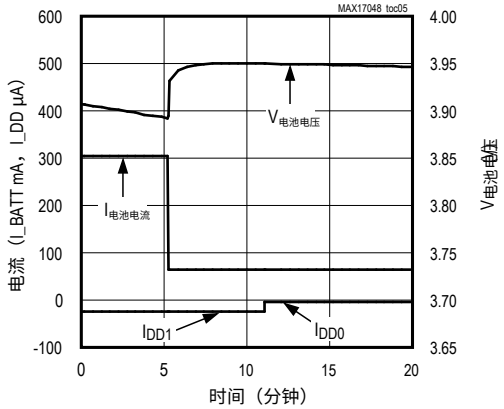
电压 ADC 误差与温度的关系



C速率精度



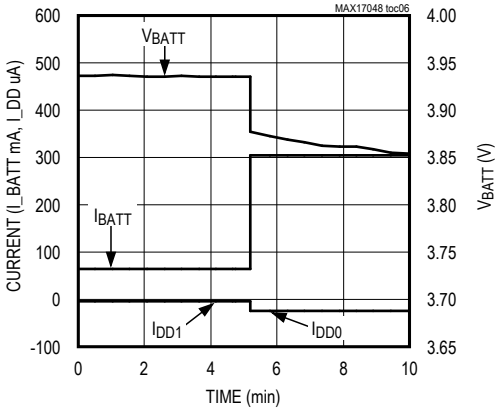
自动进入休眠模式



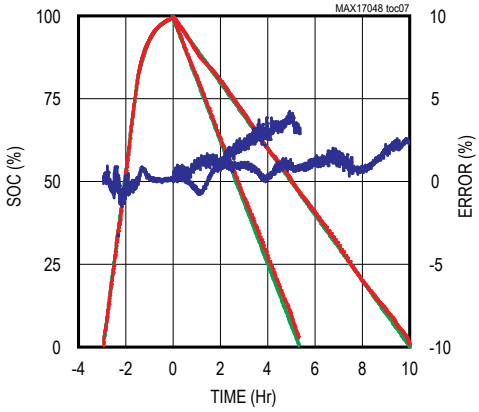
Typical Operating Characteristics (continued)

(T_A = +25°C, battery is Sanyo UF504553F, unless otherwise noted.)

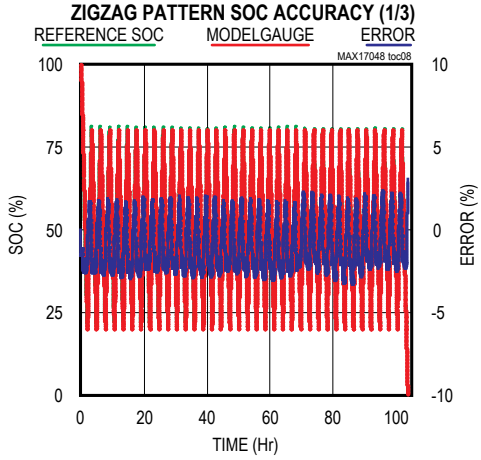
EXIT HIBERNATE MODE AUTOMATICALLY



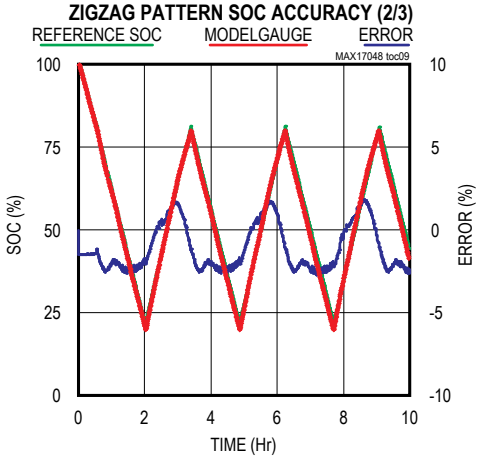
SOC ACCURACY T_A = 20°C, HIBERNATE MODE



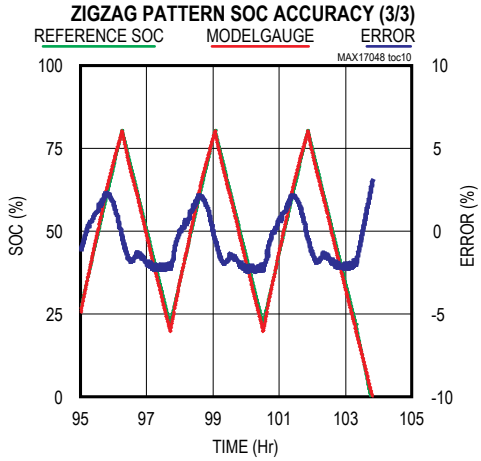
ZIGZAG PATTERN SOC ACCURACY (1/3)



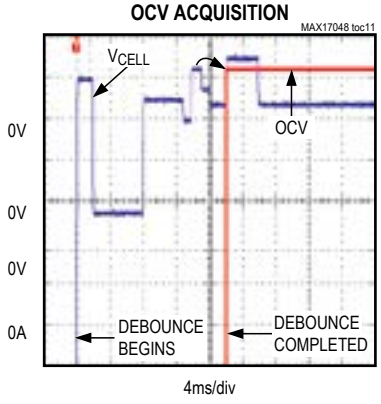
ZIGZAG PATTERN SOC ACCURACY (2/3)



ZIGZAG PATTERN SOC ACCURACY (3/3)



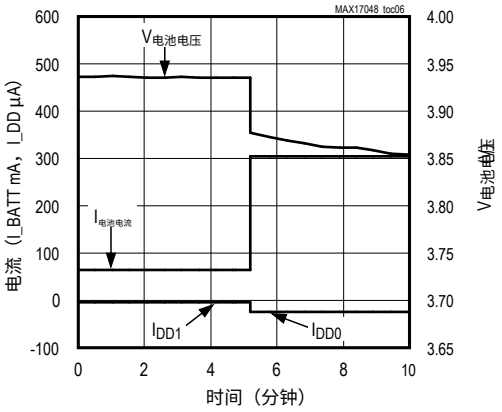
BATTERY-INSERTION DEBOUNCE/ OCV ACQUISITION



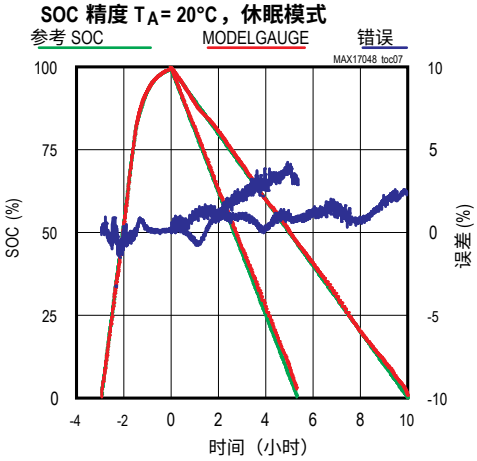
典型工作特性（续）

(T_A = +25°C，电池型号为 Sanyo UF504553F，除非另有说明。)

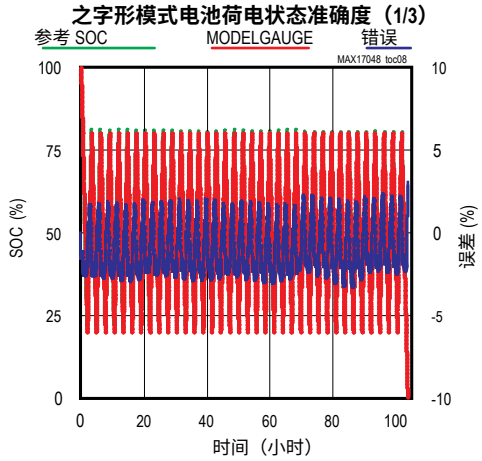
自动退出休眠模式



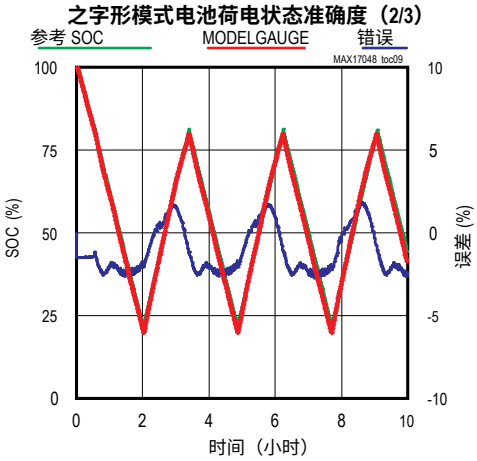
SOC 精度 T_A = 20°C，休眠模式



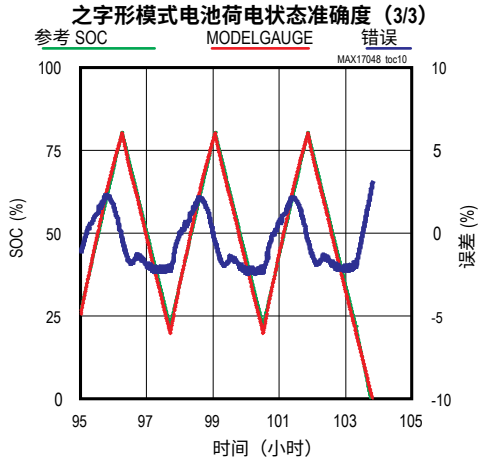
之字形模式电池荷电状态准确度（1/3）



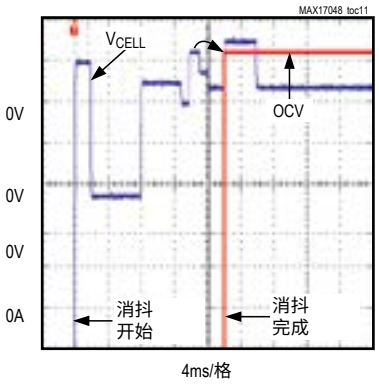
之字形模式电池荷电状态准确度（2/3）



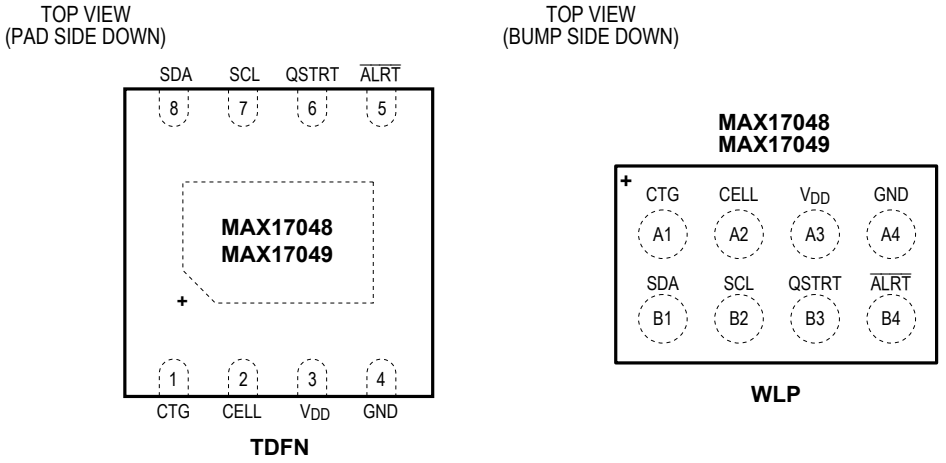
之字形模式电池荷电状态准确度（3/3）



电池插入消抖/开路电压采集



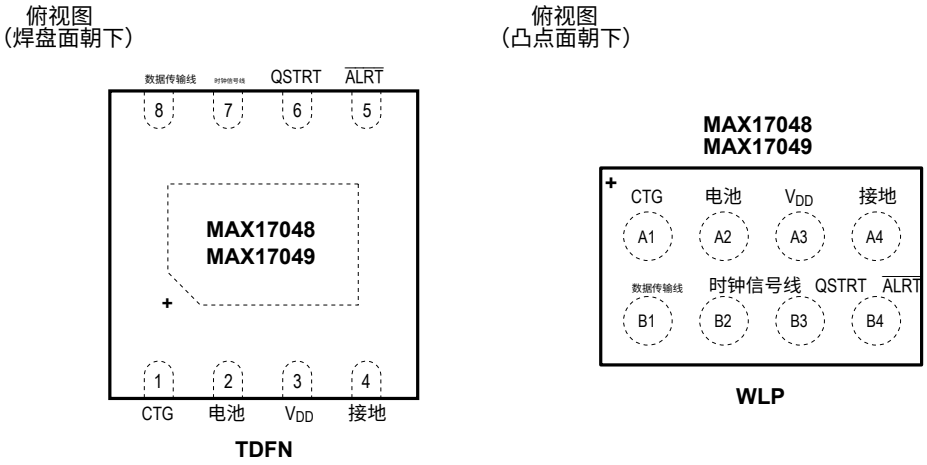
Pin/Bump Configurations



Pin/Bump Descriptions

PIN/BUMP		NAME	FUNCTION
TDFN	WLP		
1	A1	CTG	Connect to Ground
2	A2	CELL	Connect to the Positive Battery Terminal. MAX17048: Not internally connected. MAX17049: Voltage sense input.
3	A3	V_{DD}	Power-Supply Input. Bypass with 0.1µF to GND. MAX17048: Voltage sense input. Connect to positive battery terminal. MAX17049: Connect to regulated power-supply voltage.
4	A4	GND	Ground. Connect to negative battery terminal.
5	B4	$\overline{ALRT}$	Open-Drain, Active-Low Alert Output. Optionally connect to interrupt input of the system microcontroller.
6	B3	QSTRT	Quick-Start Input. Allows reset of the device through hardware. Connect to GND if not used.
7	B2	SCL	I^2C Clock Input. SCL has an internal pulldown (I_{PD}) for sensing disconnection.
8	B1	SDA	Open-Drain I^2C Data Input/Output. SDA has an internal pulldown (I_{PD}) for sensing disconnection.
—	—	EP	Exposed Pad (TDFN Only). Connect to GND.

引脚/凸点配置



引脚/凸点说明

引脚/焊点		名称	功能
TDFN	WLP		
1	A1	CTG	连接至地线
2	A2	电池	连接至电池正极端子。 MAX17048：内部无连接。 MAX17049：电压检测输入。
3	A3	V_{DD}	电源输入。通过0.1μF电容旁路至接地。 MAX17048：电压感测输入。连接至电池正极。 MAX17049：连接至稳压电源电压。
4	A4	接地	接地。连接至电池负极。
5	B4	$\overline{ALRT}$	开漏、低电平有效警报输出。可选连接至系统微控制器的中断输入。
6	B3	QSTRT	快速启动输入。允许通过硬件复位设备。若不使用，请连接至接地。
7	B2	时钟信号线	I^2C时钟输入。SCL内部带有下拉电阻（I_{PD}），用于检测断开。
8	B1	数据传输线	开漏I^2C数据输入/输出。SDA内部带有下拉电阻（I_{PD}），用于检测断开。
—	—	EP	裸露焊盘（仅限TDFN封装）。连接至接地。

Detailed Description

ModelGauge Theory of Operation

The MAX17048/MAX17049 ICs simulate the internal, nonlinear dynamics of a Li+ battery to determine its SOC. The sophisticated battery model considers impedance and the slow rate of chemical reactions in the battery (Figure 2).

ModelGauge performs best with a custom model, obtained by characterizing the battery at multiple discharge currents and temperatures to precisely model it. At power-on reset (POR), the ICs have a preloaded ROM model that performs well for some batteries. Contact Maxim if you need a custom model.

Fuel-Gauge Performance

In coulomb counter-based fuel gauges, SOC drifts because offset error in the current-sense ADC measurement accumulates over time. Instantaneous error can be very small, but never precisely zero. Error accumulates over time in such systems (typically 0.5%–2% per day) and requires periodic corrections. Some algorithms correct drift using occasional events, and until such an event occurs the algorithm's error is boundless:

- Reaching predefined SOC levels near full or empty
- Measuring the relaxed battery voltage after a long period of inactivity
- Completing a full charge/discharge cycle

ModelGauge requires no correction events because it uses only voltage, which is stable over time. As TOCs 8, 9, and 10 show, ModelGauge remains accurate despite the absence of any of the above events; it neither drifts nor accumulates error over time.

To correctly measure performance of a fuel gauge as experienced by end-users, exercise the battery dynamically. Accuracy cannot be fully determined from only simple cycles.

Battery Voltage and State-Of-Charge

Open-circuit voltage (OCV) of a Li+ battery uniquely determines its SOC; one SOC can have only one value of OCV. In contrast, a given V_{CELL} can occur at many different values of OCV because V_{CELL} is a function of time, OCV, load, temperature, age, and impedance, etc.; one value of OCV can have many values of V_{CELL}. Therefore, one SOC can have many values of V_{CELL}, so V_{CELL} cannot uniquely determine SOC.

Figure 3 shows that V_{CELL} = 3.81V occurs at 2%, 50%, and 72% SOC.

Even the use of sophisticated tables to consider both voltage and load results in significant error due to the load transients typically experienced in a system. During charging or discharging, and for approximately 30min after, V_{CELL} and OCV differ substantially, and V_{CELL} has been affected by the preceding hours of battery activity. ModelGauge uses voltage comprehensively.

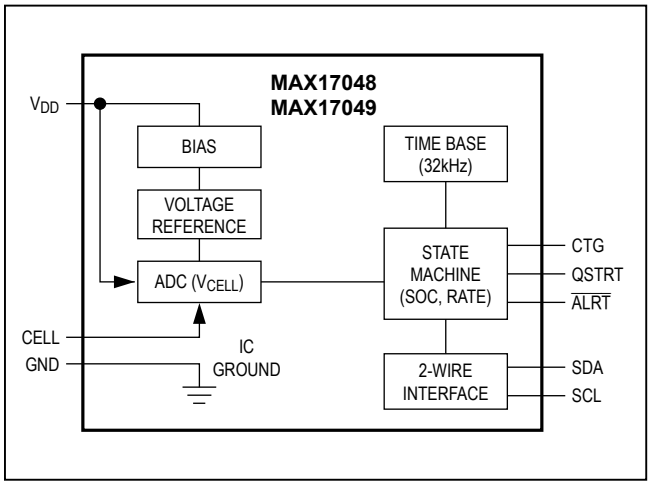


Figure 2. Block Diagram

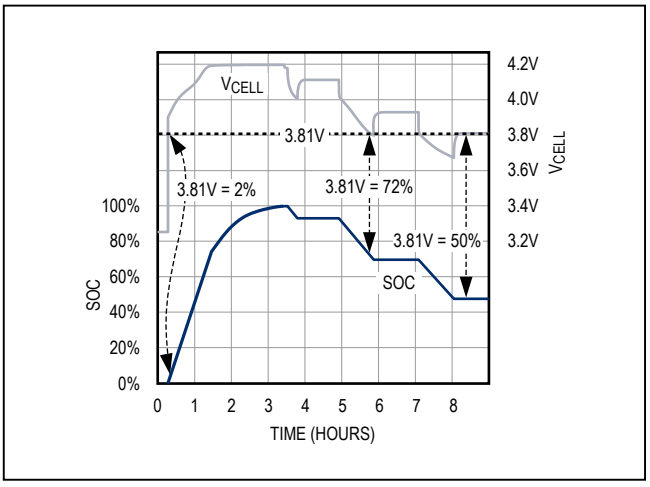


Figure 3. Instantaneous Voltage Does Not Translate Directly to SOC

详细描述

ModelGauge 工作原理

MAX17048/MAX17049 集成电路通过模拟锂离子电池的内部非线性动态行为来确定其荷电状态（SOC）。该复杂电池模型考虑了电池阻抗及其缓慢的化学反应速率（见图2）。

ModelGauge 在采用定制模型时性能最佳，该模型通过在多种放电电流和温度条件下对电池进行表征以实现精确建模。上电复位（POR）时，集成电路内置预加载的ROM模型，对部分电池表现良好。如需定制模型，请联系Maxim。

电量计性能

在基于库仑计数的电量计中，由于电流检测ADC测量的偏移误差随时间累积，SOC会产生漂移。瞬时误差可以非常小，但绝不可能精确为零。此类系统中的误差会随时间累积（通常为每天0.5%至2%），因此需要定期校正。一些算法通过偶发事件来校正漂移，在此类事件发生之前，算法的误差是无界的：

- 达到接近满电或放空的预设SOC水平
- 长时间静置后测量电池的静态电压
- 完成一次完整的充放电周期

ModelGauge无需校正事件，因为它仅依赖电压，而电压随时间保持稳定。如表8、9和10所示，尽管缺少上述任何事件，ModelGauge依然保持准确；它既不会漂移，也不会随时间累积误差。

为了准确评估终端用户体验的电量计性能，应动态使用电池。仅通过简单循环无法完全评估准确度。

电池电压与荷电状态

锂离子电池的开路电压（OCV）能够唯一确定其荷电状态（SOC）； 一个SOC只能对应一个OCV值。相比之下，给定的V_{CELL}可能对应多个不同的OCV值，因为V_{CELL}是时间、OCV、负载、温度、老化和阻抗等因素的函数；一个OCV值可以对应多个V_{CELL}值。因此，一个SOC可以对应多个V_{CELL}值，故V_{CELL}无法唯一确定SOC。

图3显示，当V_{CELL} = 3.81V时，SOC分别为2%、50%和72%。

即使采用复杂的表格同时考虑电压和负载，仍会因系统中常见的负载瞬变而产生显著误差。在充电或放电过程中及其后约30分钟内，V_{CELL}与OCV存在显著差异，且V_{CELL}受之前数小时电池活动的影响。

ModelGauge 综合利用电压信息。

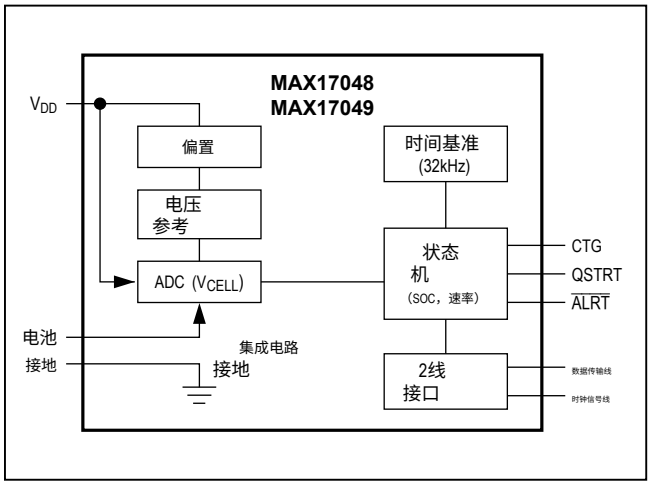


图 2. 方框图

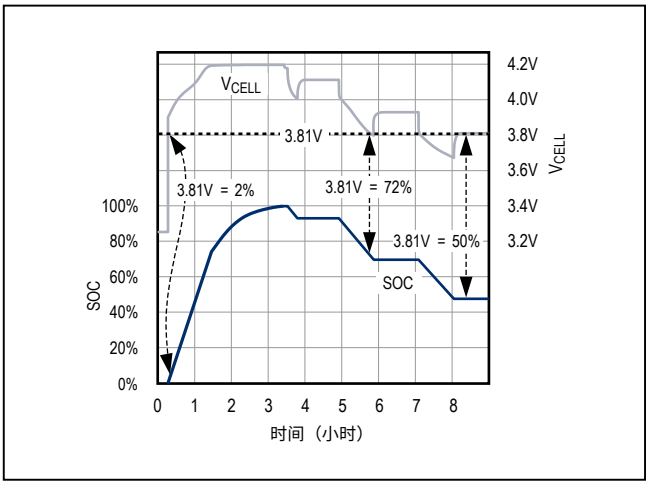


图 3. 瞬时电压不能直接反映SOC

Temperature Compensation

For best performance, the host microcontroller must measure battery temperature periodically, and compensate the RCOMP ModelGauge parameter accordingly, at least once per minute. Each custom model defines constants RCOMP0 (default is 0x97), TempCoUp (default is -0.5), and TempCoDown (default is -5.0). To calculate the new value of CONFIG.RCOMP:

```
// T is battery temperature (degrees Celsius)
if (T > 20) {
    RCOMP = RCOMP0 + (T - 20) x TempCoUp;
}
else {
    RCOMP = RCOMP0 + (T - 20) x TempCoDown;
}
```

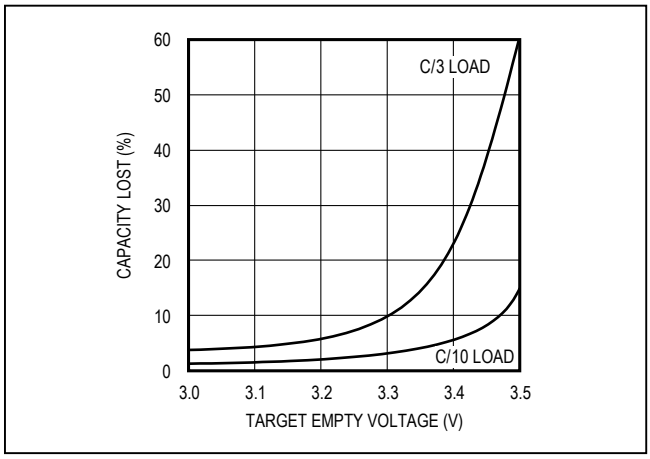


Figure 4. Increasing Empty Voltage Reduces Battery Capacity

Impact of Empty-Voltage Selection

Most applications have a minimum operating voltage below which the system immediately powers off (empty voltage). When characterizing the battery to create a custom model, choose empty voltage carefully. As shown in Figure 4, capacity unavailable to the system increases at an accelerating rate as empty voltage increases.

To ensure a controlled shutdown, consider including operating margin into the fuel gauge based on some low threshold of SOC, for example shutting down at 3% or 5%. This utilizes the battery more effectively than adding error margin to empty voltage.

Battery Insertion

When the battery is first inserted into the system, the fuel-gauge IC has no previous knowledge about the battery's SOC. Assuming that the battery is relaxed, the IC translates its first V_{CELL} measurement into the best initial estimate of SOC. Initial error caused by the battery not being in a relaxed state diminishes over time, regardless of loading following this initial conversion. While SOC estimated by a coulomb counter diverges, ModelGauge SOC converges, correcting error automatically as illustrated in Figure 5; initial error has no long-lasting impact.

Battery Insertion Debounce

Any time the IC powers on or resets (see the *VRESET/ID Register (0x18)* section), it estimates that OCV is the maximum of 16 V_{CELL} samples (1ms each, full 12-bit resolution). OCV is ready 17ms after battery insertion, and SOC is ready 175ms after that.

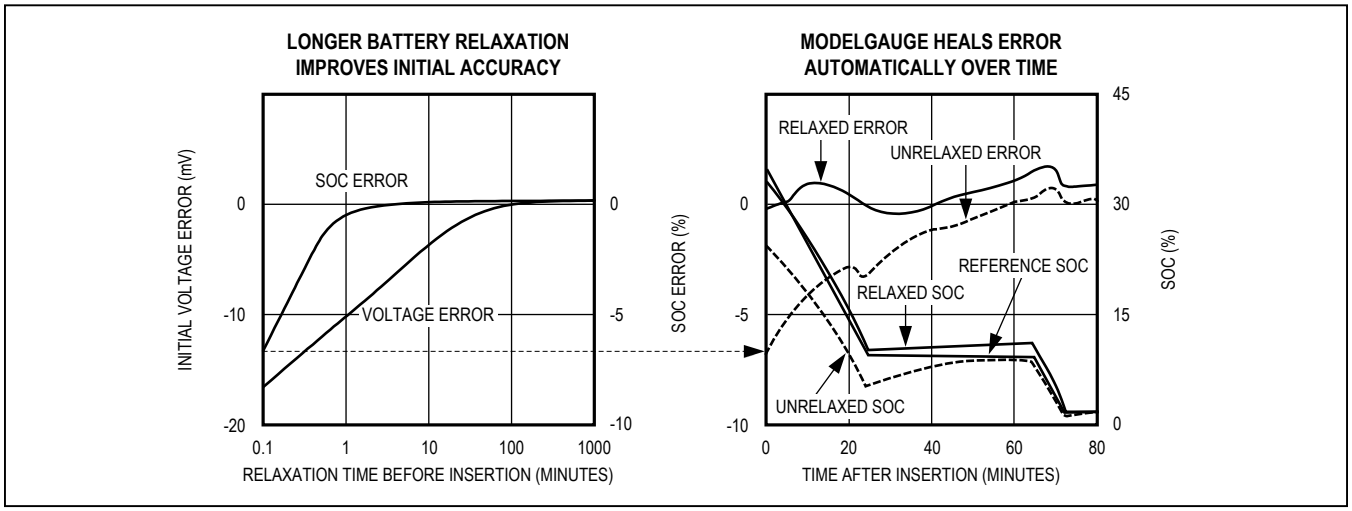


Figure 5. ModelGauge Heals Error Automatically

温度补偿

为实现最佳性能，主机微控制器必须定期测量电池温度，并相应调整RCOMP ModelGauge参数，至少每分钟一次。每个自定义模型定义了常数RCOMP0（默认值为0x97）、TempCoUp（默认值为-0.5）和TempCoDown（默认值为-5.0）。CONFIG.RCOMP的新值计算如下：

```
// T为电池温度（摄氏度）
if (T > 20) {
    RCOMP = RCOMP0 + (T - 20) x TempCoUp;
}
else {
    RCOMP = RCOMP0 + (T - 20) x TempCoDown;
}
```

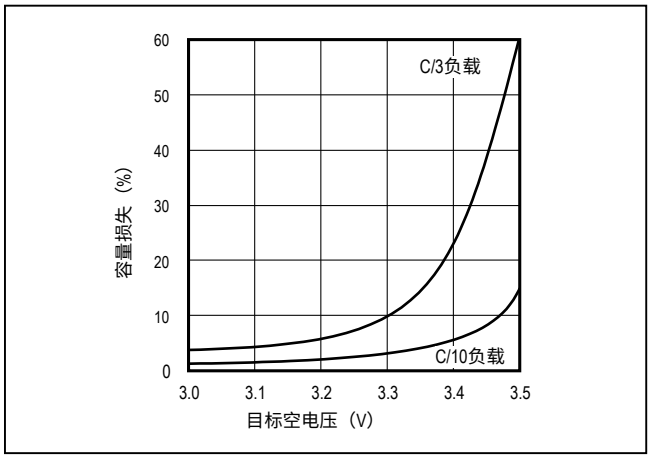


图4。 提高空电压会降低电池容量

空电压选择的影响

大多数应用设有最低工作电压，低于该电压系统将立即断电（空电压）。在对电池进行特性描述以创建自定义模型时，应谨慎选择空电压。如图4所示，随着空电压的增加，系统不可用容量以加速的速率增长。

为确保受控关机，建议基于某一低SOC阈值将操作裕度纳入电量计，例如在3%或5%时关机。这种方法比在空电压上添加误差裕度更有效地利用电池。

电池插入

当电池首次插入系统时，电量计集成电路对电池的SOC没有先验信息。假设电池处于静止状态，集成电路将首次测得的V_{CELL}值转换为SOC的最佳初始估计。由于电池未处于静止状态而产生的初始误差会随着时间推移逐渐减小，无论初始转换后负载如何变化。尽管由库仑计估算的SOC会发散，ModelGauge SOC则会收敛，并自动纠正误差，如图5所示；初始误差不会产生长期影响。

电池插入消抖

每当集成电路上电或复位（参见 *VRESET/ ID寄存器（0x18）*章节）时，IC会估算OCV为16个V_{CELL}样本（每个1ms，完整12位分辨率）中的最大值。电池插入后17ms，OCV准备就绪，SOC在此后175ms准备就绪。

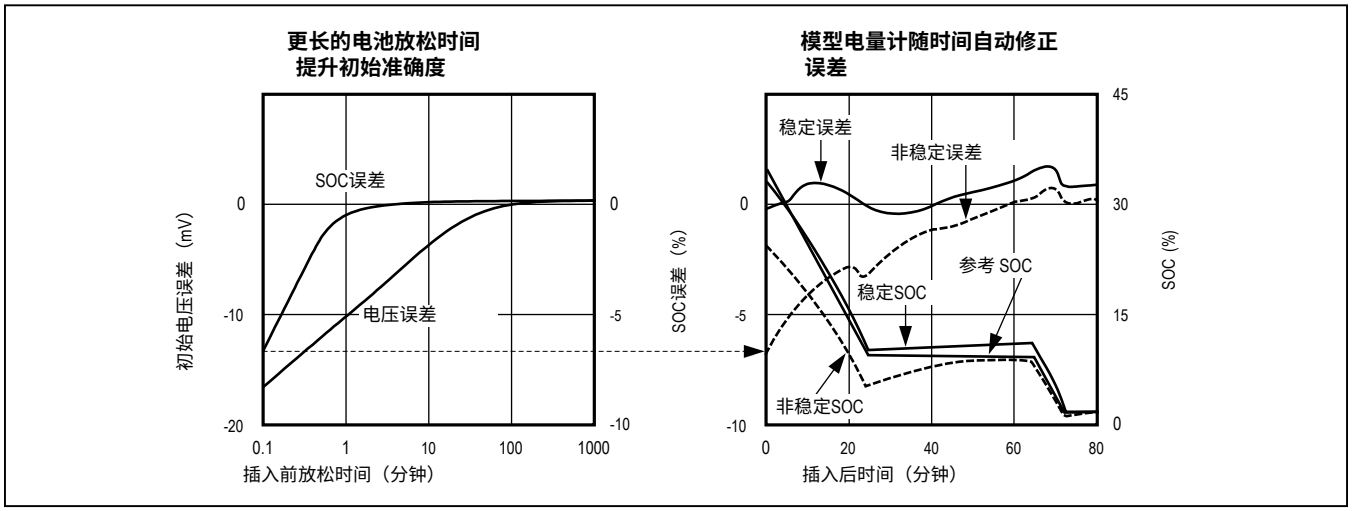


图5。 *ModelGauge*自动修正误差

Battery Swap Detection

If V_{CELL} falls below V_{RST}, the IC quick-starts when V_{CELL} returns above V_{RST}. This handles battery swap; the SOC of the previous battery does not affect that of the new one. See the *Quick-Start* and *VRESET/ID Register (0x18)* sections.

Quick-Start

If the IC generates an erroneous initial SOC, the battery insertion and system powerup voltage waveforms must be examined to determine if a quick-start is necessary, as well as the best time to execute the command. The IC samples the maximum V_{CELL} during the first 17ms. See the *Battery Insertion Debounce* section. Unless V_{CELL} is fully relaxed, even the best sampled voltage can appear greater or less than OCV. Therefore, quick-start must be used cautiously.

Most systems should not use quick-start because the ICs handle most startup problems transparently, such as intermittent battery-terminal connection during insertion. If battery voltage stabilizes faster than 17ms, as illustrated in Figure 6, then do not use quick-start.

The quick-start command restarts fuel-gauge calculations in the same manner as initial power-up of the IC. If the system power-up sequence is so noisy that the initial estimate of SOC has unacceptable error, the system microcontroller might be able to reduce the error by using quick-start. A quick-start is initiated by a rising edge on the QSTRT pin, or by writing 1 to the quick-start bit in the MODE register.

Power-On Reset (POR)

POR includes a quick-start, so only use it when the battery is fully relaxed. See the *Quick-Start* section. This command restores all registers to their default values. After this command, reload the custom model. See the *CMD Register (0xFE)* section.

Hibernate Mode

The ICs have a low-power hibernate mode that can accurately fuel gauge the battery when the charge/discharge rate is low. By default, the device automatically enters and exits the hibernate mode according to the charge/discharge rate, which minimizes quiescent current (below 5µA) without compromising fuel-gauge accuracy. The ICs can be forced into hibernate or active modes. Force the IC into hibernate mode to reduce power consumption in applications with less than C/4-rate maximum loading. For applications with higher loading, Maxim recommends the default configuration of automatic control of hibernate mode.

In hibernate mode, the device reduces its ADC conversion period and SOC update to once per 45s. See the *HIBRT Register (0x0A)* section for details on how the IC automatically enters and exits hibernate mode.

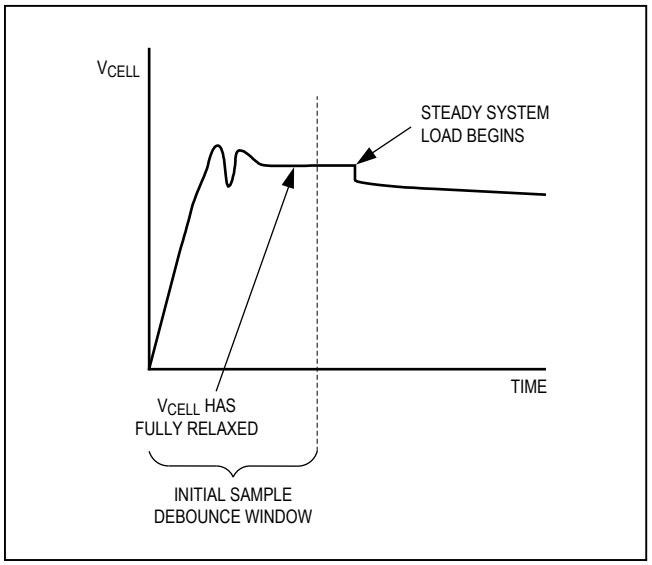


Figure 6. Insertion Waveform Not Requiring Quick-Start Command

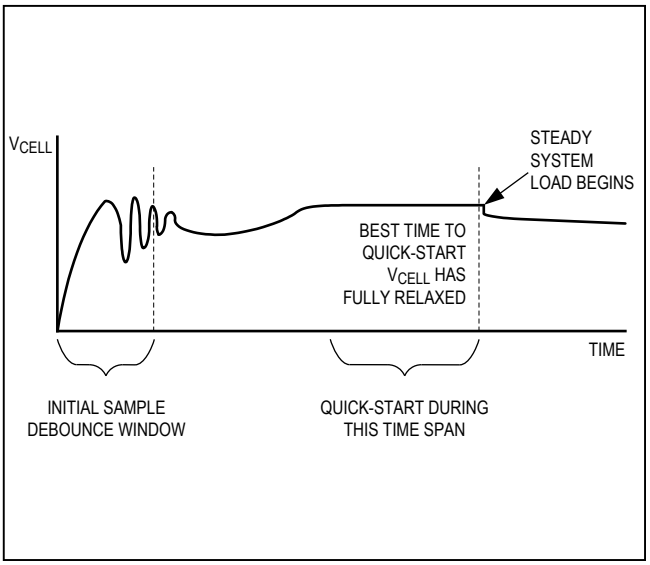


Figure 7. Insertion Waveform Requiring Quick-Start Command

电池更换检测

当V_{CELL}低于V_{RST}时，集成电路将在V CELL回升至高于V_{RST}时快速启动。此功能用于处理电池更换；前一块电池的SOC不会影响新电池的SOC。详见快速启动和*VRESET/ID寄存器（0x18）*章节。

快速启动

若集成电路产生错误的初始SOC，需检查电池插入及系统上电电压波形，以确定是否需要快速启动及执行该命令的最佳时机。集成电路在前17毫秒内采样最大VCELL。 详见电池插入消抖章节。除非VCELL完全稳定，否则即使是最佳采样的电压也可能高于或低于开路电压（OCV）。因此，快速启动必须谨慎使用。

大多数系统不应使用快速启动，因为集成电路能够透明地处理大多数启动问题，例如插入时电池端子连接不稳定。如果电池电压在17ms内稳定，如图6所示，则不应使用快速启动。

快速启动命令以与集成电路初次上电相同的方式重新启动电量计计算。如果系统上电序列噪声较大，导致SOC初始估计误差不可接受，系统微控制器可能通过使用快速启动来减少误差。快速启动通过QSTRT引脚的上升沿触发，或通过向MODE寄存器中的快速启动位写入1来启动。

上电复位（POR）

上电复位包含快速启动，因此仅在电池完全稳定时使用。请参阅快速启动章节。此命令将所有寄存器恢复为默认值。

执行此命令后，请重新加载自定义模型。请参阅*CMD寄存器 (0xFE)*章节。

休眠模式

该集成电路具备低功耗休眠模式，在充放电速率较低时，能够准确地对电池进行电量计量。设备默认根据充放电速率自动进入和退出休眠模式，从而在不影响电量计准确性的前提下，将静态电流降至最低（低于5μA）。 该集成电路可被强制切换至休眠模式或活动模式。在最大负载低于C/4速率的应用中，可强制集成电路进入休眠模式以降低功耗。

对于负载较高的应用，Maxim建议采用默认配置，即自动控制休眠模式。

在休眠模式下，设备将ADC转换周期和SOC更新频率降低至每45秒一次。有关集成电路如何自动进入和退出休眠模式的详细信息，请参见*HIBRT*寄存器*(0x0A)*章节。

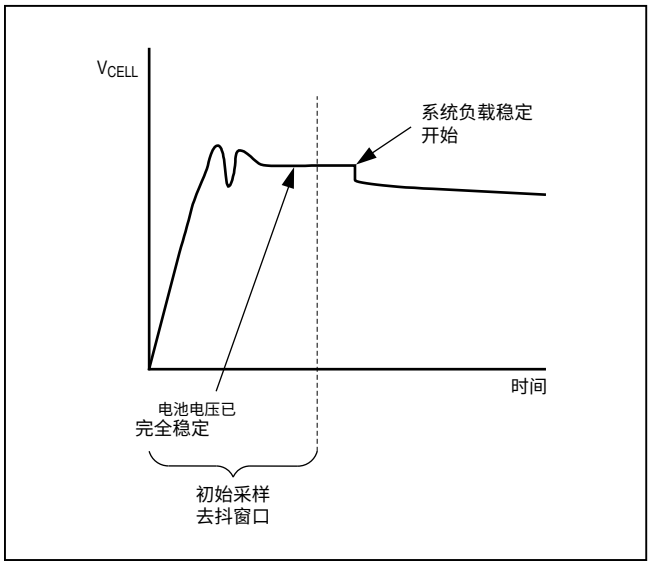


图6。 无需快速启动命令的插入波形

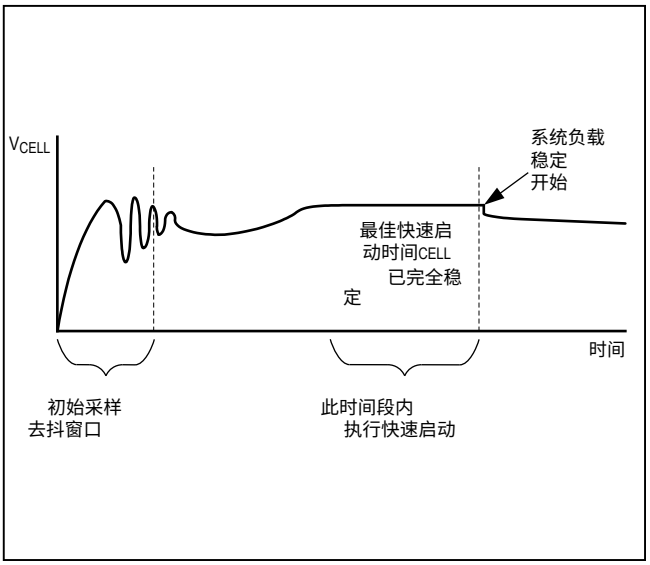


图7。 需要快速启动命令的插入波形

Alert Interrupt

The ICs can interrupt a system microcontroller with five configurable alerts (see Table 1). All alerts can be disabled or enabled with software. When the interrupt occurs, the system microcontroller can determine the cause from the STATUS register.

When an alert is triggered, the IC drives the $\overline{ALRT}$ pin logic-low and sets CONFIG.ALRT = 1. The $\overline{ALRT}$ pin remains logic-low until the system software writes CONFIG.ALRT = 0 to clear the alert. The alert function is enabled by default, so any alert can occur immediately upon power-up. Entering sleep mode clears no alerts.

Sleep Mode

In sleep mode, the IC halts all operations, reducing current consumption to below 1µA. After exiting sleep mode, the IC continues normal operation. In sleep mode, the IC does not detect self-discharge. If the battery changes state while the IC sleeps, the IC cannot detect it, causing SOC error. Wake up the IC before charging or discharging. To enter sleep mode, write MODE.EnSleep = 1 and either:

- Hold SDA and SCL logic-low for a period for t_{SLEEP}. A rising edge on SDA or SCL wakes up the IC.
- Write CONFIG.SLEEP = 1. To wake up the IC, write CONFIG.SLEEP = 0. Other communication does not wake up the IC. POR does wake up the IC.

Applications which can tolerate 4µA should use hibernate rather than sleep mode.

Register Summary

All registers must be written and read as 16-bit words; 8-bit writes cause no effect. Any bits marked X (don't care) or read only must be written with the rest of the register, but the value written is ignored by the IC. The values read from don't care bits are undefined. Calculate the register's value by multiplying the 16-bit word by the register's LSb value, as shown in Table 2.

VCELL Register (0x02)

The MAX17048 measures VCELL between the V_{DD} and GND pins. The MAX17049 measures VCELL between the CELL and GND pins. VCELL is the average of four ADC conversions. The value updates every 250ms in active mode and every 45s in hibernate mode.

SOC Register (0x04)

The ICs calculate SOC using the ModelGauge algorithm. This register automatically adapts to variation in battery size since ModelGauge naturally recognizes relative SOC.

The upper byte least-significant bit has units of 1%. The lower byte provides additional resolution.

The first update is available approximately 1s after POR of the IC. Subsequent updates occur at variable intervals depending on application conditions.

Table 1. Alert Interrupt Summary

ALERT FUNCTION	WHERE CONFIGURED	INDICATOR BIT
Low SOC	CONFIG.ATHD	STATUS.HD
SOC 1% change	CONFIG.ALSC	STATUS.SC
Reset	VRESET, STATUS.RI	STATUS.VR
Overvoltage	VALRT.MAX	STATUS.VH
Undervoltage	VALRT.MIN	STATUS.VL

Table 2. Register Summary

ADDRESS	REGISTER NAME	16-BIT LSb	DESCRIPTION	READ/WRITE	DEFAULT
0x02	VCELL	78.125µV/cell	ADC measurement of VCELL.	R	—
0x04	SOC	1%/256	Battery state of charge.	R	—
0x06	MODE	—	Initiates quick-start, reports hibernate mode, and enables sleep mode.	W	0x0000
0x08	VERSION	—	IC production version.	R	0x001_
0x0A	HIBRT	—	Controls thresholds for entering and exiting hibernate mode.	R/W	0x8030

警报中断

该集成电路可通过五个可配置警报中断系统微控制器（见表1）。 所有警报均可通过软件启用或禁用。中断发生时，系统微控制器可通过状态寄存器确定中断原因。

警报触发时，集成电路将$\overline{ALRT}$引脚拉低，并设置CONFIG.$\overline{ALRT}$ = 1。 $\overline{ALRT}$引脚保持逻辑低电平，直到系统软件写入CONFIG.$\overline{ALRT}$ = 0以清除警报。警报功能默认启用，因此任何警报可在上电后立即触发。进入睡眠模式不会清除任何警报。

睡眠模式

在睡眠模式下，集成电路停止所有操作，将电流消耗降至低于1μA。 退出睡眠模式后，集成电路恢复正常工作。在睡眠模式下，集成电路不检测自放电。若电池在集成电路睡眠期间状态发生变化，集成电路无法检测，导致SOC误差。在充电或放电前须唤醒集成电路。要进入睡眠模式，写入MODE.EnSleep = 1并满足以下任一条件：

- 保持SDA和SCL逻辑低电平持续时间为t_{SLEEP}。SDA或SCL上的上升沿将唤醒集成电路。
- 写入CONFIG.SLEEP = 1。 要唤醒该集成电路，请写入CONFIG.SLEEP = 0。 其他通信不会唤醒该集成电路。上电复位（POR）会唤醒该集成电路。

能够容忍4μA电流的应用应使用休眠模式，而非睡眠模式。

寄存器摘要

所有寄存器必须以16位字进行读写；
8位写入无效。任何标记为X（无关）或只读的位必须与寄存器的其余位一起写入，但写入的值将被集成电路忽略。无关位读取的值未定义。通过将16位字乘以寄存器的最低有效位值来计算寄存器的值，如表2所示。

VCELL寄存器（0x02）

MAX17048测量V_{DD}与接地引脚之间的VCELL。 MAX17049测量CELL与接地引脚之间的VCELL。 VCELL为四次ADC转换的平均值。该数值在活动模式下每250毫秒更新一次，在休眠模式下每45秒更新一次。

SOC寄存器（0x04）

该集成电路采用ModelGauge算法计算SOC。
该寄存器可自动适应电池容量的变化，因为ModelGauge算法天然识别相对SOC。高字节最低有效位的单位为1%。 低字节提供更高的分辨率。

首次更新约在集成电路上电复位（POR）后1秒可用，后续更新根据应用条件以可变间隔进行。

表1. 警报中断摘要

警报功能	配置位置	指示位
低电池荷电状态警报	CONFIG.ATHD	STATUS.HD
SOC 1%变化	CONFIG.ALSC	STATUS.SC
复位	VRESET, STATUS.RI	STATUS.VR
过压	VALRT.MAX	STATUS.VH
欠压	VALRT.MIN	STATUS.VL

表2. 寄存器摘要

地址	寄存器名称	16位最低有效位	描述	读/写	默认值
0x02	VCELL	78.125μV/单元	VCELL的ADC测量值。	R	—
0x04	SOC	1%/256	电池荷电状态。	R	—
0x06	MODE	—	启动快速启动，报告休眠模式，并启用睡眠模式。	写	0x0000
0x08	版本	—	集成电路生产版本。	R	0x001_
0x0A	HIBRT	—	控制进入和退出休眠模式的阈值。	读/写	0x8030

Table 2. Register Summary (continued)

ADDRESS	REGISTER NAME	16-BIT LSb	DESCRIPTION	READ/WRITE	DEFAULT
0x0C	CONFIG	—	Compensation to optimize performance, sleep mode, alert indicators, and configuration.	R/W	0x971C
0x14	VALRT	—	Configures the VCELL range outside of which alerts are generated.	R/W	0x00FF
0x16	CRATE	0.208%/hr	Approximate charge or discharge rate of the battery.	R	—
0x18	VRESET/ID	—	Configures VCELL threshold below which the IC resets itself, ID is a one-time factory-programmable identifier.	R/W	0x96__
0x1A	STATUS	—	Indicates overvoltage, undervoltage, SOC change, SOC low, and reset alerts.	R/W	0x01__
0x40 to 0x7F	TABLE	—	Configures battery parameters.	W	—
0xFE	CMD	—	Sends POR command.	R/W	0xFFFF

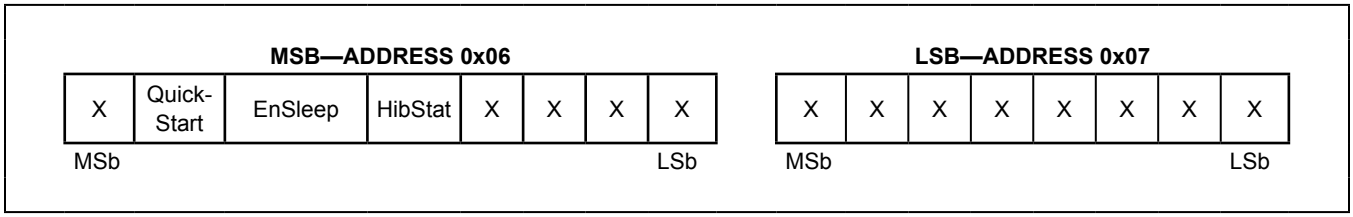


Figure 8. MODE Register Format

MODE Register (0x06)

The MODE register allows the system processor to send special commands to the IC (see Figure 8).

- **Quick-Start** generates a first estimate of OCV and SOC based on the immediate cell voltage. Use with caution; see the *Quick-Start* section.
- **EnSleep** enables sleep mode. See the *Sleep Mode* section.
- **HibStat** indicates when the IC is in hibernate mode (read only).

VERSION Register (0x08)

The value of this read-only register indicates the production version of the IC.

表 2. 寄存器摘要（续）

地址	寄存器名称	16位最低有效位	描述	读/写	默认值
0x0C	CONFIG	—	用于补偿以优化性能、睡眠模式、警报指示及配置。	读/写	0x971C
0x14	VALRT	—	配置VCELL范围，超出该范围时触发警报。	读/写	0x00FF
0x16	CRATE	0.208%/小时	电池的近似充放电速率。	R	—
0x18	VRESET/ID	—	配置VCELL阈值，低于该阈值集成电路将自动复位，ID为一次性工厂可编程标识符。	读/写	0x96__
0x1A	状态	—	指示过压、欠压、SOC变化、SOC低电量及复位警报。	读/写	0x01__
0x40至0x7F	表	—	配置电池参数。	写	—
0xFE	命令	—	发送上电复位（POR）命令。	读/写	0xFFFF

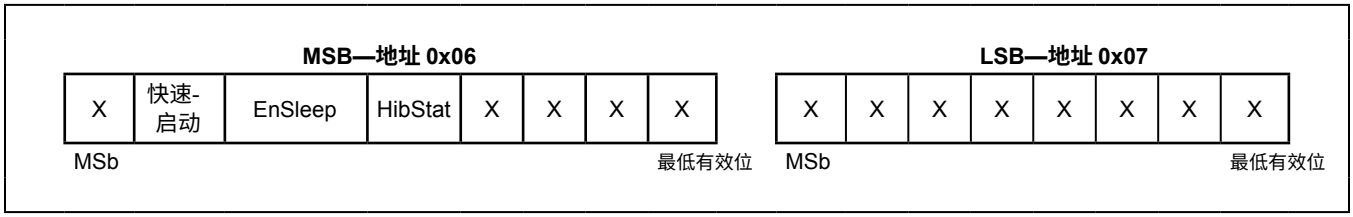


图 *8. MODE*寄存器格式

MODE寄存器（0x06）

MODE寄存器允许系统处理器向集成电路发送特殊命令（见图8）。

- **快速启动**基于即时电池电压生成OCV和SOC的初步估计，使用时请谨慎；请参阅快速启动章节。
- **EnSleep** 启用睡眠模式。请参阅睡眠模式章节。
- **HibStat**指示集成电路处于休眠模式（只读）。

VERSION寄存器 (0x08)

该只读寄存器的值表示集成电路的生产版本。

HIBRT Register (0x0A)

To disable hibernate mode, set HIBRT = 0x0000. To always use hibernate mode, set HIBRT = 0xFFFF (see Figure 9).

- **ActThr** (active threshold): If at any ADC sample |OCV-CELL| is greater than ActThr, the IC exits hibernate mode. 1 LSb = 1.25mV.
- **HibThr** (hibernate threshold). If the absolute value of CRATE is less than HibThr for longer than 6min, the IC enters hibernate mode. 1 LSb = 0.208%/hr.

CONFIG Register (0x0C)

- **RCOMP** is an 8-bit value that can be adjusted to optimize IC performance for different lithium chemistries or different operating temperatures. Contact Maxim for instructions for optimization. The POR value of RCOMP is 0x97.
- **SLEEP** forces the IC in or out of sleep mode if Mode. EnSleep is set. Writing 1 forces the IC to enter sleep mode, and 0 forces the IC to exit. The POR value of SLEEP is 0.
- **ALSC** (SOC change alert) enables alerting when SOC changes by at least 1%. Each alert remains until STATUS.SC is cleared, after which the alert automatically clears until SOC again changes by 1%. Do not use this alert to accumulate changes in SOC.
- **ALRT** (alert status bit) is set by the IC when an alert occurs. When this bit is set, the $\overline{ALRT}$ pin asserts low. Clear this bit to service and deassert the $\overline{ALRT}$ pin. The power-up default value for ALRT is 0. The STATUS register specifies why the $\overline{ALRT}$ pin was asserted.
- **ATHD** (empty alert threshold) sets the SOC threshold, where an interrupt is generated on the $\overline{ALRT}$ pin and can be programmed from 1% up to 32%. The value is (32 - ATHD)% (e.g., 00000b → 32%, 00001b → 31%, 00010b → 30%, 11111b → 1%). The POR value of ATHD is 0x1C, or 4%. The alert only occurs on a falling edge past this threshold.

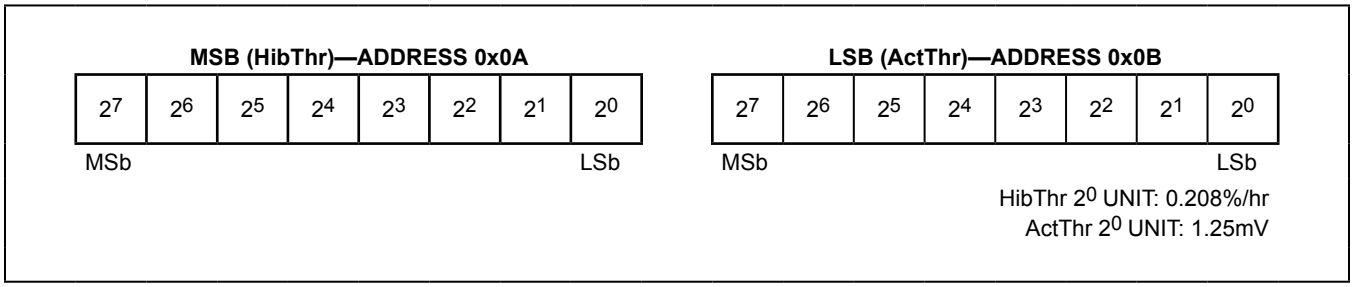


Figure 9. HIBRT Register Format

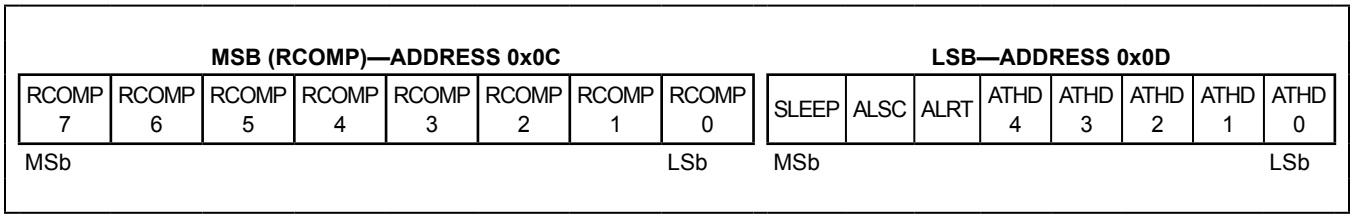


Figure 10. CONFIG Register Format

HIBRT寄存器（0x0A）

要禁用休眠模式，请将 HIBRT 设置为 0x0000。 要始终启用休眠模式，请将 HIBRT 设置为 0xFFFF（见图9）。

- **ActThr**（活动阈值）：若任一ADC采样中 |OCV - CELL| 大于 ActThr，IC将退出休眠模式。1最低有效位 = 1.25mV。
- **HibThr**（休眠阈值）。 若 CRATE 绝对值低于 HibThr 超过6分钟，IC将进入休眠模式。1最低有效位 = 0.208%/小时。

CONFIG寄存器（0x0C）

- **RCOMP**为8位数值，可调节以优化IC在不同锂电化学体系或不同工作温度下的性能。请联系Maxim获取优化指导。RCOMP的POR值为0x97。
- 当Mode.**E**n**S**leep被设置时，**SLEEP**用于强制IC进入或退出睡眠模式。写入1强制IC进入睡眠模式，写入0强制IC退出睡眠模式。SLEEP的POR值为0。
- **ALSC**（SOC变化警报）在SOC变化达到至少1%时启用警报功能。每个警报将持续有效，直到STATUS.SC被清除，之后警报自动清除，直至SOC再次变化1%。请勿使用此警报来累计SOC的变化量。
- **ALRT**（警报状态位）在发生警报时由IC置位。当该位被置位时， $\overline{\text{ALRT}}$引脚将拉低。清除此位以响应警报并释放 $\overline{\text{ALRT}}$引脚。$\overline{\text{ALRT}}$的上电默认值为0。 状态寄存器指明了 $\overline{\text{ALRT}}$引脚被触发的原因。
- **ATHD**（空警报阈值）设置SOC阈值，当达到该阈值时， $\overline{\text{ALRT}}$引脚会产生中断，该阈值可编程范围为1%至32%。 该值为(32 - ATHD)%（例如，00000b →32%，00001b → 31%，00010b →30%，11111b →1%）。 ATHD的POR值为0x1C，即4%。 警报仅在下降沿越过该阈值时触发。

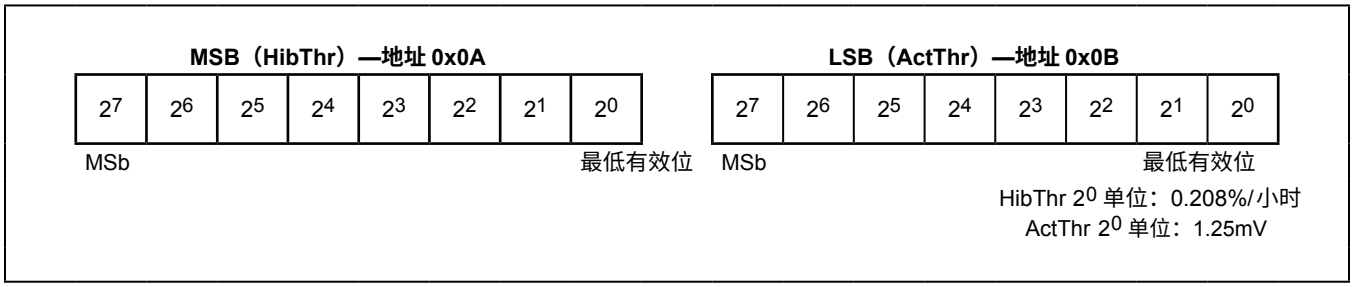


图*9. HIBRT*寄存器格式

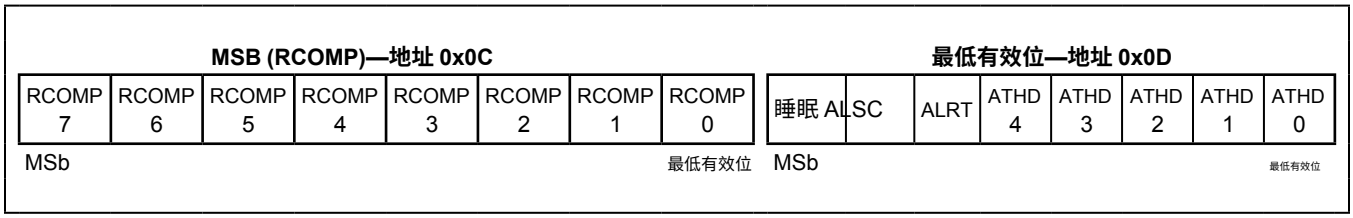


图*10. CONFIG*寄存器格式

VALRT Register (0x14)

This register is divided into two thresholds: Voltage alert maximum (VALRT.MAX) and minimum (VALRT. MIN). Both registers have 1 LSb = 20mV. The IC alerts while VCELL > VALRT.MAX or VCELL < VALRT.MIN (see Figure 11).

CRATE Register (0x16)

The IC calculates an approximate value for the average SOC rate of change. 1 LSb = 0.208% per hour (not for conversion to ampere).

VRESET/ID Register (0x18)

See Figure 12.

- **ID** is an 8-bit read-only value that is one-time programmable at the factory, which can be used as an identifier to distinguish multiple cell types in production. Writes to these bits are ignored.
- **VRESET[7:1]** adjusts a fast analog comparator and a slower digital ADC threshold to detect battery removal and reinsertion. For captive batteries, set to 2.5V. For removable batteries, set to at least 300mV below the application's empty voltage, according to the desired reset threshold for your application. If the comparator is enabled, the IC resets 1ms after VCELL rises above the threshold. Otherwise, the IC resets 250ms after the VCELL register rises above the threshold.
- **Dis.** Set Dis = 1 to disable the analog comparator in hibernate mode to save approximately 0.5µA.

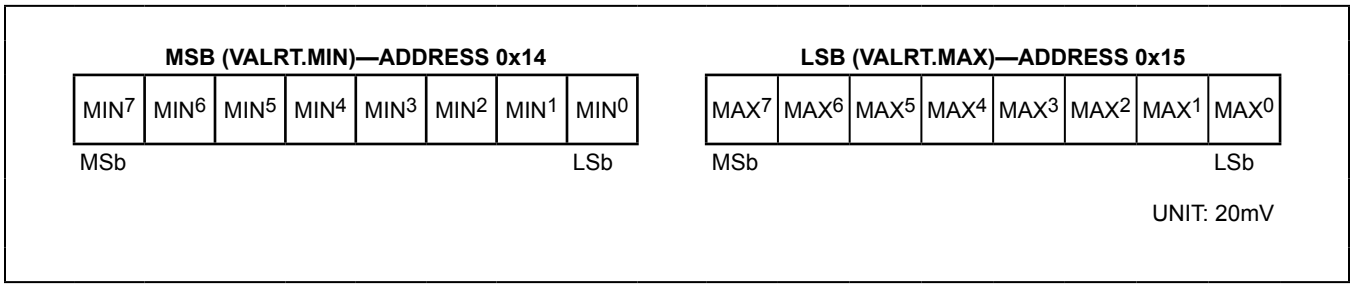


Figure 11. VALRT Register Format

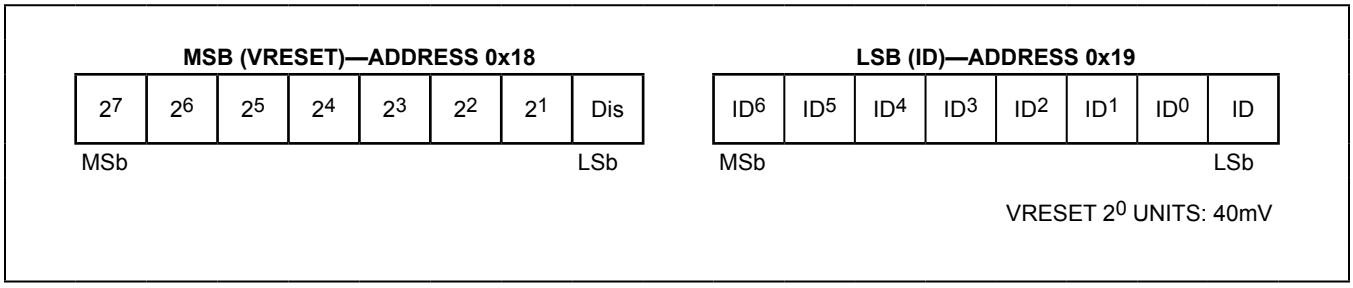


Figure 12. VRESET/ID Register Format

VALRT寄存器 (0x14)

该寄存器分为两个阈值：电压警报最大值（VALRT.MAX）和最小值（VALRT.MIN）。两个阈值的最低有效位均为20mV。 当VCELL > VALRT.MAX或VCELL < VALRT.MIN时，IC会发出警报（见图11）。

CRATE寄存器（0x16）

IC计算平均SOC变化率的近似值。1最低有效位等于每小时0.208%（不用于转换为安培）。

VRESET/ID寄存器（0x18）

参见图12。

- **ID**为8位只读值，工厂一次性编程，可用作标识符以区分生产中的多种电池类型。对这些位的写入将被忽略。
- **VRESET[7:1]**用于调整快速模拟比较器和较慢数字ADC的阈值，以检测电池的拆卸和重新插入。对于固定电池，设置为2.5V；对于可拆卸电池，应根据应用的空电压及所需复位阈值，设置为至少低于空电压300mV。 如果比较器启用，当VCELL超过阈值时，IC将在1ms后复位。否则，当VCELL寄存器超过阈值时，IC将在250ms后复位。
- **Dis.**设置Dis = 1以在休眠模式下禁用模拟比较器，从而节省约0.5µA电流。

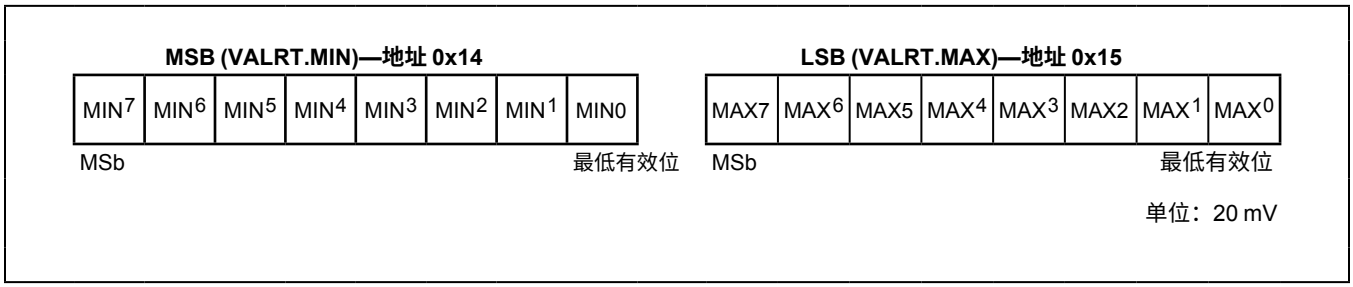


图*11. VALRT*寄存器格式

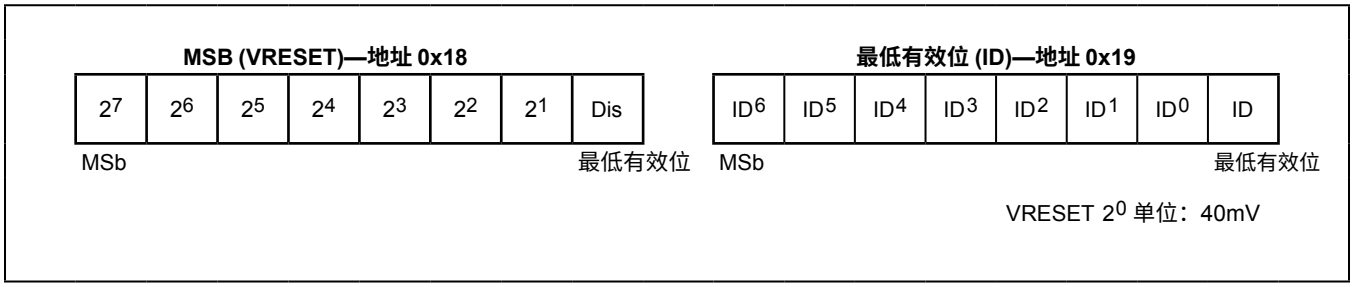


图*12. VRESET/ID*寄存器格式

STATUS Register (0x1A)

An alert can indicate many different conditions. The STATUS register identifies which alert condition was met. Clear the corresponding bit after servicing the alert (see Figure 13).

Reset Indicator:

- **RI** (reset indicator) is set when the device powers up. Any time this bit is set, the IC is not configured, so the model should be loaded and the bit should be cleared.

Alert Descriptors:

These bits are set only when they cause an alert (e.g., if CONFIG.ALSC = 0, then SC is never set).

- **VH** (voltage high) is set when VCELL has been above ALRT.VALRTMAX.
- **VL** (voltage low) is set when VCELL has been below ALRT.VALRTMIN.
- **VR** (voltage reset) is set after the device has been reset if EnVr is set.
- **HD** (SOC low) is set when SOC crosses the value in CONFIG.ATHD.
- **SC** (1% SOC change) is set when SOC changes by at least 1% if CONFIG.ALSC is set.

Enable or Disable VRESET Alert:

- **EnVr** (enable voltage reset alert) when set to 1 asserts the $\overline{\text{ALRT}}$ pin when a voltage-reset event occurs under the conditions described by the VRESET/ ID register.

TABLE Registers (0x40 to 0x7F)

Contact Maxim for details on how to configure these registers. The default value is appropriate for some Li+ batteries.

To unlock the TABLE registers, write 0x57 to address 0x3F, and 0x4A to address 0x3E. While TABLE is unlocked, no ModelGauge registers are updated, so relock as soon as possible by writing 0x00 to address 0x3F, and 0x00 to address 0x3E.

CMD Register (0xFE)

Writing a value of 0x5400 to this register causes the device to completely reset as if power had been removed (see the *Power-On Reset (POR)* section). The reset occurs when the last bit has been clocked in. The IC does not respond with an I^2C ACK after this command sequence.

Application Examples

The ICs have a variety of configurations, depending on the application. Table 3 shows the most common system configurations and the proper pin connections for each.

In all cases, the system must provide pullup circuits for $\overline{\text{ALRT}}$ (if used), SDA, and SDL.

Figure 14 shows an example application for a 1S cell pack. In this example, the $\overline{\text{ALRT}}$ pin is connected to the microcontroller's interrupt input to allow the MAX17048 to signal when the battery is low. The QSTRT pin is unused in this application and is connected to GND.

Figure 15 shows a MAX17049 example application using a 2S cell pack. The MAX17049 is mounted on the system side and powered from a 3.3V supply generated by the system. The CELL pin is still connected directly to PACK+.

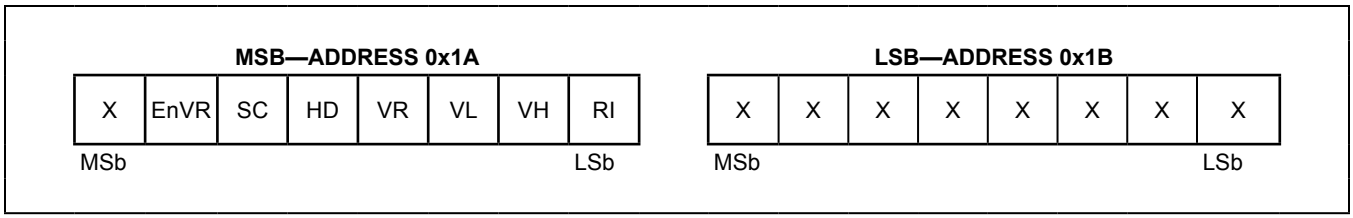


Figure 13. STATUS Register Format

状态寄存器 (0x1A)

警报可指示多种不同的状态。状态寄存器用于识别触发的警报条件。处理警报后应清除相应位（参见图13）。

复位指示器：

- **RI**（复位指示器）在设备上电时被置位。每当该位被置位时，集成电路尚未配置，因此应加载模型并清除此位。

警报描述符：

这些位仅在引发警报时被置位（例如，若CONFIG.ALSC = 0，则SC位永远不会被置位）。

- **VH**（电压高）当VCELL高于ALRT.VALRTMAX时被置位。
- **VL**（电压低）当VCELL低于ALRT.VALRTMIN时被置位。
- **VR**（电压复位）若EnVr被置位，则设备复位后该位被置位。
- 当SOC超过CONFIG.AT**HD**中设定的值时，**HD**（SOC低）标志被置位。
- 当**SOC**变化达到至少1%且**C**ONFIG.AL**SC**被设置时，**SC**（1% SOC变化）标志被置位。

启用或禁用VRESET警报：

- **EnVr**（启用电压复位警报）设置为1时，在满足VRESET/ID寄存器所描述条件的电压复位事件发生时，$\overline{\text{ALRT}}$引脚将被触发。

表 寄存器（0x40至0x7F）

有关如何配置这些寄存器的详细信息，请联系Maxim。 默认值适用于部分锂离子电池。

要解锁表寄存器，请向地址0x3F写入0x57，向地址0x3E写入0x4A。 在表寄存器解锁期间，ModelGauge寄存器不会更新，因此应尽快通过向地址0x3F写入0x00，向地址0x3E写入0x00来重新锁定。

CMD寄存器 (0xFE)

向该寄存器写入0x5400会使设备完全复位，仿佛断电一样（详见上电复位（*POR*）章节）。 复位在最后一位时钟输入后发生。该集成电路在此命令序列后不会响应I²C确认信号。

应用示例

这些集成电路根据具体应用具有多种配置。表3列出了最常见的系统配置及其对应的正确引脚连接方式。

在所有情况下，系统必须为$\overline{\text{ALRT}}$（如使用）、SDA和SDL提供上拉电路。

图14展示了一个1S电池组的示例应用。在该示例中，$\overline{\text{ALRT}}$引脚连接至微控制器的中断输入，以便MAX17048在电池电量低时发出信号。QSTRT引脚在此应用中未使用，连接至接地。图15展示了使用2S电池组的MAX17049示例应用。MAX17049安装于系统侧，由系统产生

的3.3V电源供电。CELL引脚仍直接连接至PACK+。

MSB—地址 0x1A

X	EnVR	SC	HD	VR	VL	VH	RI
MSb							最低有效位

最低有效位—地址 0x1B

X	X	X	X	X	X	X	X
MSb							最低有效位

图*13.* 状态寄存器格式

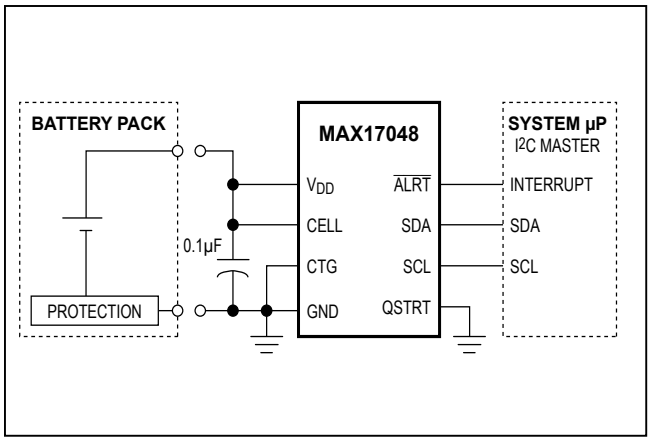


Figure 14. MAX17048 Application Circuit (1S Cell Pack)

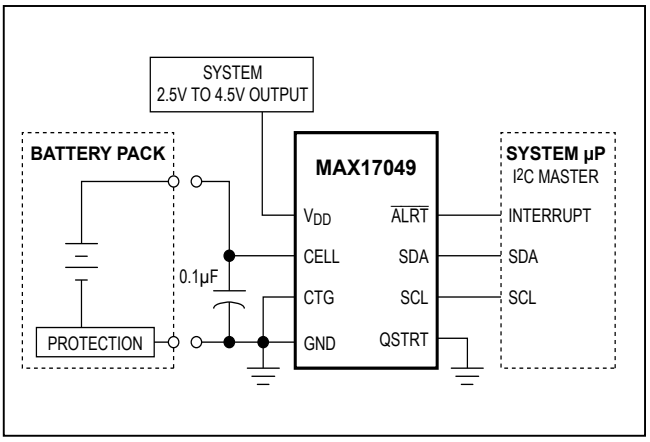


Figure 15. MAX17049 Application Circuit (2S Cell Pack)

Table 3. Possible Application Configurations

SYSTEM CONFIGURATION	IC	V_{DD}	ALRT	QSTRT
1S pack-side location	MAX17048	Power directly from battery	Leave unconnected	Connect to GND
1S host-side location	MAX17048	Power directly from battery	Leave unconnected	Connect to GND
1S host-side location, low-cell interrupt	MAX17048	Power directly from battery	Connect to system interrupt	Connect to GND
1S host-side location, hardware quick-start	MAX17048	Power directly from battery	Leave unconnected	Connect to rising-edge reset signal
2S pack-side location	MAX17049	Power from +2.5V to +4.5V LDO in pack	Leave unconnected	Connect to GND
2S host-side location	MAX17049	Power from +2.5V to +4.5V LDO or PMIC	Leave unconnected	Connect to GND
2S host-side location, low-cell interrupt	MAX17049	Power from +2.5V to +4.5V LDO or PMIC	Connect to system interrupt	Connect to GND
2S host-side location, hardware quick-start	MAX17049	Power from +2.5V to +4.5V LDO or PMIC	Leave unconnected	Connect to rising-edge reset signal

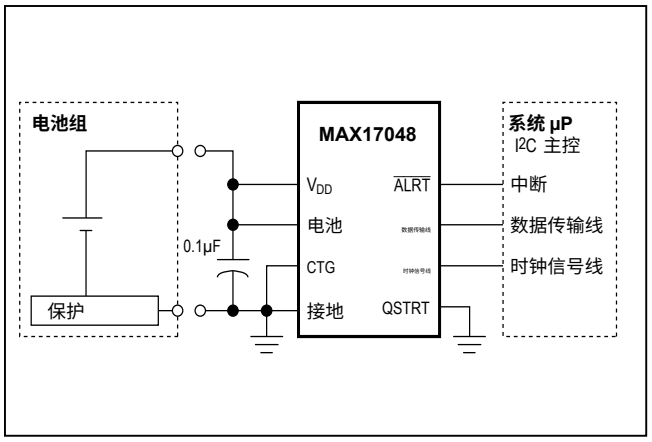


图*14. MAX17048*应用电路（*1*节电池组）

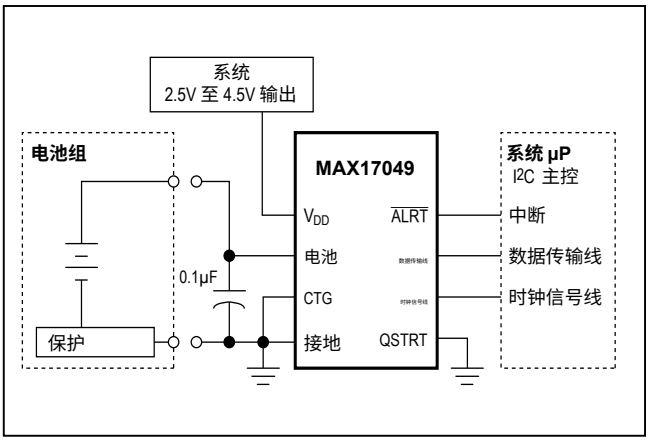


图*15. MAX17049*应用电路（*2*节电池组）

表3. 可能的应用配置

系统配置	集成电路	V_{DD}	ALRT	QSTRT
1S 电池组侧位置	MAX17048	直接由电池供电	保持悬空	连接至接地
1S 主机侧位置	MAX17048	直接由电池供电	保持悬空	连接至接地
1S 主机侧位置，低电压中断	MAX17048	直接由电池供电	连接至系统中断	连接至接地
1S 主机侧位置，硬件快速启动	MAX17048	直接由电池供电	保持悬空	连接至上升沿复位信号
2S 电池组侧位置	MAX17049	来自电池组中+2.5V至+4.5 V LDO的电源	保持悬空	连接至接地
2S 主机侧位置	MAX17049	来自+2.5V至+4.5V LDO或PMIC的电源	保持悬空	连接至接地
2S 主机侧位置，低电压中断	MAX17049	来自+2.5V至+4.5V LDO或PMIC的电源	连接至系统中断	连接至接地
2S 主机侧位置，硬件快速启动	MAX17049	来自+2.5V至+4.5V LDO或PMIC的电源	保持悬空	连接至上升沿复位信号

I²C Bus System

The I²C bus system supports operation as a slave-only device in a single or multislave, and single or multimaster system. Slave devices can share the bus by uniquely setting the 7-bit slave address. The I²C interface consists of a serial-data line (SDA) and serial-clock line (SCL). SDA and SCL provide bidirectional communication between the IC's slave device and a master device at speeds up to 400kHz. The IC's SDA pin operates bidirectionally; that is, when the IC receives data, SDA operates as an input, and when the IC returns data, SDA operates as an open-drain output, with the host system providing a resistive pullup. The IC always operates as a slave device, receiving and transmitting data under the control of a master device. The master initiates all transactions on the bus and generates the SCL signal, as well as the START and STOP bits, which begin and end each transaction.

Bit Transfer

One data bit is transferred during each SCL clock cycle, with the cycle defined by SCL transitioning low-to-high and then high-to-low. The SDA logic level must remain stable during the high period of the SCL clock pulse. Any change in SDA when SCL is high is interpreted as a START or STOP control signal.

Bus Idle

The bus is defined to be idle, or not busy, when no master device has control. Both SDA and SCL remain high when the bus is idle. The STOP condition is the proper method to return the bus to the idle state.

START and STOP Conditions

The master initiates transactions with a START condition (S) by forcing a high-to-low transition on SDA while SCL is high. The master terminates a transaction with a STOP condition (P), a low-to-high transition on SDA while SCL is high. A Repeated START condition (Sr) can be used in place of a STOP then START sequence to terminate one transaction and begin another without returning the bus to the idle state. In multimaster systems, a Repeated START allows the master to retain control of the bus. The START and STOP conditions are the only bus activities in which the SDA transitions when SCL is high.

Acknowledge Bits

Each byte of a data transfer is acknowledged with an acknowledge bit (A) or a no-acknowledge bit (N). Both the master and the MAX17048 slave generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low until SCL returns low. To generate a no- acknowledge (also called NAK), the receiver releases SDA before the rising edge of the acknowledge-related clock pulse and leaves SDA high until SCL returns low. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer can occur if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication.

Data Order

A byte of data consists of 8 bits ordered most significant bit (MSb) first. The least significant bit (LSb) of each byte is followed by the acknowledge bit. The IC registers composed of multibyte values are ordered MSB first. The MSB of multibyte registers is stored on even data-memory addresses.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by a slave address (SAddr) and the read/write (R/W) bit. When the bus is idle, the ICs continuously monitor for a START condition followed by its slave address. When the ICs receive a slave address that matches the value in the slave address register, they respond with an acknowledge bit during the clock period following the R/W bit. The 7-bit slave address is fixed to 0x6C (write)/0x6D (read):

MAX17048/MAX17049 SLAVE ADDRESS	0110110

Read/Write Bit

The R/W bit following the slave address determines the data direction of subsequent bytes in the transfer. R/W = 0 selects a write transaction with the following bytes being written by the master to the slave. R/W = 1 selects a read transaction with the following bytes being read from the slave by the master (Table 4).

I²C 总线系统

I²C 总线系统支持作为单从设备运行，适用于单从或多从、单主或多主系统。从设备可通过唯一设置的7位从设备地址共享总线。I²C 接口由串行数据线（SDA）和串行时钟线（SCL）组成。SDA 和 SCL 在最高400kHz速率下，实现集成电路从设备与主设备之间的双向通信。集成电路的 SDA 引脚支持双向操作；即当集成电路接收数据时，SDA 作为输入；当集成电路发送数据时，SDA 作为开漏输出，由主系统提供上拉电阻。

该集成电路始终作为从设备运行，在主设备的控制下接收和传输数据。

主设备启动总线上的所有事务，并生成时钟信号线（SCL）信号，以及启动条件（START）和停止条件（STOP）位，用以开始和结束每个事务。

位传输

每个SCL时钟周期传输一个数据位，该周期由SCL从低电平跳变至高电平再跳变回低电平定义。在SCL时钟脉冲的高电平期间，数据传输线（SDA）的逻辑电平必须保持稳定。

当SCL为高电平时，SDA的任何变化均被视为启动条件（START）或停止条件（STOP）控制信号。

总线空闲

当无主设备控制时，总线被定义为空闲状态或非忙状态。总线空闲时，SDA和SCL均保持高电平。停止条件（STOP）是将总线恢复至空闲状态的正确方法。

启动条件与停止条件

主设备通过在SCL为高电平时强制SDA由高电平跳变至低电平来发起启动条件（START）事务。主设备通过停止条件（P）终止事务，即在SCL为高电平时，SDA由低电平跳变至高电平。重复启动条件（Sr）可替代停止条件后紧接启动条件的序列，用于终止一个事务并开始另一个事务，而无需将总线返回空闲状态。在多主机系统中，重复启动允许主设备保持对总线的控制。启动条件和停止条件是唯一在SCL为高电平时SDA发生跳变的总线活动。

应答位

每个数据传输字节均通过应答位（A）或无应答位（N）进行确认。主设备和MAX17048从设备均会产生应答位。为产生应答，接收设备必须在与应答相关的时钟脉冲（第九脉冲）上升沿之前将SDA拉低，并保持低电平直到SCL变低。为产生无应答（也称NAK），接收设备在应答相关时钟脉冲上升沿之前释放SDA，使其保持高电平，直到SCL变低。监测应答位可用于检测数据传输是否成功。如果接收设备忙碌或系统发生故障，可能导致数据传输失败。在数据传输失败的情况下，总线主控应重新尝试通信。

数据顺序

一个字节的数据由8位组成，按最高有效位（MSb）优先排列。每个字节的最低有效位（LSb）后跟应答位。由多字节值组成的IC寄存器按最高有效位优先排列。

多字节寄存器的最高有效位存储在偶数数据存储地址。

从设备地址

总线主控通过发出启动条件，随后发送从设备地址（SAddr）和读写位（读写位）来启动与从设备的通信。当总线空闲时，集成电路持续监测启动条件及其从设备地址。当集成电路接收到与从设备地址寄存器中值匹配的从设备地址时，会在读写位后的时钟周期内响应应答位。7位从设备地址固定为0x6C（写）/0x6D（读）：

MAX17048 /MAX17049 从设备地址	0110110

读写位

紧跟从设备地址之后的读写位决定了传输中后续字节的数据方向。读写位 = 0 表示写操作，后续字节由主设备写入从设备。读写位 = 1 表示读取事务，后续字节由主设备从从设备读取（见表4）。

Table 4. I²C Protocol Key

KEY	DESCRIPTION	KEY	DESCRIPTION
S	START bit	Sr	Repeated START
SAddr	Slave address (7 bit)	W	R/W bit = 0
MAddr	Memory address byte	P	STOP bit
Data	Data byte written by master	Data	Data byte returned by slave
A	Acknowledge bit—master	A	Acknowledge bit—slave
N	No acknowledge—master	N	No acknowledge bit—slave
		R	R/W bit = 1

Bus Timing

The ICs are compatible with any bus timing up to 400kHz. No special configuration is required to operate at any speed.

I²C Command Protocols

The command protocols involve several transaction formats. The simplest format consists of the master writing the START bit, slave address, R/W bit, and then monitoring the acknowledge bit for presence of the ICs. More complex formats, such as the Write Data and Read Data, read data and execute device-specific operations. All bytes in each command format require the slave or host to return an acknowledge bit before continuing with the next byte. Table 4 shows the key that applies to the transaction formats.

Basic Transaction Formats

A write transaction transfers 2 or more data bytes to the ICs. The data transfer begins at the memory address supplied in the MAddr byte. Control of the SDA signal is retained by the master throughout the transaction, except for the acknowledge cycles:

A read transaction transfers 2 or more bytes from the ICs. Read transactions are composed of two parts, a write portion followed by a read portion, and are therefore inherently longer than a write transaction. The write portion communicates the starting point for the read operation. The read portion follows immediately, beginning with a Repeated START, slave address with R/W set to a 1. Control of SDA is assumed by the ICs, beginning with the slave address acknowledge cycle. Control of the SDA signal is retained by the ICs throughout the transaction, except for the acknowledge cycles. The master indicates the end of a read transaction by responding to the last byte it requires with a no acknowledge. This signals the ICs that control of SDA is to remain with the master following the acknowledge clock.

Write: S. SAddr W. A. MAddr. A. Data0. A. Data1. A. P

Read: S. SAddr W. A. MAddr. A. Sr. SAddr R. A. Data0. A. Data1. N. P

Write Portion | Read Portion

Write Data Protocol

The write data protocol is used to write to register to the ICs starting at memory address MAddr. Data0 represents the data written to MAddr, Data1 represents the data written to MAddr + 1, and DataN represents the last data byte, written to MAddr + N. The master indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit:

S. SAddr W. A. MAddr. A. Data0. A. Data1. A... DataN. A. P

The MSb of the data to be stored at address MAddr can be written immediately after the MAddr byte is acknowledged. Because the address is automatically incremented after the LSb of each byte is received by the ICs, the MSb of the data at address MAddr + 1 can be written immediately after the acknowledgment of the data at address MAddr. If the bus master continues an autoincremented write transaction beyond address 4Fh, the ICs ignore the data. A valid write must include both register bytes. Data is also ignored on writes to read-only addresses. Incomplete bytes and bytes that are not acknowledged by the ICs are not written to memory.

表4. I²C协议关键字

关键字	描述	关键字	描述
S	启动位	Sr	重复启动条件
从设备地址	从设备地址（7位）	写	读写位 = 0
内存地址	内存地址字节	P	停止位
数据	主设备写入的数据字节	数据	从设备返回的数据字节
应答位	应答位——主设备	应答位	应答位——从设备
无应答	无应答——主设备	无应答	无应答位——从设备
		R	读写位 = 1

总线时序

该集成电路兼容最高400kHz的任意总线时序。
无需特殊配置，即可在任意速度下正常工作。

I²C 命令协议

命令协议包含多种事务格式。最简单的格式是主设备发送START位、从设备地址和读写位，然后监控应答位以确认集成电路的存在。更复杂的格式，如写数据和读数据，则涉及读取数据并执行设备特定操作。

每种命令格式中的所有字节均要求从设备或主机返回应答位，方可继续传输下一个字节。表4显示了适用于事务格式的键值说明。

基本事务格式

写操作将两个或更多数据字节传输至集成电路。数据传输从MAddr字节中指定的存储地址开始。在整个事务过程中，数据传输线的控制权由主设备保持，确认周期除外：

读取事务从集成电路传输两个或更多字节。读取事务由写操作部分和读取部分两部分组成，因此其长度本质上长于写操作。写操作部分用于传达读取操作的起始地址。读取部分紧接其后，以重复启动条件开始，从设备地址的R/W位设置为1。

从设备从从设备地址确认周期开始接管数据传输线的控制权。在整个事务过程中，数据传输线的控制权由集成电路保持，确认周期除外。主设备指示通过对所需的最后一个字节响应无应答，表示读取事务结束。该信号通知集成电路，在应答时钟之后，数据传输线的控制权应继续由主设备保持。

写操作：S. SAddr W. A. MAddr. A. 数据0. A. 数据1. A. P

读操作：S. SAddr W. A. MAddr. A. 重复启动条件. SAddr R. A. 数据0. A. 数据1. 无应答. 停止

写入部分　　读取部分

写入数据协议

写入数据协议用于从内存地址MAddr开始向集成电路寄存器写入数据。数据0表示写入MAddr的数据，数据1表示写入MAddr + 1的数据，数据N表示写入MAddr + N的最后一个数据字节。主设备在接收到最后一个应答位后，通过发送停止或重复启动条件来指示写操作结束：

S. SAddr W. A. MAddr. A. 数据0. A. 数据1. A... 数据N. A. P

要存储在地址MAddr的数据的最高有效位（MSb）可在MAddr字节被确认后立即写入。由于地址在每个字节的最低有效位（LSb）被集成电路接收后自动递增，地址MAddr + 1处数据的最高有效位（MSb）可在地址MAddr处数据被确认后立即写入。如果总线主控在地址4Fh之后继续执行自动递增写操作，集成电路将忽略该数据。有效写操作必须包含两个寄存器字节。

对只读地址的写入操作同样会被忽略数据。
未完成的字节以及未被集成电路确认的字节不会写入存储器。

Read Data Protocol

The read data protocol is used to read to register from the ICs starting at the memory address specified by MAddr. Both register bytes must be read in the same transaction for the register data to be valid. Data0 represents the data byte in memory location MAddr, Data1 represents the data from MAddr + 1, and DataN represents the last byte read by the master:

S. SAddr W. A. MAddr. A. Sr. SAddr R. A.
Data0. A. Data1. A... DataN. N. P

Data is returned beginning with the MSb of the data in MAddr. Because the address is automatically incremented after the LSb of each byte is returned, the MSb of the data at address MAddr + 1 is available to the host immediately after the acknowledgment of the data at address MAddr. If the bus master continues to read beyond address FFh, the ICs output data values of FFh. Addresses labeled Reserved in the memory map return undefined data. The bus master terminates the read transaction at any byte boundary by issuing a no acknowledge followed by a STOP or Repeated START.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	DESCRIPTION
MAX17048G+	-40°C to +85°C	8 TDFN-EP*	1-Cell ModelGauge IC
MAX17048G+T10	-40°C to +85°C	8 TDFN-EP*	1-Cell ModelGauge IC
MAX17048X+	-40°C to +85°C	8 WLP	1-Cell ModelGauge IC
MAX17048X+T10	-40°C to +85°C	8 WLP	1-Cell ModelGauge IC
MAX17049G+	-40°C to +85°C	8 TDFN-EP*	2-Cell ModelGauge IC
MAX17049G+T10	-40°C to +85°C	8 TDFN-EP*	2-Cell ModelGauge IC
MAX17049X+	-40°C to +85°C	8 WLP	2-Cell ModelGauge IC
MAX17049X+T10	-40°C to +85°C	8 WLP	2-Cell ModelGauge IC

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 WLP	W80B1+1	**21-0555**	Refer to **Application Note 1891**
8 TDFN-EP	T822+3	**21-0168**	**90-0065**

读取数据协议

读取数据协议用于从集成电路中读取寄存器，起始地址由内存地址字节指定。必须在同一事务中读取两个寄存器字节，方可保证寄存器数据有效。数据0表示内存地址MAddr处的数据字节，数据1表示来自MAddr + 1的数据，数据N表示主控读取的最后一个字节：

S. SAddr W. A. MAddr. A. Sr. SAddr R. A.
数据0. A. 数据1. A... 数据N. N. P

数据从MAddr地址中数据的最高有效位开始返回。由于每个字节的最低有效位返回后地址会自动递增，因此MAddr + 1地址中数据的最高有效位会在MAddr地址数据应答后立即提供给主控。如果总线主控继续读取超过地址FFh，集成电路将输出数据值FFh。内存映射中标记为保留的地址返回未定义数据。总线主控通过发出无应答信号，随后发送停止或重复启动条件，可在任意字节边界终止读取事务。

订购信息

型号	温度范围	引脚-封装	描述
MAX17048G+	-40°C 至 +85°C	8 TDFN-EP*	单节电池ModelGauge集成电路
MAX17048G+T10	-40°C 至 +85°C	8 TDFN-EP*	单节电池ModelGauge集成电路
MAX17048X+	-40°C 至 +85°C	8 WLP	单节电池ModelGauge集成电路
MAX17048X+T10	-40°C 至 +85°C	8 WLP	单节电池ModelGauge集成电路
MAX17049G+	-40°C 至 +85°C	8 TDFN-EP*	双节电池ModelGauge集成电路
MAX17049G+T10	-40°C 至 +85°C	8 TDFN-EP*	双节电池ModelGauge集成电路
MAX17049X+	-40°C 至 +85°C	8 WLP	双节电池ModelGauge集成电路
MAX17049X+T10	-40°C 至 +85°C	8 WLP	双节电池ModelGauge集成电路

+ 表示无铅*(Pb)*／符合*RoHS*标准的封装。
**EP* = 外露焊盘。
T = 卷带包装。

封装信息

有关最新封装轮廓信息及焊盘布局（封装图），请访问**www.maximintegrated.com/packages**。请注意，封装代码中的“+”、“#”或“-”仅表示RoHS合规状态。封装图可能显示不同的后缀字符，但该图适用于该封装，无论RoHS合规状态如何。

封装类型	封装代码	外形编号	焊盘图编号
8 WLP	W80B1+1	**21-0555**	参见 **应用说明1891**
8 TDFN-EP	T822+3	**21-0168**	**90-0065**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/12	Initial release	—
1	4/12	Corrected byte-order errors	10, 11, 13
2	8/12	Updated soldering temperature in *Absolute Maximum Ratings*; corrected Hibernate register names that were switched	2, 12, 14
3	10/12	Corrected V_{DD} pin names in *Absolute Maximum Ratings* and *Electrical Characteristics*	2, 3
4	8/13	Corrected version number	10
5	10/13	Corrected conditions for Supply Current in *Electrical Charateristics*	2
6	10/14	Updated VRESET recommendation from 40mV–80mV below 300mW empty voltage and corrected VR bit of Status register	13, 14
7	11/16	Updated front page title, description, applications, and features	1

版本历史

版本编号	版本日期	描述	更改页数
0	2/12	初始发布	—
1	4/12	已修正字节顺序错误	10, 11, 13
2	8/12	已更新绝对最大额定值中的焊接温度；已修正休眠寄存器名称的互换错误	2, 12, 14
3	10/12	已修正绝对最大额定值和电气特性中VDD引脚名称	2, 3
4	8/13	已修正版本号	10
5	10/13	已修正电气特性中供电电流的条件	2
6	10/14	已更新VRESET建议值，从空电压300mW以下的40mV至80mV，并修正状态寄存器中的VR位	13, 14
7	11/16	已更新首页标题、描述、应用及特性	1

