

Application Note for FT6336G/U CTPM

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Terminology

CTP - Capacitive touch panel

CTPM – Capacitive touch panel module



1. CTPM interface to Host

Figure 1-1 shows how CTPM communicates with host device. I²C interface supported by FT6336G/U that is two-wire serial bus consisting of data line SDA and SCL clock line, used for serial data transferring between host and slave device.

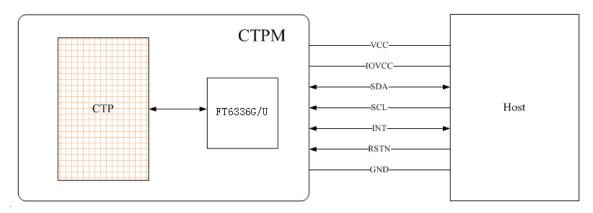


Figure 1-1 CTPM and Host connection

INT port and RSTN port form the control interface. The INT port controlled by FT6336G/U will send out an interrupt request signal to the host when there is a valid touch on CTP. The INT port also has another input function that host can wake up FT6336G/U from the Hibernate mode. Host can send the reset signal to CTPM via RSTN port to reset the FT6336G/U if needed. The Power Supply voltage of CTPM ranges from 2.8V to 3.6V, and the interface supply voltage named IOVCC ranges from 1.8V to 3.6V. For details, please refer to Table 1-1.

Port Name	Description
VCC	CTPM power supply, ranges from 2.8V to 3.6V.
	CTPM interface power supply for GPIO, ranges from 1.8V to 3.6V.
	If GPIO supply voltage is equal to VCC (2.8V~3.6V), IOVCC pin can be
IOVCC	connected to VCC.
	If GPIO supply voltage is 1.8V, IOVCC pin can be connected to VDDD pin or
	external 1.8V power supply.
SDA	I ² C data input and output.
SCL	I ² C clock input.
	The interrupt request signal from CTPM to Host.
INT	The wake up signal from host to CTPM, active low and the low pulse width
	ranges from 0.5ms to 1ms.
DCTN	The reset signal from host to CTPM, active low, and the low pulse width should
RSTN	be more than or equal to 1ms.
GND	Power ground.

Table 1-1 Description for CTPM and Host interface

1.1 I²C Read/Write Interface description

It is important to note that the SDA and SCL must connect with a pull-high resistor respectively before you read/write I²C data.



Write N bytes to I²C slave

		5	Sla	ve .	Ado	dr]	Dat	ta A	Add	lres	s[X	K]					I	Dat	a [X]						Ι	Dat	a [X	K+1	N-1]			
C	A	A	A	A	Α	A	A	R	_	R	R	R	R	R	R	R	R	٨	D	D	D	D	D	D	D	D	۸		D	D	D	D	D	D	D	D	A P	,
ြ	6	5	4	3	2	1	0	W	A	7	6	5	4	3	2	1	0	A	7	6	5	4	3	2	1	0	Α	•••	7	6	5	4	3	2	1	0	A	
S								M	A									A									A										A(1
A								\mathbb{Z}_{1}	×									×									\asymp										ᅜ)
\Box								귬																													•	•

Set Data Address

		Slave Addr]	Dat	ta A	Add	lres	ss[2	X]			
S	A	A	A	A	A	A	A	R	Α	R						R	R	Δ	р
5	6	5	4	3	2	1	0	W	А	7	6	5	4	3	2	1	0	А	1
ST								₹	$\stackrel{>}{\sim}$									$\stackrel{\sim}{\sim}$	ST
Ą								2	×									\asymp	Ö
$\ddot{\dashv}$								Ħ											·

Read X bytes from I²C Slave

		5	Slav	ve 2	Ado	lr						I	Dat	a []	N]						Ι	Dat	a [2	X+.	N-1]			
S	A 6	A 5	A 4	A 3	A 2	A 1	A 0	R W	A	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	A	•••	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	A	P
START			<u> </u>		_			READ	ACK									ACK					<u> </u>					ACK	STOP

1.2 Interrupt/Wake-up signal from CTPM to Host

As for standard CTPM, host needs to use both interrupt signal and I²C interface to get the touch data. CTPM will output an interrupt request signal to the host when there is a valid touch. Then host can get the touch data via I²C interface. If there is no valid touch detected, the INT will output high level, and the host does not need to read the touch data. There are two kinds of method to use interrupt: interrupt trigger and interrupt polling.

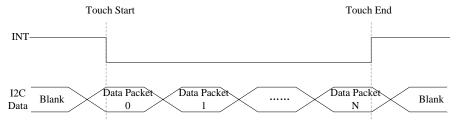


Figure 1-2 Interrupt polling mode

As for interrupt polling mode, INT will always be pulled to low level when there is a valid touch point, and be high level when a touch finished.

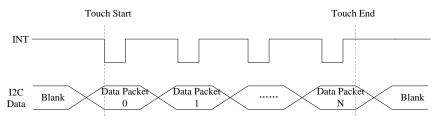


Figure 1-3 Interrupt trigger mode



While for interrupt trigger mode, INT signal will be set to low if there is a touch detected. But whenever an update of valid touch data, CTPM will produce a valid pulse on INT port for INT signal, and host can read the touch data periodically according to the frequency of this pulse. In this mode, the pulse frequency is the touch data updating rate.

When CTPM stays in hibernate mode, the INT port will act as a pull-high input port and wait for an external wake up signal. Host may send out a low pulse to wake up CTPM from the hibernate mode. The wake-up low pulse width ranges from 0.5 ms to 1 ms, the reason for this is that the INT port will act as an interrupt request signal output port after wake-up.

1.3 Reset signal from Host to CTPM

Host can send the reset signal via RSTN port to reset FT6336G/U. The reset signal should not be set to low while in normal running mode, but when programming flash, the RSTN port must be connected to GND. The RSTN port can also be used to active the CTPM in hibernate mode. Note that the reset pulse width should be more than 1ms.



2. Standard Application circuit of FT6336G/U

Table 2-1 is a brief summary of the FT6336G/U application features. Figure2-1, Figure2-2, demonstrates the typical FT6336G/U application schematic respectively. It consists of Capacitive Touch Panel (CTP), FT6336G/U chip, and some peripheral components. According to the size of CTPM, you can choose the number of channels needed.

Table 2-1 Brief features of FT6336GU

IC Type	FT6336G	FT6336U
Operating Voltage(V)	2.8 ~ 3.6	2.8 ~ 3.6
IOVCC(V)	1.8 ~ 3.6	1.8 ~ 3.6
Channel	31	39
Panel Size	≤4.5 inch	≤4.5 inch
Touch points	1 point and gestures or 2 points	1 point and gestures or 2 points
Interface	I^2C	I ² C
Report rate	>60Hz	>60Hz
Package (mm)	QFN-5x5-40L	QFN-5x5-48L

Note:

1. The scan channels Sn could be arranged in random order.



2.1 FT6336G typical application schematic for voltage of 2.8~3.6V

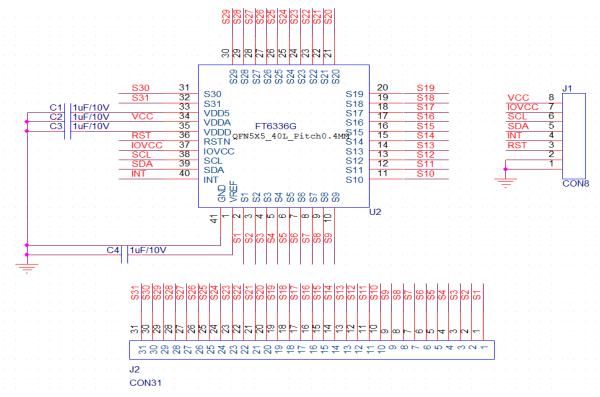


Figure 2-1 FT6336G typical application schematic for voltage of 2.8~3.6V

2.2 FT6336U typical application schematic for voltage of 2.8~3.6V

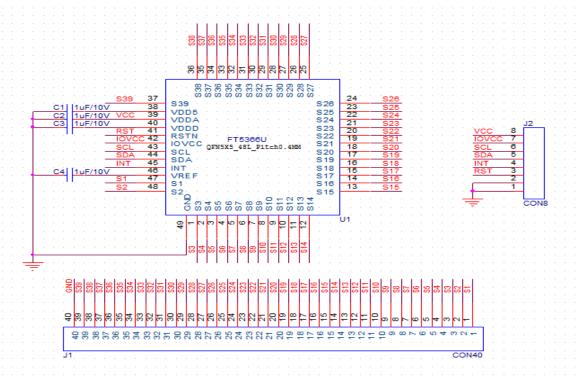


Figure 2-1 FT6336U typical application schematic for voltage of 2.8~3.6V



3. CTPM Register Mapping

This chapter describes the standard CTPM communication registers in address order for working mode. The most detailed descriptions of the standard products communication registers are in the register definitions section of each chapter.

3.1 Working Mode

The CTP is fully functional as a touch screen controller in working mode. The access address to read and write is just logical address which is not enforced by hardware or firmware. Here is the working mode register map.

Working Mode Register Map

working	Mode Register Map											
Address	Name	Defa ult Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Host Access	
0x00	Mode_Switch			Bit6:ModeSwitch								
•••												
0x02	TD_STATUS	0x00					points			ch	R	
0x03	P1_XH	0xFF	[7:6]1 Event					1 st Touc sition[1			R	
0x04	P1_XL	0xFF	[7:0]	1 st Touc	ch X Po	sition					R	
0x05	P1_YH	0xFF	[7:4]	1 st Touc	ch ID			1 st Touc sition[1			R	
0x06	P1_YL	0xFF	[7:0]	1 st Touc	h Y Po	sition					R	
0x07	P1_WEIGHT	0xFF	[7:0]	1 st Touc	ch Weig	ght					R	
0x08	P1_MISC	0xFF		1 st Touc	ch Area						R	
0x09	P2_XH	0xFF	[7:6]2 Event	Flag				2 nd Touc sition[1			R	
0x0A	P2_XL	0xFF	[7:0]	2 nd Tou	ch X P	osition					R	
0x0B	P2_YH	0xFF	[7:4]	2 nd Touc	ch ID			2 nd Tou sition[1			R	
0x0C	P2_YL	0xFF	[7:0]	2 nd Tou	ch Y Po	osition					R	
0x0D	P2_WEIGHT	0xFF		2 nd Tou							R	
0x0E	P2_MISC	0xFF	[7:4]	2 nd Tou	ch Area	ì					R	
0x80	ID_G_THGROUP	0xBB	[7:0]	Thresho	old for	touch d	etection	ı			R/W	
0x85	ID_G_THDIFF	0xA0	Filter	functio	n coeff	icient[7	7:01				R/W	
0x86	ID_G_CTRL	0x01	Filter function coefficient[7:0] [7:0] 0: Will keep the Active mode when there is no touching. 1: Switching from Active mode to Monitor mode automatically when there is no touching.							R/W		
0x87	ID_G_TIMEENT ERMONITOR	0x1E		The time			\mathcal{L}			node	R/W	
0x88	ID_G_PERIODA CTIVE	0x08	[7:0]	Report	rate in	Active	mode.				R/W	
0x89	ID_G_PERIODM ONITOR	0x08	[7:0]	Report	rate in	Monito	r mode	•			R/W	
•••												



0x8B	ID_G_FREQ_HO PPING_EN	0x00	[7:0]Charging detection function flag 0x00 : plug out 0x01 : plug in	R/W
0x96	ID_G_TEST_MO DE_FILTER	0x00	[7:0] Alpha Filter function enable/disable flag 0x00 : Disable 0x01 : Enable	R/W
0x9F	ID_G_CIPHER_M ID	0x26	[7:0] Chip Selecting Mid.	R
0xA0	ID_G_CIPHER_L OW	0x01	[7:0] Chip Selecting Low. 0x01:FT6336G 0x02:FT6336U	R
0xA1	ID_G_ LIB_VER_H	0x10	[7:0] High 8-bit of LIB Version info	R
0xA2	ID_G_ LIB_VER_L	0X01	[7:0] Low 8-bit of LIB Version info	R
0xA3	ID_G_CIPHER_H IGH	0x64	[7:0] Chip Selecting High	R
0xA4	ID_G_MODE	0x01	[7:0] 0x00: Interrupt Polling mode 0x01: Interrupt Trigger mode	R/W
0xA5	PWR_MODE	0x00	[7:0] Current power mode which system is in	R/W
0xA6	FIRMID	0X00	[7:0] Firmware Version	R
0xA8	FOCALTECH_ID	0x11	[7:0] FocalTech's Panel ID	R
0xA9	ID_G_VIRTUAL_ KEY_THRES	0x19	[7:0] The touch threshold of virtual key in the factory test mode. Touch threshold = value of register(0xA9) * 40	R/W
0xAD	ID_G_IS_CALLI NG	0x00	[7:0] Phone detection function flag 0x00 : Did not call 0x01 : In a call	R/W
0xAE	ID_G_FACTORY _MODE	0x00	[7:0] Current factory test mode 0x00 : F_NORMAL 0x01 : F_TESTMODE_1 0x02 : F_TESTMODE_2	R/W
0xAF	ID_G_RELEASE_ CODE_ID	0x01	[7:0] Release code version	R
0xB0	ID_G_FACE_DE C_MODE	0x00	Face detection function enable/disable flag 0x00 : Disable 0x01 : Enable	R/W
•••				
0xBC	ID_G_STATE	0x01	[7:0] Work Operating mode 0x00: Info Mode 0x01: Normal Mode 0x03: Factory Mode 0x04: Automatic Calibration Mode	W
0xD0	ID_G_SPEC_GES TURE_ENABLE	0x00	Special gesture function enable/disable flag 0x00 : Disable 0x01 : Enable	R/W

3.1.1 MODE_SWITCH

This is the device mode register, which is configured to determine the current mode of the chip.



Address	Bit Address	Register Name		Description
0x00	6.1	[2,0] Mode Switch	000b	WORKING Mode
UXUU	6:4	[2:0] Mode_Switch	100b	FACTORY Mode

3.1.2 TD_STATUS

This register is the Touch Data status register.

Address	Bit Address	Register Name	Description
0x02	3:0	Number of touch points [3:0]	The detected point number, 1-2 is valid.
0x02	7:4	Reserved	

3.1.3 Pn_XH (n:1-2)

This register describes MSB of the X coordinate of the nth touch point and the corresponding event flag.

Address	Bit Address	Register Name	Description				
0x03 ~ 0x09	7:6	Event Flag	00b: Press Down 01b: Lift Up 10b: Contact 11b: No event				
0.03	5:4		Reserved				
	3:0	Touch X Position [11:8]	MSB of Touch X Position in pixels				

3.1.4 Pn_XL (n:1-2)

This register describes LSB of the X coordinate of the nth touch point.

Address	Bit Address	Register Name	Description				
0x04							
~	7:0	Touch X Position [7:0]	LSB of the Touch X Position in pixels				
0x0A							

3.1.5 Pn_YH (n:1-2)

This register describes MSB of the Y coordinate of the nth touch point and corresponding touch ID.

			1 0				
Address	Bit Address	Register Name	Description				
0x05	7:4	Touch ID[3:0]	Touch ID of Touch Point, this value is 0x0F when the ID is invalid				
0x0B	3:0	Touch Y Position [11:8]	MSB of Touch Y Position in pixels				

3.1.6 Pn_YL (n:1-2)

This register describes LSB of the Y coordinate of the nth touch point.

Address	Bit Address	Register Name	Description				
0x06							
~	7:0	Touch Y Position [7:0]	LSB of the Touch Y Position in pixels				
0x0C			•				

3.1.7 **Pn_WEIGHT** (n:1-2)

This register describes weight of the nth touch point.

Ī	Address	Bit Address	Register Name	Description				
ſ	0x07							
	~	7:0	Touch Weight[7:0]	Touch pressure value				
	0x0D		G					

3.1.8 Pn_MISC (n:1-2)

This register describes the miscellaneous information of the nth touch point.

			1
Address	Bit Address	Register Name	Description
0x08			
~	7:4	Touch Area[3:0]	Touch area value
0x0E			



3.1.9 SPECIAL GESTURE ENABLE(1)/DISABLE(0) FLAG LIST.

Address	Name	Default	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Host
Address	Name	Value	7	6	5	4	3	2	1	0	Access
0xD1	Special	0x00	Gesture type support flag of special gesture function bit0: 1: Enable horizontal line drawing(from right to left) gesture bit0: 0: Disable horizontal line drawing(from right to left) gesture bit1: 1: Enable horizontal line drawing(from left to right) gesture bit1: 0: Disable horizontal line drawing(from left to right) gesture bit2: 1: Enable vertical line drawing(from down to up) gesture bit2: 0: Disable vertical line drawing(from down to up) gesture bit3: 1: Enable vertical line drawing(from up to down) gesture bit3: 0: Disable vertical line drawing(from up to down) gesture bit4: 1: Enable double tap gesture						t) gesture) gesture t) gesture gesture gesture gesture	R/W	
0xD2	gesture	0x00	d	a	g	able double C	е	m	w	0	R/W
0xD3		0x00	Gest	Gesture ID						R	
0xD4		0x00	Rese	Reserved							R/W
0xD5		0x00	u	s	p	1	q	b	Reserve d	n	R/W
0xD6		0x00	Rese	rved	Δ	v	٨	>	Reserve d	@	R/W
0xD7		0x00	Reserved		2	8	7	9	6	3	R/W
0xD8		0x00	Rese	rved			r	у	k	h	R/W
0xD9		0x00	Reserved					R/W			
0xDA		0x00	DEBUG USE						R/W		

4. Communication between host and CTPM

4.1 Communication Contents

The data Host received from the CTPM through I²C interface are different depend on the configuration in Device Mode Register of the CTPM. Please refer to Section 3---CTPM Register Mapping.

4.2 I²C Example Code

The code is only for reference, if you want to learn more, please contact our FAE staff.

*FT6336GU_i2c_Read-read data and write data by i2c

*@client: handle of i2c

*@writebuf: Data that will be written to the slave

*@writelen: How many bytes to write

*@readbuf: Where to store data read from slave

*@readlen: How many bytes to read

*Returns negative errno, else the number of messages executed

*/



```
int FT6336GU_i2c_Read(struct i2c_client *client, char *writebuf,
               int writelen, char *readbuf, int readlen)
    int ret;
    if (writelen > 0) {
          struct i2c_msg msgs[] = {
                .addr = client->addr,
                .flags = 0,
                .len = writelen,
                .buf = writebuf,
                },
                .addr = client->addr,
                .flags = I2C_M_RD,
                .len = readlen,
                .buf = readbuf,
                },
          };
          ret = i2c_transfer(client->adapter, msgs, 2);
          if (ret < 0)
               dev_err(&client->dev, "f%s: i2c read error.\n",
                    func );
     } else {
          struct i2c_msg msgs[] = {
                .addr = client->addr,
                .flags = I2C_M_RD,
                .len = readlen,
                .buf = readbuf,
                },
          };
          ret = i2c_transfer(client->adapter, msgs, 1);
               dev_err(&client->dev, "%s:i2c read error.\n", __func__);
     return ret;
/*write data by i2c*/
int FT6336GU_i2c_Write(struct i2c_client *client, char *writebuf, int writelen)
{
     int ret;
     struct i2c_msg msg[] = {
```



```
.addr = client->addr,
.flags = 0,
.len = writelen,
.buf = writebuf,
},
};
ret = i2c_transfer(client->adapter, msg, 1);
if (ret < 0)
    dev_err(&client->dev, "%s i2c write error.\n", __func__);
return ret;
}
```