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Dear Dr. Jose M. de la Rosa,
Editor-in-Chief, IEEE Transactions on Circuits and Systems II: Express Briefs

We are submitting our paper entitled "*A novel simple digital chaotic system in FPGA*" which we would like to be considered for publication in IEEE Transactions on Circuits and Systems II: Express Briefs.

Nonlinear dynamics and chaos, in particular, are evergreen subjects that address many aspects of our everyday life, from weather to cell division. Due to the frequent complexity of the resulting mathematical models, there is always the need for simple models that capture the essence of dynamical complexity, but still allow fast and efficient implementation.

Great efforts have been made to represent chaotic maps on digital circuits. However, less attention has been paid to its hardware optimization. This paper aims to implement a very simple digital chaotic system in FPGA. Using hardware description language VHDL, a polarized fixed-point number representation has been applied to depict the chaotic tent map. A hardware-efficient perturbation method is proposed to reduce chaos degradation. This approach has maintained the chaotic properties of the map; what is more, it has significantly reduced the number of logic elements compared to other articles found in the literature.

We believe that our paper opens up new frontiers in the parsimonious creation of digital chaotic models, and due to the underlying experimental and theoretical framework should thus fit perfectly to IEEE Transactions on Circuits and Systems II: Express Briefs.

Sincerely,

Dr. Erivelton Geraldo Nepomuceno, on behalf of all authors