Accelerating Protocol Synthesis and Detecting Unrealizability with Interpretation Reduction

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We synthesize TLA+ protocols

- TLA^+ (Temporal Logic of Actions) [Lamport]
    - Properties: linear, with theories
    - Model checker: TLC; Proof system: TLAPS
- Symbolic representation (not explicit state)
- Used in both academia and industry [Commun. ACM'15]
- Allows "parameterized" protocols (e.g. set of nodes)
- Prior work [FMCAD'24] only other paper on TLA^+ synthesis

Sketching
[Solar-Lezama]

Example property: not shown

Example sketch

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$$\begin{aligned} &\text{Receive}(\text{src}, \text{dst}) := \\ &\quad \land\ ???_4 \\ &\quad \land\ \text{message}' = ???_5 \\ &\quad \land\ \text{has\_lock}' = ???_6 \end{aligned}$$

Example completion

$$\begin{aligned} &\text{Send}(\text{src}, \text{dst}) := \\ &\quad \land\ \text{has\_lock}[\text{src}] \\ &\quad \land\ \text{message}' = \text{message} \cup \{(\text{src}, \text{dst})\} \\ &\quad \land\ \text{has\_lock}' = \text{has\_lock}[\text{src} \leftarrow \text{false}] \end{aligned}$$

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Sketching, SyGuS
[Solar-Lezama], [Alur et. al.]

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- Halt when no solution: *unrealizability*
- New search space reduction technique: *Interpretation Reduction*
- Improved counterexample generalization for pruning

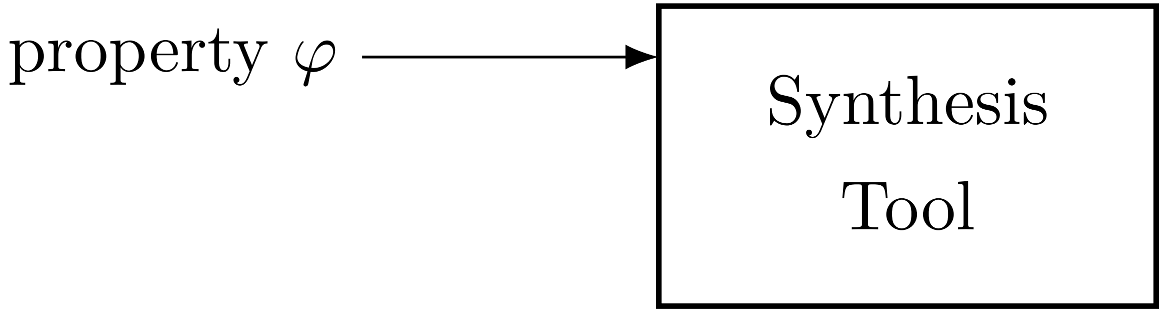
Problem Statement

Problem

Problem

Synthesis
Tool

Problem



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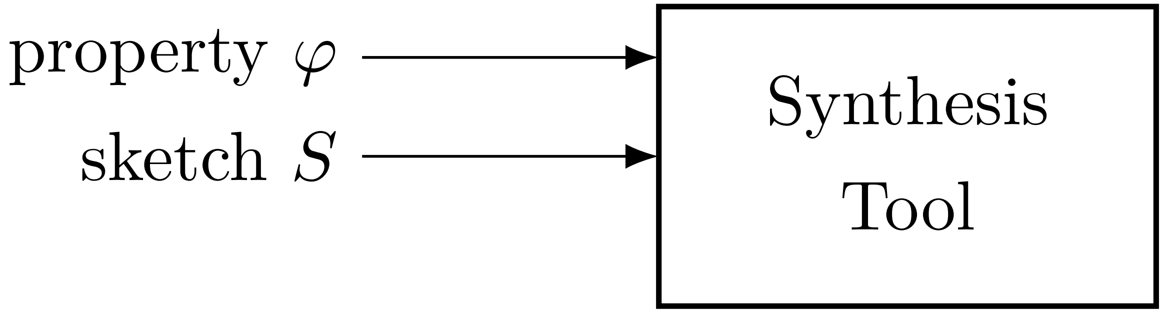

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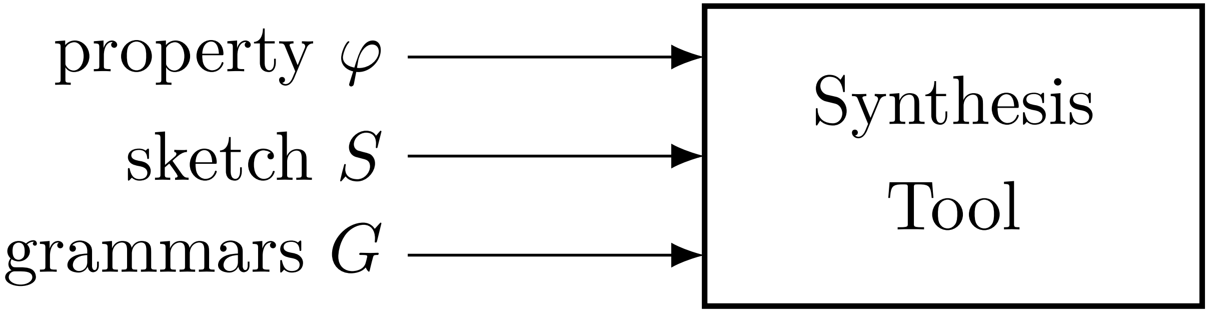

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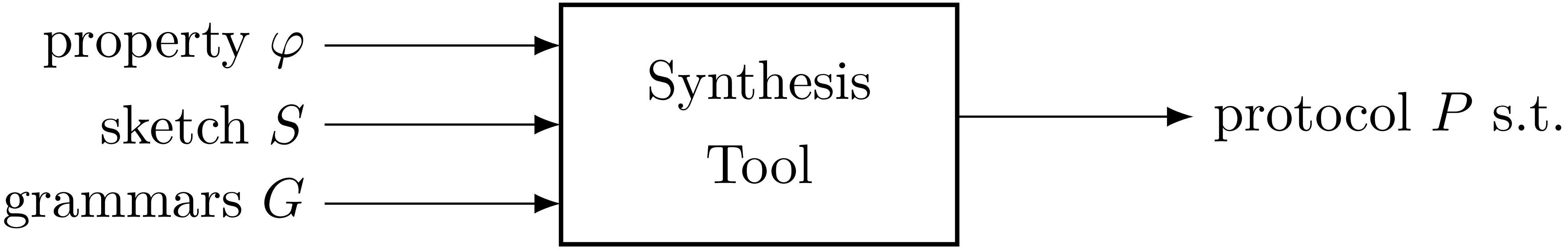

property φ
sketch S
grammars G
Synthesis Tool
protocol P s.t.

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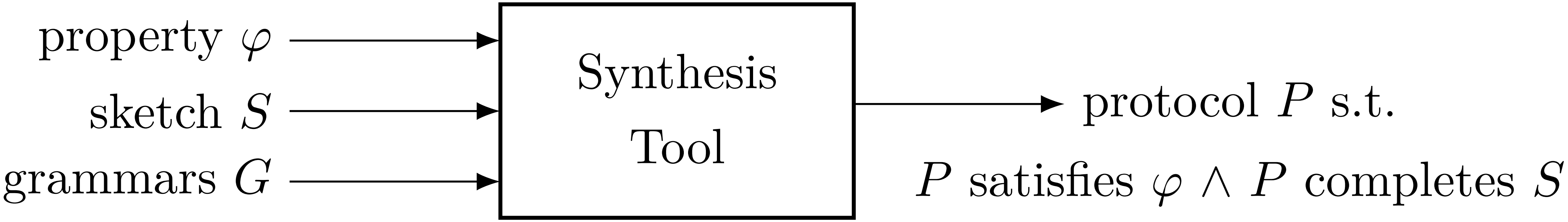
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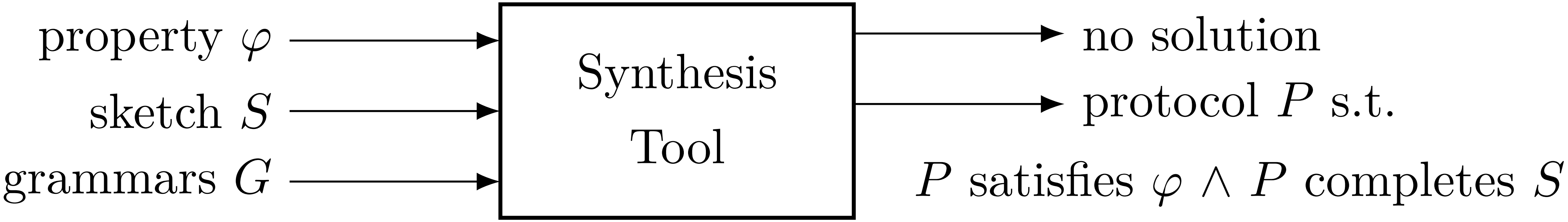
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Solution

CEGIS

Counterexample-Guided Inductive Synthesis [Solar-Lezama]

CEGIS

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Learner

CEGIS

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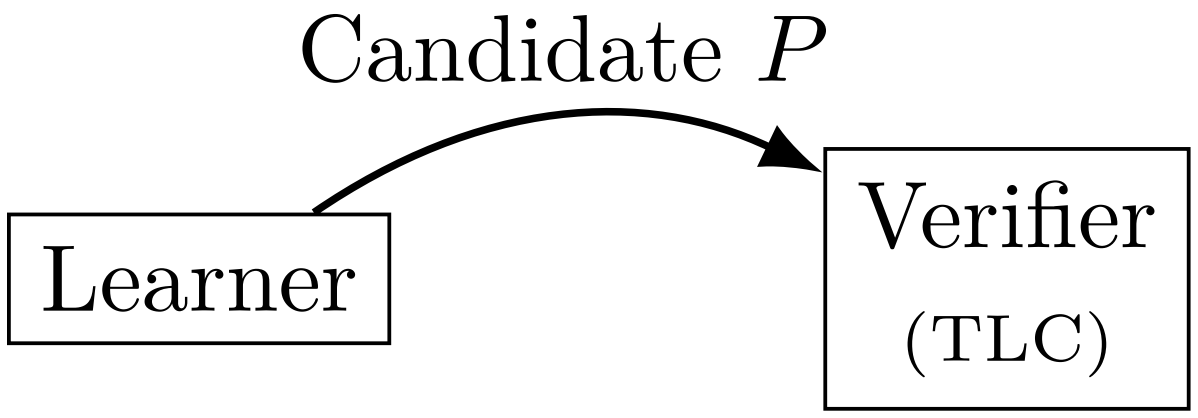
Learner

Verifier
(TLC)

CEGIS

Counterexample-Guided Inductive Synthesis [Solar-Lezama]



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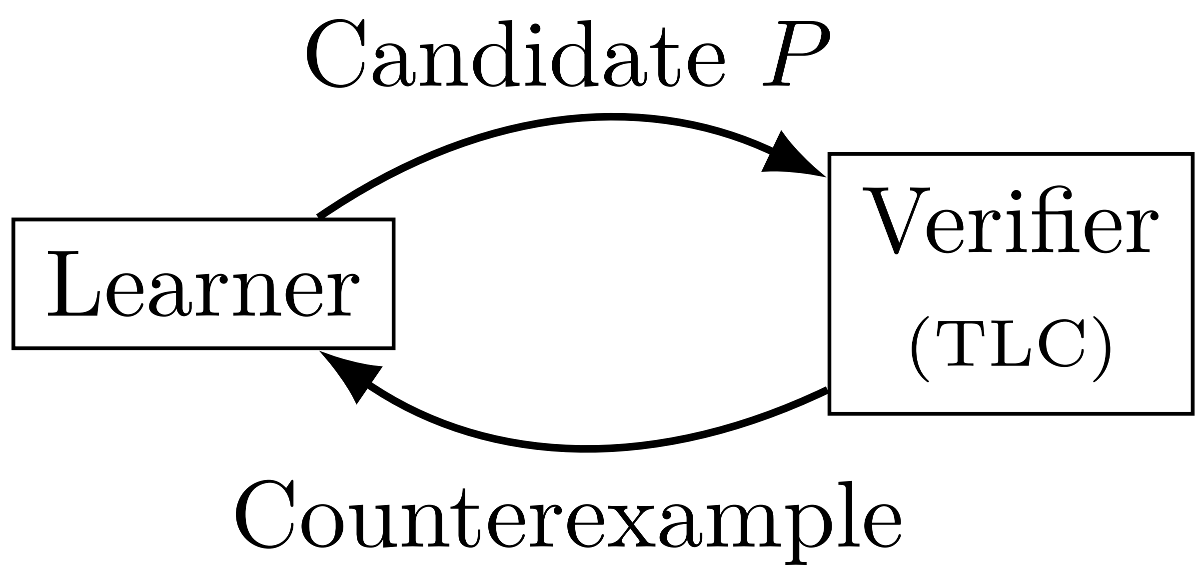

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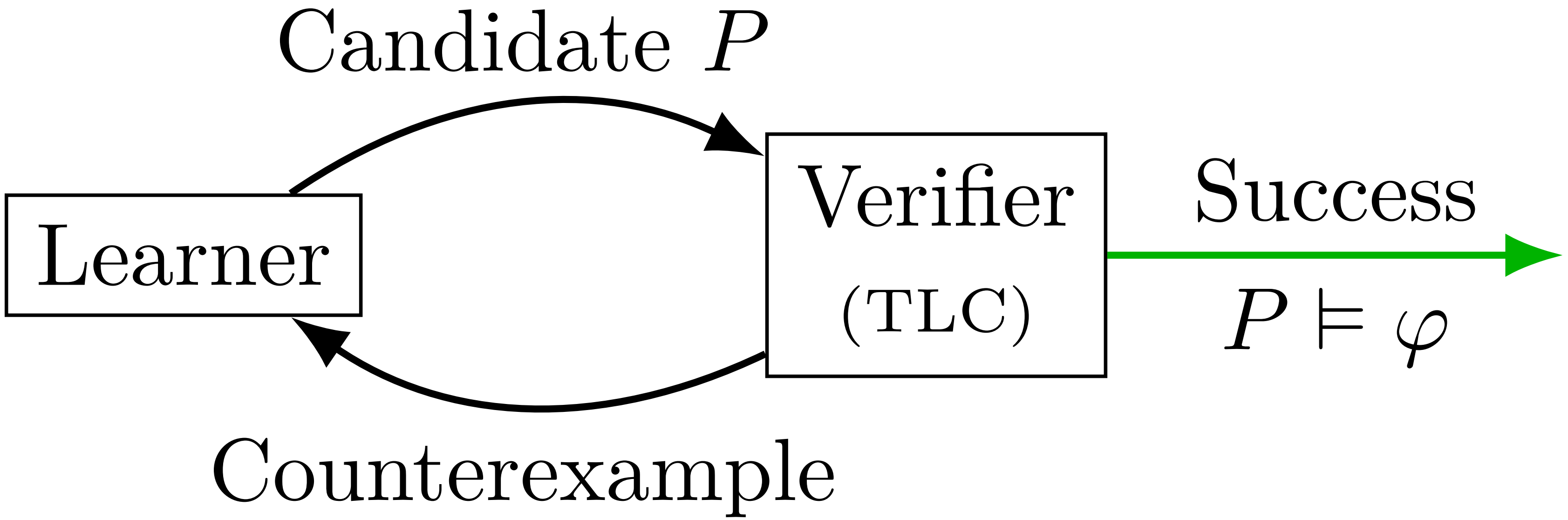

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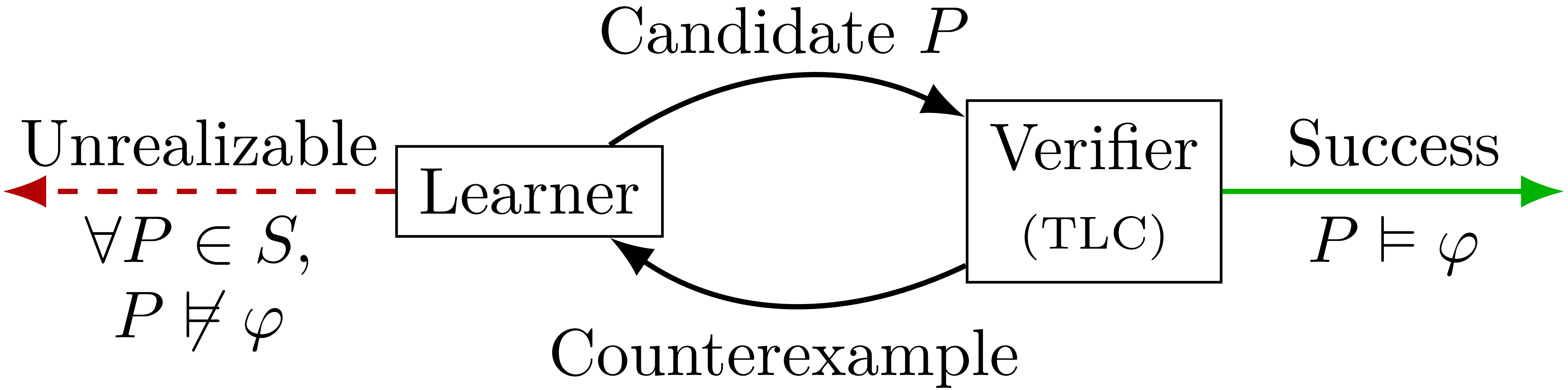

Improving the Learner

- Naive Learner: ignore cex, enumerate all protocols
    - *many protocols; model checking expensive*
- Idea 1; **discard protocols before model checking**
    - Pruning constraints: generalize counterexamples
- Idea 2; **avoids enumerating protocols in the first place**
    - Equivalence reduction: do not use equiv. subexpressions
- Idea 2++; Interpretation reduction: **use weak eq. relation**

Generalizing Counterexamples

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Idea: treat cex as a path. Disable an action or point it somewhere else.

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Generalizing Counterexamples (Cont.)

- In general: many completions violate π_{cex}
- (Ideally) **Theorem**: cex belongs to P iff $P \not\models \pi_{\text{cex}}$
- (Reality) π_{cex} underprunes when cex is stuttering violation
- π_{cex} exact for safety, deadlock, and liveness cex
- Prior work [FMCAD'24] only exact for safety
- Checking $P \models \pi_{\text{cex}}$ cheaper than model checking.

Interpretation Reduction

Standard Equivalence Reduction

Example grammar

$???_1 \to Y$

$Y \to u \mid X + Y$

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Do not enumerate, e.g.,

$0 + (0 + u)$.

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[FMCAD'24] uses standard equivalence reduction

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Note: $y \not\models \Pi$, since y evaluates to 1.

Also note: $x + y \not\models \Pi$, since $0 + 1 = 1$.

Finally, note $y \equiv_{\mathcal{A}} x + y$.

Interpretation Reduction

- Let $\mathcal{A} = \{\ [x \mapsto 0, y \mapsto 1]\ \}$ have all relevant interpretations
- Suppose we've enumerated the subexpressions x and y
- Should we enumerate subexpression $x + y$?
- No, $y \equiv_{\mathcal{A}} x + y$
- **Theorem.** one representative per eq. class mod $\mathcal{A}$ is sufficient to maintain completeness of the synthesis algorithm
- **Lemma.** $e_1 \equiv_{\mathcal{A}} e_2 \implies (e_1 \models \Pi \Leftrightarrow e_2 \models \Pi)$

Summary: Improving the Learner

- Idea 1; **discard protocols before model checking**
  - Pruning constraints: generalize counterexamples
- Idea 2; **avoids enumerating protocols in the first place**
  - Equivalence reduction: do not use equiv. subexpressions
- Idea 2++; Interpretation reduction: **use weak eq. relation**
- More details in paper!

Unrealizability

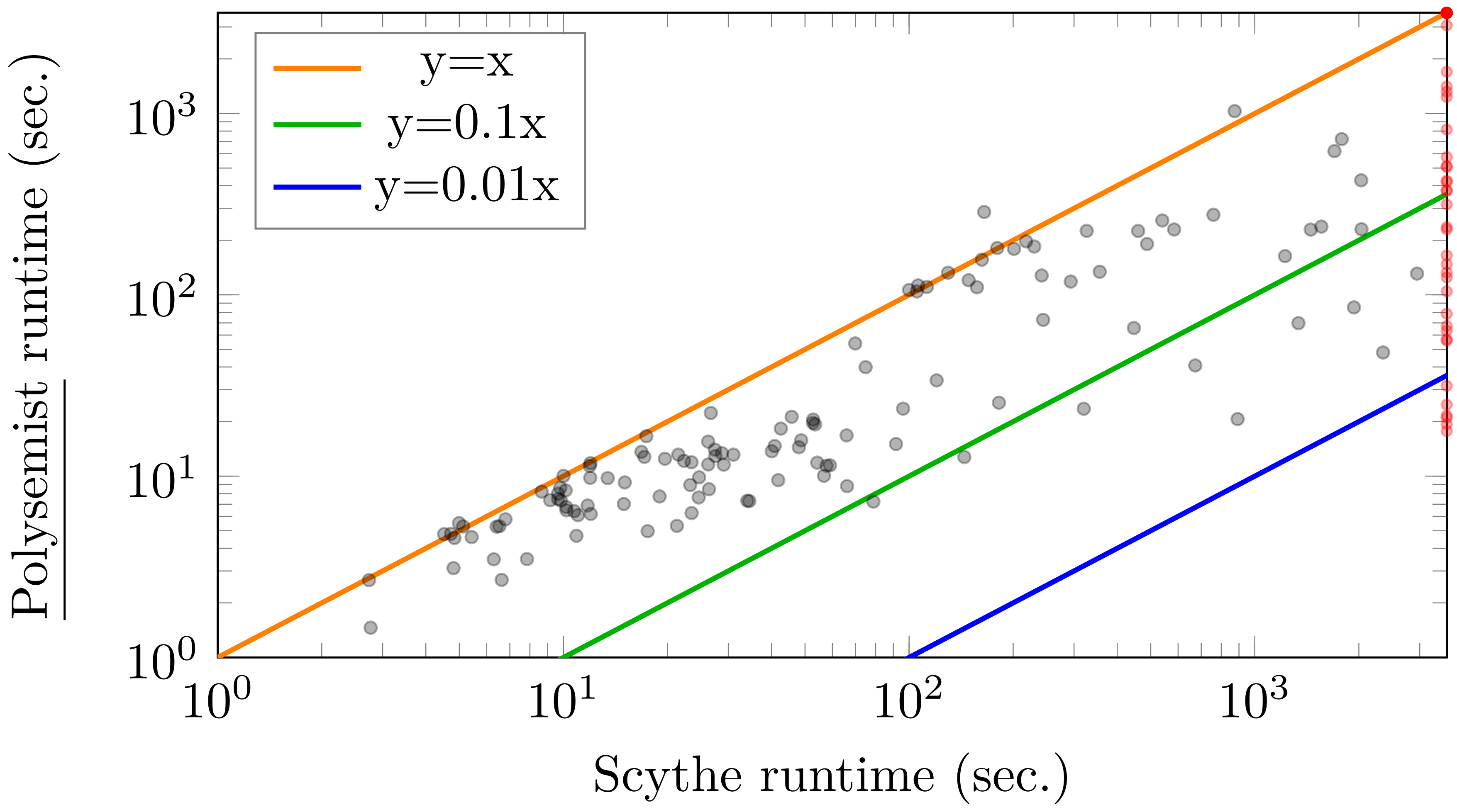
- Detected when pool of enumerated expression reaches fixed point
- Requires sufficiently weak equivalence relation
- weaker = faster fixed point

Experimental Evaluation

Setup

- Our tool: Polysemist
- Compare with state of art tool: Scythe (FMCAD 2024)
- Benchmarks based on those of Scythe
- 7 case studies, including: reconfig-raft, 2PC, SKV, locks
- Realizable ($n = 171$) and Unrealizable ($n = 123$) experiments
- Easiest: all pre- or post-conditions in 1 action
- Hardest: all pre- and post-conditions in 2 actions

Scythe vs Polysemist Runtime (Realizable Experiments)



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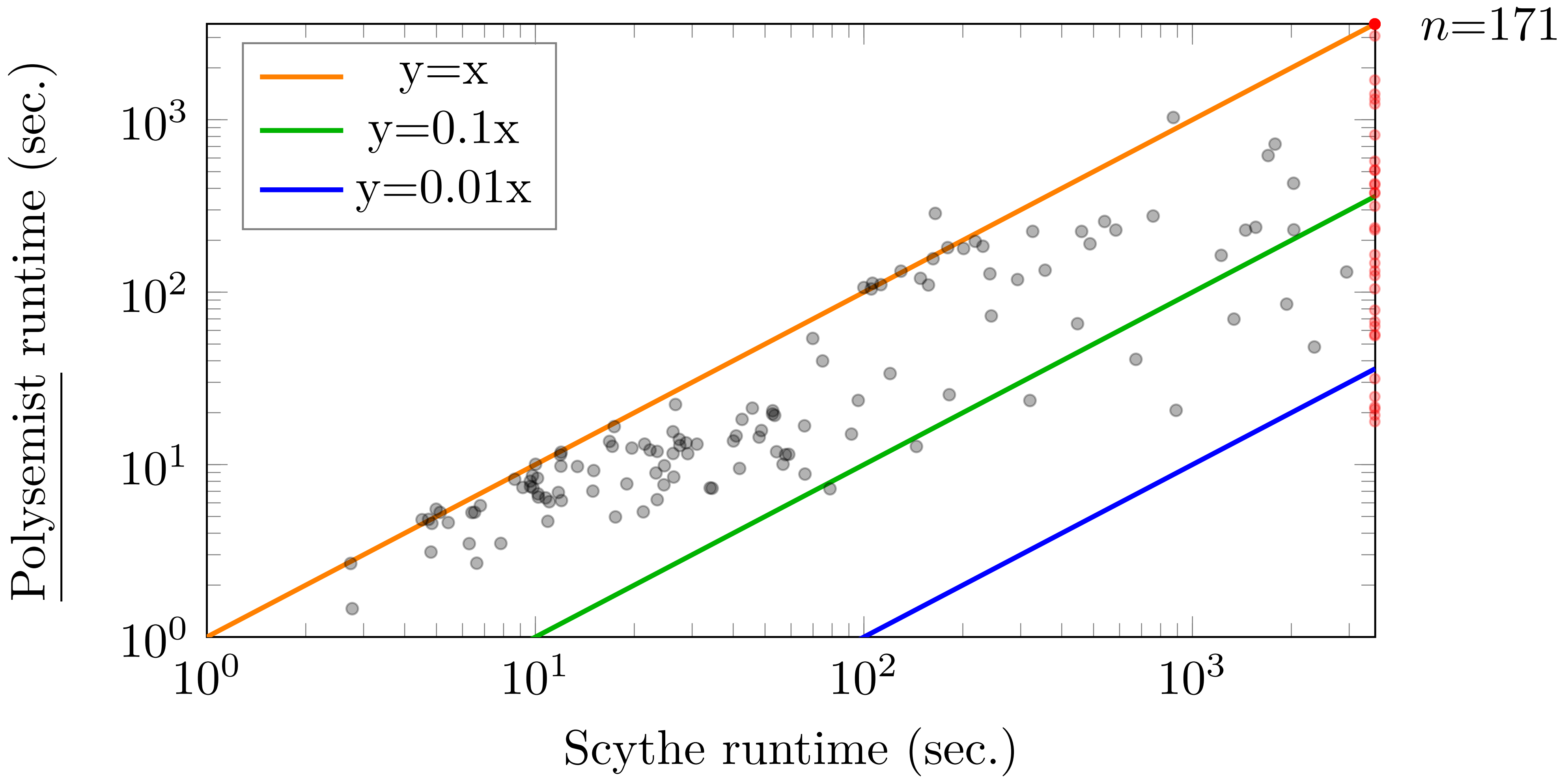

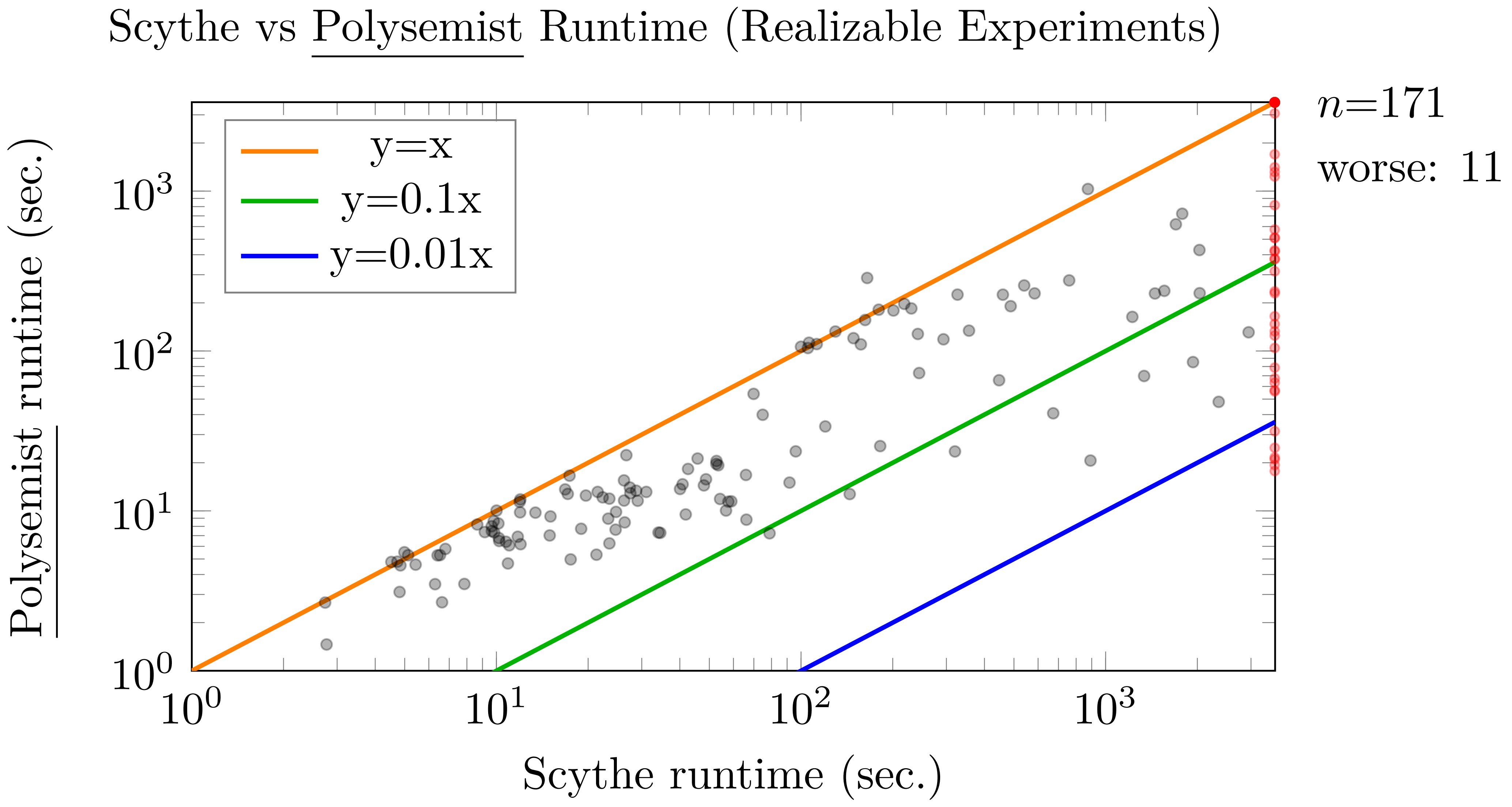

Scythe vs Polysemist Runtime (Realizable Experiments)
y=x
y=0.1x
y=0.01x
n=171
worse: 11
Polysemist runtime (sec.)
Scythe runtime (sec.)
10^0
10^1
10^2
10^3

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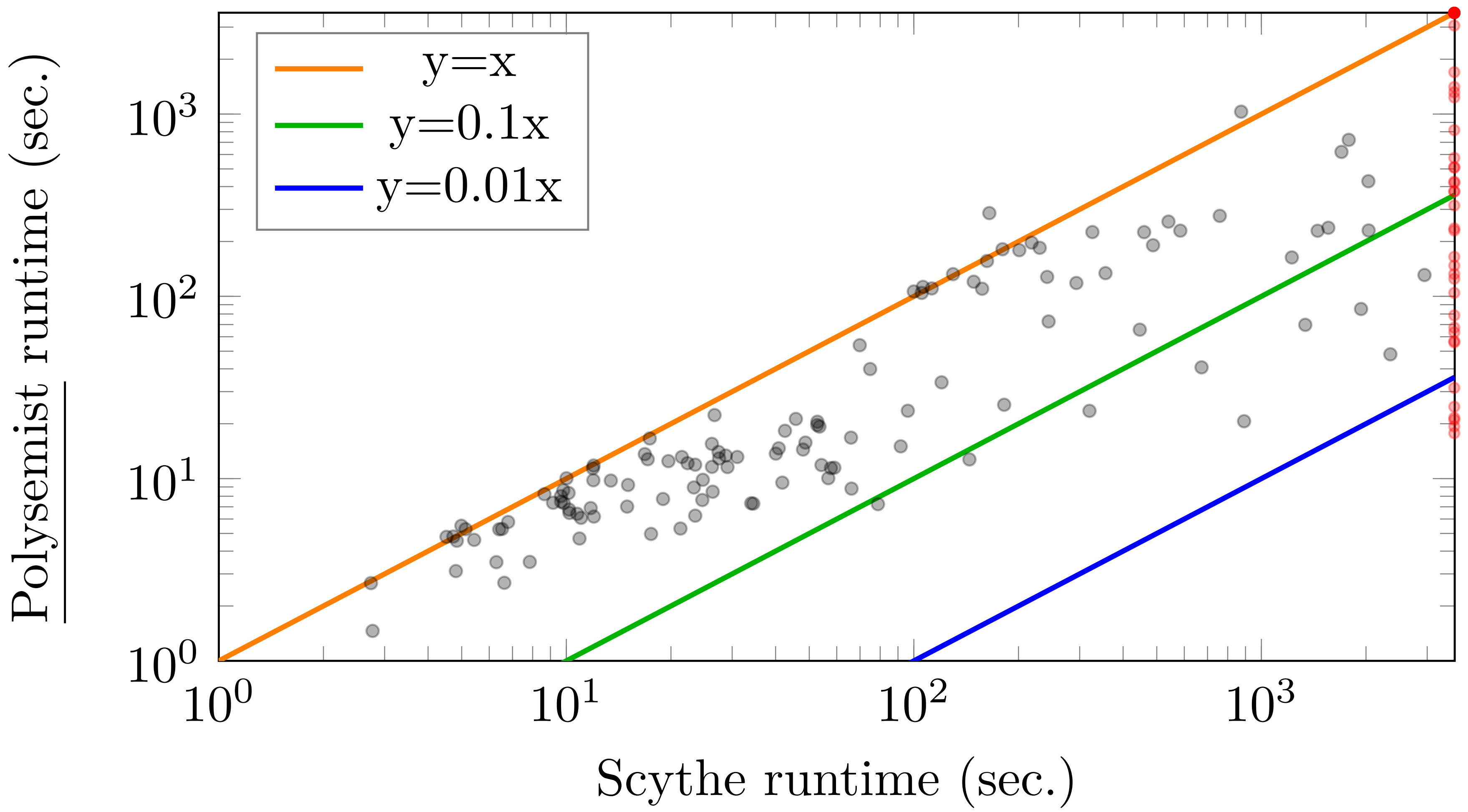
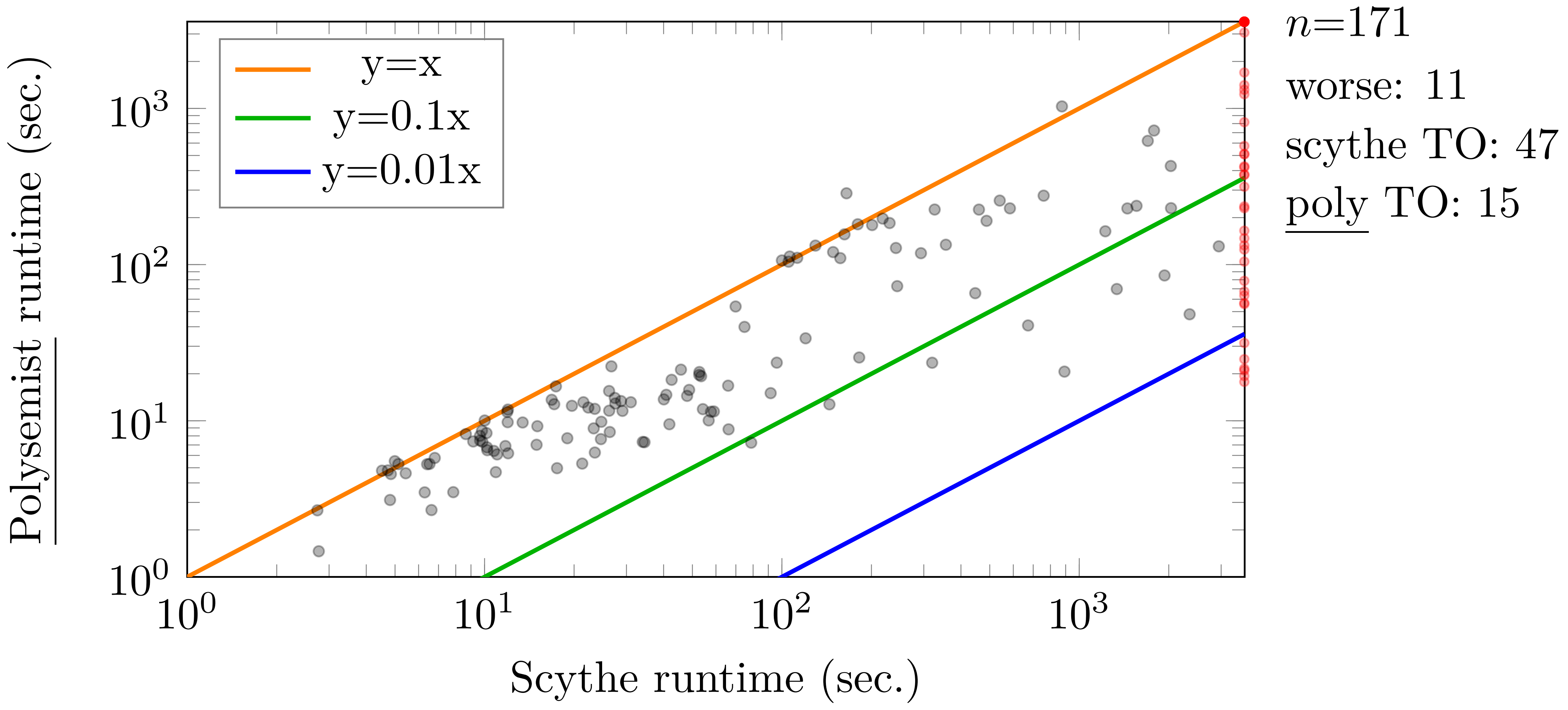


n=171
worse: 11
scythe TO: 47

Scythe vs Polysemist Runtime (Realizable Experiments)



Unrealizable Experiments

- $n = 123$
- **Scythe** : TO=107 / HALT=16
- **Polysemist** : TO=43 / HALT=80
    - Usually halted in <60 seconds
    - Did not TO unless Scythe did

Conclusion

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- Counterexample generalization avoids redundant model checking

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- CEGIS for TLA$^+$ protocols
- Counterexample generalization avoids redundant model checking
- Interpretation reduction avoids redundant enumeration

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- Interpretation reduction avoids redundant enumeration
- 100x improvements over state of art

Summary

- CEGIS for TLA$^+$ protocols
- Counterexample generalization avoids redundant model checking
- Interpretation reduction avoids redundant enumeration
- 100x improvements over state of art
- Recognize 5x more unrealizable instances than state of art

Thank you!

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Paper, Tool, Slides, Poster