IP2366 Register Description Document

Version/Revision History

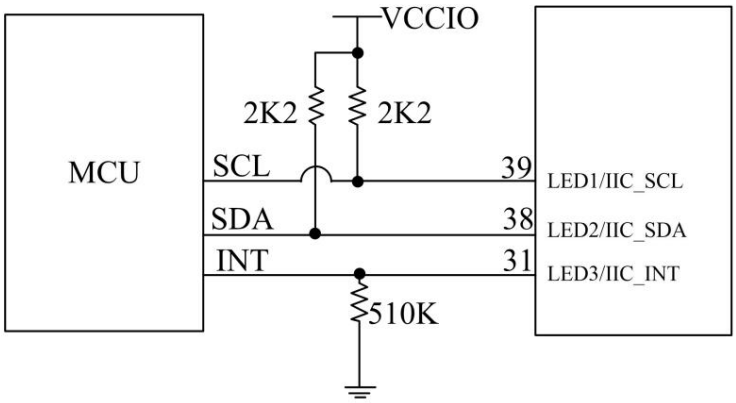
	Date Revision Content Initial release		Preparer/Reviser
Version	2023-4-18	2023-3-24	IT555
V1.00 V1.10	Modify standby EN wake-up;	Added option to charge PDO Gear	IT555
V1.11	2023-4-24 Delete I2C power reading function	Description (Read is not supported Battery Level)	IT555
V1.12	2023-6-13 Added standby charging	Power Wake-up Instructions	IT555
V1.13	2023-6-26 Low voltage gear	Low support to 2.5V	IT555

1 Typical Application Description

1.1 I2C connection method

IP2366 can be used as a slave device. MCU can read or set the voltage, current, power and other information of IP2366 through I2C interface.

The I2C connection method is as follows:



1.2 I2C Notes

ÿ I2C device address of IP2366: written as 0xEA, read as 0xEB. If you need to set it to another address, you can customize it;

ÿ The I2C communication voltage of IP2366 is 3.3V. If the voltage on the MCU side is 5V, a level conversion chip needs to be added to convert it to 3.3V;

ÿ IP2366 INT Application Description: IP2366 can be awakened by charging and EN when in sleep mode. After awakening, IP2366 actively pulls INT high for 100ms

After that, the MCU can perform I2C communication and read and write registers; before entering sleep mode, IP2366 will switch to high impedance input.

Detect the INT status. If it is high level, it is considered that the MCU does not allow IP2366 to enter sleep mode. If it is low level, IP2366 enters sleep mode.

Sleep: After the MCU detects that INT is low, it should stop accessing the IC within 16ms;

ÿ The I2C of IP2366 supports a maximum communication frequency of 250k. Considering the clock deviation, it is recommended that the I2C communication clock of MCU use 100k-200k;

ÿIf you want to modify the value of a register of IP2366, you need to read the value of the corresponding register first, and then compare the bit to be modified.

After the OR operation, the calculated value is written into the register. Other unopened registers cannot be modified at will.

The read value is the standard, and the default value of different ICs may be different;

ÿ IP2366 I2C communication is real-time data. After receiving the request, an interrupt is required to prepare the data. The preparation time is long, so the MCU

In I2C communication, it is necessary to determine whether ACK is received after sending the address and add a 50us delay (refer to the I2C application example); it is recommended to

Byte read, 100k I2C communication frequency, add 1ms delay between each byte;

ÿ At the end of I2C data reading, after reading the last byte, a NACK signal must be given, otherwise IP2366 will think that it is still continuing.

Continue to read data, the next clock will continue to output the next data, resulting in failure to receive the STOP signal, and finally a reading error;

ÿ Reserved registers cannot be written to or changed at will, otherwise unexpected results may occur.

The operation must be performed in accordance with the read-modify-write method. Only the bits to be used are modified, and the values of other unused bits cannot be modified.

ÿThis document is only for IP2366_I2C model, other models are invalid;

1.3 I2C Application Examples

After the IP2366 INT pin is continuously high for 100ms, the MCU can perform I2C communication and initialize the registers first (the special

The register is modified only when a special function is used. If no modification is needed, the register can be omitted); then read the internal information of IP2366 (charge and discharge status);

Finally, special operations are performed (such as special indicator lights, charge and discharge management, and fast charge request management). After the MCU detects that INT is low, 16ms

You need to stop accessing I2C.

For example:

Write data 0x5A to register 0x05

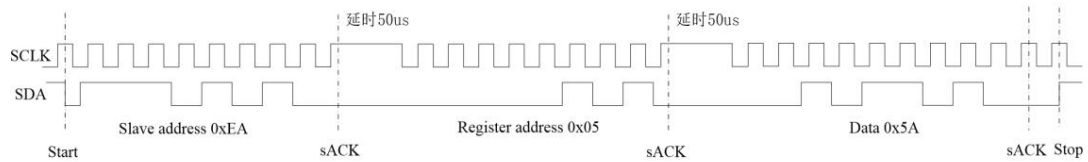


Figure 1 I2C Write 0x05

Read back data from register 0x05

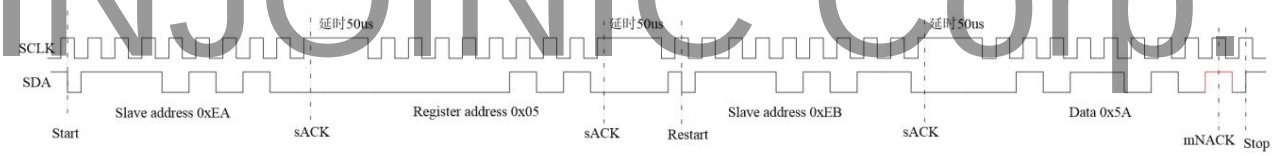


Figure 2 I2C Read 0x05

Actually read back data from register 0x31

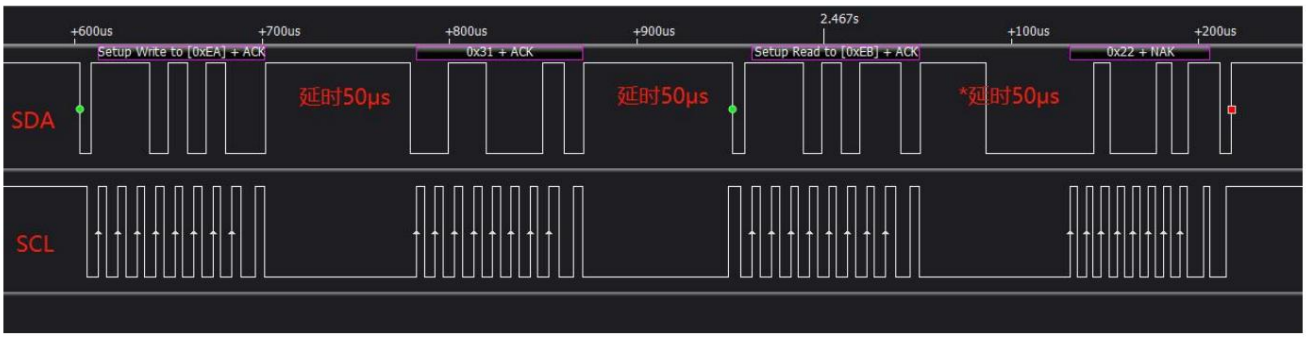


Figure 3 I2C Read 0x31

2 Register list:

2.1 Read/Write Operation Register

(0x00) SYS_CTL0 (charge enable register)

I2C address 0XEA Register address = 0x00

Bit(s)	Name	Description	R/W	RESET
7	En_LOADOTP Power on wake up and reset register value enable	0: Do not reset register values 1: Reset register value It is not recommended to change this bit to 0. If it needs to be changed, the software needs to be regularly Reset register default value, such as VINOk VBUOk signal triggered	R/W	1
6	En_RESETMCU	MCU reset register Write 1: reset the register to the default value. After reset, the bit will automatically return to the default value. After reset, wait 2 seconds before reading or writing registers.	R/W	0
5	En_INT_low When there is an abnormality, INT is pulled down for 2MS to prompt the MCU that an abnormality has occurred	1ÿEnable 0ÿdisable	R/W	0
4	En_Vbus_SinkDPd M	C port input DM DP fast charge enable 1ÿEnable 0ÿdisable	R/W	1
3	En _Vbus_SinkPd Port C input Pd fast charge enable	1ÿEnable 0ÿdisable	R/W	1
2	En_Vbus_SinkSCP C port input SCP fast charge enable	1ÿEnable 0ÿdisable	R/W	1
1	reserved		R/W	0
0	A_Charger	Charger charging enable (no charging after shutting down) 1ÿEnable 0ÿdisable	R/W	1

(0x02) SYS_CTL2 (Vset full voltage setting)

I2C address 0XEA Register address = 0x02

Bit(s)	Name	Description	R/W	RESET
7:0	Vset	Single battery full voltage Vset=N*10mV+2500mV (maximum 4.4V)	RW	

(0x03) SYS_CTL3 (Iset charging power or current setting)

I2C address 0XEA Register address = 0x03

Bit(s)	Name	Description	R/W	RESET
7:0	Iset Iset=N*100mA (maximum 9.7A)	Maximum battery current limit (cannot be configured to be less than the stop-charge current)	R/W	01100001

(0x06) SYS_CTL6 (Trickle charge current setting)

I2C address 0XEA Register address = 0x06

Bit(s)	Name	Description	R/W	RESET
7:0	Itk	Trickle charge current setting Itk=N*50mA	R/W	00000100

(0x08) SYS_CTL8 (charging stop current and recharging threshold setting)

I2C address 0XEA Register address = 0x08

Bit(s)	Name	DescriptionStop	R/W	RESET
7:4	Stop	charging and charging current setting Stop=N*50mA	R/W	0010
3:2	Top	Recharge Threshold 00: No recharging function after full charge 01ÿVTRGT – N*0.05 10ÿVTRGT – N*0.1 11ÿVTRGT – N*0.2 VTRGT ----Full charge voltage N----Number of batteries in series	R/W	10
1:0	Reserved			

(0x09) SYS_CTL9 (standby enable and low power voltage setting)

I2C address 0XEA Register address = 0x09

Bit(s)	Name	Description	R/W	RESET
7	En_Standby Standby Enable	1: Enable 0: Disable	R/W	1
6	Standby	Write 1 to enter standby mode, valid once (bit7 must be enabled to write 1) 1: Enter standby mode immediately when not charging. 0: Normal process	R/W	0

5	En_BAT_Low	5V low power shutdown enable 0ÿdisable 1: Enable (After enabling, the shutdown voltage is fixed at 5V, with only software protection. And the voltage will also change when the trickle current is converted to constant current)	R/W	0
4:0	Reserved			

(0x0A) SYS_CTL10 (low battery voltage setting)

I2C address 0XEA Register address = 0x0A

Bit(s)	Name	DescriptionBattery	R/W	RESET
7:5,	Set_BATlow	low voltage setting (Trickle current to constant current voltage will change accordingly 2.7V and below only have software low power protection) 000: 2.50V*N 001: 2.60V*N 010: 2.70V*N 011: 2.80V*N 100: 2.90V*N 101: 3.00V*N 110: 3.10V*N 111: 3.20V*N N: Number of batteries in series	R/W	010
4:0	Reserved			

(0x0B) SYS_CTL11 (output enable register)

I2C address 0XEA Register address = 0x0B

Bit(s)	Name	Description	R/W	RESET
7	En_Dc-Dc_Output discharge	output enable (no output after closing) 1: Enable 0: Disable	R/W	1
6	En_Vbus_Src_DP dM	C port output DP/DM fast charge enable 1ÿEnable 0ÿdisable	R/W	1
5	En _Vbus_SrcPd	Port C output Pd fast charge enable 1ÿEnable 0ÿdisable	R/W	1
4	En _Vbus_SrcSCP	Port C output SCP fast charge enable 1ÿEnable 0ÿdisable	R/W	1
3:0	Reserved			

(0x0C) SYS_CTL12 (output maximum power selection register)

I2C address 0XEA Register address = 0x0C

Bit(s)	Name	Description	R/W	RESET

	7:5 Vbus_Src_Power Vbus1 output/input power selection: 000ÿ30W 001ÿ45W 010ÿ60W 011ÿ65W 100ÿ100W 101ÿ140W		R/W	101
4:0	Reserved			

(0x0D) SELECT_PDO (select charging PDO gear)

You need to read the corresponding gear of 0x35 before you can select it. The maximum PD gear of the adapter is selected by default.

The configuration becomes invalid after this, and the adapter position needs to be re-identified and reconfigured.

I2C address 0XEA Register address = 0X0D

Bit(s)	Name	Description	R/W	Reset
7:3	Reserved			
2:0	Pdo_select selects the charging PDO gear 000: Default is the maximum gear of the adapter 001ÿ5V 010ÿ9V 011ÿ12V 100ÿ15V 101ÿ20V		R	

(0x22) TypeC_CTL8 (TYPE-C mode control register)

I2C address 0XEA Register address = 0x22

Bit(s)	Name	Description	R/W	RESET
7:6	Vbus_Mode_Set Vbus CC mode selection 00: UFP 01ÿDFP 11ÿDRP		R/W	11
5:0	Reserved			

(0x23) TypeC_CTL9 (output Pdo current setting register)

I2C address 0XEA Register address = 0x23

Bit(s)	Name	Description	R/W	RESET

7	En_5VPdo_3A/2.4A 5VPdo current setting	1ÿ3A 0ÿ2.4A	R/W	1
6	En_Pps2Pdo_Iset	Pps2 Pdo current setting enable 1ÿEnable 0: disable *After enabling, the output power and overcurrent are based on the set Pdo current. The current is 1.1 times the set Pdo current	R/W	0
5	En_Pps1Pdo_Iset	Pps1 Pdo current setting enable 1ÿEnable 0: disable *After enabling, the output power and overcurrent are based on the set Pdo current. The current is 1.1 times the set Pdo current	R/W	0
4	En_20VPdo_Iset	20VPdo current setting enable 1ÿEnable 0: disable *After enabling, the output power and overcurrent are based on the set Pdo current. The current is 1.1 times the set Pdo current	R/W	0
3	En_15VPdo_Iset	15VPdo current setting enable 1ÿEnable 0: disable *After enabling, the output power and overcurrent are based on the set Pdo current. The current is 1.1 times the set Pdo current	R/W	0
2	En_12VPdo_Iset	12VPdo current setting enable 1ÿEnable 0: disable *After enabling, the output power and overcurrent are based on the set Pdo current. The current is 1.1 times the set Pdo current	R/W	0
1	En_9VPdo_Iset	9VPdo current setting enable 1ÿEnable 0: disable *After enabling, the output power and overcurrent are based on the set Pdo current. The current is 1.1 times the set Pdo current.	R/W	0
0	En_5VPdo_Iset	5VPdo current setting enable 1ÿEnable 0ÿdisable	R/W	0

(0x24) TypeC_CTL10 (5VPdo current setting register)

I2C address 0XEA Register address = 0x24

Bit(s)	Name	Description	R/W	RESET
7:0	5VPdo_Iset	5VPdo Current Setting 5VPdo=20mA*N	R/W	0x96

(0x25) TypeC_CTL11 (9VPdo current setting register)

I2C address 0XEA Register address = 0x25

Bit(s)	Name	Description	R/W	RESET
7:0	9VPdo_Iset	9VPdo Current Setting 9VPdo=20mA*N	R/W	0x96

(0x26) TypeC_CTL12 (12VPdo current setting register)

I2C address 0XEA Register address = 0x26

Bit(s)	Name	Description	R/W	RESET
7:0	12VPdo_Iset	12VPdo Current Setting 12VPdo=20mA*N	R/W	0x96

(0x27) TypeC_CTL13 (15VPdo current setting register)

I2C address 0XEA Register address = 0x27

Bit(s)	Name	Description	R/W	RESET
7:0	15VPdo_Iset	15VPdo current setting 15VPdo=20mA*N	R/W	0x96

(0x28) TypeC_CTL14 (20VPdo current setting register)

I2C address 0XEA Register address = 0x28

Bit(s)	Name	Description	R/W	RESET
7:0	20VPdo_Iset	20VPdo current setting 20VPdo=20mA*N	R/W	0xFA

(0x29) TypeC_CTL23 (Pps1 Pdo current setting register)

I2C address 0XEA Register address = 0x29

Bit(s)	Name	Description	R/W	RESET
7:0	Pps1Pdo_Iset	Pps1 Pdo current setting Pps1 Pdo=50mA*N	R/W	0x3C

(0x2A) TypeC_CTL24 (**Pps2 Pdo** current setting register)

I2C address 0XEA Register address = 0x2A

Bit(s)	Name	Description	R/W	RESET
7:0	Pps2Pdo_Iset	Pps2 Pdo current setting Pps2 Pdo=50mA*N	R/W	0x3C

(0x2B) TypeC_CTL17 (**output PDO** setting register)

I2C address 0XEA Register address = 0x2B

Bit(s)	Name	Description	R/W	RESET
7	Reserved		R/W	R
6	En_Src_Pps2Pdo	Pps2 Pdo Enable 1ÿEnable 0ÿdisable * No Pps2 Pdo after disable	R/W	1
5	En_Src_Pps1Pdo	Pps1 Pdo Enable 1ÿEnable 0ÿdisable * No Pps1 Pdo after disable	R/W	1
4	En_Src_20VPdo	20VPdo Enable 1ÿEnable 0: disable * No 20V Pdo after disable	R/W	1
3	En_Src_15VPdo	15VPdo Enable 1ÿEnable 0: disable * No 15V Pdo after disable	R/W	1
2	En_Src_12VPdo	12VPdo Enable 1ÿEnable 0: disable * No 12V Pdo after disable	R/W	1
1	En_Src_9VPdo	9VPdo Enable 1ÿEnable 0: disable * No 9V Pdo after disable	R/W	1
0	Reserved		R/W	R

(0x2C) TYPEC_CTL18 (PDO plus **10mA** current enable, needs to be configured together with the current setting register)

I2C address 0XEA Register address = 0x2C

Bit(s)	Name	Description	R/W	RESET
7:5		Reserved	R/W	0
4	EN_20VPDO_ADD	20VPDO add 10mA current enable 1ÿenable 0ÿdisable	R/W	0
3	EN _15VPDO_ADD	15VPDO add 10mA current enable 1ÿenable 0ÿdisable	R/W	0
2	EN_12VPDO_ADD	12VPDO add 10mA current enable 1ÿenable 0ÿdisable	R/W	0
1	EN_9VPDO_ADD	9VPDO add 10mA current enable 1ÿenable 0ÿdisable	R/W	0
0	EN_5VPDO_ADD	5VPDO add 10mA current enable 1ÿenable 0ÿdisable	R/W	0

2.2 Read-only status indication register

A must read section!!!

Multiple registers represent the same state. Each read of the lower **8-** bit register will update the upper **8-** bit and lower **8-** bit data.

To read the register, you must read the lower **8** bits first and then the upper **8** bits to ensure that the same data is read.

The order of the two registers of **BAT** terminal voltage should be to read **0x50 first and then 0x51.**

(0x31) STATE_CTL0 (Charging status control register)

I2C address 0XEA Register address = 0X31

Bit(s)	Name	Description	R/W
7:6	Reserved		R
5	CHG_En	Charging flag 1: Charging status (VbusOk is considered charging status) 0: Not charging	R
4	CHG_End	Full status flag 1: Fully charged 0: Charging is not fully	R
3	Output_En	Discharge status flag 1: Discharging state and the output port is open, no abnormality 0: The discharge status output is not turned on or there is a discharge abnormality	R
2:0	Chg_state	Chg_state	R

		000: Standby 001: Trickle 010: Constant current charging 011: Constant voltage charging 100: Waiting for charging (including charging not started, etc.) 101: Full state 110: Charging timeout	

(0x32) STATE_CTL1 (Charging status control register)

I2C address 0XEA Register address = 0X32

Bit(s)	Name	Description	R/W
7:6	Chg_State	Chg_state 00: 5V input charging 01: High voltage input fast charging	R
5:0	Reserved		R

(0x33) STATE_CTL2 (Input **Pd** state control register)

I2C address 0XEA Register address = 0X33

Bit(s)	Name	Description	R/W
7	Vbus_Ok	Vbus_Ok 1: Vbus has power 0: Vbus has no power	R
6	Vbus_Ov	Vbus_Ov 1: Vbus input overvoltage 0: Vbus input has no overvoltage	R
5:3	Reserved		
2:0	Chg_Vbus	Charging voltage 111: 28V charging 110: 20V charging 101: 15V charging 100: 12V charging 011: 9V charging 010: 7V charging 001: 5V charging	R

(0x34) TypeC_STATE (system status indication register)

I2C address 0XEA Register address = 0X34

Bit(s)	Name	Description	R/W
7	Sink_Ok	TypeC Sink input connection flag 1: Valid	R

		0: Invalid	
6	Src_Ok	TypeC Src output connection flag 1: Valid 0: Invalid	R
5	Src_Pd_Ok	Src_Pd_Ok Output connection flag 1: Valid 0: Invalid	R
4	Sink_Pd_Ok	Sink_Pd_Ok Input connection flag 1: Valid 0: Invalid	R
3	Vbus_Sink_Qc_Ok Input fast charge valid flag Qc5V and Pd5V are not considered fast charge Ok	1: Valid 0: Invalid	R
2	Vbus_Src_Qc_Ok outputs the fast charge valid flag Qc5V and Pd5V, which are not considered fast charge OK	1: Valid 0: Invalid	R
1:0	Reserved		

(0x35) RECEIVED_PDO (receive PDO gear)

I2C address 0XEA Register address = 0X35

Bit(s)	Name	Description	R/W
7:5	Reserved		R
4	PDO_20V	The device receives PDO20V 1: Yes 0: None	R
3	PDO_15V	The device receives PDO15V 1: Yes 0: None	R
2	PDO_12V	The device receives PDO12V 1: Yes 0: None	R
1	PDO_9V	The device receives PDO9V 1: Yes 0: None	R
0	PDO_5V	The device receives PDO5V 1: Yes 0: None	R

(0x38) STATE_CTL3 (system overcurrent indication register)

I2C address 0XEA Register address = 0X38

Bit(s)	Name	Description	R/W

7:6	Reserved		R
5	Vsys_Oc	Vsys output overcurrent flag, need to write 1 to clear 0 1: Vsys output triggers an overcurrent signal 0: Vsys output does not trigger overcurrent signal If the system detects overcurrent status twice or more within 600mS, The overcurrent is considered valid and this flag is set to 1. The external master reads this flag. The flag bit can be used to determine whether an overcurrent abnormality occurs; From birth to system sleep, the time is about 1.5s	R
4	Vsys_Scdt	Vsys output short circuit flag, need to write 1 to clear 0 1: Vsys output has a short-circuit trigger signal 0: Vsys output does not trigger a short circuit signal If the system detects short circuit status more than twice within 600mS, The short circuit is considered valid and this flag is set to 1. The external master reads this flag. The flag bit can be used to determine whether a short circuit abnormality occurs; From birth to system sleep, the time is about 1.5s	R
3:0	Reserved		R

(0x50) BATVADC_DAT0 (VBAT voltage register)

I2C address 0XEA Register address = 0X50

Bit(s)	Name	Description	R/W
7:0	BATVADC[7:0] BATVADC data lower 8 bits	VBATPIN voltage	R

(0x51) BATVADC_DAT1 (VBAT voltage register)

I2C address 0XEA Register address = 0X51

Bit(s)	Name	Description	R/W
7:0	BATVADC[15:8] BATVADC data high 8 bits	VBATPIN voltage VBAT=BATVADC (mV)	R

(0x52) VsysVADC_DAT0 (Vsys voltage register)

I2C address 0XEA Register address = 0X52

Bit(s)	Name	Description	R/W
7:0	VsysVADC[7:0] Vsys voltage data lower 8 bits	VsysPIN voltage	R

(0x53) VsysVADC_DAT1 (Vsys voltage register)

Send I2C address 0XEA Register address = 0X53

Bit(s)	Name	Description	R/W
7:0	VsysVADC[15:8] High 8 bits of Vsys voltage data	VsysPIN voltage Vsys= VsysVADC (mV)	R

(0x69) TIMENODE1 (the first bit of the timestamp register) (the timestamp symbol is an **ASCII** character)

I2C address 0XEA Register address = 0x69

Bit(s)	Name	Description	R/W
7:0	TimeNode1 The first ASCII symbol corresponds to the value		R

(0x6A) TIMENODE2 (second bit of timestamp register)

I2C address 0XEA Register address = 0x6A

Bit(s)	Name	Description	R/W
7:0	TimeNode2 The second ASCII symbol corresponds to the value		R

(0x6B) TIMENODE3 (timestamp register third bit)

I2C address 0XEA Register address = 0x6B

Bit(s)	Name	Description	R/W
7:0	TimeNode3 The third ASCII symbol corresponding to the value		R

(0x6C) TIMENODE4 (the fourth bit of the timestamp register)

I2C address 0XEA Register address = 0x6C

Bit(s)	Name	Description	R/W
7:0	TimeNode4 The fourth ASCII symbol corresponding to the value		R

(0x6D) TIMENODE5 (the fifth bit of the timestamp register)

I2C address 0XEA Register address = 0x6D

Bit(s)	Name	Description	R/W
7:0	TimeNode5 The fifth ASCII symbol corresponding value		R

(0x6E) IBATIADC_DAT0 (**BAT** terminal current register)

I2C address 0XEA Register address = 0x6E

Bit(s)	Name	Description	R/W
7:0	IBATIADC[7:0]	The lower 8 bits of the cell current IBATIADC data	R

(0x6F) IBATIADC_DAT1 (**BAT** terminal current register)

I2C address 0XEA Register address = 0x6F

Bit(s)	Name	Description	R/W
7:0	IBATIADC[15:8]	High 8 bits of the cell current BATIADC data IBAT= IBATIADC(mA)	R

(0x70) ISYS_IADC_DAT0 (**Isys** terminal current register)

I2C address 0XEA Register address = 0x70

Bit(s)	Name	Description	R/W
7:0	ISYSIADC[7:0]	IVsys terminal current VsysIADC data lower 8 bits	R

(0x71) Isys_IADC_DAT1 (**Isys** terminal current register)

I2C address 0XEA Register address = 0x71

Bit(s)	Name	Description	R/W
7:0	IVsysIADC[15:8]	IVsys terminal current VsysIADC data high 8 bits IVsys = VsysIADC(mA)	R

(0x74) Vsys_POW_DAT0 (**Vsys** power register)

I2C address 0XEA Register address = 0X74

Bit(s)	Name	Description	R/W
7:0	Vsys_POW_ADC [7:0]	The lower 8 bits of the Vsys power ADC data	R

(0x75) Vsys_POW _DAT1 (Vsys power register)

I2C address 0XEA Register address = 0X75

Bit(s)	Name	Description	R/W

7:0	Vsys_POW_ADC[15:8]	High 8 bits of Vsys power ADC data Vsys_POW= Vsys_POW_ADC(10mW)	R

(0x77) INTC_IADC _DAT0 (NTC output current register)

I2C address 0XEA Register address = 0X77

Bit(s)	Name	Description	R/W
7	NTC_IADC_DAT 0: output 20uA 1: Output 80uA		R
6:0	Reserved		

(0x78) VGPIO0_NTC_DAT0 (VGPIO0_NTC_ADC voltage register)

I2C address 0XEA Register address = 0X78

Bit(s)	Name	Description	R/W
	VGPIO0_DAT0 [7:0]	VGPIO0_ADC data lower 8 bits 7:0	R

(0x79) VGPIO0_NTC_DAT1 (VGPIO0_NTC_ADC voltage register)

I2C address 0XEA Register address = 0X79

Bit(s)	Name	Description	R/W
7:0	VGPIO0_DAT1 [15:8]	VGPIO0_ADC High 8 bits of data VGPIO0_DAT= VGPIO0_ADC (mV)ÿ0~3.3Vÿ	R

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