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REAL-TIME PROCESSING STAGES OF ELECTROCARDIOGRAM SIGNAL: A REVIEW

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Abstract. Signal analysis is a multidisciplinary field that combines various processes to create robust pipelines for automating data analysis. Within the medical field, its application revolves around physiological signals. Electrocardiogram (ECG) signal provides vital information concerning various cardiac conditions affecting the human heart. ECG analysis is a central pillar of medical research with the goal of detecting and preventing potentially fatal cardiac events. This review article aims to provide a comprehensive analysis of real-time processing techniques for electrocardiogram signals. It discusses the different methods and algorithms used for detecting and analyzing ECG signals in real-time, with a focus on their effectiveness and efficiency. Where, it evaluates the use of various techniques such as ECG signal preprocessing (denoising), ECG fiducial points detecting and ECG signal classification. It also highlights the challenges faced in real-time ECG signal processing, such as High-fidelity signal acquisition and noise reduction, and computational efficiency and resource constraints. Furthermore, the article presents an overview of the existing QRS-peak detection strategies, including methods such as Haar wavelet transform, and modified MaMeMi Filter.

Keywords: Electrocardiogram (ECG), preprocessing, feature extraction, classification, FPGA.
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1 Introduction

Globally, cardiovascular diseases hold the highest position as a cause of death. ECG is a valuable diagnostic tool that records heart electrical activity and stands as a valuable diagnostic tool. However, the current clinical practice involves visually inspecting ECGs, which is a time-consuming task, especially for long-term recordings like 24-hour Holter monitoring that can have around 100,000 heartbeats (Abdulla & Al-Ani, 2020; Roth et al., 2020).

Driven by the need for clarity and understanding, this comprehensive review of real-time ECG processing is structuring as a stage-based model to highlight the significance of each step. The initial stage examines the noise removal techniques employed during ECG signal acquisition. The second stage focuses on identifying crucial fiducial points and pivotal for accurate heart condition classification. Each ECG wave and segment carries vital information for classifying arrhythmia types, enabling disease detection and diagnosis in the final stage.

Figure 1 demonstrates the three fundamental components of an ECG, namely the T wave, QRS complex, and P wave, along with their corresponding intervals (M Abdul-Jabbar & Waleed

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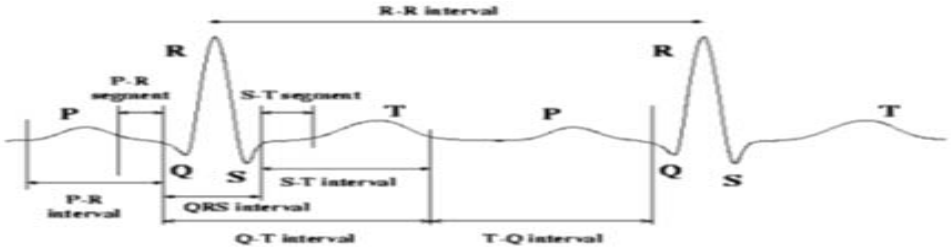

Figure 1: ECG Signal showing P-QRS-T Waves

Hamad, 2014). The appearance of the P wave results from electrical potentials when the atria undergo depolarization before contraction begins. Similarly, the QRS complex is produced by potentials generated during ventricular depolarization before contraction, as the depolarization wave spreads through the ventricles. Depolarization of the heart is indicated by both the P wave and the QRS complex. Following the ventricular depolarization, the T wave, known as repolarization, emerges during the recovery phase. This repolarization wave typically occurs within 0.25 to 0.35 seconds after depolarization in the ventricular muscle. Consequently, the ECG comprised depolarization and repolarization waves (Fikri et al., 2021; Guyton, 2006).

This paper focuses on real-time ECG processing, for the detection different arrhythmias and heart conditions. The objectives can be summarized as follows:

1. An in-depth analysis of the ECG waveform is essential for gaining a comprehensive understanding of the heart's electrical activity. This review will delve into the various components of the ECG and their significance in reflecting the heart's function.

2. Introducing a stages-based model for real-time ECG processing, this paper provides a comprehensive review of related work in ECG real-time processing by covering various stages such as ECG preprocessing and classification.

3. This review comprehensively examines real-time ECG signal processing, exploring advanced denoising techniques, accurate fiducial point detection, and robust classification algorithms for arrhythmia diagnosis.

4. This paper conducts a comprehensive examination of techniques and methodologies employed at each stage of ECG signal processing, offering valuable insights and illuminating the interconnectedness of relevant research.

5. The paper outlines of hardware and software tools for research in the field of ECG signal analysis.

The rest of this paper is structured as follows: Section 2 provides an overview of prior related work in the literature, focusing on various stages of ECG signal analysis, from data preprocessing to classification, which is divided into three subsections: Sub-Section 2.1 tackles noise reduction through smoothing and filtering. Sub-Section 2.2 presents prior related work on ECG fiducial points and other feature detection. Sub-Section 2.3 presents various established models for classifying ECGs, allowing for diagnosis and interpretation. Section 3 dives deep into the hottest research directions in real-time ECG processing, as explored by prominent researchers. In Section 4, a comparative summary is presented. Lastly, Section 5 concludes this article.

2 Literature Review of ECG Signal Processing Stages

This article reviews the implementation of ECG processing algorithms published in the last decade. It collects relevant articles from 2016 to 2024 from various resources, including Springer, Elsevier, IEEE, and World Scientific. The review analyzed hardware implementation of ECG preprocessing, feature extraction, and classification stages, comparing different works and providing insights to researchers.

2.1 Stage 1: Preprocessing (Denoising)

ECG processing relies on body-connected sensors. Noise affects signal quality and classification. Preprocessing is crucial for accurate analysis, using digital filters to remove unwanted frequencies and artifacts while preserving relevant components. Researchers have adopted various filters to enhance signal quality, improving interpretation, diagnosis, and patient care in cardiac conditions.

Al-Khammasi et al. (2016) designed FIR filters for ECG denoising, attenuating 60 Hz frequencies using VHDL and Quartus II. Performance analysis favored pipelined MAC implementation with fewer resources, suggesting its use for industrial ECG monitoring to reduce risks.

Gaikwad and Chavan (2016) implemented an ECG noise reduction IIR Chebyshev filter using XSG. The paper emphasized the importance of considering quantization and overflow for filter stability. The filter is analytically designed, simulated in Simulink, and improved speed on FPGA compared to DSPs. It effectively removes noise in ECG signals, and the paper included a comparison of filter types.

Gaikwad and Chavan (2018) proposed an IIR Elliptic digital filter on FPGA for ECG signal noise reduction. The design included MATLAB Simulink and Xilinx System Generator blocks for implementation demonstration. The Vedic multiplier is used for filter implementation. The filter's performance is evaluated in terms of area, power, and speed, highlighting its advantages. The paper presented a detailed step-by-step design process and simulated the results of the filter.

Pathak et al. (2018) introduced an architecture capable of acting as both a notch and anti-notch filter. The architecture was implemented as a 2nd order IIR filter on the Xilinx ISE 14.4 program, specifically on the Zynq FPG kit. By applying the retiming concept, the filter's speed was improved by 1.56 times while maintaining accuracy. To reduce hardware complexity in terms of kit area, the notch, and anti-notch filters were combined, resulting in a more efficient solution.

ECG (2018) proposed an architecture for real-time ECG denoising using an adaptive dual threshold filter. The implementation involved structural VHDL description of functional blocks, along with parallelization for accelerated processing and high performance. The architecture is designed for low-cost FPGA-based systems, prioritizing low complexity and resource occupancy. Optimization and simplification were achieved through VHDL implementation.

Venkatesan et al. (2019) introduced a DENLMS adaptive filter to remove white Gaussian noise, improving the quality of ECG signals. The architecture improves operational speed by minimizing critical paths using delay elements. Performance comparisons were made with the ENLMS and DNLMS algorithms. The pipelined DENLMS filter enhances speed and reduces power consumption but increases area due to latches. The evaluation was done using the Virtex 5 FPGA for speed, logic utilization, and power consumption analysis.

Sohal and Jain (2019) proposed a low-power FPGA-based hardware implementation for ECG signal preprocessing. The paper focused on designing FIR filters to remove high- and low-frequency ECG noises. It evaluated various window-based filter designs for their resource utilization and power consumption on the Zynq evaluation board. The preprocessing module is implemented using XSG and targets the Zynq-7000 with the Vivado program. Performance

comparisons revealed Kaiser and Bartlett's window as the most effective in terms of resource utilization and power consumption.

Thirrunavukkarasu et al. (2021) designed an FIR filter using the Kaiser Bessel window for ECG waveform noise removal. The Kaiser filter implemented using the FPGA consists of three Verilog blocks connected by wires. The Kaiser filter, similar to Hamming, incorporates a beta variable to control the filter threshold and is known for its high efficiency and low power consumption.

Mejhoudi et al. (2021) developed an FPGA architecture for ECG signal denoising using a hybrid technique: DWT and ADTF. The hardware-software co-design divided the architecture into functional blocks for parallel processing. This achieved high-performance noise reduction without impacting signal morphology. Simulation results demonstrated the system's effectiveness, processing in 0.3 ms at a 360 Hz acquisition frequency. The architecture efficiently utilized FPGA resources, occupying less than 1% of total registers and logic elements.

Following Patel and Shah (2022), the design was presented for a bandpass filter that can remove many kinds of noises from the ECG signal. The effectiveness of the filter was proved by means of evaluating and performing the power spectrum analysis which means that it is a applicable and real time method for decreasing the noise.

Sohal and Jain (2022) used FPGA-based waveform regeneration algorithms of ECG signals using series window and DWT. The Haar wavelet-based design showed a very good sterling, saving resources and it may be integrated into portable biological devices. There is the capability to compare efficiency between systems and also the systems are evaluated.

A model of reservoir computing at an economical expense by means of FPGA and ECG denoising of high-speed was done by Elbedwehy et al. (2022). An architecture was applied here employing the back propagation recurrence bound with technologically advanced and less complex modules.

Shanmugaraja et al. (2023) designed a pipelined LMS adaptive filter aiming at ECG signal processing, which not only brings the good features of adaptive filters but also is low power consumption. The investigation considered FPGA, which showed the rising speed as compare to other rival methods.

In addition, Vaishnavi et al. (2023) came with a new adaptive filter, which plays efficaciously as an LMS adaptive filter to banish the baseline wander noise from the ECG signals, showing its outstanding result in improving the signals' quality.

Gon and Mukherjee (2023) suggested the efficient reconstruction of FPGA with multiplierless lifting-based wavelet denoising for ECG noise cancellation. Their architecture with the ability to lower resource consumption as well as increase the operating frequency with existing ones and even future ones.

Boumehrez et al. (2023) proposed Lifting 9/7 Wavelet Filter Bank for the analysis of an ECG-signal on the FPGA platform (Cyclone-II). The papers presented alternatives shifting logic instead of the standard left-right (shifting) for multiplication-division operations, which reduces execution time, logic complexity, and power consumption. To be a feasible, we proposed a data structure to facilitate implementing the lifting filter in two-dimensional discrete wavelet transforms.

2.2 Stage 2: Feature Extraction

ECG classification relies on detecting fiducial points, particularly the QRS complex, which reflects ventricular contraction. Its shape enables automated detection of various characteristics, forming the basis for classification techniques. QRS detection is foundational for ECG analysis algorithms. Several approaches have been proposed for feature extraction, targeting the ST-segment, QRS complex, R-peak, and other fiducial points. This section explores the literature on different methods and techniques for hardware implementation of QRS complex, ST-segment, and fiducial point detection.

Table 1: Summarizes the different noise elimination approaches utilized by researchers in recent studies for the ECG signal

(Reference)	Method	Database	Noise	Kit Type
(Al-Khammasi et al., 2016)	FIR filter	MIT-BIH arrhythmia	60 Hz Gaussian White Noise	N/A*
(K. Gaikwad & Chavan, 2016)	IIR Chebyshev type II	MIT-BIH arrhythmia	High-Frequency Noise	FPGA Spartan 3E
(K. M. Gaikwad & Chavan, 2018)	IIR Elliptic	N/A*	High Frequency Noise	FPGA Spartan 3E
(Pathak et al., 2018)	IIR Notch/anti-notch	N/A*	N/A*	FPGA Zynq
(ECG, 2018)	Adaptive Dual Threshold Filter	MIT-BIH arrhythmia	High Frequency Noise	N/A*
(Venkatesan et al., 2019)	LMS Adaptive Filter	N/A*	White Gaussian Noise	FPGA Virtex 5
(Sohal & Jain, 2019)	FIR filter	MIT-BIH arrhythmia	Electromyography Noise and BLW Noise	FPGA Zynq
(Thirrunavukkarasu et al., 2021)	Kaiser FIR filter		Noise Occurs Due to Outer Surface of The Thermal and Electromagnetics Field	FPGA
(Mejhoudi et al., 2021)	Adaptive Dual Threshold Filter	MIT-BIH arrhythmia	High-Frequency Noises, Electromyogram Noises, Power Line Interferences	FPGA Intel-Altera
(Patel & Shah, 2022)	Multiband FIR Filter	Physionet	Baseline Wandering, Motion Artefacts , High Frequency Noises Power Line Interference	FPGA Spartan 3E
(Sohal & Jain, 2022)	Linear Windowing Techniques and Non-Linear DWT	MIT-BIH arrhythmia	Low-Frequency Noise and High-Frequency Noise	different FPGA boards (Virtex, Kintex, and Zedboards)
(Elbedwehy et al., 2022)	Single-Node Reservoir Computing architecture, based on Recurrent Neural Network	MIT-BIH arrhythmia	Electromyogram (EMG) Nois, Power Line Interference (PLI) Noise	FPGA Artix-7
(Shanmugaraja et al., 2023)	LMS adaptive filter	N/A*	White Gaussian Noise	FPGA Vertex 5
(Vaishnavi et al., 2023)	LMS Adaptive Filter	MIT-BIH	Baseline Wander Noise	N/A*
(Gon & Mukherjee, 2023)	Lifting-Based Wavelet	MIT-BIH arrhythmia	N/A*	FPGA Nexys 4DDR
(Boumehrez et al., 2023)	Lifting 9/7 Wavelet FBs	N/A*	N/A*	FPGA Altera

N/A*: Not Available.

Ma et al. (2016) proposed an R wave detection algorithm using lifting wavelet and differential operations and implemented it on an FPGA. The algorithm ensured low computational complexity and high accuracy, making it suitable for portable electrocardiogram monitoring devices. Evaluation on databases like MIT-BIH ST Change, MIT-BIH Arrhythmia, and Supraventricular Arrhythmia databases, achieved high accuracy rates of over 99.8% in MATLAB simulations and an average recognition rate of 99.68% in FPGA experiments. The algorithm occupied minimal FPGA resources, according to the resource estimation report.

Abdullah and Abd (2016) developed a reliable FPGA-based ECG analysis system for accurate QRS complex determination and beat-to-beat interval extraction. The system included a VHDL-based R peak detection module implemented using Xilinx ISE 14.6 and simulated with MATLAB System Generator. Performance testing used MITBIH Arrhythmia ECG database. FPGA system handled preprocessing, feature extraction, and classification with validated results.

Zhang et al. (2017) introduced an algorithm based on wavelets for detecting QRS complexes from ECG signals. Their method outperformed the Pan-Tompkins algorithm in terms of resource consumption and design simplicity. The algorithm enabled real-time QRS complex detection, suitable for telemonitoring high-risk cardiac patients.

Kumar and Chari, (2018) presented an efficient FPGA architecture for ECG R-peak detection by combining Shannon energy and Hilbert transform. The smooth Shannon energy envelope is obtained through extraction and filtering. The Hilbert transform accurately locates the R-peak, and FFT techniques improve performance. The technique achieved 99.86% accuracy, 99.95% sensitivity, and 99.90% positive predictivity with the MIT-BIH arrhythmia database.

Martínez-Suárez and Alvarado-Serrano (2019) developed a prototype ambulatory ECG monitoring system that acquires and stores 3 leads with real-time R-wave detection using a spline wavelet transform on an FPGA. The system included a 4-channel ECG front end ADS1294,

16 GB micro SD memory, and Artix-7 FPGA with a 200 Hz bandwidth, 112 dB CMRR, 0.76 μV resolution, and 125 mA average current consumption lasting at least 30 hours. Evaluating the R wave detection algorithm on the VF lead with 30-minute records of 5 resting subjects, it achieved 99.4% accuracy. The system provided real-time beat-to-beat heart rate measurements, making it valuable for long-term ECG monitoring applications.

Nez-Suárez and Alvarado-Serrano (2019) proposed a module that detected R waves and calculated beat-to-beat RR intervals using continuous spline wavelet transform. Tested on the Basys 3 development card with an Artix-7 FPGA, the module achieved over 90% accuracy in analyzing five 30-minute and one 24-hour ECG recordings. It enabled heart rate variability analysis in long and short ECG recordings when implemented on an FPGA.

Talukder et al. (2020) introduced a real time QRS detection method utilizing Integer Haar Wavelet Transform. The algorithm was implemented on a Digilent Nexys 4 FPGA board, making it suitable for medical equipment and IoT systems. They simplified the hardware architecture by approximating floating point arithmetic to integer arithmetic. An architecture was demonstrated through simulation and hardware testing, achieving an error percentage of less than 1.4% in RR interval computation and 98.76% accuracy in QRS detection. The synthesis of the architecture using 130 nm technology resulted in only 0.717% leakage power.

Meddah et al. (2020) presented an FPGA-based system for ECG monitoring and arrhythmia detection. It used the Tompkins and Pan algorithm for QRS detection and was optimized for the Spartan 3E FPGA board. Comparative studies validated its effectiveness and reliability, achieving high sensitivity and accuracy.

Chen et al. (2020) proposed a lightweight QRS detection algorithm employing adaptive threshold techniques. It achieved high sensitivity, positive predictivity, and accuracy. The algorithm's effectiveness was demonstrated using MIT-BIH databases, making it suitable for wearable heart rate monitoring and automatic ECG analysis.

García-Limón et al. (2021) created an FPGA-based prototype for ambulatory ECG monitoring, acquiring and storing 3 leads for real-time measurements. The system utilized a Xilinx Artix-7 FPGA, an ADS1294 circuit for lead acquisition, and a micro-SD memory for storage. It met the required electrocardiograph characteristics, including a bandwidth of 0.05-100 Hz and a CMRR of at least 80 dB.

Wei et al. (2021) proposed a method to suppress baseline drift in ECG acquisition using a digital-analog mixing approach. They presented an adaptive threshold-based feature recognition algorithm for real-time analysis of ECG signal morphology. The system achieved high accuracy in detecting QRS waves (over 99%) and T waves (94%). The paper integrated analog and digital signal processing, along with PCB drawing, to automatically extract, process, and detect user ECG signals. The Savitzky-Golay (SG) filter effectively suppressed low-frequency baseline drift and noise in the digital ECG signal.

Ganatra and Vithalani (2022) proposed an approach for analyzing ECG signals using FPGA technology, focusing on morphological feature extraction. The architecture utilized GSST and a detrended fluctuation analyzer to extract QRS complexes and P-waves. QRS regions are accurately localized using a correntropy envelope, and true P-waves are detected through an adaptive heuristic framework. Root mean square error estimation is employed to guide adaptive thresholding, enabling accurate T-wave measurements. Utilizing the Virtex 7 FPGA platform, the implemented architecture underwent a comprehensive comparative study with other feature descriptors to assess its performance and efficiency.

Malathi and Vijay Kumar (2023) proposed a high-performance, low-complexity QRS detector design called QRS-MoMaMeMi-MOA. It utilized the MoMaMeMi filter optimized with the Mayfly optimization algorithm to suppress high-frequency noise and remove baseline wander in ECG signals. The filter outperforms existing methods such as QRS-HD-MaMeMi, QRS-KF-ATA, and QRS-CAF in terms of accuracy and detection error rates. The filter design is implemented on FPGAs.

Table 2: Summary of various ECG feature extraction approaches

(Reference)	Fiducial Points	Method for Detection	Kit Type
(Ma et al., 2016)	R-Wave	Lifting Wavelet	FPGA Altera
(Abdullah & Abd, 2016)	R-R Interval	FPGA-Based ECG Analysis System	FPGA Spartan 3A
(Zhang et al., 2017)	QRS Complex	Integer Haar Transform	FPGA Cyclone
(Aravind Kumar & Manjunatha Chari, 2018)	R-Wave	Method combines a Band-pass filter, first-order differentiation process, Shannon energy extraction, and Hilbert Transform	FPGA Vertex 5
(Martínez-Suárez & Alvarado-Serrano, 2019)	R-Wave	Prototype Ambulatory ECG Monitoring System	FPGA Artix-7
(Nez-Suárez & Alvarado-Serrano, 2019)	R-Wave	Continuous Wavelet Transform	N/A*
(Talukder et al., 2020)	QRS Complex	Integer Haar Wavelet Transform	FPGA Artix-7
(Meddah et al., 2020)	QRS Complex	FPGA-based system for ECG signal monitoring and cardiac arrhythmia detection	FPGA Nexys 2
(A. Chen et al., 2020)	QRS Complex	ET and PD Controlled Threshold Strategy	FPGA Altera
(García-Limón et al., 2021)	QRS, T-Wave	Prototype of an Ambulatory Long-Term ECG Monitoring System	FPGA Artix-7
(Wei et al., 2021)	QRS, T-Wave	SG Filter	FPGA Altera
(Ganatra & Vithalani, 2022)	QRS, P-Wave	Generalized Synchros queezing Transform, Correntropy Function and Adaptive Heuristic Framework	FPGA Vertex 7
(Malathi & Vijay Kumar, 2023)	QRS Complex	Modified MaMeMi Filter	FPGA Zynq
(Yan et al., 2023)	R-Wave	FIR , High-Order Adaptive Median Filter	FPGA Altera
(García Limón et al., 2023)	RT interval	Continuous Wavelet Transform	FPGA Artix-7

Yan et al. (2023) focused on automatic detection of QRS wave groups in ECG signals for data analysis. MIT-BIH database and human ECG data were used. A high-order FIR low-pass filter and Shannon energy algorithm are applied to process the data and minimize noise. The proposed method accurately extracted R-waves and controlled the left ventricular assist device (LVAD) for blood pumping. Feasibility was tested with normal and abnormal ECG signals using the R-R interval and threshold method.

García Limón et al. (2023) implemented algorithms using the CWT with splines in an ambulatory ECG monitor prototype. The prototype features an ADS1294 analog-digital converter, Xilinx XC7A35T-ICPG236C FPGA Artix-7, LCD, and 16 GB micro-SD memory. The FPGA algorithm enabled real time detection of various T wave and QRS complex morphologies, facilitating heart rate and RT interval analysis. Table 2. presents a compilation of approaches that extract features from the ECG signal.

2.3 Stage 3: Classification

After noise filtration and feature engineering, the ECG signals are categorized into various classes based on detected fiducial points and the specific issue being addressed. This section covers literature approaches for ECG signal classification with hardware implementation.

Abubakar et al. (2018) presented a patient-specific processor for classifying shockable cardiac arrhythmia without using machine learning. The processor included an efficient hardware-based engine for extracting a reduced set of five features. A patient-specific, adaptive thresholding engine was implemented for robust peak and interval detection, along with simplified decision logic for real time arrhythmia discrimination. With a specificity of 99.75% and an average sensitivity of 98.66%, the SCAD processor achieves high classification accuracy. Additionally, consumed low power, with a classification energy consumption of $0.89\mu J$. The system is designed for wearable defibrillators, providing immediate response time and continuous monitoring of SCA and non-SCAs. The paper compared the proposed system with state-of-the-art works, highlighting its comparable performance and advantages.

Sharabaty et al. (2018) proposed a classification system based on FPGA for identifying

various heart malfunctions using standard ECG features. The system was implemented on Xilinx Spartan 3AN FPGA using Labview and Verilog. Two classifiers, NVG-RAM and TD weightless neural network, were used for decision-making in the system. The NVG-RAM and TD classifiers were compared to assess their suitability for the ECG classification system. Experimental data demonstrated a 100% PCC for heart conditions with the NVG-RAM classifier and a 98.84% PCC with the TD classifier.

Alfaro-Ponce et al. (2019) developed an algorithm using a continuous neural network for automatic detection of arrhythmias. The algorithm was implemented on FPGA with fixed point arithmetic. Validation achieved 93.80% accuracy and 98% average sensitivity using fivefold cross-validation on the entire set of EKG signal samples. CoNN was introduced as a real-time classifier, representing an early attempt to directly classify arrhythmias using EKG signals.

Saadi et al. (2019) developed a system that utilizes Xilinx System Generator blocks to implement an ECG-neuro classifier on an FPGA kit. They employed an approximate linear phase BLWDF to extract the QRS complex from the ECG signal. The classifier categorized ECG signals from European databases into four heart disease classes: Normal, RBBB, LVH, and LBBB. The neural network training process included using the Matlab toolbox to acquire the necessary weights and biases. VHDL translation of the models helped measure chip resource usage and calculate the maximum operating frequency.

Zairi et al. (2020) developed an FPGA-based arrhythmia recognition system using an artificial neural network. They optimized the software-based diagnostic approach to minimize the FPGA energy consumption and prototype size. The classification method involved wavelet-based feature extraction, multilayer perception (MLP) classification, and class decision. The methodology was implemented using the Nexys4 Artix7 evaluation kit and XSG for DSP. Performance comparison with MATLAB floating point validated the FPGA fixed point architecture as a customized mobile classifier for real-time patient monitoring.

Liu et al. (2020) utilized DWT for feature extraction from ECG signals, specifically using the "db2" wavelet's approximate coefficient as feature vectors. ECG signal classification employed the SVM algorithm, known for effective classification. The SVM circuit was generated through high-level synthesis (HLS), optimizing it through source code rewriting and additional directives. The system was implemented on the Xilinx ZYNQ SoC, integrating the processing system and programmable logic on a single chip. The system achieved 98.7% classification accuracy and a real-time classification time of 280 ps per heartbeat.

Lu et al. (2021) used a 1-D CNN structure with a GAP layer for ECG beats classification. The architecture was designed to meet the specific requirements of this task, incorporating data reuse strategies to optimize memory access and increase parallelism. The Relu function implementation was moved to the processing unit to reduce hardware resource consumption. The irregular GAP operation was implemented without additional overhead. The trained parameters were saved in weight and bias RAM before making predictions. Data Scatter was used for data distribution and padding. The PU array ran in a pipeline to generate efficient calculation results, which were then quantized using a Bit-width Converter.

Lee et al. (2021) introduced a system for real time ECG diagnosis using hardware accelerators and an approximated template-based algorithm. This personalized approach improves detection rates and reduces memory usage compared to existing methods. The algorithm adapts to individual reference beats, allowing personalized diagnosis for each person's signal. Experimental results demonstrated a significant reduction in diagnosis time, with an 89.96% shorter execution time compared to software when diagnosing ECG signals from five individuals containing 1987 beats. Additionally, a signal processing unit is introduced for real-time ECG data processing.

Xing et al. (2022) introduced a power resource of recognition of heartbeat-ECG by model of spiking neural networks and, moreover, operated the attention mechanism as splitted in channels. The optimized model was the most accurate, low power consumption, and it was

possible to track the ECG signal variations in real time, thus, effectively detecting anomalies in ECG signals.

Chen and Wong (2022) introduced neuromorphic based standardization methodology to classify ECG signal utilizing spike timing dependent plasticity. They really made ECG classifier on a FPGA-based neuromorphic circuit with the use of the efficient resource occupation.

Dal and Aşkar (2022) showed their FPGA classifier based on ANN architecture that did not require the necessity of using a feature extraction method. ANN was being developed using the MITBIH arrhythmia dataset by applying training and validation. A mathematical model of the feed-forward network was developed using Verilog HDL on Xilinx Zybo FPGA. Network parameters, including weights and biases, were converted from 32-bit floating-point to 8-bit fixed-point numbers for efficient FPGA mapping. The ANN model achieved approximately 97% accuracy during training. The entire procedure was completed within 232 clock cycles, showcasing the efficiency of the approach.

Lu et al. (2022) proposed a CNN accelerator for ECG classification using tile-first dataflow and a specialized data compression format. The system architecture has a central controller with an FSM for instruction fetching and control signal provision. The PE array consisted of four cascade PE structures for addition and multiplication operations, generating partial sums of a tile. The pooling module supported various operations such as average pooling, max pooling, and global average pooling on the calculation results. The network employs 16-bit data quantization, which maintains accuracy for ECG classification with minimal loss.

Ku et al. (2023) proposed a high-performance AIA for arrhythmia classification on ECG using an efficient 1DCNN. The architecture achieved real time low-power consumption and high-accuracy classification. It reduced memory access time by 29x and latency by 22.5x compared to a single MAC operation. The hardware implementation on Xilinx PYNQ-Z2 had small latency and provided high performance. Software simulation achieved accuracies of 97.3% and 98.3%, while hardware implementation with quantization and pruning achieved accuracies of 96.6% and 96.5%.

Chang et al. (2023) developed a smart clothing system for the automatic detection of cardiovascular diseases (CVDs) in daily life. An FPGA-based ECG analysis module implemented a CVD detection algorithm for real-time data extraction and analysis. The fabric of the smart clothing was coated with graphene oxide to improve conductivity and enable non-contact sensing. ECG was recognized as an important diagnostic technique, providing detailed information about cardiac activity during muscle depolarization and repolarization.

Lu et al. (2023) presented an LMA network for ECG classification, tailored to the signal characteristics and classification model requirements. An accelerator that employs multiple channels in parallel and utilizes output data reuse has successfully achieved efficient pipeline processing and low-power acceleration. Deployed on Xilinx's ZYNQ-7100 platform, the accelerator achieves 116.7 GOPs throughput with 6.67W power consumption. It boasted a hardware resource utilization rate of 0.33 GOPS/DSP and 2.85 GOPS/kLUT, surpassing general CPUs/GPUs in hardware utilization and energy efficiency. This accelerator met the demands of high-performance, low-power intelligent terminal devices. These different classification methods are summarized in Table 3.

3 Trend Directions of Researchers

This section provides an overview of the major trends identified by prominent researchers in ECG real-time processing stages as a reference and starting point for new researchers (Azzouz et al., 2024; Brindha & Manjula, 2023; Chinmayi & Padmaja, 2023; Manga et al., 2024; Shekhawat et al., 2024; Sinha & Kar, 2024; Swetha & Ramakrishnan, 2024; Thannoon & Hashim, 2024; Yang et al., 2024).

- LMS Adaptive Filter for denoising.

Table 3: Summary of various ECG classification approaches

(Reference)	Algorithm	Database	Platform Type
(Abubakar et al., 2018)	SCA processor	ECG-ID, MIT-arrhythmia	FPGA
(Sharabaty et al., 2018)	TD, NVG-RAM	MIT-BIH arrhythmia	FPGA Spartan 3AN
(Alfaro-Ponce et al., 2019)	Continuous Neural Network	MIT-BIH Arrhythmia	FPGA Zinq
(Saadi et al., 2019)	BLWDF	European ST-T and QT	FPGA Spartan 6
(Zairi et al., 2020)	ANN	Physiobank	FPGA Artix7
(Liu et al., 2020)	DWT and SVM	MIT-BIH arrhythmia	FPGA Zynq
(J. Lu et al., 2021)	Convolutional Neural Network	MIT-BIH arrhythmia	FPGA Zynq
(Lee et al., 2021)	Energy-Efficient FPGA Accelerator	MIT-BIH arrhythmia	FPGA Alveo U200
(Xing et al., 2022)	SNN	MIT-BIH arrhythmia	FPGA
(D. R. Chen & Wong, 2022)	neuromorphic methods	MIT-BIH Arrhythmia	FPGA Zedboard
(Dal & Aşkar, 2022)	ANN	MIT-BIH Arrhythmia	FPGA Zybo
(J. Lu et al., 2022)	CNN	N/A*	FPGA Zynq
(Ku et al., 2023)	1DCNN	MIT-BIH Arrhythmia	FPGA PYNQ-Z2
(Chang et al., 2023)	Smart Clothing System	MIT-BIH arrhythmia, MIT-BIH AF, and MGHMF waveform	FPGA Artix-7
(T. Lu et al., 2023)	Multi-Scale Attention Network	PTB-XL dataset	FPGA Zynq

- Adaptive Filter Incorporating Systolic Architecture to remove PLI noise from ECG signals.
- Lifting-Based Wavelet Denoising.
- combination of particle swarm optimisation and wavelet transform for denoising.
- Generalized Synchrosqueezing Transform, Correntropy Function and Adaptive Heuristic Framework for denoising.
- Arithmetic optimised APT-VDF using reusable Vedic multiplier with simplified combinational logics for denoising.
- An adaptive and effective signed error normalized least mean square algorithm (SE-NLMS) or Mixed Noise Removal and Classification
- Integer Haar Wavelet and EMD Algorithm for feature extraction.
- A-CLT and digital fractional order differentiation for QRS-complex identification.
- Modified MaMeMi Filter Optimized with Mayfly Optimization Algorithm for QRS Detection.
- A WOA optimized fractional-order digital differentiator for QRS complex detection.
- Wavelet-Transform for RT Interval Measurements.
- Binarized spiking neural network optimized with momentum search algorithm for arrhythmia detection and classification.
- SVM classifier for arrhythmia detection.
- Convolutional Neural Network Accelerator for Wearable ECG Classification.
- Accelerating CNN Inference for ECG Classification.
- Real-time ECG monitoring and diagnosis through IoT.

4 Comparative Study

To highlight the contribution of this review compared to related review papers, a comparison with other relevant reviews in the field is presented. Given the extensive research conducted on ECG, numerous survey papers have been published. This review carefully selected reputable papers for a comparative analysis, as shown in Table 4. Notably, this survey distinguishes itself by focusing on research tools employed at each stage of the real-time ECG signal analysis process. This structure offers a comprehensive and stage-based approach to ECG research, serving as a valuable resource for both new and experienced researchers in this competitive field.

Table 4: Comparative summary of ECG Review papers

	ECG Signal processing stages				
(Reference)	Stage1: Preprocessing (Denoising)	Stage2: Feature Extraction	Stage3: Classification	Real-Time processing	Focus Area
(Iqbal, Wah, & Rehman, 2018)	No	Yes	Yes	No	Feature Extraction
(Satija, Ramkumar, & Manikandan, 2018)	Yes	Yes	Yes	No	Denoising Classification
(Lamba & Rawal, 2019)	No	Yes	Yes	No	Classification
(Chatterjee, Thakur, Yadav, Gupta, & Raghuvanshi, 2020)	Yes	No	No	No	Denoising
(Sahoo, Dash, Behera, & Sabut, 2020)	Yes	Yes	Yes	No	Arrhythmia Detection
(Fikri et al., 2021)	No	No	Yes	No	Classification
(Xiao et al., 2023)	Yes	Yes	Yes	No	Arrhythmia Classification
(Talwar & Cecil, 2023)	Yes	No	No	No	Denoising
(Singh & Krishnan, 2023)	No	Yes	No	No	Feature Extraction
(Ardeti, Kolluru, Varghese, & Patjoshi, 2023)	Yes	Yes	Yes	Yes	Processing Methods: Form Traditional To AI
Our article	Yes	Yes	Yes	Yes	3-Stages ECG Real-Time Processing Denoising, Feature Extraction, Classification

5 Conclusion

Electrocardiography (ECG) is a crucial diagnostic tool for identifying irregularities in the heart's electrical activity, which can signify underlying abnormalities in heart function. This paper presented a review of real time ECG signal processing. In general, there are three stages of ECG processing, namely, preprocessing stage, feature extraction stage and classification stage, Most ECG research falls into one or more of the three processing stages outlined in this model. This paper guides researchers through the vast ECG literature, highlighting how signals progress through processing stages and what each stage entails. Our survey compiled a diverse range of

recently published ECG analysis methods, conveniently presented in a table for easy comparison. A striking observation from our survey: the vast majority of researchers leverage the MIT-BIH dataset for evaluating their one-dimensional ECG analysis and classification techniques. This review's insights illuminate the path for future researchers, empowering them to bridge knowledge gaps and conquer challenges in this growing field.

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