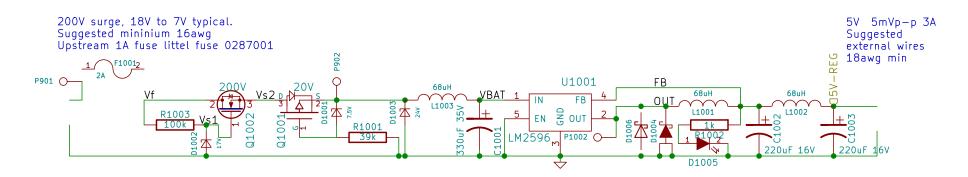
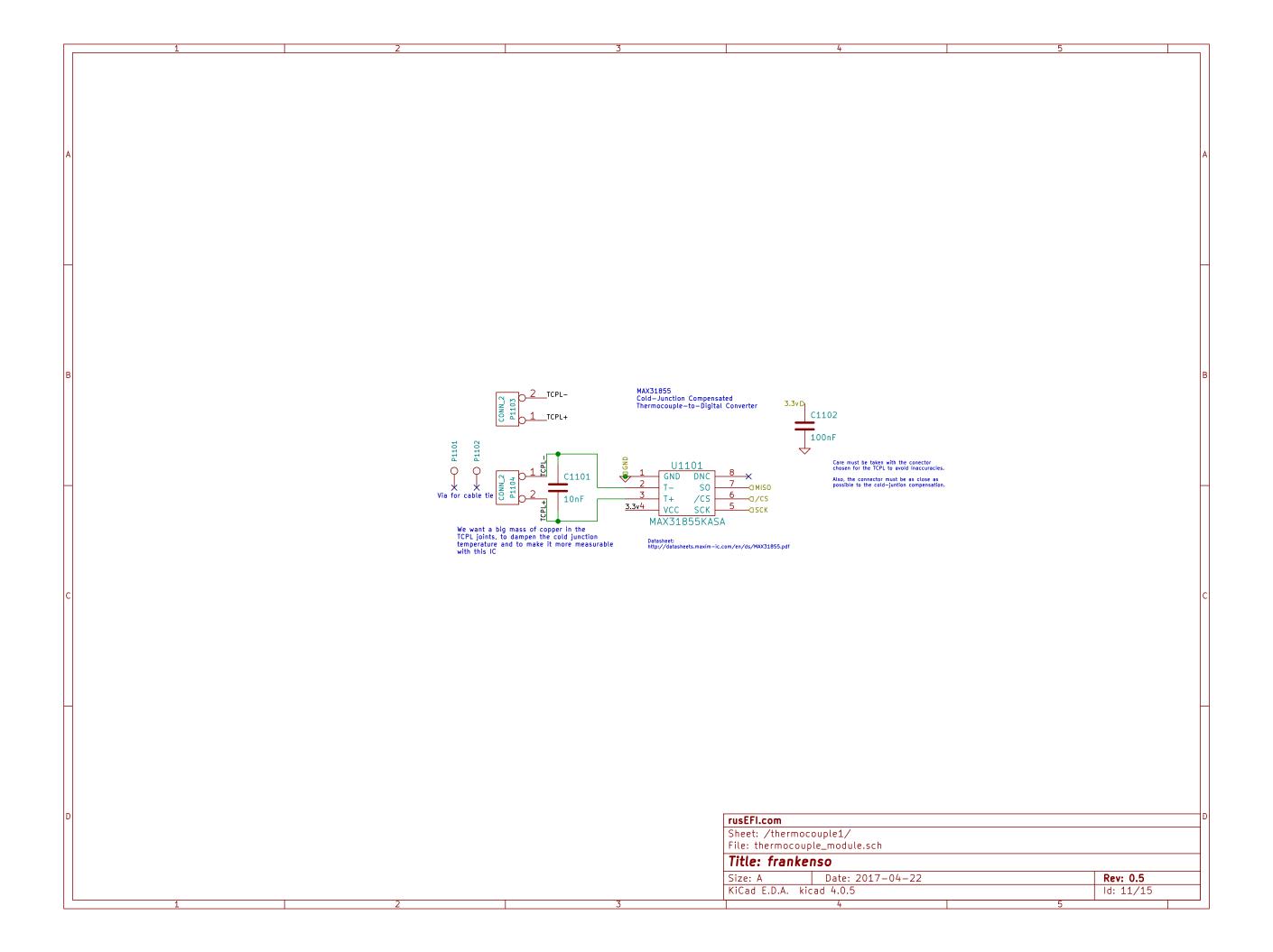


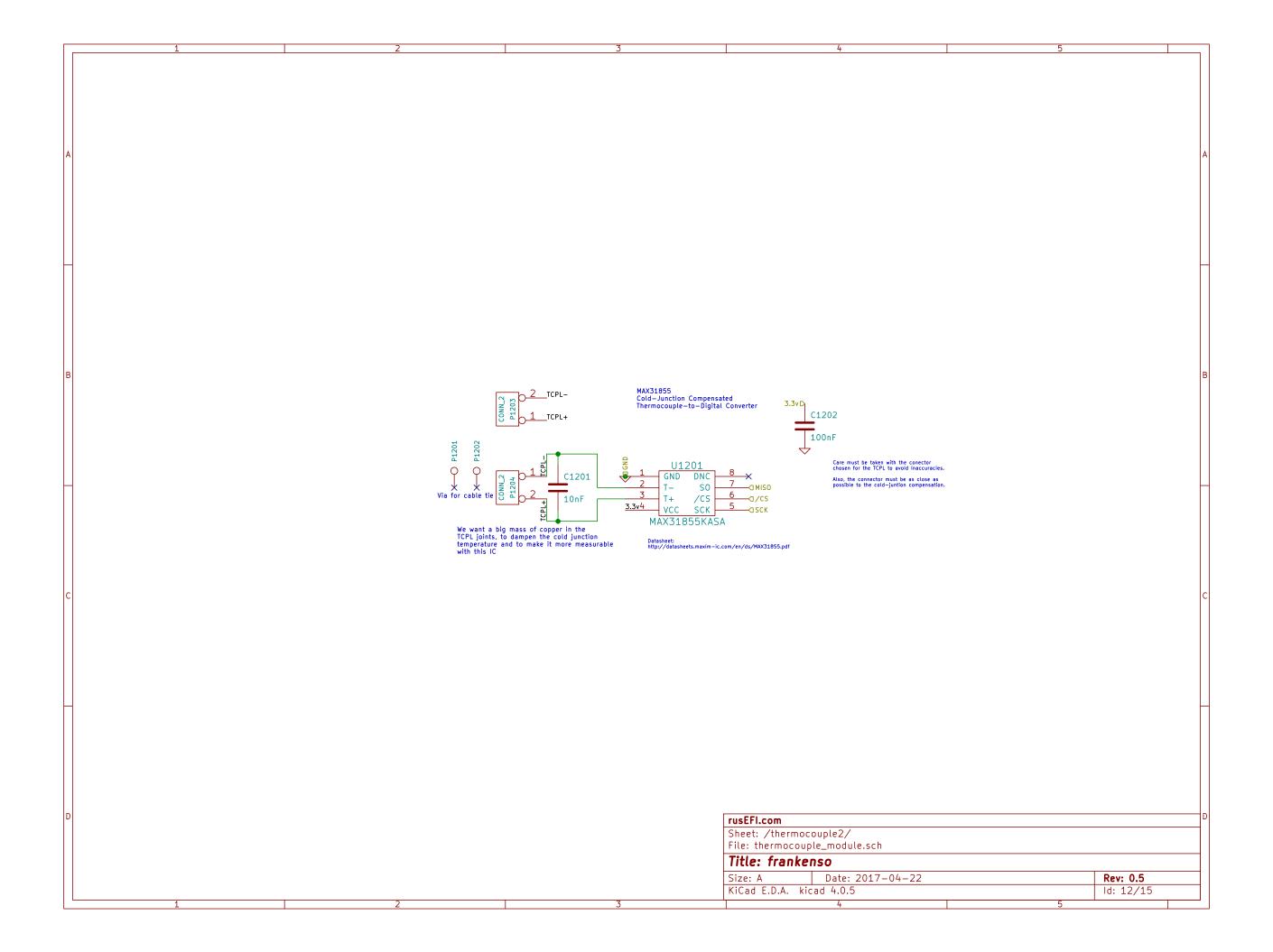
## Brief overview

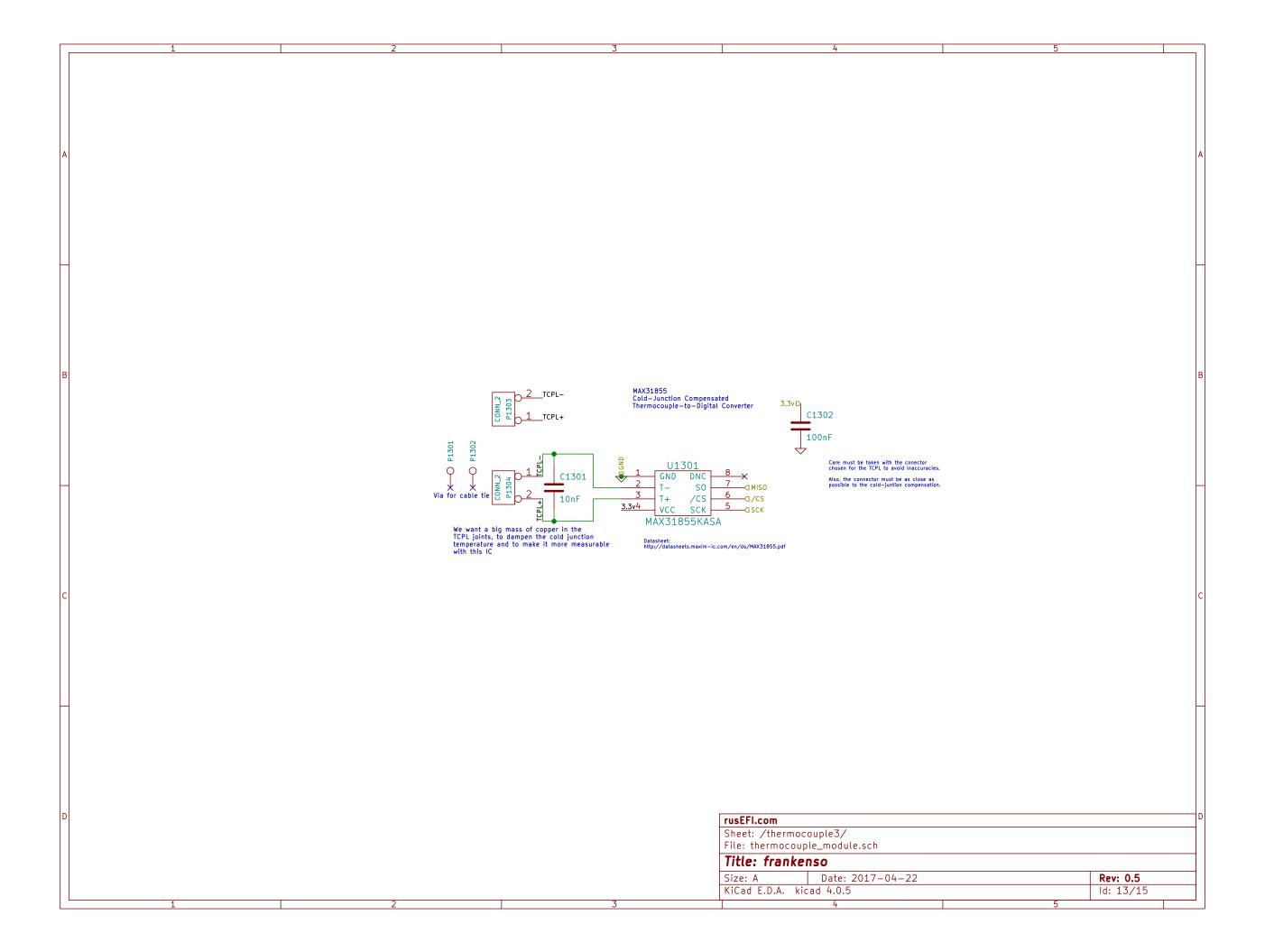
-- Q1002, R1003, D1002 preform an active transient protection. It will suppress voltages up to 200V down to 19V.
-- Q1001, R1001, D1001 preform a reverse polarity protection. If the input signal is the wrong polarity, the gate will not conduct which will prevent current from flowing.
-- D1003 is a second transient suppressor, it would catch faster transients allowing a brief amount of time for Q1002 to preform it's duty.
-- L1003 is a choke, it simple prevents switching noise from going up the power wire where it can get into other circuits.
-- C1001 is a bulk cap, it simply stores energy locally such that the regulator can draw large currents in short periods of time.
-- U1001 and the components to the right, are a buck style switching regulator, that will pull the 5V line up to 5V. It will not pull it down from 5V if there is an external voltage.
The U1001 circuit has been designed for 3A output and up to 20V input, but typically 14.4V or 12.4V input. L1001 wants to be about 68uH to 100uH with less than 0.3 ohms resistance.

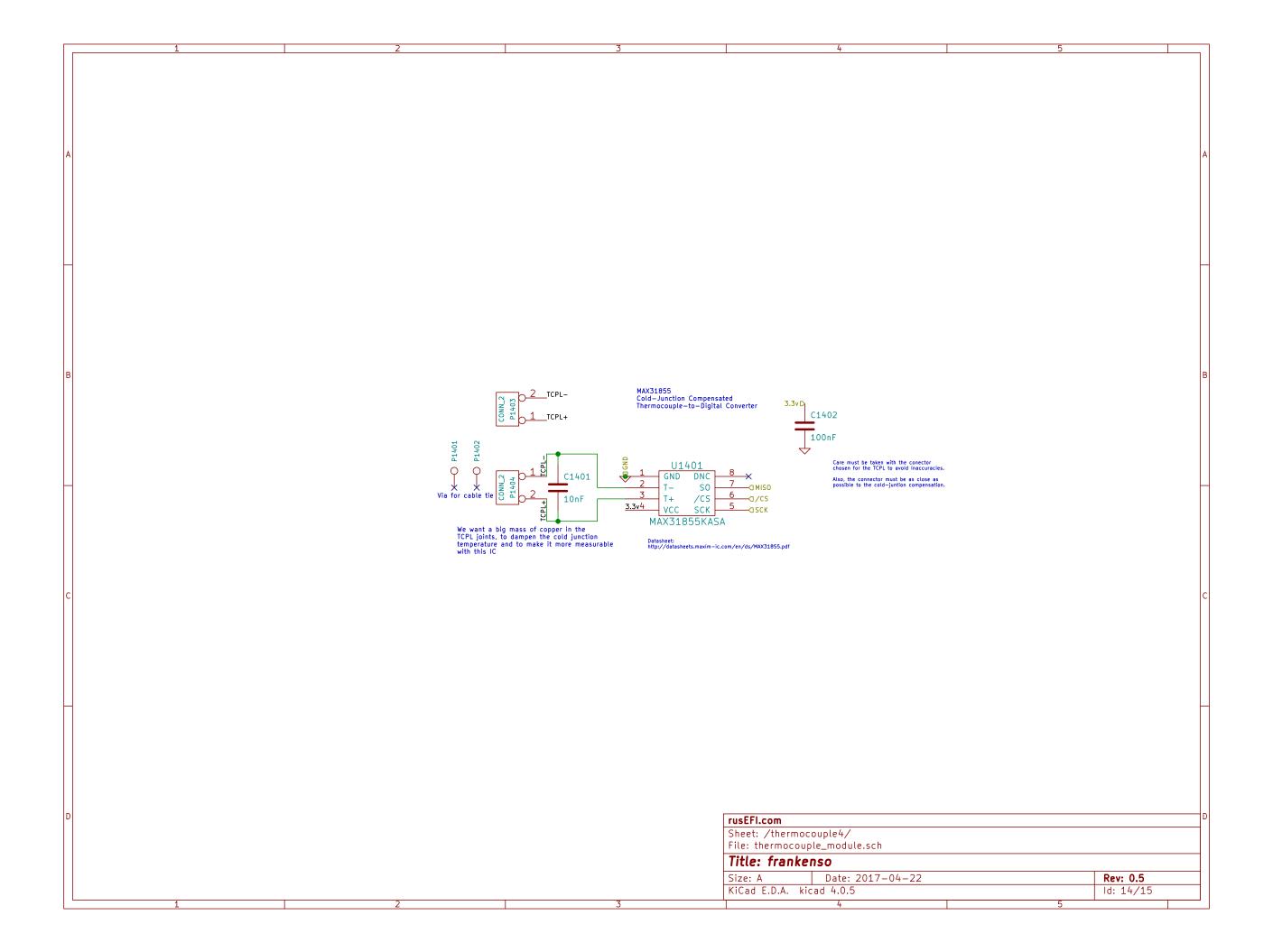


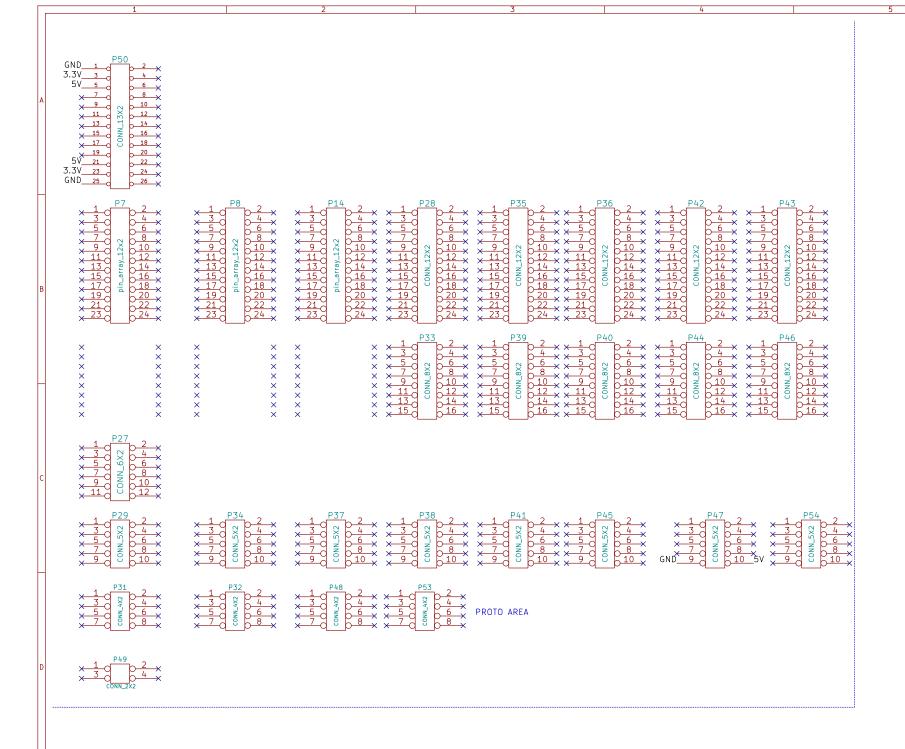
	22 22	11	50	9	
94 BOOTO	YDDA .	QQA	QQA	/BAT	
14 NRST	> >				PE2/TRACECLK/FSMC_A23/ETH_MII_TXD3/EVENTOUT
PHO/OSC_IN/EVENTOUT					PE5/TRACED1/FSMC_A20/DCML_D4/EVENTOUT PE5/TRACED2/FSMC_A21/TIM9_CH1/DCML_D6/EVENTOUT PE6/TRACED3_/FSMC_A22/TIM9_CH2/DCML_D7/EVENTOUT  PE6/TRACED3_/FSMC_A22/TIM9_CH2/DCML_D7/EVENTOUT  9
PH1/OSC_OUT/EVENTOUT					PE9/FSMC_D6/TIM1_CH1/EVENTOUT PE10/FSMC_D7/TIM1_CH2/EVENTOUT 41 PE11/FSMC_D8/TIM1_CH2/EVENTOUT 42 PE12/FSMC_D9/TIM1_CH3/EVENTOUT 43 PE13/FSMC_D10/TIM1_CH3/EVENTOUT PE14/FSMC_D11/TIM1_CH4/EVENTOUT PE15/FSMC_D12/TIM1_BKIN/EVENTOUT 45 PE15/FSMC_D12/TIM1_BKIN/EVENTOUT
23 24 25 26 27 28 29 29 29 20 20 20 20 20 20 20 20 20 20 20 20 20	I_RX_CLK/TIM5_CH2/TIMM2_CH2/ DIO/EVENTOUT	EVENTOUT			PD0/FSMC_D2/CAN1_RX/EVENTOUT   81
30 31 32 67  PA5/SPI1_SCK/OTG_HS_ULPI_CK/TIM2_CH1_ETR/TIM8_CI PA6/SPI1_MISO/TIM8_BKIN/TIM13_CH1/DCMI_PIXCLK/TI PA7/SPI1_MOSI/TIM8_CH1N/TIM14_CH1/TIM3_CH2/ETH_ PA8/MC01/USART1_CK/TIM1_CH1/I2C3_SCL/OTG_FS_SC	M3_CH1/TIM1_BKIN/EVENTOUT MIL RX DV/TIM1 CH1N/RMIL CRS	_DV/EVENTOUT			PD5/FSMC_NUE/USART2_TX/EVENTOUT
70 71 72 72 76 77 78 79 79 79 79 79 79 79 79 79 79 79 79 79	TUOTK				PD10/FSMC_D15/USART3_CK/EVENTOUT  PD13/FSMC_A18/TIM4_CH2/EVENTOUT  PD14/FSMC_D0/TIM4_CH3/EVENTOUT/EVENTOUT  PD15/FSMC_D1/TIM4_CH4/EVENTOUT  62
35 36 37 PB0/TIM3_CH3/TIM8_CH2N/OTG_HS_ULPI_D1/ETH_MII_R) PB1/TIM3_CH4/TIM8_CH3N/OTG_HS_ULPI_D2/ETH_MII_R) PB2/B0011/EVENTOUT		/ENTOUT			PCO/OTG_HS_ULPI_STP/EVENTOUT PC1/ETH_MDC/_EVENTOUT PC2/SPI2_MISO/OTG_HS_ULPI_DIR/ETH_MII_TXD2/I2S2ext_SD/EVENTOUT
90 PB4/NJTRST/SPI3_MISO/TIM3_CH1/SPI1_MISO/I2S3ext_ 91 PB5/I2C1_SMBA/CAN2_RX/OTG_HS_ULPI_D7/ETH_PPS_0 92 PB6/I2C1_SCL/TIM4_CH1/CAN2_TX/DCML_D5/USART1_TX 93 PB7/I2C1_SDA/FSMC_NL/DCML_VSYNC/USART1_RX/TIM5 95 PB8/TIM4_CH3/SDI0_D4/TIM10_CH1/DCML_D6/ETH_MIL_ 96 PB9/SPI2_NSS/I2S2_WS/TIM4_CH4/TIM11_CH1/SDI0_D5 PB10/SPI2_SCK/I2S2_CK/I2C2_SCL/USART3_TX/OTG_HS	UT/TIM3_CH2/SPI1_MOSI/SPI3_M K/EVENTOUT _CH2/EVENTOUT TXD3/I2C1_SCL/CAN1_RX/EVENT 5/DCMI_D7/I2C1_SDA/CAN1_TX/E	DUT EVENTOUT	тоит	PC	PC4/ETH_RMII_RX_D0/ETH_MII_RX_D0/EVENTOUT PC5/ETH_RMII_RX_D1/ETH_MII_RX_D1/EVENTOUT C6/I2S2_MCK/TIM8_CH1/SDI0_D6/USART6_TX/DCML_D0/TIM3_CH1/EVENTOUT C7/I2S3_MCK/TIM8_CH2/SDI0_D7/USART6_RX/DCML_D1/TIM3_CH2/EVENTOUT PC6/TIM8_CH3/SDI0_D0/TIM3_CH3/USART6_CK/DCML_D2/EVENTOUT C5_ C5_CKIN/MC02/TIM8_CH4/SDI0_D1/I2C3_SDA/DCML_D3/TIM3_CH4/EVENTOUT C6_ C6_
51 52 PB12/SPI2_NSS/I2S2_WS/I2C2_SMBA/USART3_CK/TIM1. 52 PB13/SPI2_SCK/I2S2_CK/USART3_CTS/TIM1_CH1N/CAN PB14/SPI2_MISO/TIM1_CH2N/TIM12_CH1/OTG_HS_DM/U PB15/SPI2_MOSI/I2S2_SD/TIM1_CH3N/TIM8_CH3N/TIM1	2_TX/OTG_HS_ULPI_D6/ETH_RMII.  SART3_RTS/TIM8_CH2N/I2S2ext_	TXD1/ETH_MII_TXD1/EVENTOU	Ī	OP TI	12/UART5_TX/SDIO_CK/DCMI_D9/SPI3_MOSI/I2S3_SD/USART3_CK/EVENTOUT

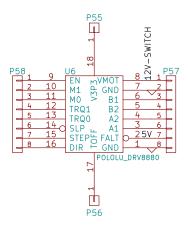


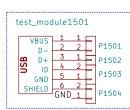












These two jumpers are here to accomodate stm32f4discovery

GND\_OGO\_GND 12V\_SWITCHD\_OGO\_GND 5V
GND\_OGO\_GND GND\_OGO\_GND 3.3VD\_OGO\_3.3V

That's alternative signal OUTPUT — these traces

That's alternative signal OUTPUT — these traces should be routable to PC6 and PA5 via jumpers. Aleternative to W212 and W212 routung of op—amps ch 11 and ch 12

CRANKD—ODO CAM

See below links about barriers in GND planes. The current loops in the layout do not appear to need barriers.

http://rusefi.com/wiki/index.php?title=Manual:Hardware:PCB\_design\_rules http://www.maximintegrated.com/en/app-notes/index.mvp/id/5450

rusEFI.com					
Sheet: /Misc_Vias/					
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