EASIROC User's Guide

December 10, 2019

1 About EASIROC

We can construct a tightly integrated detector with monolithic MPPC array. However, to cover the large area of the detector, we need to handle large amount of MPPCs. MPPCs on the single monolithic MPPS array have different break down voltage and gain, thus it is necessary to adjust the operation voltage for each MPPC.
To much these needs, KEK and openIt developed EASIROC board (GN-1101-1,GN-1101-2R) in 2013. This chip has some characteristics listed below:

- Readout 32 channels simultaneously
- Take positive voltage as input, amplifying, shaping output positive voltage
- Adjust bias voltage by 8 bit (0-4.5 V)
- Have discriminator in it
- Set parameters through slow control
- Cover the dynamics of 160 fC - 320 pC as input charge (this corresponds to 1-2000 p.e. with the assumption that MPPC's gain is 10^6)

University of Tokyo upgraded the EASIROC for the use of MPPC mass test for WAGASCI experiment and attached the function for scaler and TDC information.

2 Internal Operation of EASIROC

The board has 2 EASIROC chips and can read out 64 channels at the same time at maximum. The analog signals from EASIROC chips are converted to digital signal with 4 ADC. Discriminator output is sent to MHTDC and Scaler, then transported to data taking PC (DAC) through Gatherer, Sender, SiTCP.
DAC and EASIROC board are connected with Ethernet cable. The board's operation voltage is +6 V and it can be supplied from NIM crate.

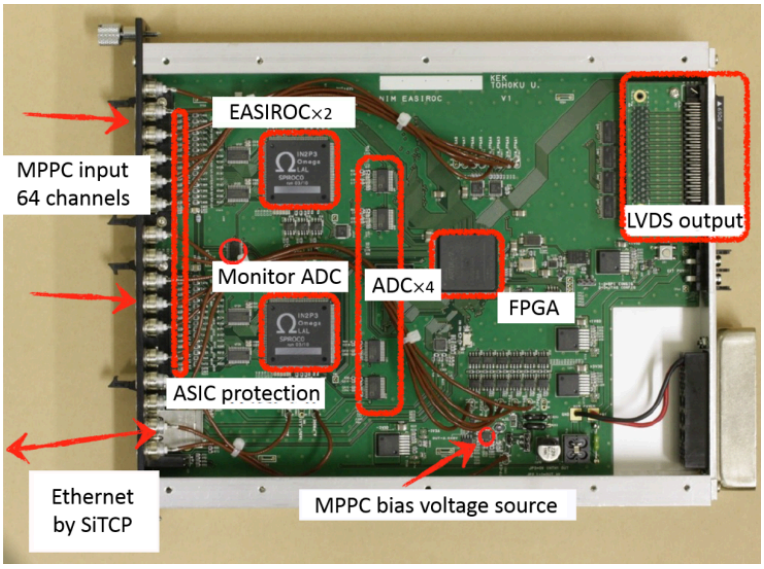

Figure 1: Side-view of NIM-EASIROC board

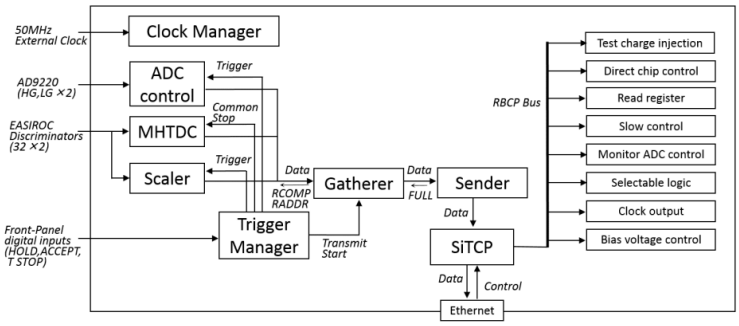

Figure 2: Circuit diagram of NIM-EASIROC board

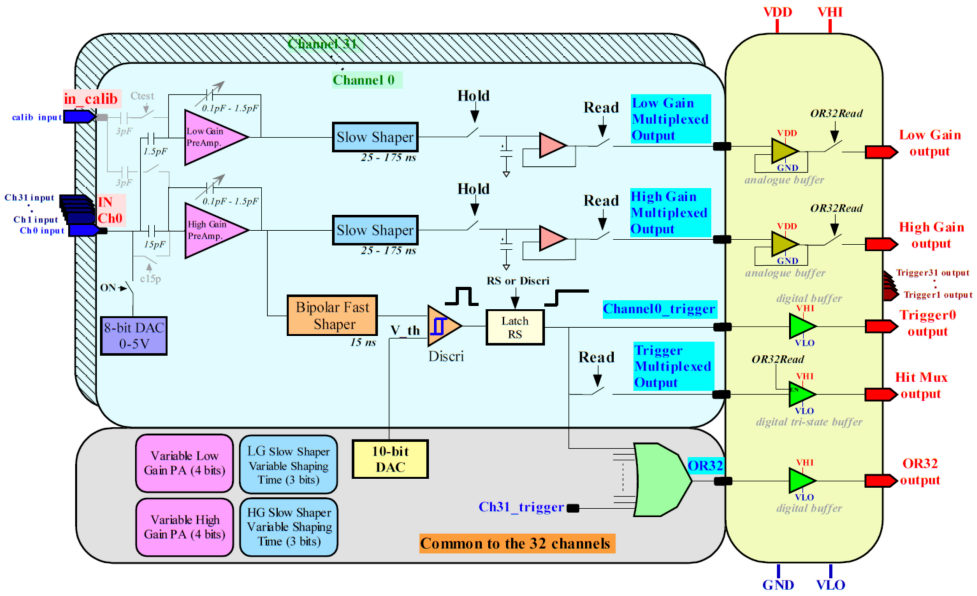

Figure 3: Diagram of EASIROC chip

The way of converting the analog signal to the digital one is like this:

1. Integrate and amplify the charge by pre-amplifier which has two types of gain (low and high).
2. Send the pre-amplifier output to fast-shaper and slow-shaper.
3. Signal sent to the fast-shaper is shaped with the time constant 15 ns and converted to the digital signal if it is over the threshold of discriminator.
4. Signal sent to the slow-shaper is shaped with the time constant 25-175 ns and recorded its voltage value when it get HOLD signal.

3 How to Use EASIROC

3.1 Trigger signals

Basically, only external trigger can be used. When you want to use self trigger, use output signals with appropriate delay. In that case, you should enter the signal with the order; "HOLD", "T STOP", "ACCEPT". You should insert more than about 2 us between HOLD and ACCEPT. It depends on ADC converting rate but 2.5 us is maybe enough.

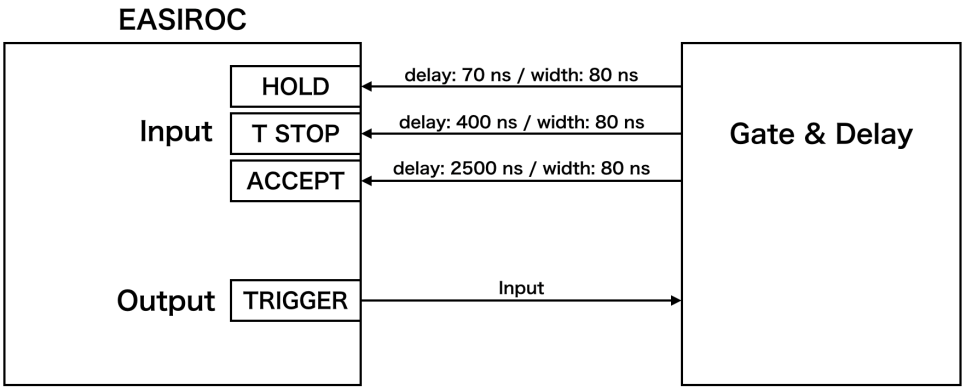

Figure 4: An example of self trigger circuit[1]

Figure 5: The front panel of EASIROC board

3.2 Interactive mode

EASIROC has an inner read line so you can handle EASIROC module interactively.

3.2.1 Handle interactive mode

Start interactive mode.

```
$ ./Controller.rb [IP Address (default: 192.168.10.16)]
```

Stop interactive mode.

```
> exit [quit]
```

3.2.2 Set bias voltage

Print the voltage and current value of HV.

```
> statusHV
```

Set the HV at the value of [bias voltage].

```
> setHV [bias voltage]
```

Increase HV with some steps. In each step, check the current and stop if it reaches to the limit.

```
> increaseHV [bias voltage]
```

3.2.3 Data taking

Reset the slow control values.

```
> slowcontrol
```

Start data aquisition.

```
> read [Event #] [Filename]
```

ON/OFF the ADC [TDC/Scaler].

```
> adc [on/off]
> tdc [on/off]
> scaler [on/off]
```

It makes data taking faster if you off the ADC [TDC/Scaler] when you don't need them.

3.2.4 Other information

- 対話時に入力されたコマンドは CommandDispatcher クラスによって処理される
- 対話モードで help と入力してヘルプが見られる
- 各コマンドは変数 COMMANDS に含まれているものが利用可能で、それぞれのコマンドはメソッドによって処理される
- シェルのコマンドも一部使えるようになっている (ex. ls, mv, root)
- それらは変数 DIRECT_COMMANDS に含まれているものが利用可能
- Controller ディレクトリ内で hist.cc を make してプログラムを生成していれば、read 終了後に自動でヒストグラムを生成する。出力先は Controller/data ディレクトリ内。

3.3 Slow Controll

Slow Controll は yaml ディレクトリ下の YAML ファイル（拡張子：yml）によって指定される。
YAML は構造化されたデータを表現するフォーマットで、XML と似ているが YAML の方が人間にとって理解しやすい形式になっている。よく使いそうなものを以下に紹介する。

3.3.1 RegisterValue.yml

```
EASIROC1:  # Set for each chip
         Capacitor HG PA Fdbck: 100fF  # Define amplifying level. Capacitor values
         Capacitor LG PA Fdbck: 100fF  # are contained in RegisterValueAlias.yml
         Time Constant HG Shaper: 100ns  # Time constant of slow-shaper
         Time Constant LG Shaper: 50ns
         DAC code: 600  # Threshold of the discriminator after fast-shaper

EASIROC2:
         Capacitor HG PA Fdbck: same
         Capacitor LG PA Fdbck: same
         Time Constant HG Shaper: same
         Time Constant LG Shaper: same
         DAC code: same

High Gain Channel 1: 0   # Read out channel from HG1/HG2
High Gain Channel 2: -1  # 0 : read out || 1 : not read out
Probe Channel 1: -1      # Output from the probe of front panel
Probe Channel 2: -1
Probe 1: Out_fs
Probe 2: Out_fs  # Out_PA_HG, Out_PA_LG, Out_ssh_HG, Out_ssh_LG, Out_fs
SelectableLogic:
         Pattern: Or64        # OneCh_#, Or32u, Or32d, Or64, Or32And,...
         HitNum Threshold: 4  # Threshold for each OR logic. 0~64. Default: 0
         And Channels: -1     # Cannels used in And Logic. 0~63. Default: -1
TimeWindow: 4095ns
UsrClkOut: "OFF"  # Periodic signal from syn out of front panel # "ON", 1Hz,...
Trigger:          ## This "Trigger" values are not used for this version.
         Mode: 0  #0-7
         DelayTrigger: -1   #500MHz #default:-1, 0-253 #trig -> hold -> l1 -> l2
         DelayHold: -1      #25MHz
         DelayL1Trig: -1    #6MHz
         Width: raw
```

When increase the DAC of discriminator, threshold get lower.

3.3.2 InputDAC.yml

There written the 8-bit Input DAC values for 32 channels by chip. They can be changed between 256-511 (The top bit is always set to 1 (=enable)).
When increase the DAC value, bias voltage get lower.

```
---
EASIROC1:
  Input 8-bit DAC:
  - 350
  - 350
  - 350
  - 350
  - 350
  - 350
  - 350
  - 350
```

3.3.3 Calibration.yml

```
HVControl:   # Coefficient for converting the HV into DAC
        - 413.9 #423.06 #483.183
        - 747.8 #767.17 #780.0
MonitorADC:  # Coefficient for converting Monitor ADC values
             # into voltage, current and temperature
        HV: 0.00208 #0.3235 #0.00208
        HVOffset: 0.0355 #4.1694
        Current: 0.0364 #0.034
        InputDac: 0.00006866 #4.5/2^16 #0.0000685
        Temperature: 4500.0
```

3.4 Other information

3.4.1 Probe output

信号処理中の中間信号を取り出すための Probe 出力ラインがフロントパネルに用意されている。出力することができる中間信号を以下に示す。

- HighGain PreAmp 出力
- LowGain PreAmp 出力
- HighGain Slow shaper 出力
- LowGain Slow shaper 出力
- Fast shaper

前述の RegisterValue.yml から出力する情報を指定することができる。

PreAmp を選択した場合、波形全体ではなくピーク付近の一部のみ出力される。注意点としては、2 ch 以上を同時に ON にしない、データ取得中は Probe 1,2 を OFF にすること。

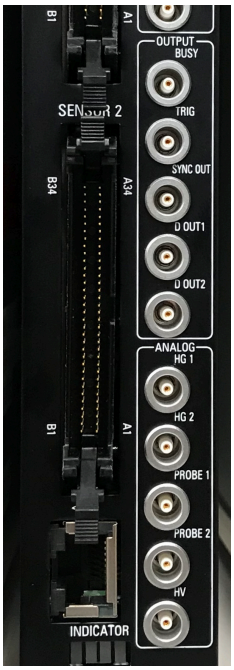

Figure 6: フロントパネルの Probe 出力

```
High Gain Channel 1: 0   # HG で読み出すチャンネルの指定
High Gain Channel 2: -1  # 読み出すなら ch_#、読み出さないなら-1
Probe Channel 1: -1      # Probe からの出力チャンネル選択
Probe Channel 2: -1      # 2 ch 以上同時に使用しない
Probe 1: Out_PA_HG
Probe 2: Out_fs  # Out_PA_HG, Out_PA_LG, Out_ssh_HG, Out_ssh_LG, Out_fs
```

また、SYNC OUT からの周期信号も RegisterValue.yml より変更が可能である。

```
UsrClkOut: "OFF"  # "OFF", "ON", 1Hz, 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, 3MHz, ...
```

3.4.2 Yokoyama-lab's EASIROCs

2019 年 5 月 9 日現在、5 つの EASIROC ボードの存在が確認された。うち一つは京大高エネルギー研究室の備品と思われる。IP アドレスは DAC との接続の際に必要となる。

Table 1: 横山研所有の EASIROC

管理 No.	IP Adress	備考
1	192.168.10.11	
2	192.168.10.12	
3	192.168.10.13	
2 号	192.168.10.18	ch.32 の読み出し不調。バイアス HV にふらつきあり。
京大高エネ備品	不明	後半 32ch の InputDAC が動かない。連絡先：075-753-3837。

4 References

1,2,3 は EASIROC 開発時の資料、4,5 はアップグレード後の資料である。

1. OpenIt のサイト
   http://openit.kek.jp/project/MPPC-Readout-Module/public/MPPC-Readout-Module
2. 石島さんの修論
   http://osksn2.hep.sci.osaka-u.ac.jp/theses/master/2013/ishijima_mthesis.pdf
3. 塩崎さんの修論
   http://lambda.phys.tohoku.ac.jp/~db/human_resource/thesis/2009_B_2_M_1.pdf
4. 竹馬さんのマニュアル
   http://hep.phys.s.u-tokyo.ac.jp/~nchikuma/easiroc_manual.html
5. 竹馬さんの修論
   http://hep.phys.s.u-tokyo.ac.jp/wordpress/wp-content/uploads/2016/06/mth2016_chikuma.pdf