Radstone PME 68-14

# Instrumentation Single Board Computer (SBC)

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# PME 68-14
# Manual

## Issue 4

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## Board Identification

Radstone PME boards can be identified by a label fitted to the component side of Connector P1.

| MADE IN ENGLAND | | SERIAL NUMBER | REV NO. |
|---|---|---|---|
| | | | |

**Revision number, e.g. C or 2F, revision 1 number is not shown**

**Unique board serial number**

**Drawing list number, used during manufacture**

**Part/variant number, all PME board numbers begin with 421/1/ so this is not shown**

This publication describes the PME 68-14 at Rev 3 (all letter codes).

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## Chapter 3 - Technical Description

# Chapter 1 - Introduction

This manual describes the Radstone PME 68-14 Instrumentation Single Board Computer (SBC). It also includes configuration and installation details. Throughout the manual, signals marked '*' are active LOW, eg RESET*. Where hexadecimal numbers are used, they are preceded with a dollar sign ($), eg $FFEE.

## Overview

The PME 68-14 is a high performance, VMEbus compatible processor board that features an IEEE 488, General Purpose Interface Bus (GPIB) interface.

The IEEE 488 interface, originally developed by Hewlett-Packard, was designed to connect programmable devices to computer systems. It was adopted by the Institute of Electrical and Electronic Engineers (IEEE) in 1975, and is now the accepted standard for interfacing and controlling instrumentation. Very few existing IEEE 488 interface boards offer on-board intelligence and consequently a separate processor board is required to control data flow through the interface.

The PME 68-14, however, provides real on board intelligence for control of its own IEEE 488 interface. It can be used as a high-performance SBC or as a system controller in a multi-processor system. Access to on-board devices is through an EPROM resident Monitor. This powerful software package may be used for program development and debugging, and provides boot-up routines for all on board devices. The Monitor is fully described in a separate publication: Radstone Universal Monitor (PLUM), Firmware Reference Manual, 651/HH/19050.

## Variants

PME 68-14 has several variants according to the choice of processor, dual port RAM and interface; current variants are:

| Product Code | Part Number | Board Type |
|---|---|---|
| PME 68-14/100 | 421/1/23852/100 | 10 MHz 68000, 512 kbyte DRAM |
| PME 68-14/101 | 421/1/23852/101 | 10 MHz 68010, 512 kbyte DRAM |
| PME 68-14M/102 | 421/1/23941/102 | 10 MHz 68000, 2 Mbyte DRAM |
| PME 68-14M/103 | 421/1/23941/103 | 10 MHz 68010, 2 Mbyte DRAM |

The above variants all contain RS 232C drivers; the following variants all contain RS 422A drivers:

| | | |
|---|---|---|
| PME 68-14/400 | 421/1/23852/400 | 10 MHz 68000, 512 kbyte DRAM |
| PME 68-14/401 | 421/1/23852/401 | 10 MHz 68010, 512 kbyte DRAM |
| PME 68-14M/402 | 421/1/23941/402 | 10 MHz 68000, 2 Mbyte DRAM |
| PME 68-14M/403 | 421/1/23941/403 | 10 MHz 68010, 2 Mbyte DRAM |

Full details of on-board devices are contained in the relevant manufacturers' data sheets, available from your supplier.

**PME 68-14**

# Main Features of the PME 68-14

- High performance VMEbus Single Board Computer
- Choice of 68000 or 68010 processor running at 10 MHz
- System Controller functions

  4 level Arbiter using RRS, PRI, or single level (link-selectable BCLR* option)
  SYSCLK driver module
  Bus Timeout module
  IACK* daisy-chain driver module

- Other VMEbus functions

  VMEbus Requester with ROR and early BBSY* release
  Interrupt Generator on any level (software-selectable)
  Interrupt Handler for any/all levels (software-selectable)
  SYSRESET* sensing and driving
  SYSFAIL* sensing and driving
  ACFAIL* sensing

- Dual Port RAM

  512 kbyte or 2 Mbyte of dual-ported RAM organised as
  256k x 16 or 1M x 16 bits
  1 wait state for internal access
  Mailbox interrupt

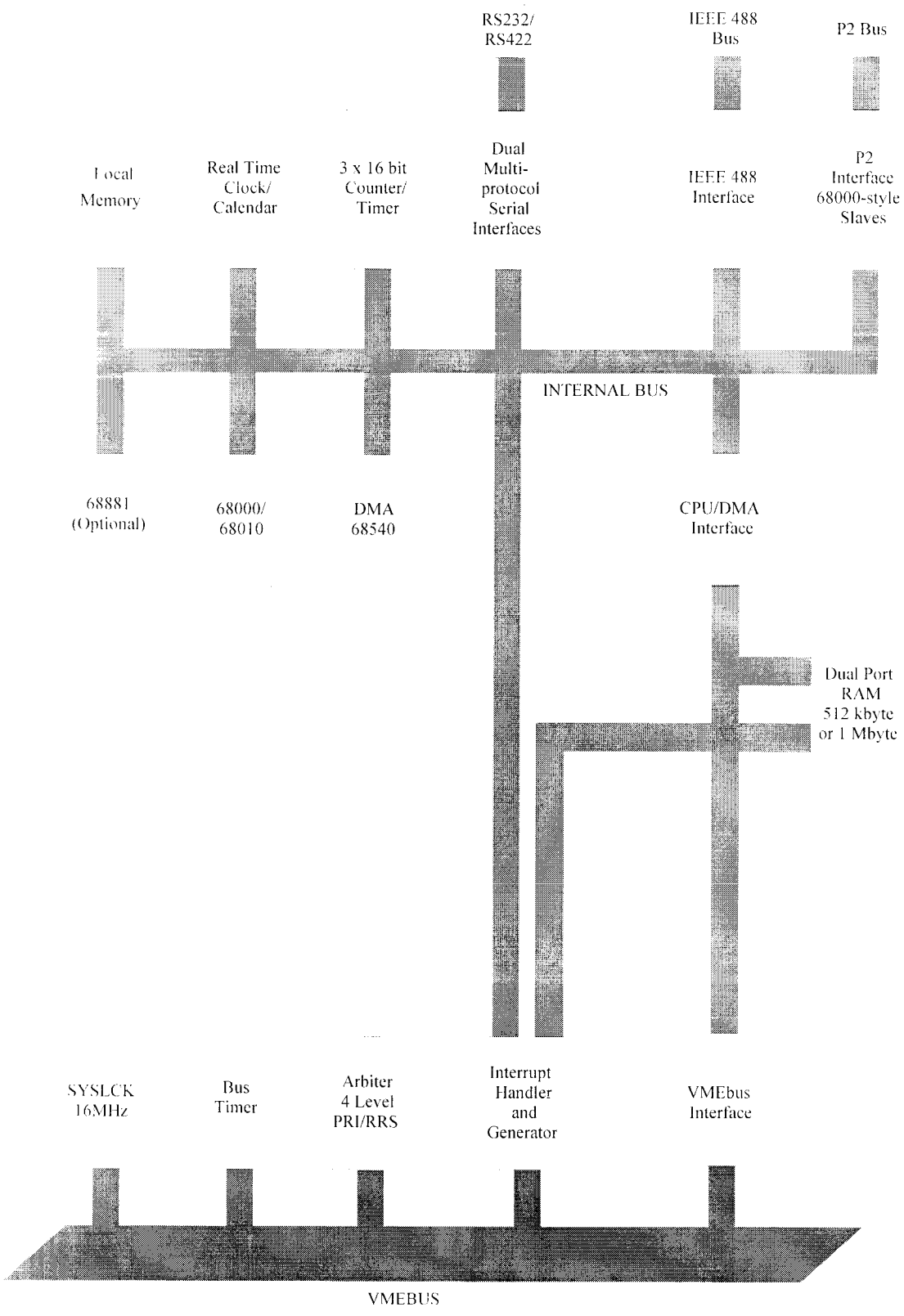
- Local resources

  IEEE 488 interface (TMS9914A, 75160, 75162)
  68450 DMA Controller
  Up to 4 Mbytes of Local Memory in 4 x 32 pin JEDEC sockets
  3 x 16 bit counter/timers (68B40)
  Dual synchronous/asynchronous multi-protocol serial interfaces
  with RS 232C or RS 422A (68562)

  Real Time Clock (MSM6242)
  68000 style slave interface on P2
  16 bit status register containing IEEE 488 address and user-selectable code

  Extended Address register to give A32 master capability
  Front panel status LED (software controlled)

## Block Diagram of PME 68-14



# Functional Overview

The PME 68-14 provides an intelligent IEEE 488 interface with full talker, listener and controller functions. Data is transferred at speeds of up to 500k bytes per second. The full interrupt handling capability and the dual-ported RAM make the board ideal for high performance VMEbus multi-master systems. Equally, the on-board functions allow use as a powerful single board system.

## Processor

The board can be supplied with either a 68000 or 68010 processor running at 10MHz. The processor is housed in a 64 pin dual in-line package.

## DMA Controller

The controller used is a 68450 DMAC giving four DMA channels. It is housed in a 64 pin dual-in-line package.

The channels are allocated as follows:

| | |
|---|---|
| Channel 0 | IEEE 488 interface |
| Channel 1 | Channel A of the DUSCC in half-duplex |
| Channel 2 | Link-selectable between:<br>Channel A of the DUSCC in full-duplex<br>Channel B of the DUSCC in half-duplex<br>P2 interface |
| Channel 3 | P2 interface |

Any of the four channels may be used for memory to memory transfers between local memory and the Dual Port RAM, local memory and the VMEbus, and Dual Port RAM and the VMEbus.

## Serial Interface

The 68562 DUSCC provides two independant serial channels that may operate in either synchronous or asynchronous mode. In asynchronous mode, rates of up to 38400 baud may be used with character lengths of 5 to 8 bits.

Other options include:

Odd/even/no parity
Up to 2 stop bits in 1/16 bit increments
Parity/overrun/framing error detection
False start bit detection
Start and end break detection
Character compare with optional interrupt on match

In synchronous mode, character and bit-orientated protocols are supported with data transfer rates of up to 4 Mbits per second. Character-orientated protocols include BISYNC and DDCMP. Bit-orientated protocols include HDLC, SDLC and X.25.

In both synchronous and asynchronous modes, either channel can be programmed for full or half duplex, local loopback and various data encoding options including NRZ, NRZI, FM0, FM1 and Manchester. A DPLL ensures reliable reception of incoming data. Both channels are fed through RS 232C or RS 422A transmitters and receivers. Two 9 way 'D' type connectors are provided on the front panel for connection to the serial channels.

## IEEE 488 Interface

The PME 68-14 contains an IEEE 488 interface to handle all functions defined in the 1975/78 specification and is compatible with IEEE 488A 1980 supplement. It provides full talker and listener functions (T, TE, L, LE), and automatic source and acceptor handshakes (SH, AH). It also has System Controller capabilities.

Data transfer rates of up to 500 kbytes per second are possible.

The IEEE 488 interface is brought out to a connector on the front panel.

## Counter/Timers

The 68B40 device contains three independant 16 bit counter/timers and can be programmed to interrupt on certain conditions. The interrupt is taken to Level 6 of the Interrupt Handler, to enable 'ticks' or 'heartbeats' for operating systems to be accurately maintained.

## Real Time Clock

The Real Time Clock (RTC) is powered from + 5V or + 5VSTDBY. The change to + 5V STDBY occurs automatically on a power failure. No on-board battery is provided.

The RTC is programmed to supply year, month, date, day of the week, hours, minutes and seconds. It has the option of a 12 or 24 hour format display, and automatic allowance for leap years.

An output, selectable between 1/64 second, 1 second, 1 minute and 1 hour is provided by the RTC. This output is available to the counter timer and may be used in control applications for process timing or scheduling, with minimal use of the CPU.

## P2 Interface

This is a 68000 style interface connected via a buffer to the CPU Local Bus. It is intended for Slave functions that the user may wish to implement to enhance the system performance. It is provided with a Level 1 interrupt and two DMA channels.

## Local Memory

The PME 68-14 contains four 32 pin JEDEC compatible mounting sites. These are arranged as two blocks, each 16 bits wide. Both blocks are powered from + 5V or + 5VSTDBY. Block 0 is decoded for devices up to 1 Mbyte, and Block 1 is decoded for devices up to 512 kbytes. Each block can be fitted with either EPROM, EEPROM or SRAM.

## Dual Port RAM

The Dual Port RAM (DPR) size is either 512 kbytes arranged as 256k x 16 bit or 2 Mbytes arranged as 1M x 16 bits.

The CPU Exception Vector tables reside at the bottom of the DPR, so VMEbus access is denied in this area. A VMEbus access to the 32 byte area above generates an on-board interrupt, thus providing an efficient means of multi-processor communications.

The DPR, as addressed by the VMEbus, may be anywhere within the full 4 Gbyte VMEbus address map, on 512 kbyte or 2 Mbyte boundaries, dependent on the size of the memory fitted.

## Interrupt Handler

The Interrupt Handler (IVHAN) provides the PME 68-14 with full interrupt handling capabilities. It sets the priorities on VMEbus interrupts, up to six local interrupts, and one non-maskable interrupt, thus providing the CPU with the appropriate interrupt level code.

Internal interrupts can be generated by any of: the Abort switch, the counter/timers, ACFAIL*, SYSFAIL*, the IEEE 488 interface, the DUSCC, the DMA controller, the Dual Port RAM or via the P2 interface. In cases where the interrupting device is unable to provide an interrupt vector, the Interrupt Handler will do so in lieu.

Interrupt masking is implemented under software control.

## Interrupt Generator

The Interrupt Generator (IGOR) places an interrupt on the VMEbus and then provides a user-programmable status/ID byte in response to the Interrupt Acknowledge. The level of interrupt is software controlled. The Interrupt Generator device also contains the IACK* daisy-chain driver module.

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# Chapter 2 - Specification

## General Specification

| | |
|---|---|
| **VMEbus Compliance** | Fully compatible with ANSI/IEEE std. 1014-1987 |
| **Data Transfer Bus** | A32:D16:RMW, A24:D16:RMW as Bus Master/Slave<br>A32:D16:BLT, A24:D16:BLT Bus Master |
| **Requester** | ROR, Early BBSY* release |
| **Interrupt Handler** | IH(1-7):D08(O)<br>Any interrupt level software maskable |
| **Interrupt Generator** | I(1-7);D08(O):ROAK<br>Interrupt level is software selectable |
| **System Controller** | PRI, RRS or SGL Arbiter<br>BTO(x) Bus Timer (0.8µs to 6554µs). |
| **Processor** | 68000 or 68010 operating at 10MHz |
| **Local Memory** | Two 27512 (128 kbyte) EPROMs containing Monitor and boot firmware. Expandable to 2 Mbyte firmware. Additional 32 pin sites for up to 1 Mbyte EPROM, EEPROM or SRAM. |
| **Dual Port RAM** | 512 kbytes or 2 Mbytes of dual-ported DRAM, organised as 256k x 16 bit or 1M x 16 bit. 1 wait state on local accesses. |
| **DMA** | 68540 DMA Controller with four channels.<br>Channel 0 is dedicated to the IEEE 488 interface<br>Channel 1 is dedicated to serial interface Channel A Rx/Tx<br>Channel 2 is link selectable between: Channel A Rx<br>Channel B Tx/Rx<br>P2 Interface<br>Channel 3 is dedicated to the P2 interface<br><br>Any of the four channels can be used for memory to memory transfers. |

*continued*

| | |
|---|---|
| **Serial I/O** | 68562 DUSCC with two independent channels.<br>Synchronous/asynchronous operation (software and link-selectable options)<br>Asynchronous operation, 16 rates from 50 to 38.4 kbaud.<br>BREAK start and end detect.<br>Synchronous BOP or COP operation, generation and checking.<br>RS 232C or RS 422A interface, hardware selectable. |
| **IEEE 488 Interface** | TMS9914A device. Conforms to IEEE 488 1975/78 standards and IEEE 488A 1980 supplement. Full Talker, Listener and Controller capability. |
| **Counter/Timers** | 68B40 PTM device with three, 16-bit timers.<br>Timer 1 is clocked at 250kHz<br>Timer 2 and 3 clocks are link selectable between 250kHz, previous stage output and RTC output. |
| **Real Time Clock** | MSM6242 device. Year, month, date, hour, minute, second and day of the week output.<br>12/24 hour display.<br>Automatic leap year compensation.<br>1/64 second, 1 second, 1 minute or 1 hour output fed to PTM. |
| **P2 Interface** | Buffered, 68000-style interface with two DMA channels and one interrupt level. |
| **Front Panel** | Single width containing: RESET switch, ABORT switch, RUN LED, user LED, 2 × 9-way 'D' type connectors and an IEEE 488 connector. |
| **Supply Voltages** | + 5V + 5%<br>+ 12V + 5%<br>-12V + 5% |
| **Power** | 24W (typical), 39W (maximum at maximum supply voltage) |
| **Weight** | 0.6kg 1.32 lb. |

# Operating Environment

The PME 68-14 will operate under the following conditions:

| | |
|---|---|
| **Temperature Range** | 0 to + 55°C ambient. |
| **Cooling Requirement** | A linear airflow of not less than 500 ft./min across each card is recommended. |
| **Relative Humidity** | Up to 95% without condensation. |
| **Thermal Shock** | ± 5°C per minute. |
| **Altitude** | -300 to + 3000 metres (1,000 to 10,000 ft. approx.) |
| **Vibration** | 5 to 100 Hz with 2.0g acceleration. |
| **Mechanical Shock** | 20g for 6ms (half sine), mounted in a suitable racking system. |

# Storage Environment

The PME 68-14 may be stored or transported without damage within the following limitations:

| | |
|---|---|
| **Temperature Range** | -55 to + 85°C. |
| **Relative Humidity** | Up to 95% without condensation. |
| **Thermal Shock** | ± 10°C per minute. |
| **Altitude** | -300 to + 16000 metres. (-1,000 to 50,000 ft. approx.) |
| **Vibration** | 5 to 500 Hz with 2g acceleration. |
| **Mechanical Shock** | 20g for 6ms (half sine). |

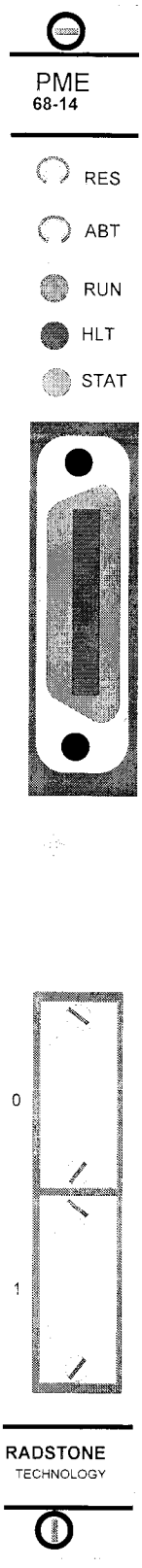
# Mean Time Between Failures (MTBF)

The calculated MTBF figure for PME 68-14 is 68,027 hours. The failure rates used in this calculation are based on a combination of British Telecom HRD3, MIL HDBK 217D and Radstone in-house data. See Appendix D for the figures and calculations.

# Mechanical Construction

The PME 68-14 is constructed on a multi-layer printed circuit board, the dimensions of which conform to the double Eurocard standard. Some components are double stacked.

## PME 68-14 Front Panel Layout



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# Chapter 3 - Technical Description

This chapter describes the features and functions of the PME 68-14 in greater detail.

## Processor

The 68000 processor provides a 16 Mbyte direct addressing range via a 24 bit address bus. It contains eight 32 bit data registers, seven 32 bit address registers and a 16 bit status register. The processor has fifty-six distinct instruction types with fourteen addressing modes and five data types including bit, BCD (Binary Coded Decimal), byte (8 bit), word (16 bit) and longword (32 bit). The PME 68-14 is a D16 VMEbus device and so will not perform 32 bit data transfers.

The 68010 processor is similar to the 68000 but has fifty-seven instruction types including high performance looping instructions. It also contains additional registers.

The processor has access to all on-board devices and to the VMEbus. The address map is shown overleaf.

### Function Codes

The processor generates three function code signals on each cycle to indicate the state of the processor (ie User or Supervisor mode) and the cycle type (Data/Program access or Interrupt Acknowledge). The function codes are used in the generation of Address Modifier codes for the VMEbus. The DMA controller can also provide these function codes.

The following function codes can be generated:

| FC2 | FC1 | FC0 | Cycle Type |
|---|---|---|---|
| Low | Low | Low | Reserved |
| Low | Low | High | User Data Transfer |
| Low | High | Low | User Program Transfer |
| Low | High | High | Reserved |
| High | Low | Low | Reserved |
| High | Low | High | Supervisor Data Transfer |
| High | High | Low | Supervisor Program Transfer |
| High | High | High | CPU Space Cycle |

# PME 68-14 Address Map

| 512 kbytes Dual Port RAM | Address Function | 2 Mbytes Dual Port RAM |
|---|---|---|
| FF0000 to FFFFFF | Global Short Address | FF0000 to FFFFFF |
| FEFF00 to FEFFFF | Counter/Timers | FEFF00 to FEFFFF |
| FEFE00 to FEFEFF | Real Time Clock | FEFE00 to FEFEFF |
| FEFD00 to FEFDFF | Interrupt Handler | FEFD00 to FEFDFF |
| FEFC00 to FEFCFF | Interrupt Generator | FEFC00 to FEFCFF |
| FEFB00 to FEFBFF | IEEE 488 Interface | FEFB00 to FEFBFF |
| FEFA00 to FEFAFF | DUSCC | FEFA00 to FEFAFF |
| FEF900 to FEF9FF | Extended Address Register | FEF900 to FEF9FF |
| FEF800 to FEF8FF | GPIB Controller Register | FEF800 to FEF8FF |
| FEF700 to FEF7FF | Status Register | FEF700 to FEF7FF |
| FEF600 to FEF6FF | DMA Controller | FEF600 to FEF6FF |
| FC0000 to FEF5FF | Reserved | FC0000 to FEF5FF |
| F80000 to FBFFFF | Local Memory Block 1 | F80000 to FBFFFF |
| F00000 to F7FFFF | Local Memory Block 0 | F00000 to F7FFFF |
| E80000 to EFFFFF | P2 Interface | E80000 to EFFFFF |
| 080000 to E7FFFF | Global Standard Access | 200000 to E7FFFF |
| 000000 to 07FFFF | Dual Port RAM | 000000 to 1FFFFF |

## VMEbus Address Modifier Codes

The PME 68-14 can generate the following address modifier codes. Where figures are included in brackets, these refer to a board with a 2 Mbyte DPR.

| Hex Code | Function Codes FC2 | FC1 | FC0 | Address | Extended Address Register |
|---|---|---|---|---|---|
| 3F | 1 | 0 | 0 | 080000 to EFFFFF (200000 to EFFFFF) | Clear |
| 3E | 1 | 1 | 0 | 080000 to EFFFFF (200000 to EFFFFF) | Clear |
| 3D | 1 | 0 | 1 | 080000 to EFFFFF (200000 to EFFFFF) | Clear |
| 3B | 0 | 0 | 0 | 080000 to EFFFFF (200000 to EFFFFF) | Clear |
| 3A | 0 | 1 | 0 | 080000 to EFFFFF (200000 to EFFFFF) | Clear |
| 39 | 0 | 0 | 1 | 080000 to EFFFFF (200000 to EFFFFF) | Clear |
| 2D | 1 | 1 | 0 | FF0000 to FFFFFF | Clear |
| 2D | 1 | 0 | 1 | FF0000 to FFFFFF | Clear |
| 29 | 0 | 1 | 0 | FF0000 to FFFFFF | Clear |
| 29 | 0 | 0 | 1 | FF0000 to FFFFFF | Clear |
| 0F | 1 | 0 | 0 | 080000 to EFFFFF (200000 to EFFFFF) | Written to |
| 0F | 1 | 0 | 0 | FF0000 to FFFFFF | Written to |
| 0E | 1 | 1 | 0 | 080000 to EFFFFF (200000 to EFFFFF) | Written to |
| 0E | 1 | 1 | 0 | FF0000 to FFFFFF | Written to |
| 0D | 1 | 0 | 1 | 080000 to EFFFFFF (200000 to EFFFFF) | Written to |
| 0D | 1 | 0 | 1 | FF0000 to FFFFFF | Written to |
| 0B | 0 | 0 | 0 | 080000 to EFFFFFF (200000 to EFFFFF) | Written to |
| 0B | 0 | 0 | 0 | FF0000 to FFFFFF | Written to |
| 0A | 0 | 1 | 0 | 080000 to EFFFFF (200000 to EFFFFF) | Written to |
| 0A | 0 | 1 | 0 | FF0000 to FFFFFF | Written to |
| 09 | 0 | 0 | 1 | 080000 to EFFFFF (200000 to EFFFFF) | Written to |
| 09 | 0 | 0 | 1 | FF0000 to FFFFFF | Written to |

Codes are defined in a PAL and may be redefined by re-programming the device.

# Dual Port RAM

The PME 68-14 contains either 512 kbytes or 2 Mbytes of Dual Port RAM (DPR) depending on the variant. The RAM array consists of sixteen 256 kbit or 1 Mbit, 100ns DRAM devices.

The start address of the DPR may be on any memory size boundary within the 4 Gbyte VMEbus memory map. The start address is selected by switches SW3 and SW4 (see Chapter 4, Configuration). Internally the DPR is mapped from $00 to either $07FFFF or $1FFFFF depending on the DPR fitted (see memory map, Page 16). Accesses to the DPR will incur 1 wait state.

The Exception Vector table is stored in the Dual Port RAM from $00 to $3FF. To prevent any system fault corrupting it, global WRITE accesses to the first $400 locations are denied. An attempt to WRITE to these locations will generate a BERR* signal on the VMEbus.

The DPR controller arbitrates between processor and VMEbus accesses to the Dual Port RAM.

# Mailbox

A WRITE access to the 32 bytes above the Exception Vector table will produce a local interrupt on Level 2. This mailbox interrupt facility provides an efficient means of inter-processor communications for multi-processing configurations.

# Local Resources

The PME 68-14 contains a number of local resources:

Local Memory

DMA Controller

IEEE 488 Interface

Two Serial Interfaces

P2 Interface

Three 16 bit Counter/Timers

Real Time Clock

Status Register

Status LED

Each of these is now described separately.

## Local Memory

The PME 68-14 is provided with four 32 pin JEDEC sockets, arranged in two blocks to give 16 bit capability. Each block is independent of the other, and may be configured for 8k x 8 to 1M x 8 EPROM or 8k x 8 to 512k x 8 SRAM or EEPROM. Chapter 4 gives details on configuring local memory size, type and access time.

The number of wait states inserted is link-selectable and should be set to the slowest memory fitted. The table below shows the relationship between inserted wait states and device access time.

| Read Cycle Access Time | Wait States | Write Cycle Write Time | Wait States |
|---|---|---|---|
| 85ns | 0 | 70ns | 0 |
| 100ns | 0 | 80ns | 0 |
| 120ns | 0 | 100ns | 1 |
| 150ns | 1 | 120ns | 1 |
| 200ns | 1 | 150ns | 1 |
| 250ns | 1 | 200ns | 2 |
| 300ns | 2 | | |
| 350ns | 2 | | |
| 400ns | 3 | | |
| 450ns | 3 | | |

Where the Access Time is greater than the Write Cycle Time, the link settings must reflect the slower delay (see Chapter 4 - Configuration, for link settings).

Examples: A 150 ns device with WE* of 100ns will incur 1 wait state on WRITE
A 450 ns device with WE* of 150ns will incur 3 wait states on READ

Address $00 in the first DPR block (Block 0) is mapped to internal address $00 after RESET then swapped to $F00000 after four internal accesses. This allows the initial SSP and initial PC to be stored in the PROM. The address swap is automatic and requires no software support. Block 1 is mapped from $F80000. The memory map is on Page 16.

## DMA Controller

The PME 68-14 is supplied with a 68450 four channel DMA controller. This allows transfers to and from:

Channel 0 and IEEE 488 interface
Channel 1 and Serial Channel A in half-duplex
Channel 3 and P2 interface
Channel 2 link-selectable between: Serial Channel A in full-duplex
Serial Channel B in half-duplex
P2 DMA channel

This gives the system the capability of real-time operation whilst maintaining high speed data transfers. Any of the four channels may be used for memory to memory transfers.

A major feature of the DMA controller is its flexible Bus Request generation. This may be programmed for Cycle Steal (in which DMA and CPU cycles are interleaved) or

Block Transfer (in which the DMA controls the bus until a complete block is transferred). The amount of bus use by the DMA controller is also programmable.

To obtain the bus, the DMA controller requests it from the CPU. The CPU will respond with a Bus Grant to indicate that the bus will be available at the end of the current cycle. When the DMA controller gains control of the bus, it asserts an Acknowledge signal and removes its request. The Acknowledge signal is removed at the end of DMA ownership of the bus.

**Function Codes**

The DMA controller provides function codes in a similar manner to the processor; these codes are user-programmable. To maintain compatibility with the processor when performing global accesses and hence generating Address Modifier codes, the following codes have been defined. Note that there are codes to define block transfers.

| FC2 | FC1 | FC0 | Cycle Type |
|---|---|---|---|
| Low | Low | Low | User Block Transfer |
| Low | Low | High | User Data Transfer |
| Low | High | Low | User Program Transfer |
| Low | High | High | Reserved |
| High | Low | Low | Supervisor Block Transfer |
| High | Low | High | Supervisor Data Transfer |
| High | High | Low | Supervisor Program Transfer |
| High | High | High | Reserved |

The DMA controller registers are mapped locally from $FEF600 to $FEF6FF. READ accesses to the DMA controller will incur 3 wait states, WRITE accesses will incur 4 wait states.

It is the programmer's responsibility to program the device function code and the base function code registers for each channel with the required value.

## DMA Controller Channel Offsets

Channel Offset

| Offset (Hex) | Function |
|---|---|
| + 00 | Channel 0 |
| + 40 | Channel 1 |
| + 80 | Channel 2 |
| + C0 | Channel 3 |

Register Offset (add to channel offset)

| Offset (Hex) | Function |
|---|---|
| + 00 | Channel Status Register |
| + 01 | Channel Error Register |
| + 04 | Device Control Register |
| + 05 | Operation Control Register |
| + 06 | Sequence Control Register |
| + 07 | Channel Control Register |
| + 0A | Memory Transfer Count Register |
| + 0C | Memory Address Register |
| + 14 | Device Address Register |
| + 1A | Base Transfer Count Register |
| + 1C | Base Address Register |
| + 25 | Normal Interrupt Vector |
| + 27 | Error Interrupt Vector |
| + 29 | Memory Function Code Register |
| + 2D | Channel Priority Register |
| + 31 | Device Function Code Register |
| + 39 | Base Function Code Register |

Register Offset (not channel dependent)

| Offset (Hex) | Function |
|---|---|
| + FF | General Control Register |

## IEEE 488 Interface

The PME 68-14 contains an IEEE 488 interface that performs all talker, listener and controller functions. Data transfers may be polled, interrupted, or controlled by the DMA. The interface can also generate a Level 5 interrupt under various conditions that are user programmable.

For the PME 68-14 to be System Controller of the IEEE 488 interface, the GPIB system controller register must be correctly set up; refer to the section on the GPIB Sytem Controller.

The IEEE 488 interface is available for use via an IEEE 488 connector mounted on the front panel. Appendix B shows the connector pin-out.

The interface is mapped locally from $FEFB00, Page 16 shows the full address map. Processor accesses will incur 2 wait states. During a DMA transfer, DMA requests are passed to channel 0 of the DMA controller.

The device contains six READ registers and seven WRITE registers, the offsets are given below. Transfers to and from the interface take place on the lower eight data lines only.

READ Registers

| Offset (Hex) | Function |
|---|---|
| + 01 | Interrupt Status 0 |
| + 03 | Interrupt Status 1 |
| + 05 | Address Status |
| + 07 | Bus Status |
| + 09 | Not used |
| + 0B | Not used |
| + 0D | Command Pass through |
| + 0F | Data in |

WRITE Registers

| Offset (Hex) | Function |
|---|---|
| + 01 | Interrupt Mask 0 |
| + 03 | Interrupt Mask 1 |
| + 05 | Not used |
| + 07 | Auxiliary Command |
| + 09 | Address |
| + 0B | Serial Poll |
| + 0D | Parallel Poll |
| + 0F | Data out |

### GPIB System Controller Register

A control register is provided in the interface circuitry for it to be used as IEEE 488 System Controller.

On power up or after a RESET, the PME 68-14 is not configured as System Controller. Any READ or WRITE access to the GPIB system controller register will cause it to change state. The register is mapped at $FEF800 and will incur zero wait states on access.

Note that no data is transferred during accesses to the GPIB System Controller register.

## Serial Interfaces

The PME 68-14 has two independent multi-protocol serial interfaces. These are implemented using the 68562 Dual Universal Serial Communications Controller (DUSCC). The board is supplied with an RS 232C transmitter and receiver. These devices may be replaced with RS 422A devices (see Chapter 4, Configuration). Each channel is made available via the 9 way 'D' type front panel connector. See Appendix C for the interface specification and Appendix B for the connector pin-out.

Each channel within the DUSCC is completely independent and may be set up for synchronous or asynchronous operation. In synchronous mode, data rates of up to 4 Mbits per second are obtainable, while in asynchronous mode, sixteen rates are supported, ie 50, 75, 110, 134.5, 150, 200, 300, 600, 1050, 1200, 2000, 2400, 4800, 9600, 19.2k and 38.4k Baud.

To ease problems with over-run and under-run, each channel contains a four deep FIFO buffer. The DUSCC also contains a 16 bit counter/timer (used for baud rate generation), a DPLL (used for clock recovery in some encoding schemes) and a general purpose output to drive the user status LED.

The device also contains a DMA interface. Channel A is fed to the on-board DMA controller to allow half duplex DMA operation. Additionally Channel A may be operated in full duplex mode; alternatively, both channels may be operated in half duplex DMA mode.

## Serial Interfaces, Software-selectable Features

### General

| | |
|---|---|
| Synchronous/asynchronous operation | |
| Character length | 5, 6, 7 or 8 bits |
| Data encoding | NRZ, NRZI, FM0, FM1, Manchester |
| Full/half duplex | |
| Data transfer mode | polled, interrupt, DMA |
| Channel interrupt priority | |
| Interrupt vector | |

### Asynchronous Mode

| | |
|---|---|
| Baud | 16 rates supported, see Page 23 |
| Parity | odd, even or no parity |
| Stop bit size | up to 2 in 1/16 increments |
| Clock factor | 1X or 16X |

### Synchronous Mode

| | |
|---|---|
| Protocol | BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75<br>COP: BISYNC, DDCMP |
| Clock | Internal/external transmit or receive clocks |

Note: For synchronous operation, TxC and RxC must be correctly linked. See Chapter 4, Configuration.

The DUSSC contains a set of registers locally mapped from $FEFA00; the register offsets are shown overleaf. Transfers to and from the DUSCC take place on the lower 8 data lines only. Processor READ accesses to the DUSCC will incur 3 wait states; WRITE accesses will incur 4 wait states. A repeat READ from the DUSCC is not allowed due to the requirement for CS*. The user is referred to the 68562 data sheet for further information.

The serial interface offsets are listed on the following page.

## Serial Interface Offsets

| Offset (Hex) | Function |
|---|---|
| + 01 | Channel A Mode Register 1 |
| + 03 | Channel A Mode Register 2 |
| + 05 | Channel A SYN 1/Secondary Address 1 Register |
| + 07 | Channel A SYN 2/Secondary Address 2 Register |
| + 09 | Channel A Transmitter Parameter Register |
| + 0B | Channel A Transmitter Timing Register |
| + 0D | Channel A Receiver Parameter Register |
| + 0F | Channel A Receiver Timing Register |
| + 11 | Channel A Counter/Timer Pre-set Register High |
| + 13 | Channel A Counter/Timer Pre-set Register Low |
| + 15 | Channel A Counter/Timer Control Register |
| + 17 | Channel A Output and Miscellaneous Register |
| + 19 | Channel A Counter/Timer High (READ only) |
| + 1B | Channel A Counter/Timer Low (READ only) |
| + 1D | Channel A Pin Configuration Register |
| + 1F | Channel A Command Register |
| + 21 to + 27 | Channel A Transmitter FIFO (WRITE only) |
| + 29 to + 2F | Channel A Receiver FIFO (READ only) |
| + 31 | Channel A Receiver Status Register |
| + 33 | Channel A Transmitter and Receiver Status Register |
| + 35 | Channel A Input and Counter/Timer Status Register |
| + 37 and + 77 | General Status Register |
| + 39 | Channel A Interrupt Enable Register |
| + 3B | Not used |
| + 3D | Unmodified Interrupt Vector Register |
| + 3F | Interrupt Control Register |
| + 41 | Channel B Mode Register 1 |
| + 43 | Channel B Mode Register |
| + 45 | Channel B SYN 1/Secondary Address 1 Register |
| + 47 | Channel B SYN 2/Secondary Address 2 Register |
| + 49 | Channel B Transmitter Parameter Register |
| + 4B | Channel B Transmitter Timing Register |
| + 4D | Channel B Receiver Parameter Register |
| + 4F | Channel B Receiver Timing Register |
| + 51 | Channel B Counter/Timer Pre-set Register High |
| + 53 | Channel B Counter/Timer Pre-set Register Low |
| + 55 | Channel B Counter/Timer Control Register |
| + 57 | Channel B Output and Miscellaneous Register |
| + 59 | Channel B Counter/Timer High (READ only) |
| + 5B | Channel B Counter/Timer Low (READ only) |
| + 5D | Channel B Pin Configuration Register |
| + 5F | Channel B Command Register |
| + 61 to + 67 | Channel B Transmitter FIFO (WRITE only) |
| + 69 to + 6F | Channel B Receiver FIFO (READ only) |
| + 71 | Channel B Receiver Status Register |
| + 73 | Channel B Transmitter and Receiver Status Register |
| + 75 | Channel B Input and Counter/Timer Status Register |
| + 79 | Channel B Interrupt Enable Register |
| + 7B | Not used |
| + 7D | Modified Interrupt Vector Register (READ only) |
| + 7F | Not used |

## P2 Interface

The interface on P2 is a buffered 68000 bus, intended to allow the addition of 68000-style Slaves to enhance the performance of the system. No Master capability is provided via the P2 interface. The interface has a 16 bit wide data bus, an 8 bit wide address bus, 68000 control lines, 6800 peripheral control lines, a user programmable clock, two DMA channels, a Level 1 Local Interrupt and an output from the counter/timers. Also included are ± 12V supplies. The interface is addressed from $E80000 to $EFFFFF.

The P2 pin connections are shown below.

| Pin | Row A | Row B | Row C |
|---|---|---|---|
| 1 | P2_D00 | + 5V | P2_D08 |
| 2 | P2_D01 | GND | P2_D09 |
| 3 | P2_D02 | Reserved | P2_D10 |
| 4 | P2_D03 | P2_A24 | P2_D11 |
| 5 | P2_D04 | P2_A25 | P2_D12 |
| 6 | P2_D05 | P2_A26 | P2_D13 |
| 7 | P2_D06 | P2_A27 | P2_D14 |
| 8 | P2_D07 | P2_A28 | P2_D15 |
| 9 | E | P2_A29 | P2_DTC* |
| 10 | P2_CLK | P2_A30 | P2_DONE* |
| 11 | VMA* | P2_A31 | P2_BERR* |
| 12 | P2_DS1* | GND | P2_RESET* |
| 13 | P2_DS0* | + 5V | P2_INT* |
| 14 | P2_R/W* | P2_D16 | PTMO |
| 15 | VPA* | P2_D17 | P2_A23 |
| 16 | P2_DTACK* | P2_D18 | P2_A22 |
| 17 | P2_DREQ1* | P2_D19 | P2_A21 |
| 18 | P2_AS* | P2_D20 | P2_A20 |
| 19 | P2_DREQ0* | P2_D21 | P2_A19 |
| 20 | P2_IACK* | P2_D22 | P2_A18 |
| 21 | P2_DACK1* | P2_D23 | P2_A17 |
| 22 | P2_DACK0* | GND | P2_A16 |
| 23 | P2_CS* | P2_D24 | P2_A15 |
| 24 | P2_A07 | P2_D25 | P2_A14 |
| 25 | P2_A06 | P2_D26 | P2_A13 |
| 26 | P2_A05 | P2_D27 | P2_A12 |
| 27 | P2_A04 | P2_D28 | P2_A11 |
| 28 | P2_A03 | P2_D29 | P2_A10 |
| 29 | P2_A02 | P2_D30 | P2_A09 |
| 30 | P2_A01 | P2_D31 | P2_A08 |
| 31 | P2_PCL1 | GND | P2_PCL0 |
| 32 | -12V | + 5V | + 12V |

## P2 Signal Description

In this description the following abbreviations are used: O = Output, I = Input, B = Bidirectional, TP = Totem Pole, TS = Three State, OC = Open Collector

| Signal Mnemonic | Type | Description |
|---|---|---|
| A01 to A07 | O TP | P2 address bus. Addresses up to 128 words and provides addressing information during all cycles except Interrupt Acknowledge cycles. |
| D00 to D15 | B TS | P2 data bus. May transmit or receive data in byte or word length. |
| AS* | O TP | Indicates a valid address on the P2 address bus |
| R/W* | O TP | Defines the current cycle as either READ or WRITE. The signal is high for READ cycles and LOW for WRITE cycles. |
| DS0* | O TP | Denotes that data will be transferred on the least significant 8 bits of the P2 data bus. |
| DS1* | O TP | Denotes that data will be transferred on the most significant 8 bits of the P2 data bus. |
| DTACK* | I OC | Indicates that the data transfer is complete. |
| BERR* | I OC | Indicates that for some reason the data transfer did not complete successfully. |
| INT* | I OC | Indicates that a device on the P2 bus is interrupting the CPU. |
| IACK* | O TP | Indicates that an Interrupt Acknowledge cycle is taking place across the P2 bus. |
| RESET* | O OC | Reset to external devices. |
| E | O TP | 6800 enable |
| VPA* | I TS | Denotes that the current cycle should be 6800 style transfer synchronised to E. |
| VMA* | O TP | Informs 6800 peripherals that the current cycle is synchronised to E |

**P2 Signal Descriptions continued**

| Signal Mnemonic | Type | Description |
|---|---|---|
| CLK | O TP | A free running clock, not synchronised to any other signal. User-selectable from the following frequencies: 5 MHz, 10 MHz, 12.5 MHz, 16 MHz, 20 MHz, 25 MHz, 32 MHz or 40 MHz. See Chapter 4. |
| PTMO | O TP | Output from Counter/Timer 3 |
| DREQ0*<br>DREQ1* | I TP | Data Transfer Request to DMA controller Note that DREQ0* must be correctly linked. See Chapter 4 - Configuration. |
| DACK0*<br>DACK1* | O TP | Data Transfer Acknowledge from DMA controller. Note that DACK0* must be correctly linked. See Chapter 4 - Configuration |
| PCL0<br>PCL1 | I TP | Multi-function inputs to DMA controller. See Chapter 4 - Configuration. |
| DTC* | O TS | Indicates that a DMA cycle has been successfully completed. |
| DONE* | B OC | Indicates that the current data item is the last in a block. Asserted by the DMA controller when the count register equals zero and the Continue bit in the DMAC is not set. May be asserted by a peripheral device to terminate DMA activity on the current channel. |
| P12V | O | Positive 12 volts supply. |
| M12V | O | Negative 12 volts supply |

For timing diagrams of the P2 interface, see Chapter 5. For loading and drive specifications for the P2 interface see Appendix A.

## Counter Timers

The PME 68-14 contains three 16 bit counter/timers. These are provided by the 68B40 which is a 6800 compatible device. The interrupt output from the 68B40 is fed to Local Interrupt Level 6 to provide accurate system 'ticks' or 'heartbeats'. The input to Counter/Timer 1 is fixed at 250 kHz. The inputs to Counter/Timers 2 and 3 are link-selectable between either the previous stage, the RTC output, or 250 kHz. See Chapter 4 - Configuration. The counter/timers have a base address of $FEFF00. Data is transferred to the counter/timers on the least significant 8 data bits only and is synchronised to P2 signal 'E' to give 6800 type transfers. The user is referred to the device data sheet for further information.

READ Registers

| Offset (Hex) | Function |
|---|---|
| + 01 | Not used |
| + 03 | Status Register |
| + 05 | Timer 1 Counter |
| + 07 | LSB Buffer Register |
| + 09 | Timer 2 Counter |
| + 0B | LSB Buffer Register |
| + 0D | Timer 3 Counter |
| + 0F | LSB Buffer Register |

WRITE Registers

| Offset (Hex) | Function |
|---|---|
| + 01 | Timer 1 and 3 Control Registers (selected from Timer 2 Control Register) |
| + 03 | Timer 2 Control Register |
| + 05 | MSB Buffer Register |
| + 07 | Timer 1 Latches |
| + 09 | MSB Buffer Register |
| + 0B | Timer 2 Latches |
| + 0D | MSB Buffer Register |
| + 0F | Timer 3 Latches |

## Real-Time Clock

The MSM6242 device provides the PME 68-14 with an accurate RTC (Real-Time Clock). When fed into the counter/timer, the clock can function as a Real-Time interrupter. Other applications include 'date stamp' readings from the IEEE 488 interface.

The clock is powered from either + 5V or + 5V STDBY. The change over is automatic on power failure. There is no provision for an on-board battery. The features of the RTC clock include:

year, month, date, hours, minutes, seconds, days of the week

12/24 hour display format

automatic compensation for leap years

1/64 second, 1 second, 1 minute, 1 hour output

The RTC has a base address of $FEFE00; the offsets are shown below. Data is transferred on the least significant 4 data bits only and will incur 6 wait states. The user is referred to the MSM6242 data sheet for further information.

| Offset (Hex) | Function |
|---|---|
| + 01 | 1 second digit register |
| + 03 | 10 second digit register |
| + 05 | 1 minute digit register |
| + 07 | 10 minute digit register |
| + 09 | 1 hour digit register |
| + 0B | AM/PM and 10 hour digit register |
| + 0D | 1 day digit register |
| + 0F | 10 day digit register |
| + 11 | 1 month digit register |
| + 13 | 10 month digit register |
| + 15 | 1 year digit register |
| + 17 | 10 year digit register |
| + 19 | Week register |
| + 1B | Control Register D |
| + 1D | Control Register E |
| + 1F | Control Register F |

## Status Register

The PME 68-14 contains a 16 bit status register to allow the CPU to be aware of certain functions. The status register is mapped at $FEF700. Status register accesses incur zero wait states. The individual bit assignments of the status register are given below.

| Bit | Function |
|---|---|
| Bit 0 | IEEE 488 address A1 |
| Bit 1 | IEEE 488 address A2 |
| Bit 2 | IEEE 488 address A3 |
| Bit 3 | IEEE 488 address A4 |
| Bit 4 | IEEE 488 address A5 |
| Bit 5 | User-defined Status |

= Bit 6 User-defined Status

| | |
|---|---|
| Bit 7 | User-defined Status |
| Bit 8 | GPIB Sytem Controller* |
| Bit 9 | Local Memory Block 0 Busy* |
| Bit 10 | Local Memory Block 1 Busy* |
| Bit 11 | Extended Address* |
| Bit 12 | Bus Timeout* |
| Bit 13 | SYSFAIL* |
| Bit 14 | Status LED |
| Bit 15 | Reserved (High) |

## Status LED

The Status LED is controlled via the Channel B Output and Miscellaneous Register of the DUSCC. To light the Status LED, bit 2 of this register must be 0. The state of the LED can be monitored by reading the Status Register. Bit 14 is 0 when the Status LED is ON.

# VMEBus Functions

The PME 68-14 contains five VMEbus functions, these are:

Interrupt Generator
Interrupt Handler
Extended Address Register
Requester
System Controller

Each of these functions is now described separately.

## Interrupt Generator

The Interrupt Generator allows the PME 68-14 to generate an interrupt on any of the seven VMEbus interrupt lines and to monitor when the interrupt has been acknowledged. The user programs the most significant 5 bits of the interrupt vector to be supplied during the Interrupt Acknowledge cycle, the least significant 3 bits being A01 to A03. The Interrupt Generator also provides the IACK* daisy-chain driver.

The device operates in Release On Acknowledge (ROAK) mode. During an Interrupt Acknowledge cycle, when the Interrupt Generator does not have an interrupt pending on the acknowledged level, IACKIN* will be passed straight to IACKOUT*.

The registers within the Interrupt Generator are mapped into local memory space with a base address of $FEFC00. All arbitration between VMEbus and local access to registers is performed within the device. Data is transferred on the least significant 8 data bits only and will incur 4 wait states. The offsets are listed below. The user is referred to the 68154 device data sheet for further information..

| Offset (Hex) | Function |
|---|---|
| + 01 | Interrupt Vector Register |
| + 03 | Interrupt Request Register |

## Interrupt Handler

The PME 68-14 is provided with full VMEbus and internal interrupt handling capability by the 68155 Interrupt Handler. This device sets the priorities of the seven VMEbus interrupts, six local interrupts, and one non-maskable interrupt; it also provides the interrupt level code to the CPU and the appropriate interrupt acknowledgement.

During VMEbus Interrupt Acknowledge cycles, the 68155 works with the Bus Requester to obtain the Interrupt Vector. During a local Interrupt Acknowledge cycle, either the interrupting device or the 68155 may supply the Interrupt Vector.

Interrupts can be individually masked, except for Non-Maskable Interrupts (NMI). In addition, local interrupts can be programmed as level or edge sensitive, NMI are low level sensitive interrupts.

The interrupt priority level outputs are encoded as follows:

| Local Request | VMEbus Request | ILP2* | ILP1* | ILP0* |
|---|---|---|---|---|
| NMI* | IRQ7* | Low | Low | Low |
| LRQ6 | IRQ6* | Low | Low | High |
| LRQ5 | IRQ5* | Low | High | Low |
| LRQ4 | IRQ4* | Low | High | High |
| LRQ3 | IRQ3* | High | Low | Low |
| LRQ2 | IRQ2* | High | Low | High |
| LRQ1 | IRQ1* | High | High | Low |
| None | None | High | High | High |

The local interrupt sources are allocated as follows:

| Interrupt Source | Level | Vector Source |
|---|---|---|
| ABORT switch | NMI | IVHAN |
| Counter/Timer | 6 | IVHAN |
| ACFAIL* | 6 | IVHAN |
| SYSFAIL* | 6 | IVHAN |
| IEEE 488 | 5 | IVHAN |
| DUSCC | 4 | IVHAN or DUSCC |
| DMA | 3 | IVHAN or DMA |
| DPR Mailbox | 2 | IVHAN |
| P2 Bus | 1 | P2 Device |

Note: The Level 6 interrupter may be determined by reading the Counter/Timer status register and the System status register.

Registers within the 68155 are mapped into Local Memory space at a base address of $FEFD00. Data is transferred using the least significant 8 data bits only and will incur 3 wait states. The register offsets are given below.

| Offset (Hex) | Function |
|---|---|
| + 01 | Local Interrupt Control Pointer Register (WRITE only) |
| + 03 | Local Interrupt Control Register |
| + 05 | Local Interupt Vector Register |
| + 07 | Local Interrupt Mask Register |
| + 09 | Local Interrupt Status Register (READ only) |
| + 0B | VMEbus Interrupt Mask Register |
| + 0D | VMEbus Interrupt Status Register (READ only) |
| + 0F | Last Interrupt Acknowledged Register (READ only) |

## Extended Address Register

The PME 68-14 has the ability to address the VMEbus using extended addressing. This is achieved by writing the most significant 8 bits of the address to the Extended Address register. After a WRITE to this register, all VMEbus accesses will be Extended Address accesses until the register is read by the CPU. Note that no data is returned during this Read operation.

The Status register contains a flag bit to inform the CPU when extended addressing is in effect.

Extended Address Modifier codes are generated whilst extended addressing is in effect.

The Extended Address register is mapped at $FEF900. Data is transferred to the Extended Address register on the least significant 8 data bits only and will incur zero wait states.

## Requester

The Requester on the PME 68-14 is implemented using a 68172 device. This provides bus requests to the VMEbus from an on-board MASTER, 'Buffer Enable' signals, direction controls and release logic.

VMEbus accesses to the Dual Port RAM are also passed through the Requester to provide buffer control.

The Requester is a Release On Request (ROR) type with early BBSY* release to reduce arbitration overheads during heavy bus usage by the board.

The Bus Request level is determined by means of links. Unused Bus Grants should be linked to pass the signal down the Bus Grant daisy chain. See Chapter 4 for configuration details.

### Early BBSY* Release

This feature allows the PME 68-14 to release ownership of the bus during the final cycle of a transfer. This in turn allows the System Arbiter to perform arbitration during that cycle, thereby reducing arbitration latency and increasing system performance.

### Release On Request (ROR)

Release On Request allows the PME 68-14 to retain control of the VMEbus, even though it may not currently be using the bus. Control is retained by continually asserting BBSY* until another request is detected. When another request is detected, the PME 68-14 releases the bus by de-asserting BBSY* at the appropriate point in the cycle, thus allowing arbitration to occur. This scheme offers a significant improvement in system performance over that obtained using Release When Done (RWD) arbitration (where a Bus Master releases the bus at the end of each transfer).

## System Controller Functions

To allow the PME 68-14 to be used in slot 1 of a VMEbus backplane, the PME 68-14 supports all System Controller functions. These are:

4 level Arbiter supporting RRS or PRI with BCLR*, or SGL
SYSCLK Driver module
Bus Timeout module
IACK* Daisy chain Driver Module

### Arbiter

The PME 68-14 contains a fast, 4 level Arbiter, the main features of which are:

- Fully synchronous operation, eliminating glitchy outputs
- Metastable-hardened latches to ensure correct operation
- Schmidt-triggered inputs to increase noise immunity on BRx* and BBSY* inputs
- BBSY* noise filtering

The PME 68-14 arbiter supports Priority (PRI), Round Robin (RRS) and Single Level (SGL) arbitration as standard. These options are link-selectable (see Chapter 4, Configuration).

When configured for PRI or RRS, BCLR* will be driven when a higher level request is detected. BCLR* is enabled by means of a link. It must be enabled during PRI arbitration and may or may not be enabled during RRS arbitration.

The Arbiter can be disabled by means of a link. This must be done when the PME 68-14 is fitted in any slot other than slot 1.

In all arbitration schemes, boards in the system are given a further order of priority by their slot positions along the backplane. For a given request level, a board nearer slot 1 has a higher priority than a board on the same level but further away from slot 1.

Each of the arbitration schemes is described below.

### PRI

In a Priority arbitration scheme, the four Bus Request lines have fixed priority levels, BR3* being the highest and BR0* the lowest. This means that if more than one request is pending at arbitration time, the level granted depends entirely on the request levels. This can be useful if a particular Bus Master needs guaranteed access to the bus as quickly as possible, or if it is desired to spread bus usage asymetrically. Care should be taken, however, to avoid the situation where boards on a lower priority request level are never granted use of the bus.

The Arbiter will assert BCLR* if a higher level request than the one currently granted is pending. For PRI operation, the link to enable BCLR* **must** be fitted.
See Chapter 4 - Configuration, for link details.

### RRS

The Round Robin arbitration scheme removes the problems associated with PRI arbitration but does not guarantee access to the bus in any given situation. In RRS, each of the bus requests is rotated in priority every time a Master is granted the use of the bus. Once a given level has been granted, it then becomes the lowest priority. This evens out bus usage between Masters within the system.

The Arbiter will assert BCLR* if a higher level request than that currently granted is pending, ie any other request. The link to enable BCLR* may be fitted for RRS operation.

### SGL

The third option is Single Level arbitration. The Arbiter will perform SGL arbitration in either mode. In SGL arbitration, all requesters generate requests on the same level, usually Level 3. All prioritisation is then dependent on the BGIN*/BGOUT* daisy chain and the physical slot positions of the boards in a system.

### SYSCLK Driver Module

The PME 68-14 contains a SYSCLK driver module of 16 MHz frequency. It must be enabled when the board is fitted in slot 1 and disabled in any other slot.
See Chapter 4 - Configuration, for details.

### Bus Timeout Module

The Bus Timeout module is used to drive BERR* when a Bus Timeout occurs. The timer is triggered on the first falling edge of DS0* or DS1* and will drive BERR* provided no other Slave has driven DTACK* or BERR* within the timeout period.

The output from the Bus Timeout module is also latched and fed to the Status Register to inform the PME 68-14 that a Bus Timeout has occurred. This will be cleared by a READ of the Status Register. The time out period is link-selectable and may be any period ranging from 0.8µs to 6554µs.

### IACK* Daisy Chain Driver Module

See under Interrupt Generator.

# System Considerations

## PME 68-14 as a Bus Slave

The PME 68-14 contains either 512 kbytes or 1 Mbyte of Dual Port RAM, addressable by the VMEbus. The local resources of the PME 68-14 cannot be accessed by the VMEbus.

The start address of the DPR can be mapped on any 64 kbyte boundary within the 4Gbyte address map of the VMEbus, using SW3 and SW4. See Chapter 4 - Configuration, for the switch settings. The board may be configured as either an A24 or A32 VMEbus Slave device.

PME 68-14 will respond to the following Address Modifier codes:

| Hex Code | Function |
|---|---|
| 3E | Standard Supervisory Program Access |
| 3D | Standard Supervisory Data Access |
| 3A | Standard Non-privileged Program Access |
| 39 | Standard Non-privileged Data Access |
| 0E | Extended Supervisory Program Access |
| 0D | Extended Supervisory Data Access |
| 0A | Extended Non-privileged Program Access |
| 09 | Extended Non-privileged Data Access |

These codes are defined in a PAL and may be redefined by suitable programming of the device.

The PME 68-14 is a D16 Slave device and therefore cannot respond to LWORD*. Any attempted LWORD* accesses will result in BERR*; no other action is performed.

## PME 68-14 as Bus Master

The PME 68-14 may generate VMEbus accesses from either the CPU or the DMA Controller. Depending on the VMEbus address accessed, it will either be a standard (24 bit) or short (16 bit) address access. See the address map on Page 16 for memory addresses.

All VMEbus accesses may be changed to extended 32 bit addresses by writing to the Extended Address register. The change will remain in effect until the register is read from.

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# Chapter 4 - Configuration

**CAUTION: The PME 68-14 uses power from both the J1 and J2 VMEbus connector.**

**Use of the J1 connector only may cause excessive current to be drawn through the + 5V connector pins.**

## Introduction

The PME 68-14 contains a number of links and wire wrap areas, which enable the board to be configured to suit system requirements. This chapter shows the possible configurations and also the default state of the board on delivery.

The orientation of the detailed link connection diagrams assumes that the board is component side uppermost with the front panel facing the top of the page. Pin 1 of the link blocks is identified by a square solder pad on the underside of the board and is represented by a square pin in the configuration diagrams.

Spare links are supplied with the board in addition to those already fitted. It is not advisable to solder the wire-wrap areas, as this may cause damage to the pins.

## Board Identification

Each board is marked with a Radstone part number which includes a variant number. The variant number is the three digits at the end of the part number, eg 421/1/23852/100.

The variants currently available are:

| | |
|---|---|
| 421/1/23852/100 | 10 MHz 68000, 512 kbyte DRAM, RS 232C drivers |
| 421/1/23852/101 | 10 MHz 68010, 512 kbyte DRAM, RS 232C drivers |
| 421/1/23941/102 | 10 MHz 68000, 2 Mbyte DRAM, RS 232C drivers |
| 421/1/23941/103 | 10 MHz 68010, 2 Mbyte DRAM, RS 232C drivers |
| 421/1/23852/400 | 10 MHz 68000, 512 kbyte DRAM, RS 422A drivers |
| 421/1/23852/401 | 10 MHz 68010, 512 kbyte DRAM, RS 422A drivers |
| 421/1/23941/402 | 10 MHz 68000, 2 Mbyte DRAM, RS 422A drivers |
| 421/1/23941/403 | 10 MHz 68010, 2 Mbyte DRAM, RS 422A drivers |

# User-selectable Functions

The following functions are user-selectable by means of either links, switches or IC replacement:

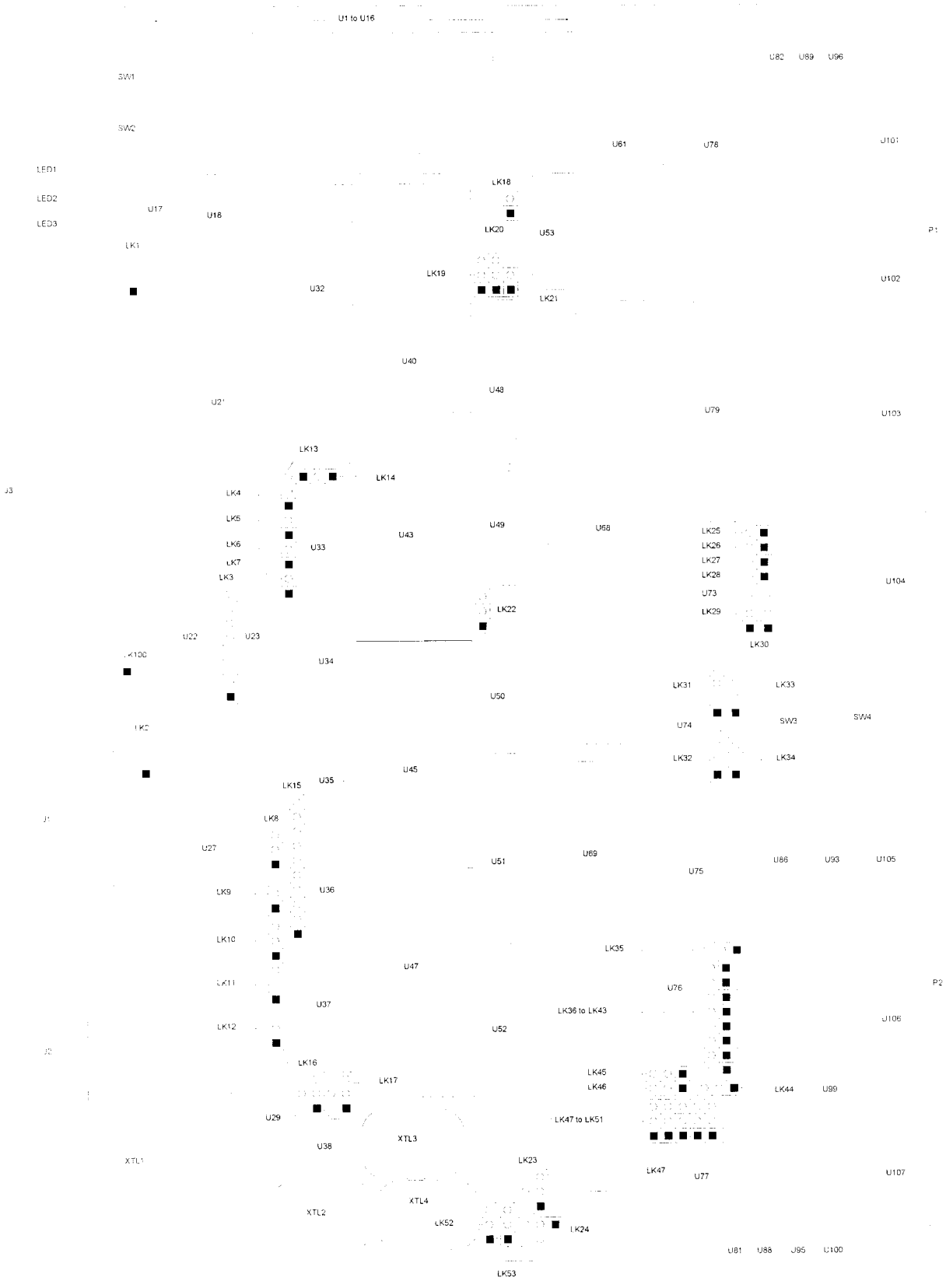
| | | |
|---|---|---|
| **Addressing** | Start address<br>A32 or A24 slave operation | |
| **Requester** | Bus request level<br>Bus grant level | |
| **Arbiter** | Arbitration method<br>Enable/disable<br>BCLR* enable/disable | |
| **DMA device** | DUSCC: | Channel A Tx/DUSCC<br>Channel B Tx/Rx/P2 |
| **Local Memory** | Access time<br>Size<br>SRAM/EPROM/EEPROM | |
| **Counter/Timers** | 250 kHz or previous stage or RTC output/input source | |
| **IEEE 488 Interface** | IEEE 488 interface address | |
| **Serial Interface** | Synchronous/asynchronous operation<br>RS 232C or RS 422A driver/receivers | |
| **P2 Interface**<br>**Utilities** | Clock rate<br>User Status links | |
| **SYSCLK** | enable/disable | |
| **Utilities** | Bus Timeout enable/disable<br>Bus Timeout period | |

# Delivery Configuration

The delivery condition of the board is given below. The board can be configured for individual requirements by referring to the remainder of this chapter.

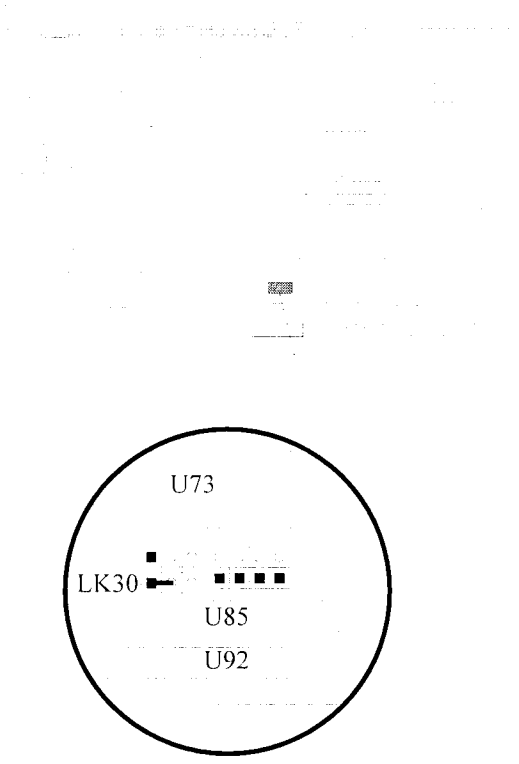
| | |
|---|---|
| **Addressing** | A32 Slave operation<br>Default base address $400000 |
| **Requester** | Bus request BR3*<br>Bus grant BG3IN*<br>All other bus grants linked through |
| **Arbiter** | PRI arbitration method<br>Enabled<br>BCLR* enabled<br>DMA device DUSCC channel B Tx/Rx |
| **Local Memory** | 200ns access time<br>256 kbytes EPROM |
| **Counter/Timers** | previous stage as input source |
| **IEEE 488 Interface** | $01 address |
| **Serial Interface** | Asynchronous 14.7456 Mhz clock rate |
| **P2 Interface** | 10 MHz clock rate |
| **Utilities** | 0 user status<br>SYSCLK enabled<br>Bus Timeout enabled<br>6554µs Bus Timeout period |

## PME 68-14 Board Layout



# VMEbus Addressing

The start address and the type of addressing (24/32 bit) of the PME 68-14 within the VMEbus memory map is selected by two banks of eight switches and one 3-pin link. Link 30 selects 24/32 bit addressing; its default setting (32 bit addressing) and relative position are shown below.




Setting the start address is described on the following page.

## VMEbus Start Address Selection

The table below shows the relationship between SW3 and SW4 switch poles and the VMEbus address bits. An address bit is high when the switch is OFF (open). The start address is the sum of OFF switch addresses obtained from the table below.

| Bank and Switch | VMEbus Address | Start Address | Boundary |
|---|---|---|---|
| SW4/8 | A31 | 80000000 | 2G |
| SW4/7 | A30 | 40000000 | 1G |
| SW4/6 | A29 | 20000000 | 512M |
| SW4/5 | A28 | 10000000 | 256M |
| SW4/4 | A27 | 8000000 | 128M |
| SW4/3 | A26 | 4000000 | 64M |
| SW4/2 | A25 | 2000000 | 32M |
| SW4/1 | A24 | 1000000 | 16M |
| SW3/8 | A23 | 800000 | 8M |
| SW3/7 | A22 | 400000 | 4M |
| SW3/6 | A21 | 200000 | 2M |
| SW3/5 | A20 | 100000 | 1M |
| SW3/4 | A19 | 80000 | 512k |

SW3/3, 2 and 1 are in a 'don't care' state

Note: SW3/5 and 3/4 are not used in 2 Mbyte variants

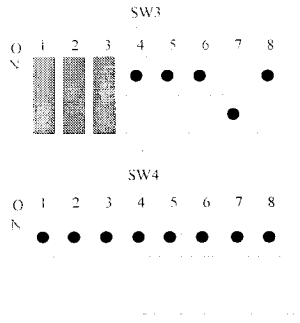
Examples:

1. To set start address $02080000, SW4/2 and SW3/4 must be OFF (open). All other switches must be ON (closed), and Link 30 should be in position 1-2.

2. To set start address $EDC80000, SW4/8, SW4/7, SW4/6, SW4/4, SW4/3, SW4/1, SW3/8, SW3/7, SW3/4 must be OFF. All other switches must be ON with Link 30 in position 1-2.

3. To set start address $F80000, SW3/8, SW3/7, SW3/6, SW3/5 and SW3/4 must be OFF. SW4 is in a 'don't care' state, and Link 30 should be in position 2-3.

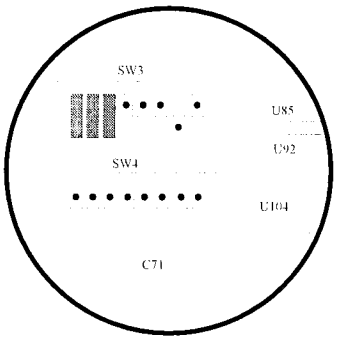
Switch settings for the default base address of $400000




KEY:

● This symbol represents the position of the switch. The shaded switches are in a don't care state for this configuration.

The position of the start address selection switches SW3 and SW4 are shown below.



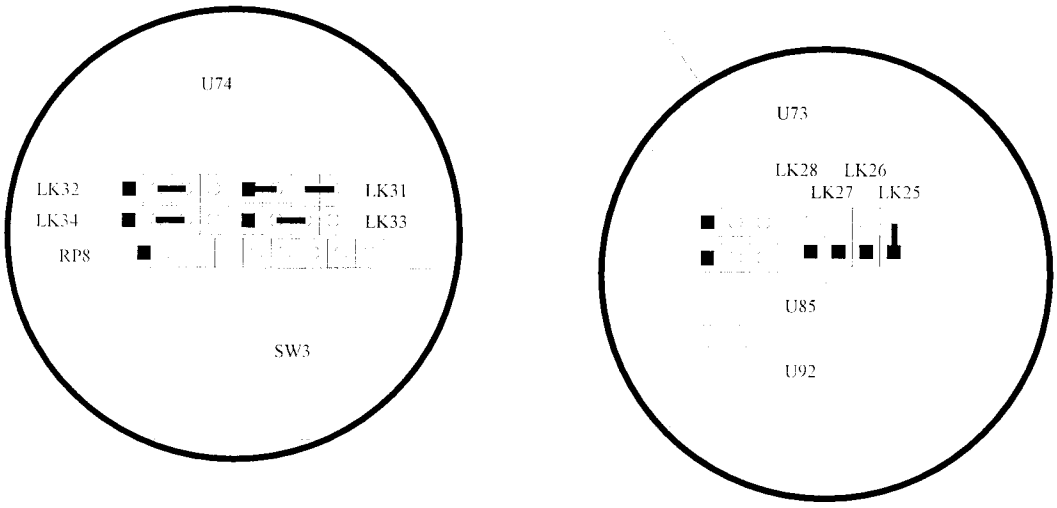
# Requester

The Bus Request and Bus Grant level are configured by means of four 2-pin and four 4-pin links as follows:

| Link | Function | Configuration Options |
|---|---|---|
| LK25<br>LK27<br>LK26<br>LK28 | Bus Request Level 3<br>Bus Request Level 2<br>Bus Request Level 1<br>Bus Request Level 0 | Only one of these links is fitted to set the Bus Request to the required level. The other 3 links in this group must be left open. |
| LK31<br>LK33<br>LK34<br>LK32 | Bus Grant Level 3<br>Bus Grant Level 2<br>Bus Grant Level 1<br>Bus Grant Level 0 | o—o o—o<br>o o—o o<br>o o—o o<br>o o—o o<br>1 | Receives BG3IN* and passes on all other levels. BG3OUT* is driven if no other request is pending. LK25 must be fitted. |
| LK31<br>LK33<br>LK34<br>LK32 | Bus Grant Level 3<br>Bus Grant Level 2<br>Bus Grant Level 1<br>Bus Grant Level 0 | o o—o o<br>o—o o—o<br>o o—o o<br>o o—o o<br>1 | Receives BG2IN* and passes on all other levels. BG2OUT* is driven if no other request is pending. LK27must be fitted. |
| LK31<br>LK33<br>LK34<br>LK32 | Bus Grant Level 3<br>Bus Grant Level 2<br>Bus Grant Level 1<br>Bus Grant Level 0 | o o—o o<br>o o—o o<br>o—o o—o<br>o o—o o<br>1 | Receives BG1IN* and passes on all other levels. BG1OUT* is driven if no other request is pending. LK26 must be fitted. |
| LK31<br>LK33<br>LK34<br>LK32 | Bus Grant Level 3<br>Bus Grant Level 2<br>Bus Grant Level 1<br>Bus Grant Level 0 | o o—o o<br>o o—o o<br>o o—o o<br>o—o o—o<br>1 | Receives BG0IN* and passes on all other levels. BG0OUT* is driven if no other request is pending. LK28 must be fitted. |

The relative position and default setting of these links are shown overleaf.

The relative positions of links 25 to 28 and links 31 to 34 are shown below.



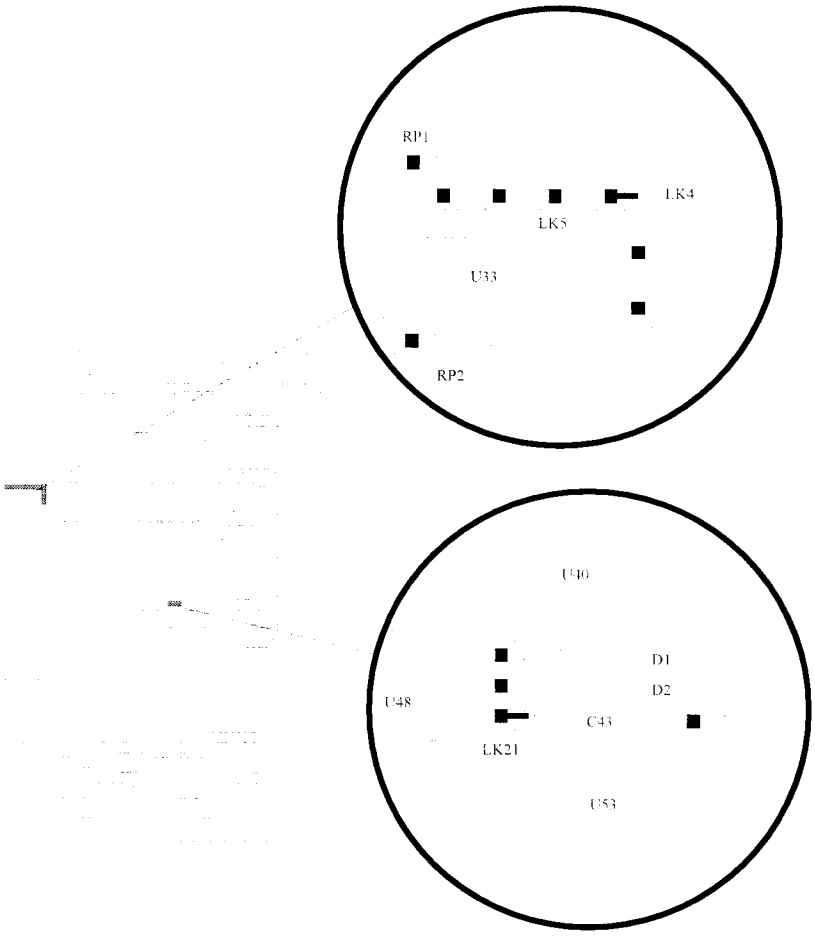
# Arbiter

The arbiter is configured by means of three 2-pin links as follows:

| Link | Function | Configuration Options |
|---|---|---|
| LK4 | Arbiter enable | Fitted: Arbiter enabled<br>Omitted: Arbiter disabled |
| LK21 | BCLR* enable | Fitted: BCLR* driven<br>Omitted: BCLR* not driven |
| LK5 | Arbitration scheme | Fitted: RRS arbitration<br>Omitted: PRI arbitration |

Note: LK4 must be fitted when the board is used in Slot 1 and must not be fitted when the board is used in any other slot.

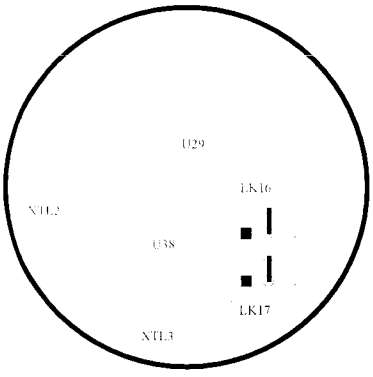
The relative position of links 4, 5 and 21 and the default settings (Arbiter enabled with PRI arbitration scheme) are shown below.

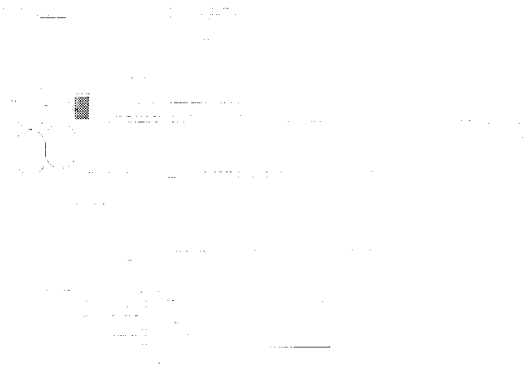


# DMA Device

Channel 2 of the 68450 DMAC can be configured to a number of different devices. This is done by means of two 4-pin links. Note LK16 and LK17 must be set to the same device.

| Link | Function | Configuration Options | |
|---|---|---|---|
| LK16 | DMA device select | o<br>o o—o<br>1 | DUSCC Channel A: Tx selected |
| LK16 | DMA device select | o<br>o o o<br>1 | DUSCC Channel B: Rx/Tx selected |
| LK16 | DMA device select | o<br>o—o o<br>1 | P2 selected |
| LK17 | DMA device select | o<br>o o—o<br>1 | DUSCC Channel A: Tx selected |
| LK17 | DMA device select | o<br>o o o<br>1 | DUSCC Channel B: Rx/Tx selected |
| LK17 | DMA device select | o<br>o—o o<br>1 | P2 selected |



# Local Memory

The local memory of the PME 68-14 is in two independent blocks, each configured for size and technology by means of seven 3-pin links per block. Access time is set up by means of an 8-pin, wire-wrap area, LK3. The access time of a block must be set to the slowest device in that block. Block 0 is U43 (LSB) and U47 (MSB), block 1 is U40 (LSB) and U45 (MSB).

## Local Memory Size and Technology

These are the functions of each link in the Local Memory blocks:

| Block 0 Links | Block 1 Links | Function |
|---|---|---|
| LK47 | LK20 | Vcc/A13 select |
| LK48 | LK45 | WRITE*/A14 select |
| LK49 | LK50 | A14/A15 select |
| LK52 | LK53 | Vcc/A17 select |
| LK46 | LK19 | A15/A18 select |
| LK51 | LK44 | A18/A19 select |
| LK22 | LK35 | Block BUSY* to system status register |

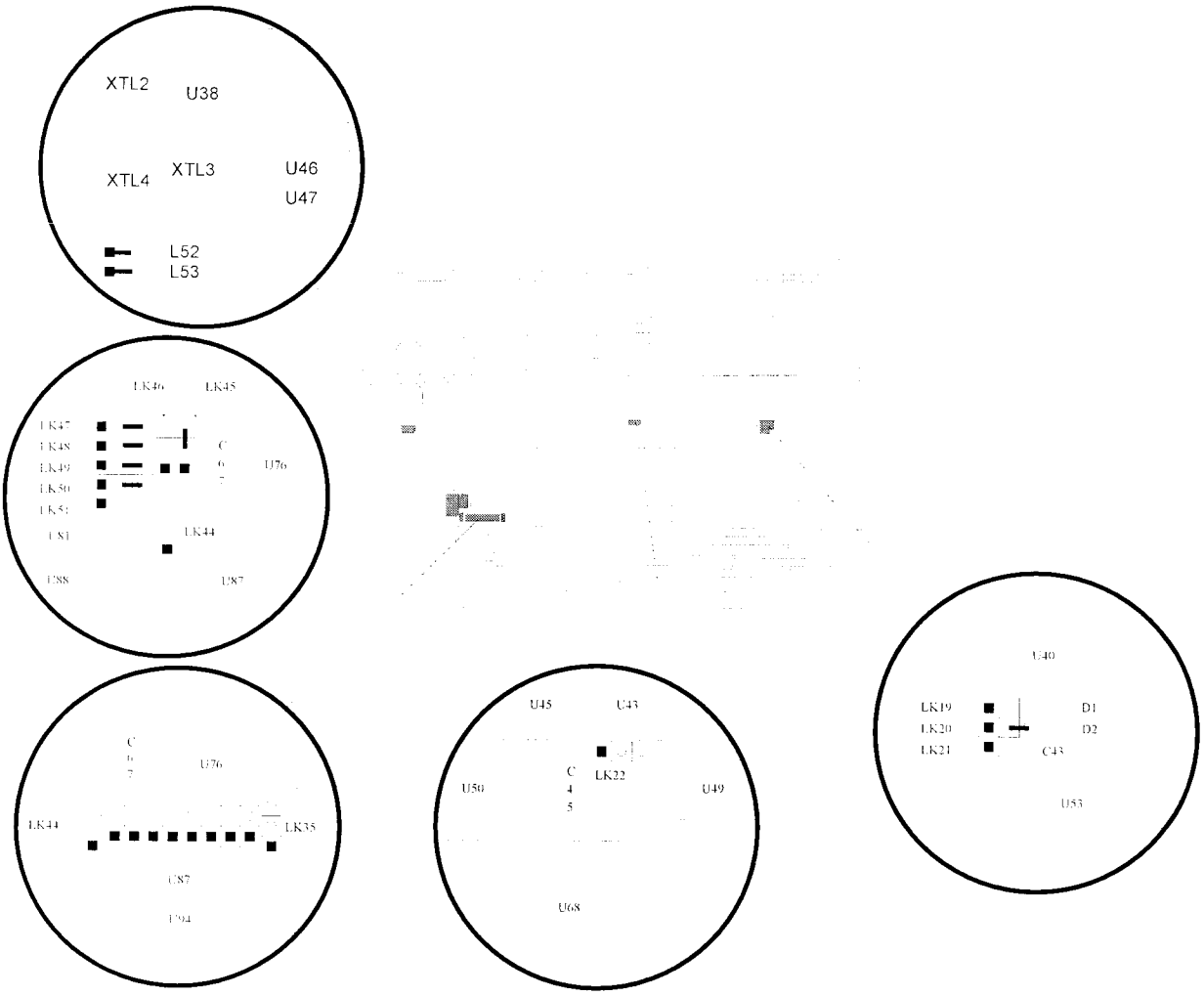
The following table shows the link settings to configure the board for a particular memory type and size.

Key to table: * = 'don't care', 0 = OPEN (ie no link fitted)

| DEVICE | SIZE | | BLOCK 1 | | | | | | LINK | BLOCK 0 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 20 | 45 | 50 | 53 | 19 | 44 | 35 | 47 | 48 | 49 | 52 | 46 | 51 | 22 |
| EPROM | 8k X 8 | 64k | 0 | 1-2 | 0 | 1-2 | * | * | 0 | 0 | 1-2 | 0 | 1-2 | * | * | 0 |
| | 16k X 8 | 128k | 2-3 | 1-2 | 0 | 1-2 | * | * | 0 | 2-3 | 1-2 | 0 | 1-2 | * | * | 0 |
| | 32k X 8 | 256k | 2-3 | 2-3 | 0 | 1-2 | * | * | 0 | 2-3 | 2-3 | 0 | 1-2 | * | * | 0 |
| | 64k X 8 | 512k | 2-3 | 2-3 | 2-3 | 1-2 | * | * | 0 | 2-3 | 2-3 | 2-3 | 1-2 | * | * | 0 |
| | 128k X 8 | 1M | 2-3 | 2-3 | 2-3 | 0 | 0 | 0 | 0 | 2-3 | 2-3 | 2-3 | 0 | 0 | 0 | 0 |
| | 256k X 8 | 2M | 2-3 | 2-3 | 2-3 | 2-3 | 0 | 0 | 0 | 2-3 | 2-3 | 2-3 | 2-3 | 0 | 0 | 0 |
| | 512k X 8 | 4M | 2-3 | 2-3 | 2-3 | 2-3 | 2-3 | 0 | 0 | 2-3 | 2-3 | 2-3 | 2-3 | 2-3 | 0 | 0 |
| | 1M X 8 | 8M | | | | | | | | 2-3 | 2-3 | 2-3 | 2-3 | 2-3 | 2-3 | 0 |
| EEPROM | 8k X 8 | 64k | 1-2 | 1-2 | 0 | 1-2 | * | * | 1-2 | 1-2 | 2-3 | 0 | 1-2 | * | * | 1-2 |
| | 32k X 8 | 256k | 2-3 | 1-2 | 1-2 | 1-2 | * | * | 1-2 | 2-3 | 1-2 | 1-2 | 1-2 | * | * | 1-2 |
| | 64k X 8 | 512k | 2-3 | 1-2 | 1-2 | 1-2 | 1-2 | 0 | 2-3 | 2-3 | 1-2 | 1-2 | 1-2 | 1-2 | 0 | 2-3 |
| | 128k X 8 | 1M | 2-3 | 1-2 | 1-2 | 1-2 | 1-2 | 0 | 2-3 | 2-3 | 1-2 | 1-2 | 1-2 | 1-2 | 0 | 2-3 |
| | 256k X 8 | 2M | 2-3 | 1-2 | 1-2 | 0 | 1-2 | 0 | 2-3 | 2-3 | 1-2 | 1-2 | 0 | 1-2 | 0 | 2-3 |
| | 512k X 8 | 4M | 2-3 | 1-2 | 1-2 | 0 | 1-2 | 1-2 | 2-3 | 2-3 | 1-2 | 1-2 | 0 | 1-2 | 1-2 | 2-3 |
| SRAM | 8k X 8 | 64k | 1-2 | 1-2 | 0 | 1-2 | * | * | 0 | 1-2 | 1-2 | 0 | 1-2 | * | * | 0 |
| | 32k X 8 | 256k | 2-3 | 1-2 | 1-2 | 1-2 | * | * | 0 | 2-3 | 1-2 | 1-2 | 1-2 | * | * | 0 |
| | 64k X 8 | 512k | 2-3 | 1-2 | 1-2 | 1-2 | 1-2 | 0 | 0 | 2-3 | 1-2 | 1-2 | 1-2 | 1-2 | 0 | 0 |
| | 128k X 8 | 1M | 2-3 | 1-2 | 1-2 | 1-2 | 1-2 | 0 | 0 | 2-3 | 1-2 | 1-2 | 1-2 | 1-2 | 0 | 0 |
| | 256k X 8 | 2M | 2-3 | 1-2 | 1-2 | 0 | 1-2 | 0 | 0 | 2-3 | 1-2 | 1-2 | 0 | 1-2 | 0 | 0 |
| | 512k X 8 | 4M | 2-3 | 1-2 | 1-2 | 0 | 1-2 | 1-2 | 0 | 2-3 | 1-2 | 1-2 | 0 | 1-2 | 1-2 | 0 |

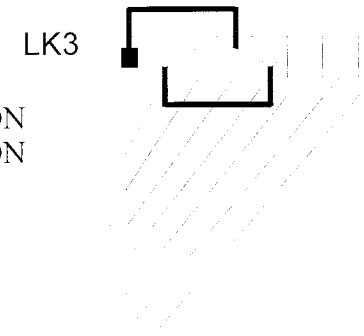
The relative position and default setting of the links is shown overleaf.

The default setting of links 19, 20 and 22, and links 44 to 51, and Link 35 are shown below.



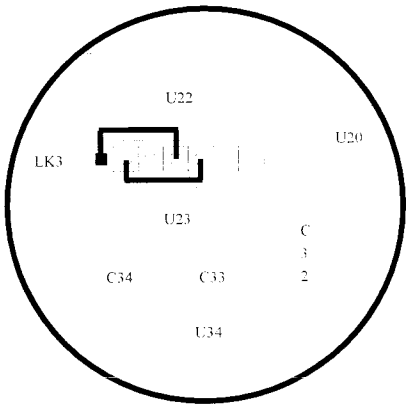
# Access Time Selection

The access time for each block is set up independently by wire wrapping between the appropriate block COMMON pin and the pin that indicates the delay time required. The relationship between the pins of LK3 and the delay time is shown below.



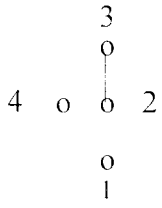
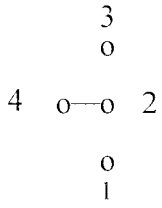
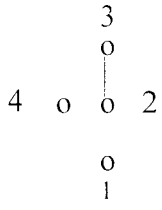
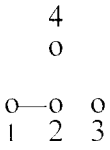
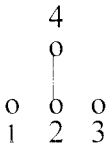
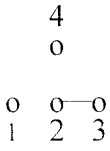

| | |
|---|---|
| Block 0 COMMON | |
| Block 1 COMMON | |
| 3 wait states | |
| 2 wait states | |
| 2 wait states | |
| 1 wait state | |
| 1 wait state | Default configuration, accesses to both memory blocks will incur 1 wait state |
| 0 wait states | |

The position of LK3 is shown below.



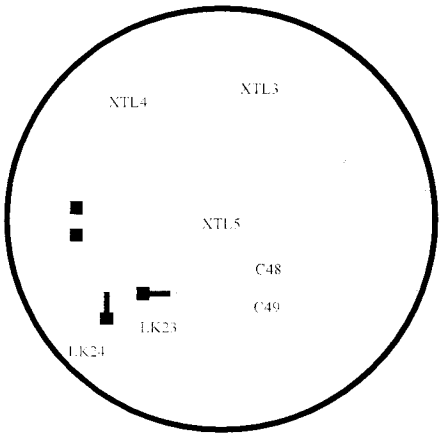
# Counter/Timers

The input to Counter Timer 1 is fixed at 250 kHz. The inputs to the other counter/timers can be from three different sources depending on the configuration of the two 4-pin links LK23/24.

| Link | Function | Configuration Options | |
|---|---|---|---|
| LK24 | C/T 2 input select |  | C/T 1 O/P selected |
| LK24 | C/T 2 input select |  | 250kHz clock selected |
| LK24 | C/T 2 input select |  | RTC O/P selected |
| LK23 | C/T 3 input select |  | C/T 2 O/P selected |
| LK23 | C/T 3 input select |  | 250kHz clock selected |
| LK23 | C/T 3 input select |  | RTC O/P selected |

The relative position of these links and their default setting is shown over the page.

Position and default setting of LK23 and LK24.



# IEEE 488 Interface

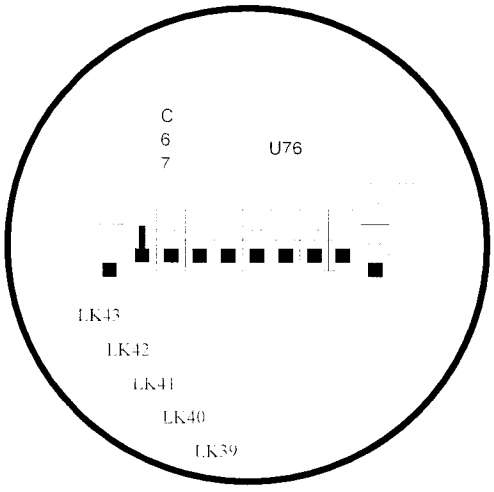
The address of the IEEE 488 interface is set by links and is made available to the processor via the status register.

The address bit is high when the link is open. A device on the IEEE 488 must not have an address consisting entirely of '1's (ie $1F).

The relationship between the address bits and the links is shown below:

| Link | Address Bit | Status Register Bit |
|---|---|---|
| LK43 | A1 | 0 |
| LK42 | A2 | 1 |
| LK41 | A3 | 2 |
| LK40 | A4 | 3 |
| LK39 | A5 | 4 |

The relative positions of links 39 to 43 are shown below along with the default settings.



# Serial Interface

The PME 68-14 is supplied with RS 232C drivers and receivers, and is configured for asynchronous operation. The user may replace the drivers with RS 422A drivers and receivers. As both channels use the same device, it is not possible to have a mixture of RS 232C and RS 422A.

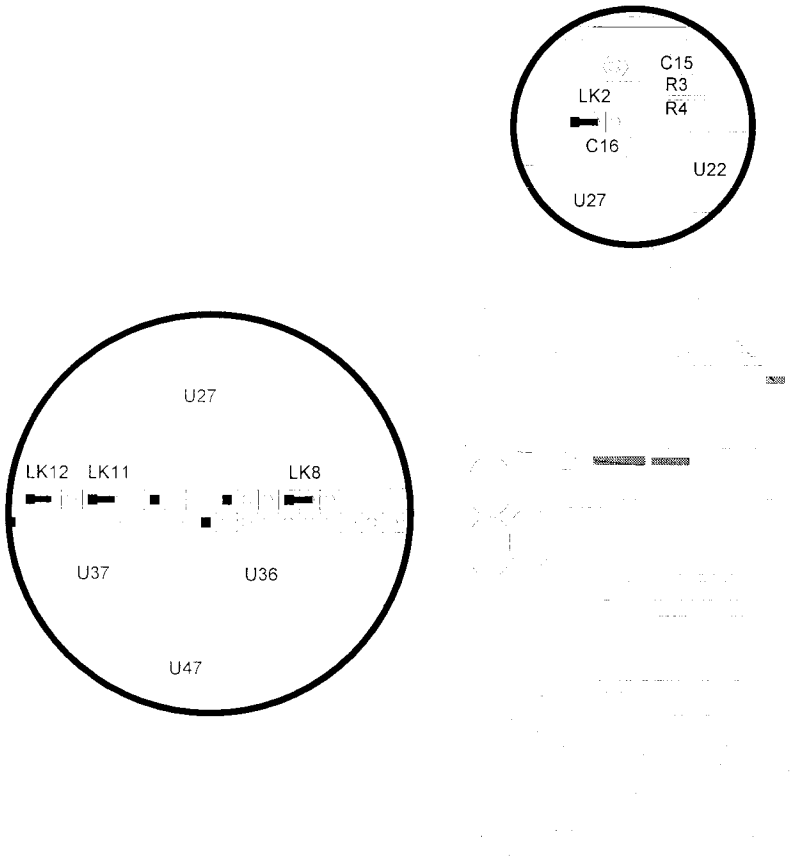
Note: For RS422A, resistors R7 to R13 should be 100kΩ, for maximum noise immunity.

| | **IC No.** | **IC Type** |
|---|---|---|
| **RS 232C** | | |
| Driver | U28 | MC1488 or equivalent |
| Receiver | U24 | MC1489 or equivalent |
| **RS 422A** | | |
| Driver | U26 | MC3487 or equivalent |
| Receiver | U25 | MC3486 or equivalent |

| **Link** | **Function** | **Configuration Options** | |
|---|---|---|---|
| LK2 | Channel A RxC/CTS* | o—o<br>o<br>o | CTS* selected |
| LK2 | Channel A RxC/CTS* | o<br>o—o<br>o | RxC selected |
| LK8 | Channel B RxC/CTS* | o—o<br>o<br>o | CTS* selected |
| LK8 | Channel B RxC/CTS* | o<br>o—o<br>o | RxC selected |
| LK12 | Channel A TxC/RTS* | o—o<br>o<br>o | RTS* selected |
| LK12 | Channel A TxC/RTS* | o<br>o—o<br>o | TxC selected |
| LK11 | Channel B TxC/RTS* | o—o<br>o<br>o | RTS* selected |
| LK11 | Channel B TxC/RTS* | o<br>o—o<br>o | TxC selected |

The relative positions and the default settings of links 2, 8, 11 and 12 are shown over the page.

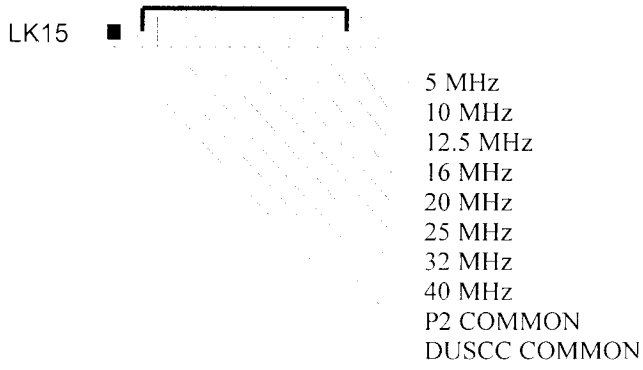
Positions and default settings of LK2, 8, 11 and 12.



# P2 Interface and DUSCC Clock Rate

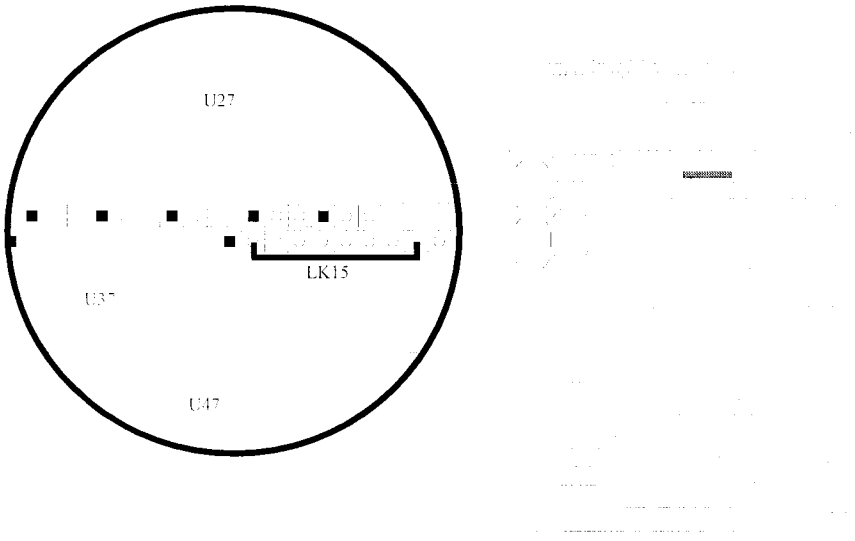
The clock rate fed to the P2 interface and the DUSCC is selectable by means of a 10-pin wire-wrap area, LK15.

To select the clock rate, the appropriate COMMON pin should be wire-wrapped to the pin that gives the required frequency referring to the figure below.




The above setting reflects the default configuration.

Note that if the DUSCC clock rate is set up using Link 15, it is necessary to remove C17, C18 and XTAL 1. The maximum clock rate for the DUSCC is 16 MHz.



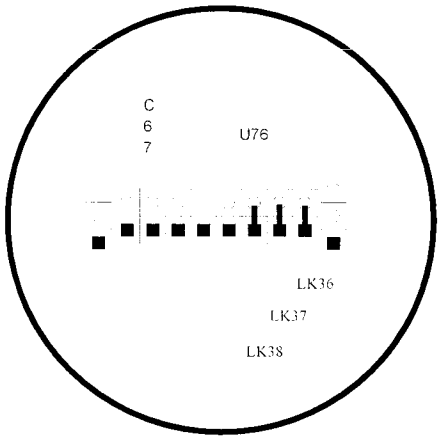
# User Status Links

The PME 68-14 has three user status links.

User status links are read via the status register. A bit is HIGH when the corresponding link is open. The relationship between links and status bits is given below.

| Link | Status Bit |
|---|---|
| LK36 | Bit 7 |
| LK37 | Bit 6 |
| LK38 | Bit 5 |

The relative positions of links 36 to 38 are shown below along with their default settings.

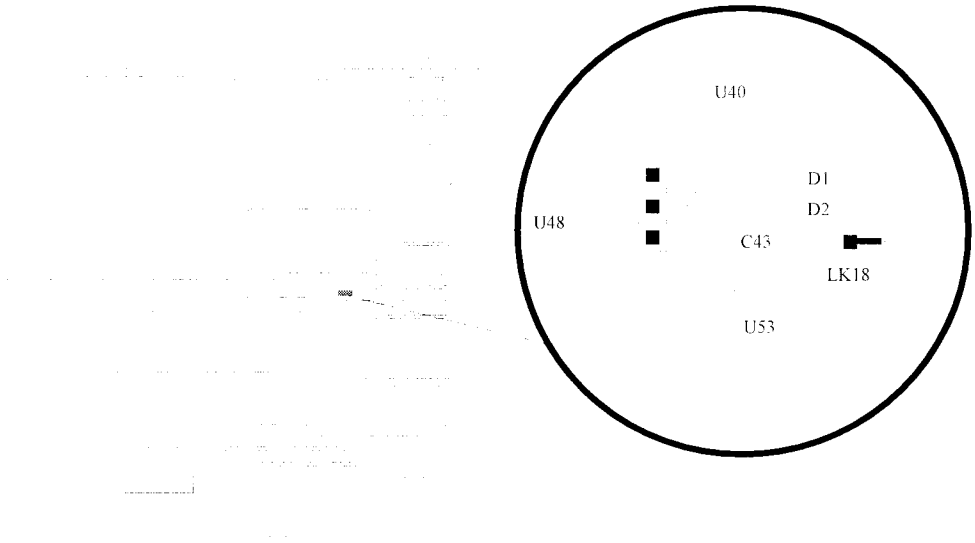


# SYSCLK Driver Module

The PME 68-14 provides a 16 MHz system clock as per the VMEbus specification. This facility may be disabled by removing LK18 as described below.

| | |
|---|---|
| Fitted: | PME 68-14 drives SYSCLK |
| Omitted: | PME 68-14 does not drive SYSCLK |

The relative position of LK18 is shown below.



# Bus Timeout Module

The Bus Timeout period is selected by means of four 2-pin links. These link positions correspond to the bit positions in a binary number; a bit is set when the link is removed. The timeout period is calculated by raising 2 to the power of this number and then multiplying the result by 200ns. The number must be between two and fifteen. The relationship between the links and the bit positions is shown below.

| Link | Bit |
|---|---|
| LK7 | Bit 3 |
| LK13 | Bit 2 |
| LK6 | Bit 1 |
| LK14 | Bit 0 |

The Bus Timeout module may be disabled by changing the position of LK1 as described below.

| Link | Function | Configuration Options | |
|---|---|---|---|
| LK1 | Bus Timeout enable/disable | o—o o<br>1 | Bus Timeout enabled |
| LK1 | Bus Timeout enable/disable | o o—o<br>1 | Bus Timeout disabled |

# Other Links

The PME 68-14 has other links provided that are not intended as user options. A description of these links is included here for completeness.

THESE LINKS SHOULD NOT BE ALTERED.

| Link | Function | Configuration Option | |
|---|---|---|---|
| LK29 | Master Request selection | Position 1<br>o—o o<br>1 | AS* is used as the strobe for CPU requests to the VMEbus |
| | | Position 2<br>o o—o<br>1 | The logical OR of DS0* and DS1* is used as the strobe for requests to the VMEbus |
| LK10 | Arbiter clock rate | Position 1<br>o—o o<br>1 | Arbiter clock rate is 20 MHz |
| | | Position 2<br>o o—o<br>1 | Arbiter clock rate is 32 MHz |
| LK9 | CPU clock rate | Position 1<br>o—o o<br>1 | CPU clock rate is 10 MHz |
| | | Position 2<br>o o—o<br>1 | CPU clock rate is 12.5 MHz |
| LK100 | DRAM RAS | Position 1<br>o—o o<br>1 | RAS connected to 74F764 |
| | | Position 2<br>o o—o<br>1 | RAS delayed from 74F764 |

# Chapter 5 - Timing

This chapter includes timing diagrams for VMEbus READ and WRITE cycles, and also for peripheral and miscellaneous transfers.

## P2 Interface Timing

The P2 interface is a buffered 68000 style interface. The complete AC Electrical Specification is given in Appendix A.

When using the P2 interface, The following points should be noted:

1. The P2 address bus, P2 data strobes and P2 address strobe are active during all CPU cycles, not just P2 accesses.

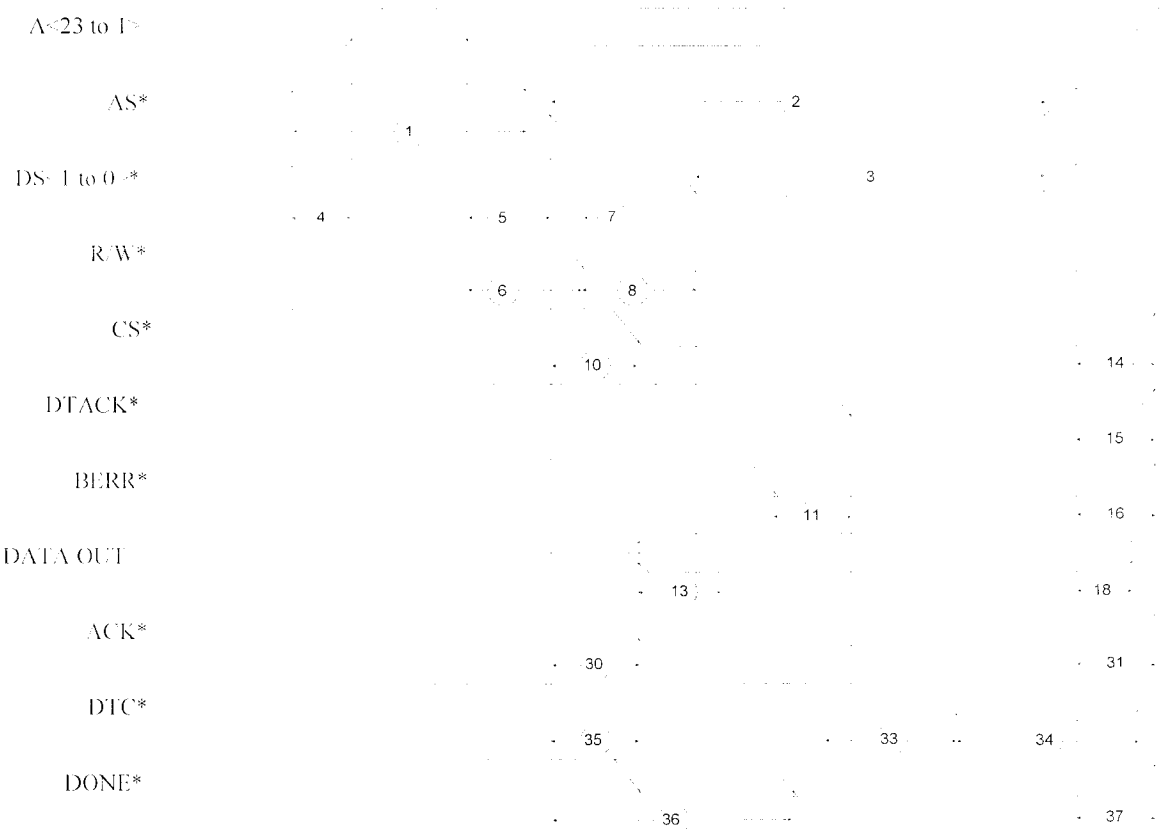
2. The CS* signal denotes a P2 access. It becomes active after the address bus, data strobe and address strobe, and it is used to enable the data bus. Usually the P2 data and address strobes will be gated with this signal, and will be part of any decode.

The table overleaf provides a key to the timing values used in the diagrams that follow. All the values are measured in nanoseconds except for "RESET width low" (number 40) which is measured in milliseconds.

## Timing Translation Table

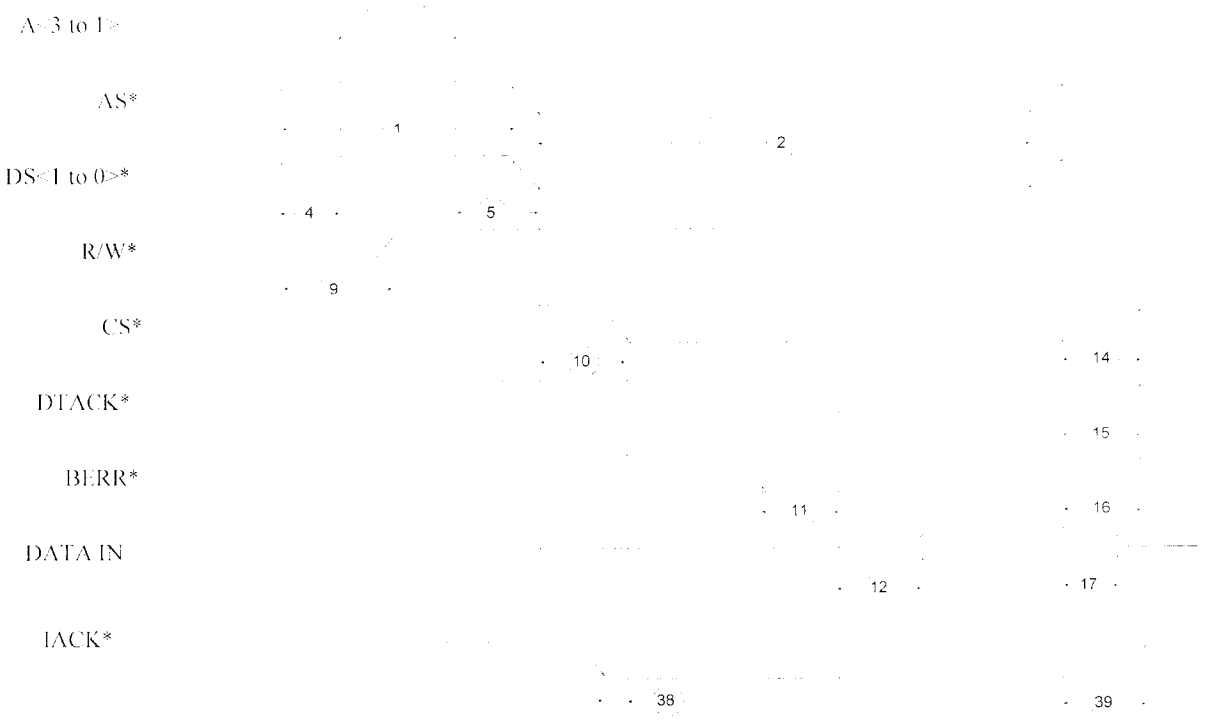
| Number | Characteristic | Min | Max |
|---|---|---|---|
| 1 | AS*/DS* width high | | |
| | AS*/DS* width low (READ) | 105 | - |
| 2 | AS* width low (WRITE) | 195 | - |
| 3 | DS* low (WRITE) | 95 | - |
| 4 | AS*/DS* high to ADDRESS invalid | 15 | - |
| 5 | ADDRESS valid to AS*/DS* low (READ) | | |
| | ADDRESS valid to AS* low (WRITE) | 5 | - |
| 6 | ADDRESS valid to R/W* low | 15 | - |
| 7 | AS* low to R/W* valid | - | 25 |
| 8 | R/W* low to DS* low (WRITE) | 35 | - |
| 9 | AS*/DS* high to R/W* high | 15 | - |
| 10 | AS* low to CS* low | 10 | 60 |
| 11 | BERR* low to DTACK* low | 30 | - |
| 12 | DTACK* low to DATA IN valid | - | 50 |
| 13 | DATA OUT valid to DS* low | 10 | - |
| 14 | AS*DS* high to CS* high | 10 | 60 |
| 15 | AS*/DS* high to DTACK* high | 0 | 175 |
| 16 | AS*/DS* high to BERR* high | 0 | - |
| 17 | AS*/DS* high to DATA IN invalid | 0 | - |
| 18 | AS*/DS* high to DATA OUT invalid | 15 | - |
| 19 | E width low | 550 | - |
| 20 | E width high | 350 | - |
| 21 | E rise and fall time | - | 55 |
| 22 | E extended rise time | - | 80 |
| 23 | E low to ADDRESS/VMA* invalid | 10 | - |
| 24 | AS* high to VPA* high | 0 | 80 |
| 25 | VPA* low to VMA* low | 120 | 1170 |
| 26 | DATA OUT valid to VMA* low | 235 | - |
| 27 | E low to DATA OUT invalid | 20 | - |
| 28 | VMA* high to DATA IN valid | - | 510 |
| 29 | REQ* width low | - | 300 |
| 30 | AS* low to ACK* low | 50 | - |
| 31 | AS* high to ACK* high | 100 | - |
| 32 | PCL width low | - | 300 |
| 33 | DTACK* low to DTC* low | 120 | - |
| 34 | DTC* width low | 100 | - |
| 35 | AS* low to DONE* low (DONE* as output) | - | 50 |
| 36 | AS* low to DONE* low (DONE* as input) | - | 300 |
| 37 | AS* high to DONE* high | - | 50 |
| 38 | IACK* low to CS* low | 0 | 20 |
| 39 | AS* high to IACK* high | - | 20 |
| 40 | RESET* width low | 1 | - |

## P2 Interface WRITE Cycle

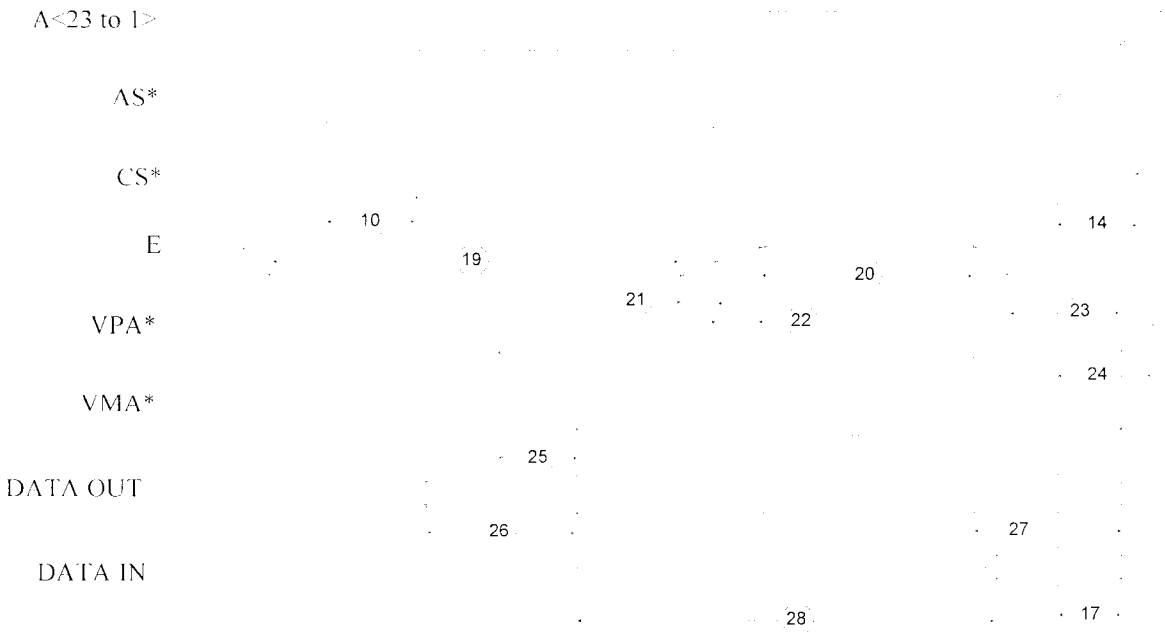


## P2 Interface READ Cycle

## P2 Interface IACK Cycle



## P2 Interface Peripheral Transfer



## P2 Interface Miscellaneous Transfer

| | | |
|---|---|---|
| REQ* | 29 | |
| PCL | 32 | |
| RESET* | 40 | |

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# Appendix A - P2 Interface Drive and Loading Specification

These specifications are over the full temperature and voltage operating range.

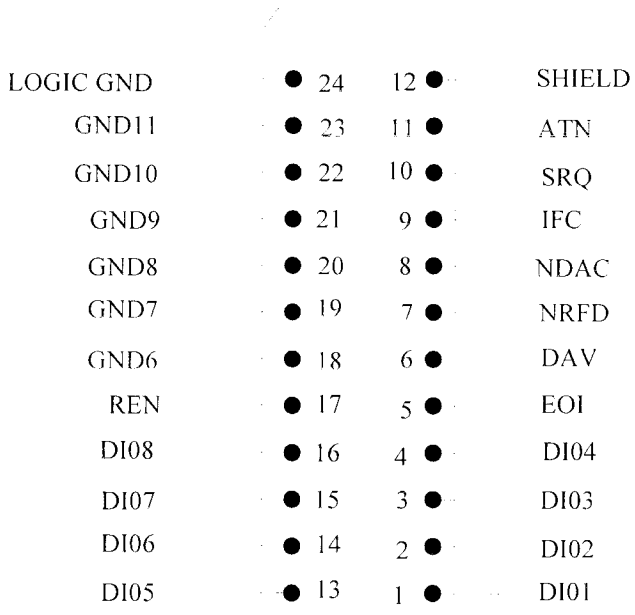
| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input High Voltage | VIH | 2.0 | Vcc + 0.5 | V |
| Input Low Voltage | VIL | -0.5 | 0.8 | V |
| Output High Voltage @max IOH | VOH | 2.0 | - | V |
| Output Low Voltage @max IOL | VOL | - | 0.55 | V |
| Input High Impedance Current (0 < VI < 5.5) | IIZ | - | 50 | µA |
| P2_AS*, P2_DS0*, P2_DS1*, P2_A01 to A07, P2_R/W*, P2_D00 to D15 | | - | 50 | µA |
| Input High Current (VI = 0V) | IIH | - | 10 | µA |
| P2_DREQ0*, P2_DREQ1*, P2_PCL0, P2_PCL1 | | - | 10 | µA |
| P2-INT*, VPA* | | - | 150 | µA |
| P2_DTACK*, P2_BERR* | | - | 400 | µA |
| Input Low Current (VI = 0V) | IIL | - | -10 | µA |
| P2_DREQ0*, P2_DREQ1*, P2_PCL0, P2_PCL1 | | - | -10 | µA |
| P2_INT*, VPA* | | - | -150 | µA |
| P2_DTACK*, P2_BERR* | | - | -400 | µA |
| Output High Current @ VOH | IOH | - | -12 | mA |

*P2 Drive and Loading Specifications continued*

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| P2_AS*, P2_DS0*, P2_DS1*, P2_CLK, P2_A01 to A07, P2_R/W*, P2-D00 to D15 | | - | -12 | mA |
| P2_IACK* | | - | -1 | mA |
| P2_DACK0*, P2_DACK1*, P2_DTC*, P2_DONE* | | - | -400 | µA |
| E, VMA* | | - | -375 | µA |
| PTMO | | - | -200 | µA |
| Output Low Current @VOL | IOL | - | 48 | mA |
| P2_AS*, P2_DS0*, P2_DS1*, P2_CLK, P2_A01 to A07, P2_R/W*, P2_D00 to D15 | | - | 48 | mA |
| P2_IACK* | | - | 20 | mA |
| P2_DONE* | | - | 8.9 | mA |
| P2_DACK0*, P2_DACK1*, P2_DTC* | | - | 5.3 | mA |
| P2_RESET* | | - | 5.0 | mA |
| E,VMA* | | - | 4.5 | mA |
| PTMO | | - | 3.2 | mA |
| P2_P12V, P2_M12V | | - | PSU -25 | mA |

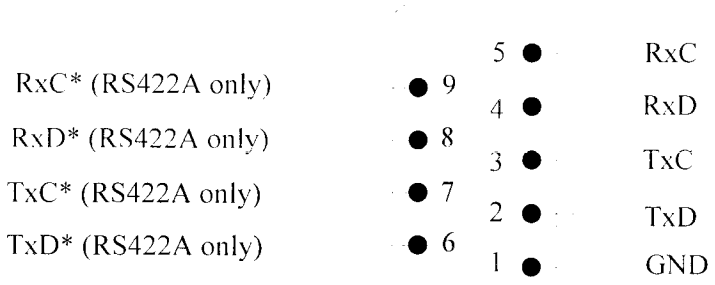
# Appendix B - Front Panel Connector Pin-outs

## IEEE 488 Interface Connector Pin-out (J3)

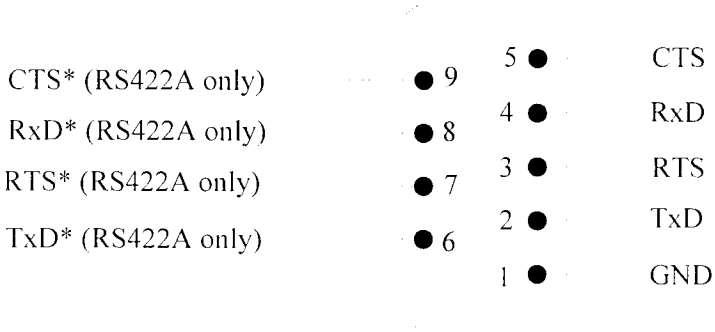


## Serial Interface Connector Pin-out (J1 and J2)

### Synchronous Signals




### Asynchronous Signals



# Appendix C - RS232C And RS422A Specification

## RS 232C Specification

When fitted with a 1488 driver and 1489 receiver, the PME 68-14 provides electrical signal characteristics compatible with RS 232C August 1969. This is equivalent to CCITT Recommendation V.24.

The interface circuits supported together with their equivalents are shown below.

AB (102) Signal Ground

BA (103) Transmitted Data

BB (104) Received Data

CA (105) Request to Send

CB (106) Clear to Send

DA (113) Transmission Signal Element Timing (DTE Source)

DB (114) Transmission Signal Element Timing (DCE Source)

DD (115) Receiver Signal Element (DCE Source)

Selection between DA and DB circuits is under software control. Selection between C* and D* are link selectable.

Inter-connection cables should be made up to conform to the RS 232C standard; the following notes are provided for general guidance.

The maximum recommended cable length is 15 metres (50 feet) at a transmission rate of 20k bits per second. Longer cables are permitted however, provided the resulting load capacitance, measured at the interface point and including the signal terminator, does not exceed 2500pF.

## RS422A Specification

When fitted with a 3487 driver and 3486 receiver, the PME 68-14 provides electrical signal characteristics compatible with RS 422A December 1978. This is equivalent to CCITT Recommendation V.11.

Inter-connection cables should be made up to conform to the RS 422A standard; the notes given here are for general guidance.

The maximum recommended cable length is 15 metres (50 feet) at a data rate of 10M bits per second using 24 AWG wires. Longer cables are permitted however, if slower data rates and/or thicker wires are used.

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# Appendix D - Reliability Figures

The failure rates used in this prediction are based on a combination of HRD3, MIL HDBK 217D and Radstone in-house data. They apply to commercial equipment in a benign environment.

| Part Type | Generic Class | Qty | lamda p | Total |
|---|---|---|---|---|
| PCB | | 1 | 0.375 | 0.375 |
| PAL | CMOS PAL | 7 | 0.01 | 0.07 |
| 68000/68010 | MOS VLSI | 1 | 0.6 | 0.6 |
| 68440/68450 | MOS VLSI | 1 | 0.6 | 0.6 |
| 68562 | MOS VLSI | 1 | 0.6 | 0.6 |
| 68154 | BIPOLAR VLSI | 1 | 0.8 | 0.8 |
| 68155 | BIPOLAR VLSI | 1 | 0.8 | 0.8 |
| 68172 | BIPOLAR VLSI | 1 | 0.8 | 0.8 |
| 6840 | MOS VLSI | 1 | 0.6 | 0.6 |
| MSM6242 | MOS VLSI | 1 | 0.6 | 0.6 |
| TMS9914A | MOS VLSI | 1 | 0.6 | 0.6 |
| 74LS764 | BIPOLAR SSI | 1 | 0.8 | 0.8 |
| 256k DRAM | DRAM | 16 | 0.1 | 1.6 |
| 74ALS541 | BIPOLAR MSI | 2 | 0.04 | 0.08 |
| 74ALS573 | BIPOLAR MSI | 2 | 0.04 | 0.08 |
| 74ALS621 | BIPOLAR MSI | 1 | 0.04 | 0.04 |
| 74ALS645-1 | BIPOLAR MSI | 21 | 0.04 | 0.84 |
| 74AS574 | BIPOLAR MSI | 1 | 0.04 | 0.04 |
| 74F00 | BIPOLAR SSI | 3 | 0.04 | 0.12 |
| 74F04 | BIPOLAR SSI | 2 | 0.04 | 0.08 |
| 74F08 | BIPOLAR SSI | 1 | 0.04 | 0.04 |
| 74F32 | BIPOLAR SSI | 5 | 0.04 | 0.2 |
| 74F74 | BIPOLAR SSI | 2 | 0.04 | 0.08 |
| 74F85 | BIPOLAR SSI | 2 | 0.04 | 0.08 |
| | | | Sub-total | 10.525 |

*calculations continued overleaf*

| Part Type | Generic Class | Qty | lamda p | Total |
|---|---|---|---|---|
| | | *carried forward* | | 10.525 |
| 74F86 | BIPOLAR SSI | 1 | 0.04 | 0.04 |
| 74F138 | BIPOLAR SSI | 3 | 0.04 | 0.12 |
| 74F139 | BIPOLAR SSI | 1 | 0.04 | 0.04 |
| 74F148 | BIPOLAR SSI | 1 | 0.04 | 0.04 |
| 74F161 | BIPOLAR SSI | 1 | 0.04 | 0.04 |
| 74F175 | BIPOLAR SSI | 1 | 0.04 | 0.04 |
| 74F367 | BIPOLAR MSI | 3 | 0.04 | 0.12 |
| 74F521 | BIPOLAR SSI | 1 | 0.04 | 0.04 |
| 74LS05 | BIPOLAR SSI | 1 | 0.04 | 0.04 |
| 74LS14 | BIPOLAR SSI | 1 | 0.04 | 0.04 |
| 74LS57 | BIPOLAR SSI | 1 | 0.04 | 0.04 |
| 74LS294 | BIPOLAR MSI | 1 | 0.04 | 0.04 |
| 74S38 | BIPOLAR SSI | 1 | 0.04 | 0.04 |
| AM29825 | BIPOLAR MSI | 1 | 0.04 | 0.04 |
| 1488/3487 | LINEAR | 1 | 0.12 | 0.12 |
| 1489/3486 | LINEAR | 1 | 0.12 | 0.12 |
| 75160 | LINEAR | 1 | 0.12 | 0.12 |
| 75162 | LINEAR | 1 | 0.12 | 0.12 |
| 555 | LINEAR | 1 | 0.12 | 0.12 |
| Delay Line | | 1 | 0.3 | 0.3 |
| Shottky Diode | | 2 | 0.012 | 0.024 |
| LED | | 3 | 0.07 | 0.21 |
| Crystal Oscillator | | 3 | 0.06 | 0.18 |
| Crystal | | 2 | 0.06 | 0.12 |
| Resistor Network | | 20 | 0.02 | 0.4 |
| Resistor | | 3 | 0.0004 | 0.0012 |
| Ceramic Capacitor | | 77 | 0.0006 | 0.0462 |
| Tantalum Capacitor | | 2 | 0.005 | 0.01 |
| DIL Switch | | 16 | 0.03 | 0.48 |
| Toggle Switch | | 2 | 0.2 | 0.4 |
| Link | | 40 | 0.01 | 0.4 |
| 9 way Connector | | 2 | 0.0063 | 0.0126 |
| 24 way Connector | | 1 | 0.0072 | 0.0072 |
| 96 way Connector | | 2 | 0.0288 | 0.0576 |
| IC Socket | | 492 | 0.000007 | 0.003444 |
| Solder Joint | | 26400 | 0.000007 | 0.1848 |
| | | | Total | 14.678044 |
| | | Failures per 1,000,000 hours | | 14.7 |
| | | | MTBF | 68,027 hours |