3827 OH

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Overview

1. Announcements
   - Upcoming Exams and Homework
   - Midterm
   - Feedback

2. Homework 5 Material
   - Overview and Relevant Lectures
   - General Part 3 Structure

3. Homework 6 Material
   - Relevant Lectures

Announcements

Announcements: Upcoming Exams and Homework

- HW5 due 4/1 (Ed post #252)
- HW6 due 4/4 (Ed post #256)

Announcements: Midterm

- Do not throw away your exam if you plan to request a regrade
- Form: `https://forms.gle/8S8WYGD2B8LSsRmt9`
- I cannot comment on how a certain question was scored since I may not have scored it
- I do not know how the different exams are relatively curved

Ed # 274

Announcements: Feedback

- Form: `https://forms.gle/cnUmKVNYN7WvRbHA6`

	Mean	Median	Stdev
Sec 1/2:	70	76	22.2
Sec 3:	49	51	21.5

Homework 5 Material

correct output with main → 3

no main → 2.5

→ 2

email

- All Part *n* references are for Part 2.*n* in the "Coding Details" part of HW5 (i.e. the programming parts)
- Introduction to MIPS programming (Lecture 07, Slides 35-81)
- Conditional logic in MIPS (Lecture 07, Slides 82-95)
- Stack pointer and recursion (Lecture 07, Slides 96-111)   *testing*
- MIPS calling conventions (Lecture 07, Slides 112-166)   *Part 1*
- For Part 3 (AddAndVerify), use new testing program   *Part 2*
  test—AddAndVerify—plus.s on CourseWorks
  - The original does not print any decrypted string even if you are correct
  - Also original says "ALL DONE" even if you are wrong   *ALL DONE*
  - It is fairly clear when the new testing code outputs correct string
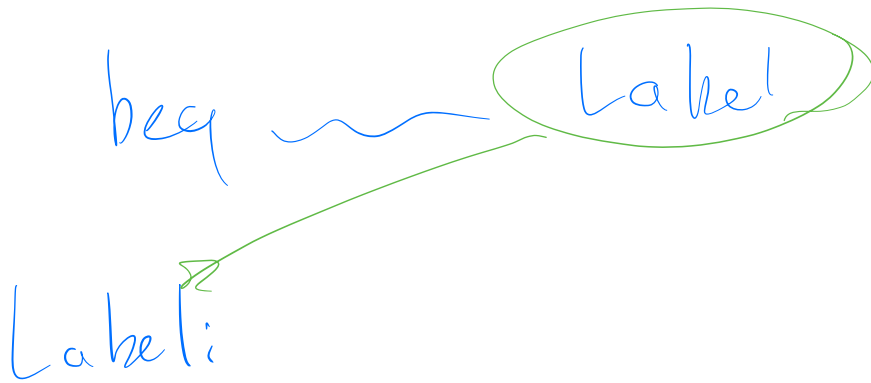- For the main message (Part 4), the last four characters can be ignored

COMPLETE   *"DOAH"*

beq ⟶ Label

Label:

Part l:

be sure to use
unsigned instructions

(addu, sltu)

sorry in breakout
room.

```
1    AddAndVerify:
2        # Base case checking/branching
3        # If not base case, push to stack using 'sw'
4        # Other necessary operations
5        jal   AddAndVerify
6        # Pop from stack
7        # Check $v0 to see if suffix is valid for branching
8        # Other necessary operations
9        jal   WordDecrypt
10       # Other necessary operations
11       jal   IsCandidate
12       # Other necessary operations such as writing to destination address
13       jr    $ra
```
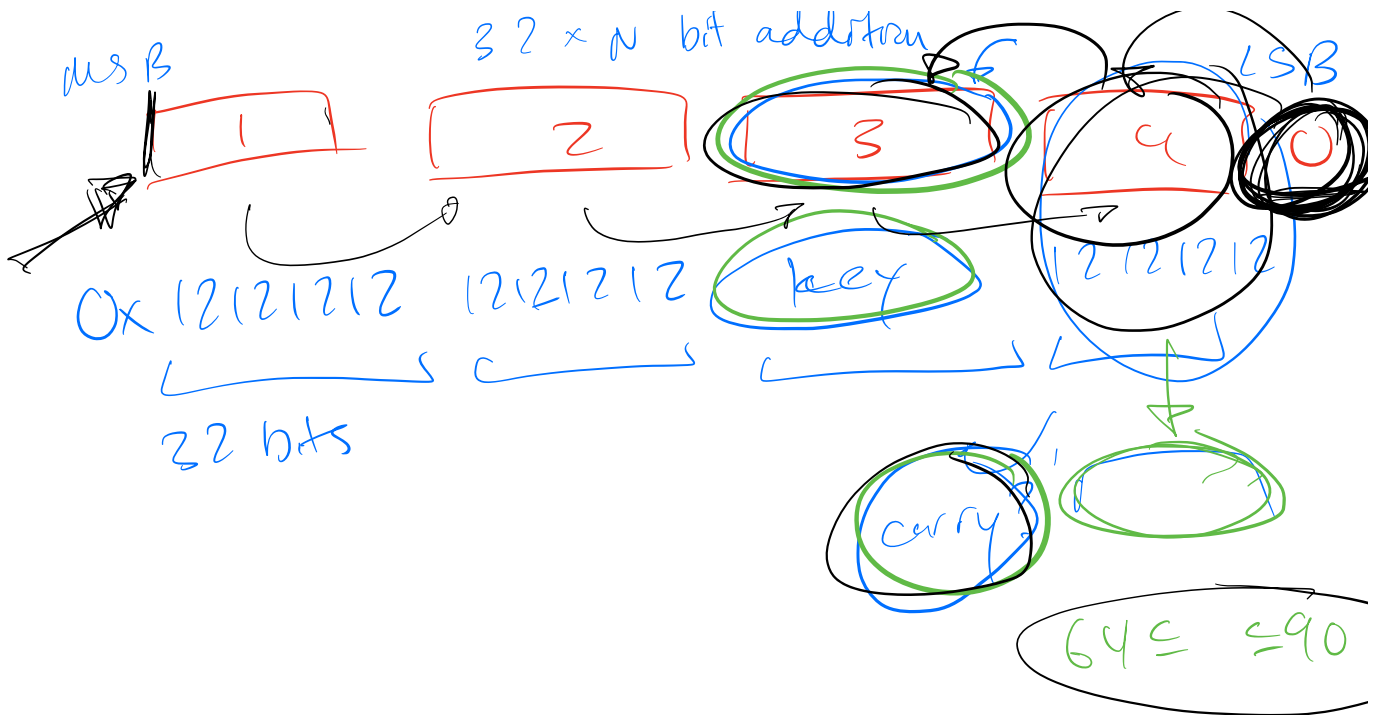
addi $a0, 4

Base case:
li $v0,
jr $ra

load in $v1

carry

0 into

- This is just a rough outline – you must fill in the rest of the code

MSB

32 × N bit addition

LSB

| 1 | 2 | 3 | 4 | 0 |

Ox 12121212   12121212   key   12121212

32 bits

carry

$64 \subseteq \ \leq 90$

Homework 6 Material

- Coincident selection (Lecture 10, Slides 41-58)
- Scaling memory using multiple chips (Lecture 10, Slides 59-85)