

3827 OH

Eumin Hong (eh2890)

Columbia University

April 12, 2022

Overview

1 Announcements

- Upcoming Exams and Homework

2 Homework 8 Material

- Feedback
- Overview and Relevant Lectures

Announcements

Announcements: Upcoming Exams and Homework

- HW8 due 4/15

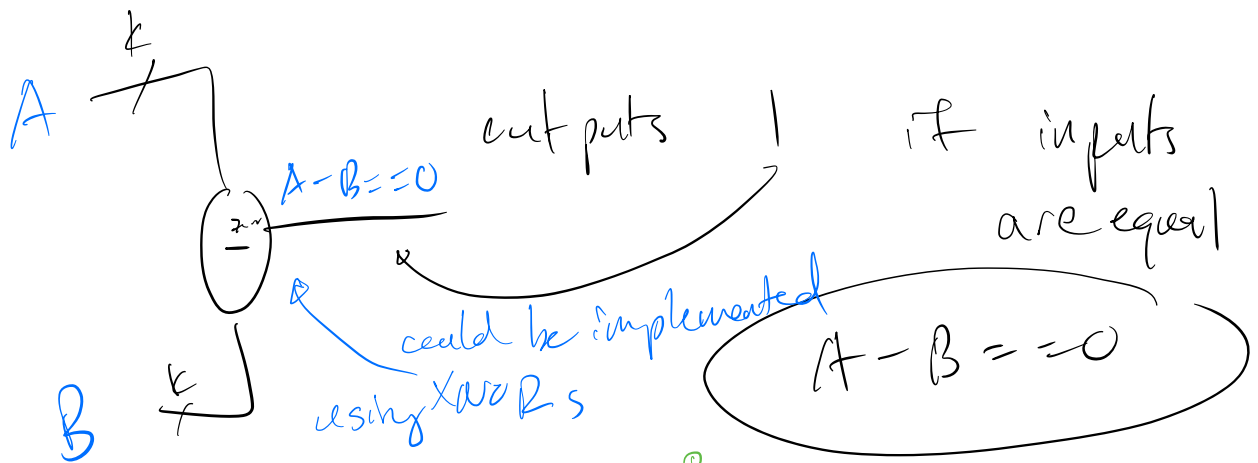
Announcements: Feedback

- Form: <https://forms.gle/cnUmKVNYN7WvRbHA6>

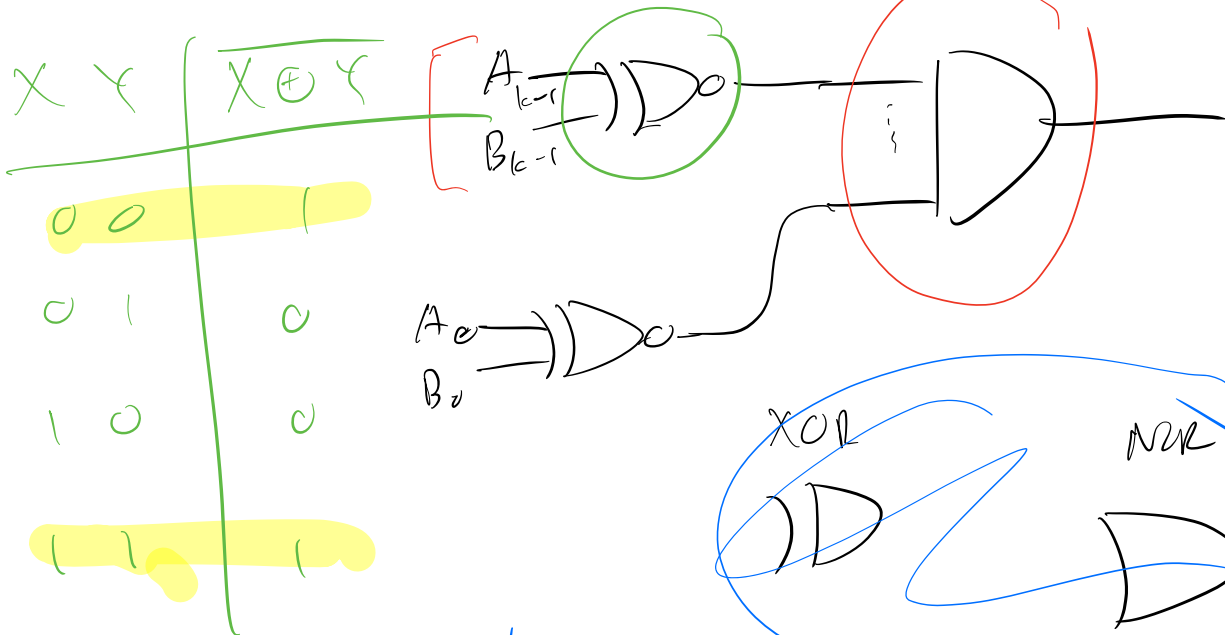
Homework 8 Material

Homework 8 Material: Overview and Relevant Lectures

- Q1, Q2
 - Five stages of MIPS pipeline, but without pipeline registers (Lecture 12, Slide 17)
 - Pipelined CPU with controls (Lecture 12, Slide 58)
 - Q3
 - Examples of instructions in pipeline (Lecture 12, Slides 32-53)
 - Q3, Q4
 - Dependencies (Lecture 12, Slides 59-67) *Q3a*
 - Hazards (Lecture 12, Slides 68-81) *Q3b*
 - Avoiding Hazards with NOP (Lecture 12, Slides 82-87) *also stalls*
 - Write-before-Read Reg File (Lecture 12, Slides 88-100)
 - Data Hazard Handling (Lecture 12, Slides 108-171)
 - Data Forwarding (Lecture 12, Slides 132-171) *Q3c*
 - Q5
 - Branching Hazard Resolution (Lecture 12, Slides 188-199)
 - Move Conditional Check Forward, or Early Branch Resolution (Lecture 12, Slides 200-220) *TD*
 - Example for early branch resolution (Lecture 12, Slides 241-249)
 - Hazard Resolution Examples (Lecture 12, Slides 221-249)
- Handwritten notes:* Q1, Q2 (ALU vs. Mem), data, control, build pipeline register, add \$t0, add \$t0, \$t0



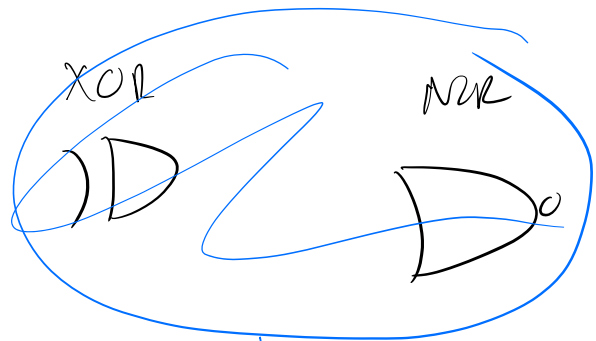
$$A_{k-1} == B_{k-1}$$



Shift left by 2
 \rightarrow multiplying by 4

(or concatenating 2 "0"s)

$$\dots B_k \dots B_0 \xrightarrow{\text{sl2}} \dots B_k \dots B_0 00$$



transistor count