

# 3827 OH

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# Overview

## 1 Announcements

- Upcoming Exams and Homework

## 2 Homework 8 Material

- Feedback
- Overview and Relevant Lectures

# Announcements

# Announcements: Upcoming Exams and Homework

- HW8 due 4/15

# Announcements: Feedback

- Form: <https://forms.gle/cnUmKVNYN7WvRbHA6>

# Homework 8 Material

# Homework 8 Material: Overview and Relevant Lectures

- Five stages of MIPS pipeline, but without pipeline registers (Lecture 12, Slide 17) *Q1, Q2* *IF ID EX WB 5 → 4* *lw \$s1, \$s2 ALU vs Mem*
- Pipelined CPU with controls (Lecture 12, Slide 58)
- Examples of instructions in pipeline (Lecture 12, Slides 32-53)
- Dependencies (Lecture 12, Slides 59-67) *Q3a* *data and control*
- Hazards (Lecture 12, Slides 68-81) *add \$t0, \$t0, \$t0* *sub \$t0, \$t0, \$t0*
- Avoiding Hazards with NOP (Lecture 12, Slides 82-87) *Q3b* *add \$t0, \$t0, \$t0* *sub \$t0, \$t0, \$t0*
- Write-before-Read Reg File (Lecture 12, Slides 88-100) *10/11*
- Data Hazard Handling (Lecture 12, Slides 108-171)
  - Data Forwarding (Lecture 12, Slides 132-171)
- Branching Hazard Resolution (Lecture 12, Slides 188-199) *beg \$t0, \$t0, \$t0* *label*
- Move Conditional Check Forward, or Early Branch Resolution (Lecture 12, Slides 200-220)
  - Example for early branch resolution (Lecture 12, Slides 241-249) *Q5*
- Hazard Resolution Examples (Lecture 12, Slides 221-249)