3827 OH

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Overview

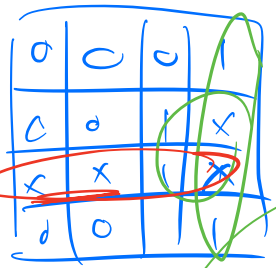
Announcements

Announcements: Upcoming Assessments

- For HW4, do not hand in "Warmup Problems"
- HW4 is due on Friday 2/25
- HW2 is graded

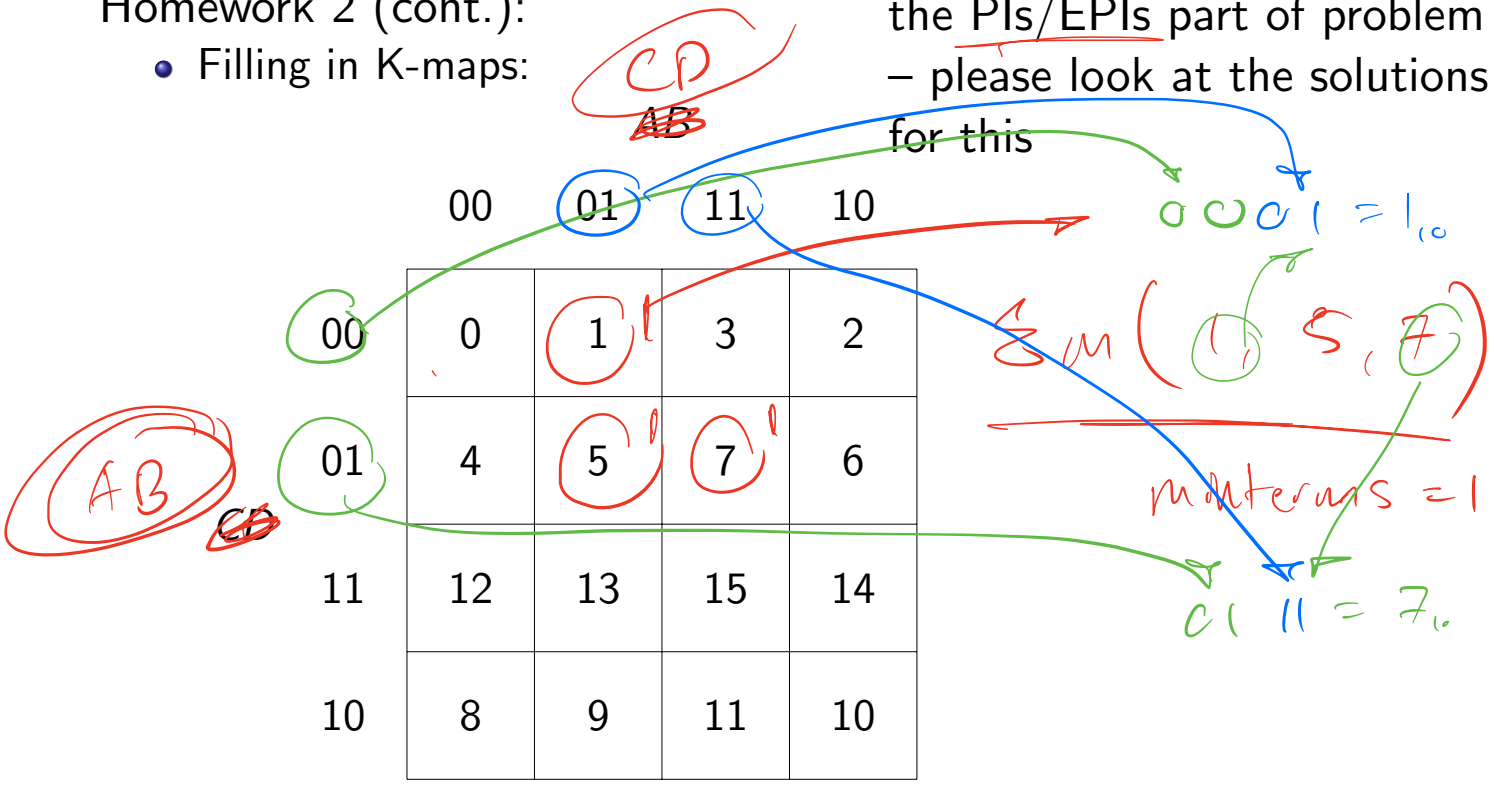
Announcements: Homework 2 Feedback

- Common errors from Homework 2:
  - Neither $AB + \bar{A}\bar{B}$ nor $A\bar{B} + \bar{A}B$ are equal to 0 (XNOR and XOR respectively)
  - SoP and PoS forms must be logically equivalent – PoS is not the negation of SoP form, but can be found by negating twice
  - Don't cares do not have to be included when choosing prime implicants (hence their name)



Announcements: Homework 2 Feedback (cont.)

- Common errors from Homework 2 (cont.):
  - Filling in K-maps:



- I did not comment much on the PIs/EPIs part of problem 7 – please look at the solutions for this

Announcements: Feedback

- Form: `https://forms.gle/cnUmKVNYN7WvRbHA6`

Homework 4 Warmup

Homework 4 Warmup: Problem 1

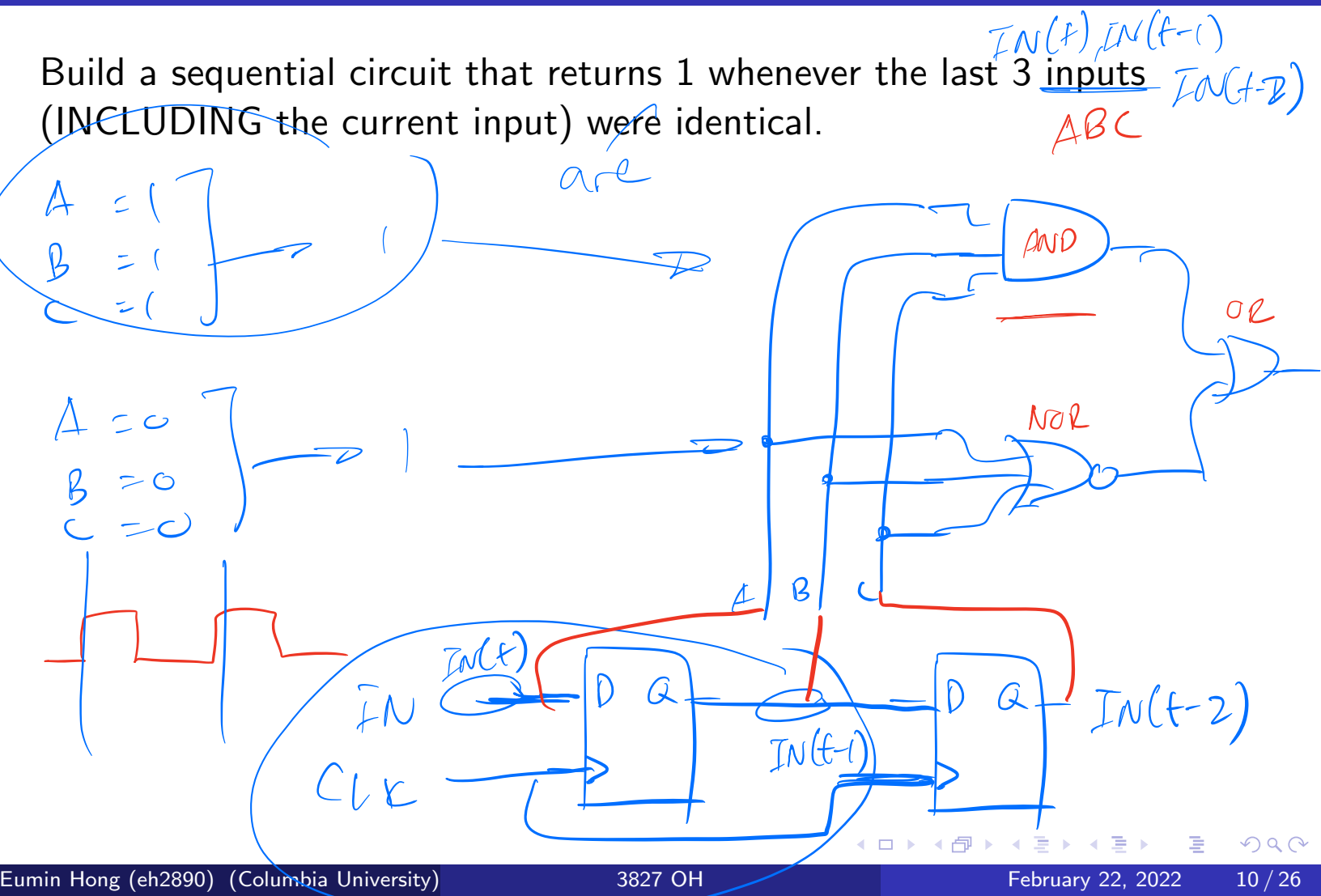
Build

(a) a T flip-flop out of a D flip-flop and combinational circuitry.

(b) a D flip-flop out of a T flip-flop and combinational circuitry.

Homework 4 Warmup: Problem 2

Build a sequential circuit that returns 1 whenever the last 3 inputs (INCLUDING the current input) were identical.



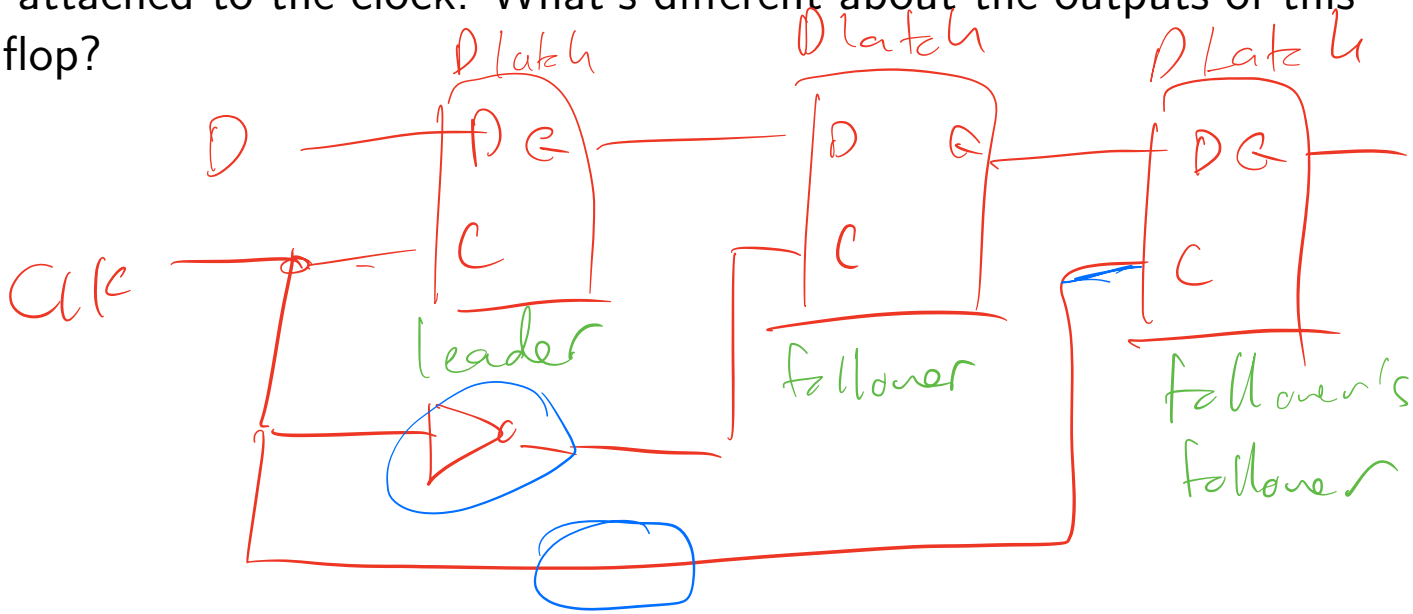
Homework 4 Warmup: Problem 3

Build a sequential circuit that returns 1 whenever the last 3 inputs (PRIOR to the current input) were identical.

Homework 4 Harder Problems

Homework 4 Harder Problems: Problem 1

A special flip-flop is formed from three latches, arranged in sequence. The first two latches behave as in a normal flip-flop: the leader latch's enable is attached to the clock, and the followers enable is attached to the complement of the clock. The third latch, which follows the follower, is also attached to the clock. What's different about the outputs of this flip-flop?



Homework 4 Harder Problems: Problem 2

Design a circuit using JK flip-flops that takes in a binary stream $B_0B_1B_2B_3\cdots$ and outputs a 1 at time t if the streams received thus far (i.e., $B_0B_1\cdots B_{t-1}B_t$), when read as an unsigned binary number from low bit to high, is divisible by 3.

The following table depicts a sample input stream and what should be output.

t	0	1	2	3	4	5	6	7	8
$In(t)$	0	0	1	1	0	0	1	0	0
Val of input	0	0	4	12	12	12	76	76	76
Val mod 3	0	0	1	0	0	0	1	1	1
Output	1	1	0	1	1	1	0	0	0

1) understand table 3) Truth table 5) Boolean expr.

2) FSM 4) Add FF logic 6) Circuit.

$B_t B_{t-1} \cdots B_1 B_0 = B$

$B = B_1 B_0 = 10$

$B_2 = 0$

010

2 mod 3

$B_3 = 1$

1010 → $(10)_{10}$

1 mod 3

$B_2 = 1$

110 → $(6)_{10}$

0 mod 3

$(2)_{10}$

2 mod 3

for B_t where t is even → 4^n

for B_t t is odd

$2 \cdot B_{t-1}$

$2 \cdot 4^n \equiv 2 \cdot 1 \bmod 3$

$4 \equiv 1 \bmod 3 \Rightarrow 4^n \equiv 1^n \bmod 3$

B_2, B_4

B_6

4 → 100 → 64 → 1000000

16 → 10000

Homework 4 Harder Problems: Problem 2 (cont.)

Hint: The value of the new bit starts as equal to 1 which is 1 $\mod 3$, then is 2 which is 2 $\mod 3$, then is 4 which is back to 1 $\mod 3$, etc.

a. Draw the state machine, numbering your states in an "obvious" manner. You may assume that the machine starts in the right state at time $t = 0$.

$0_0\ 0_1\quad 1_0\ 1_1\quad 2_0\ 2_1$

b. Give the algebraic formula (simplified as much as possible) for the J and K inputs of your flip-flops, and also for the output.

Homework 4 Harder Problems: Problem 3

Consider a sequential circuit that reads in an input $X(t)$ during clock cycle t. The circuit should look for the sequence 011. Design the sequential circuit (i.e., give simplified algebraic expressions) using D flip-flops for each of the following versions:

(a) If the second 1 arrives during clock cycle t, then the circuit should output a 1 during clock cycle t, and otherwise outputs a 0.

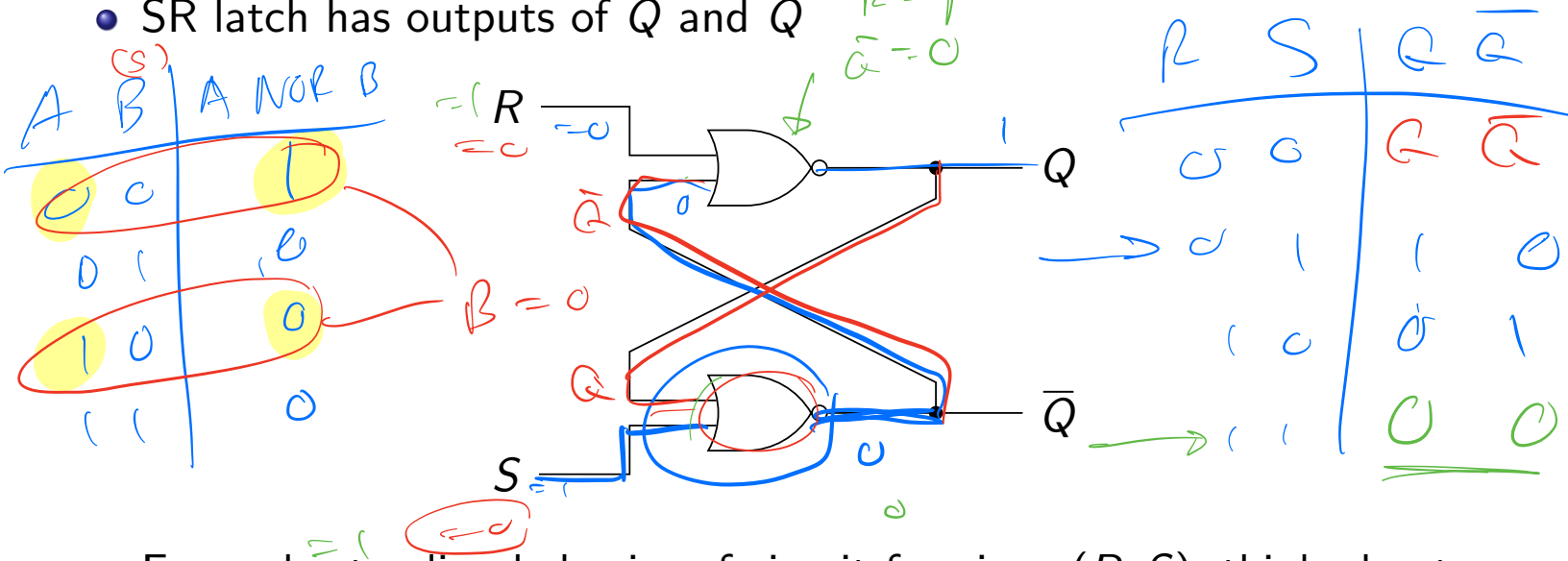
(b) If the second 1 arrives during clock cycle t, then the circuit should output a 1 during clock cycle $t+1$, and otherwise outputs a 0.

(c) Suppose the sequence is 111 instead of 011. If at time t, the current and two previous inputs were all 1, then a 1 should be output during clock cycle t, and otherwise a 0 should be output. Note that multiple consecutive outputs of 1 are possible.

Homework 4 Topics

Homework 4 Topics: SR Latch

- Latches just hold state – can be changed by changing the values of the inputs
- SR latch has inputs of "Set" (S) and "Reset" (R)
- SR latch has outputs of Q and $\overline{Q}$



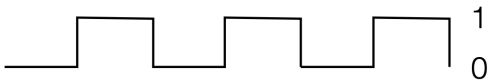
- For understanding behavior of circuit for given (R, S), think about when NOR operation gives 0
  - Or more generally, passing a constant to a gate can make its output constant as well

Homework 4 Topics: D Latch

- Basically SR latch with some more circuitry to avoid "illegal" combinations of inputs (e.g. when $R = 1, S = 1$ what does the SR latch do? How can it "set" $Q = 1$ and "reset" $Q = 0$ at the same time?)
- D latch has inputs D and C (control, which ensures $S \neq R$ in the underlying SR latch)
  - D is the value to store/write if $C = 1$
  - C can also be E for enable

Homework 4 Topics: Clocking

- Clock signal oscillates between 0 and 1 with a fixed period
  - "Rising edge" of clock signal is the transition from "low" to "high" (i.e. $0 \rightarrow 1$)



  - Kind of like a metronome, gives the circuit a sense of time on which it can operate
  - Why should I care about clock? It determines the rate at which instructions are executed

Apple M1

Apple M1 chip

General information

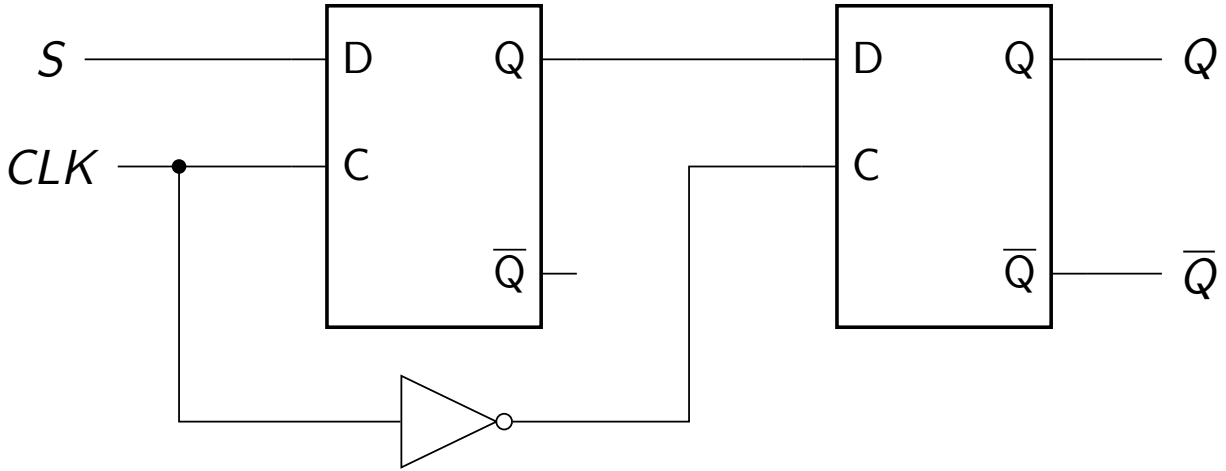
Launched	November 10, 2020[1]
Designed by	Apple Inc.
Common manufacturer(s)	TSMC
Product code	APL1102[2]

Performance

Max. CPU clock rate	3.2 GHz[1]

Homework 4 Topics: Flip-Flops

- Latches do not support clocking individually
- Connecting latches in series (and ensuring that the clock inputs are complemented or staggered) acts as a flip-flop
- Example of D Flip-Flop:



- Left D latch is updated when $CLK = 1$ (new inputs read to left D latch), right D latch is updated when $CLK = 0$ (load new inputs to right D latch)

Homework 4 Topics: Flip-Flop Behavior

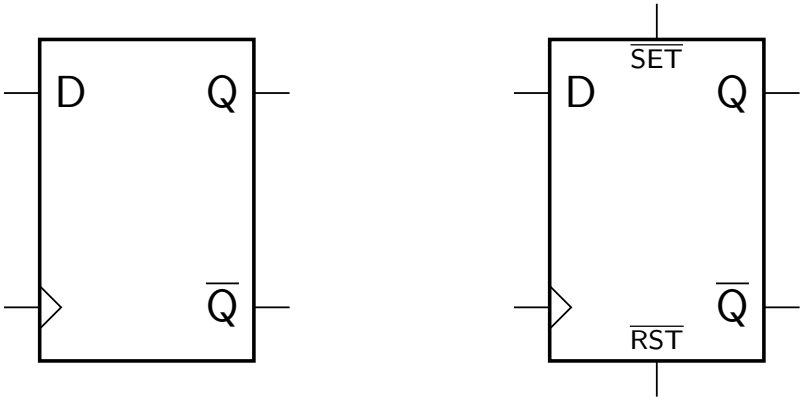
- For the D flip-flop:

$D(t)$	$Q(t+1)$
0	0
1	1

- The input t is time, or more specifically, the tth clock cycle
  - A clock cycle is one period of the clock
- In other words, the input D at clock cycle t becomes the output Q at clock cycle $t+1$ (the next clock cycle)

Homework 4 Topics: Flip-Flop Abstraction

- The two latch circuit from earlier is abstracted and is a D flip-flop (D since it has the same inputs as a D latch) (left circuit)



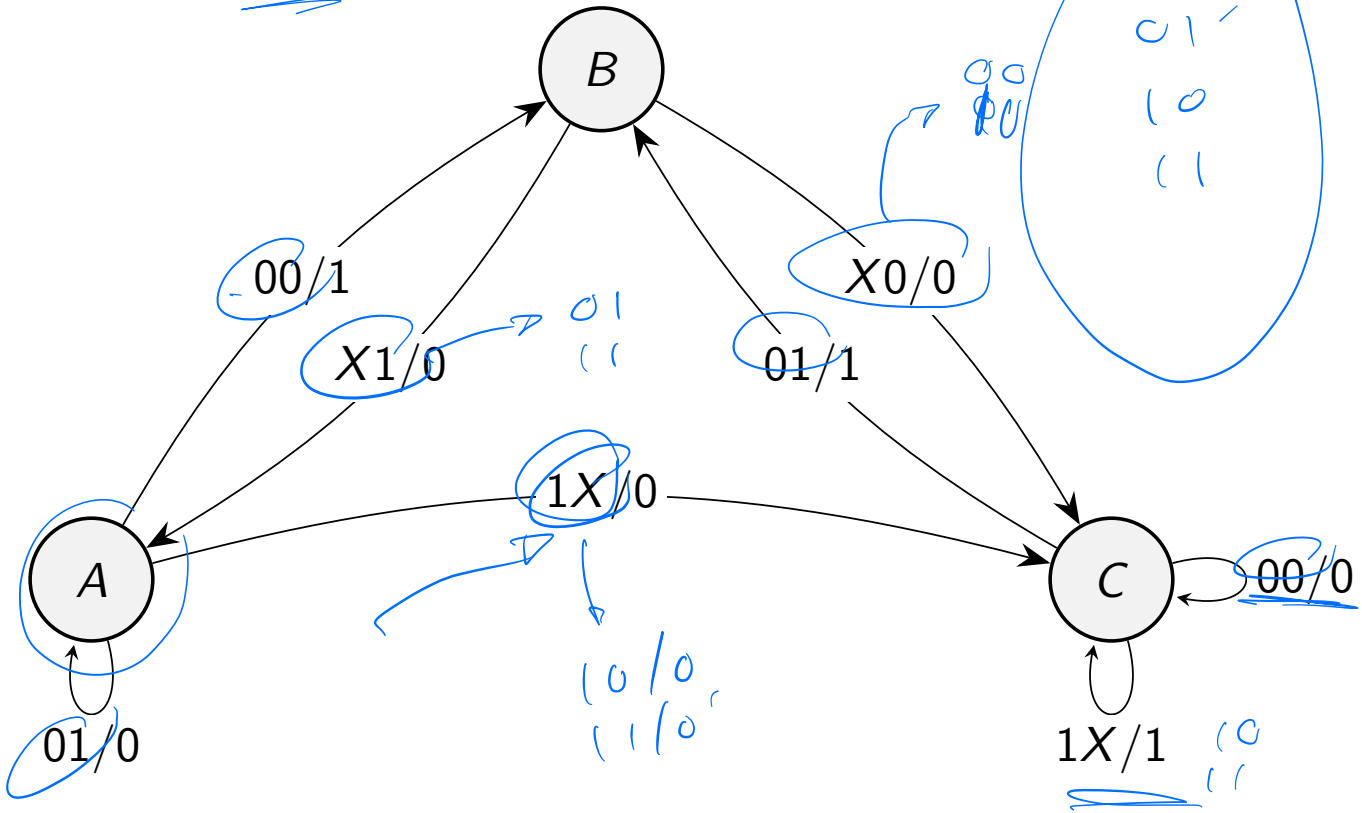
- The triangular input (bottom left) is for the clock signal
- How do we initialize the values of a flip-flop?
  - Use set and reset inputs (right circuit), implementation is not necessary to know (we are not really worried about initialization in this course)

Homework 4 Topics: State Machines

- We will worry about Mealy form – output is based on ~~transition~~ input and state, rather than just state
- Let the inputs be $I = I_{n-1}I_{n-2}\cdots I_1 I_0$ and the outputs be $O = O_{m-1}O_{m-2}\cdots O_1 O_0$
- Then, for every state in the FSM, there must be $2^{|I|}$ transitions accounted for, each corresponding to $I_{n-1}I_{n-2}\cdots I_1 I_0 / O_{m-1}O_{m-2}\cdots O_1 O_0$ (but replace with 0s and 1s, so something like $01\cdots00/11\cdots10$)
  - Why $2^{|I|}$? Because every combination of inputs must appear exactly once for each state since we will deal with deterministic FSMs

Homework 4 Topics: State Machines (cont.)

- Example: $I = I_1 I_0$, $O = O_0$



Homework 4 Topics: FSM to Circuits

- High-level approach to go from problem to circuit
  1. FSM
  2. Truth table in terms of just current state bits and next state bits
  3. Add columns for flip-flops to go from state bit $A(t)$ to next state bit $A(t+1)$
  4. Derive K-maps for each output (overall output and flip-flop inputs)
  5. Boolean expression
  6. Circuit
- Choice of flip-flop
  - D flip-flops results in fewer outputs/K-maps
  - JK flip-flops results in simpler expressions
  - You will be told which flip-flop to use