Final Exam

CSEE W3827 - Fundamentals of Computer Systems S2: April 22, 2021
Spring 2021 Prof. Rubenstein

This final contains 3 questions (not counting question 0), totaling 90 points. Question 0 gives an additional 10 points. To get full credit you must answer all questions. **BOOKS AND NOTES ARE PERMITTED, ELECTRONIC DEVICES CAN BE USED FOR NON-COMPUTATIONAL PURPOSES AND NON-SEARCH PURPOSES.** The time allowed is 180 minutes, plus an additional 15 minute grace period to deal with upload/download issues.

Please format your exam as follows:

- Start each question on a separate page
- The file you upload should start with your UNI (preferably all lower-case).

Some advice:

- Be sure to leave some time to work on each problem. The right answer to each problem does not require a very long answer.
- Be sure to start every problem. And take some time to think about how to set the problem up before you start writing.

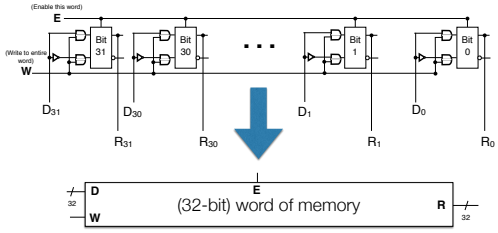
0. **10 points** The filename of your upload must start with your UNI (all lower case letters preferred) to receive these 10 points.

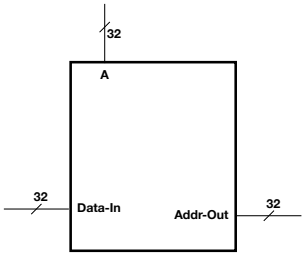
1. Given $s0 holds a 32-bit data value and $s1 holds an address, the MIPS code that sets $s1 to the address in memory (after where $s1 initially points) that holds a value matching the value in $s0 is as follows:

```
START:
    lw $s2, 0($s1)
    beq $s2, $s0, DONE
    addi $s1, $s1, 4
    j START
DONE:
```

Each loop in the above takes 4 clock cycles, so if the first match occurs 4*N addresses later, finding that address would take 4*N clock cycles.

We could, instead, build this functionality into the memory itself.

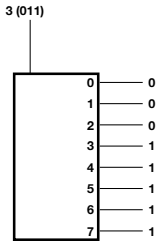


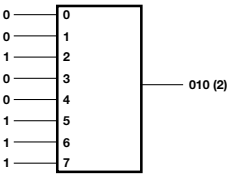


Show how to implement a memory whose circuitry can provide this result. (Do not worry about having your memory implement normal "reads" and writes"). The memory is depicted above right takes in a starting address A, a value to search for (Data-In), and returns the first address after A that matches this value, returning 0 if no such address is found.

To build your memory you may use:

- Word slices of memory whose design is depicted above left.
- A specialized decoder that takes as input a k-bit string S and outputs a 0 on all outputs whose number is less than S (interpreted as an unsigned binary), and outputs 1 on all other outputs. An example with $S = 3$ is depicted below left.
- A specialized encoder circuit that takes 2^k inputs (numbered from 0 to $2^k - 1$) and returns the number (as an unsigned binary) of the lowest-numbered input that equals 1, returning 0 if no input equals 1 (and of course if the 0th input equals 1). An example is depicted below right where input 2 is the first non-0.





2. (30 points) Recall that the following code snippets respectively "push" and "pop" items on/off the stack:

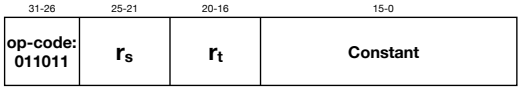
```
## code for push                    ## code for pop
addi $sp, $sp, -4                   lw $s0, 0($sp)
sw $s0, 0($sp)                      addi $sp, $sp, 4
```

Suppose the following instructions are added to the instruction set architecture that have the same behavior as above:

```
## copy $s0 onto top of stack       ## remove stack top, place in $s0
push $s0                            pop $s0
```

(a) (10 pts) The architecture in the above figure is enhanced from the normal architecture only in that the MUX that feeds into the Write Register of the Register File can select from three possible locations in the instruction word (instead of the normal two).

Assuming the stack pointer register $sp remains in the register file as register number 29 (11100 in 5-bit binary), using the existing architecture, explain how to implement **push $rx** within this architecture when the 32-bit instruction has the format:



Explain:

i. (5 pts) How the fields in the instruction should be filled in? (I.e., what should r_s, r_t and constant be set to, given that the only information in the instruction itself is the register $rx whose data should be pushed onto the stack?)

ii. (5 pts) What should the value of each of the fields exiting the Control circuit be? For ALUOp, you can just indicate the operation (i.e., '+', '-', AND, OR, shift-left, etc.) as opposed to giving the 2-bit Op code.

(b) (5 pts) To implement pop, we need to implement the $sp register outside of the register file (similar to how the program counter lies outside the register file). Explain why (one sentence should suffice).

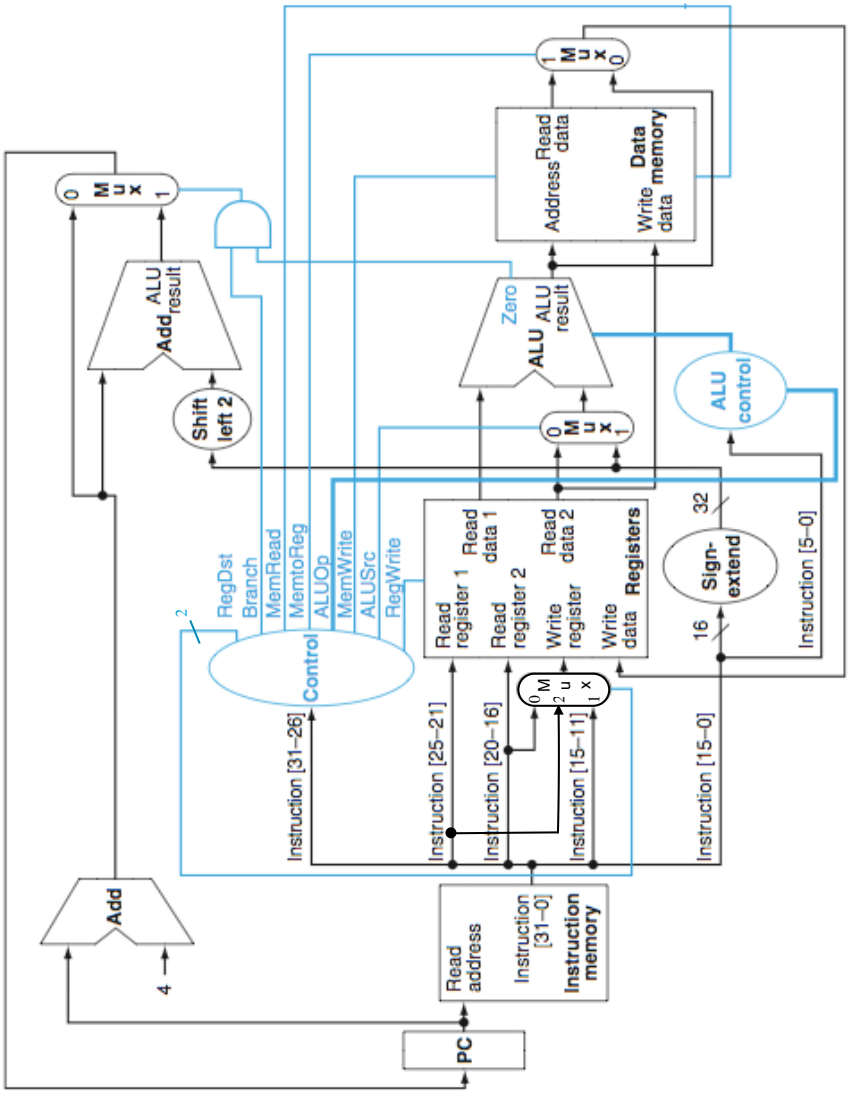
(c) (15 pts) With $sp implemented outside of the register file, show how to implement the **pop** instruction. Assume Control has one additional 1-bit output, Pop, that equals 1 only when the instruction is a pop. (Do not worry about implementing push for this case).

i. (5 pts) How should the various fields exiting Control be set?

ii. (5 pts) How should the fields of the instruction be filled in (you can assume a different op-code in this case of 010011).

iii. (5 pts) How $sp, now outside the register file, interfaces with the single cycle circuitry. You need only draw the regions/enhancements to the circuitry that involve the stack pointer register.

(This figure is the enhanced arch for problem 2a.)



3. (30 points) A procedure often places its own return address value (in the $ra register) on the stack when making its own call to another procedure. To return, the procedure must pull the return value off the stack and then return, as follows:

```
lw $ra, 0($sp)
addi $sp, $sp, -4
jr $ra
```

   (a) (10 points) Just like jump, the instruction that initially follows jr into the pipeline will be invalid and force a stall. However, in the existing architecture, there is an additional stall that will happen prior to the aforementioned stall. In one sentence, explain what causes it.

   (b) (20 points) Show what data forwarding should be added to avoid this stall. Depict only the additional circuitry needed. You can assume that the hazard detector and forwarding circuitry are adjusted to accommodate your changes.

   (Hint: recall that only the registers in the register file perform write before read within a clock cycle.)

You have reached the end of the exam. Have a great Summer!