HW #4

CSEE W3827 - Fundamentals of Computer Systems Spring 2022

Prof. Rubenstein
Due 2/25/22, 5pm

Topics: flip-flops, state design, sequential circuit design
Note that this homework has 3 HARDER problems and is 2 pages long.

Warmup Problems

1. Build
   (a) a T flip-flop out of a D flip-flop and combinational circuitry.
   (b) a D flip-flop out of a T flip-flop and combinational circuitry.
2. Build a sequential circuit that returns 1 whenever the last 3 inputs (INCLUDING the current input) were identical.
3. Build a sequential circuit that returns 1 whenever the last 3 inputs (PRIOR to the current input) were identical.

Harder Problems

1. A special flip-flop is formed from three latches, arranged in sequence. The first two latches behave as in a normal flip-flop: the leader latch's enable is attached to the clock, and the followers enable is attached to the complement of the clock. The third latch, which follows the follower, is also attached to the clock. Whats different about the outputs of this flip-flop?
2. Design a circuit using JK flip-flops that takes in a binary stream$B_0B_1B_2B_3\cdots$ and outputs a 1 at time t if the stream received thusfar (i.e., $B_0B_1\cdots B_{t-1}B_t$), when read as an unsigned binary number from low bit to high, is divisible by 3.

   The following table depicts a sample input stream and what should be output.

t	0	1	2	3	4	5	6	7	8
$In(t)$	0	0	1	1	0	0	1	0	0
Val of input	0	0	4	12	12	12	76	76	76
val mod 3	0	0	1	0	0	0	1	1	1
output	1	1	0	1	1	1	0	0	0

   Hint: The value of the new bit starts as equal to 1 which is 1 mod 3, then is 2 which is 2 mod 3, then is 4 which is back to 1 mod 3, etc.

   (a) Draw the state machine, numbering your states in an "obvious" manner. You may assume that the machine starts in the right state at time $t = 0$.
   (b) Give the algebraic formula (simplified as much as possible) for the J and K inputs of your flip-flops, and also for the output.
3. Consider a sequential circuit that reads in an input $X(t)$ during clock cycle t. The circuit should look for the sequence 011. Design the sequential circuit (i.e., give simplified algebraic expressions) using D flip-flops for each of the following versions:

   (a) If the second 1 arrives during clock cycle t, then the circuit should output a 1 during clock cycle t, and otherwise outputs a 0.

(b) If the second 1 arrives during clock cycle t, then the circuit should output a 1 during the clock cycle $t+1$, and otherwise outputs a 0.

(c) Suppose the sequence is 111 instead of 011. If at time t, the current and two previous inputs were all 1, then a 1 should be output during clock cycle t, and otherwise a 0 should be output. Note that multiple consecutive outputs of 1 are possible.