

3827 OH

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Announcements

Announcements: Upcoming Exams and Homework

- HW5 due 4/1 (Ed post #252)
- HW6 due 4/4 (Ed post #256)

Announcements: Midterm

- Do not throw away your exam if you plan to request a regrade
- Form: <https://forms.gle/8S8WYGD2B8LSsRmt9>
- I cannot comment on how a certain question was scored since I may not have scored it
- I do not know how the different exams are relatively curved

Announcements: Feedback

- Form: <https://forms.gle/cnUmKVNYN7WvRbHA6>

Homework 5 Material

Homework 5 Material: Overview and Relevant Lectures

- All Part n references are for Part 2. n in the “Coding Details” part of HW5 (i.e. the programming parts)
- Introduction to MIPS programming (Lecture 07, Slides 35-81)
- Conditional logic in MIPS (Lecture 07, Slides 82-95)
- Stack pointer and recursion (Lecture 07, Slides 96-111)
- MIPS calling conventions (Lecture 07, Slides 112-166)
- For Part 3 (AddAndVerify), use new testing program
test—AddAndVerify—plus.s on CourseWorks
 - The original does not print any decrypted string even if you are correct
 - Also original says “ALL DONE” even if you are wrong
 - It is fairly clear when the new testing code outputs correct string
- For the main message (Part 4), the last four characters can be ignored

Homework 5 Material: General Part 3 Structure

1 AddAndVerify:

2 # Base case checking/branching

3 # If not base case, push to stack using 'sw'

4 # Also save the decrypted word to the stack

5 # Other necessary operations

6 jal AddAndVerify

7 # Pop from stack (only what you need)

8 # Check \$v0 to see if suffix is valid for branching

9 # Other necessary operations

10 jal WordDecrypt

11 # Other necessary operations

12 jal IsCandidate

13 # Pop from stack stuff such as '\$ra' since WordDecrypt/IsCandidate
overwrite it

14 # Write to the DecryptStringSpace if valid word

15 # Other necessary operations such as writing to destination address

16 jr \$ra

Homework 6 Material

Homework 6 Material: Relevant Lectures

- Coincident selection (Lecture 10, Slides 41-58)
- Scaling memory using multiple chips (Lecture 10, Slides 59-85)