Notes:

1) Active Low Signals Names end in B or _B
2) PCI Edge Connector P1 is keyed as 3.3V ONLY
3) +IOV for PCI edge connector is wired to 3.3V
4) Ref. Sheet 6:

PCIe CEM Spec, Pg. 56 footnotes:

- By default the PETpx and PETnx pins shall be connected to the PCI Express transmitter differential pair on the system board, and the PCI Express receiver pair on the add-in card

- By default the PERpx and PERnx pins shall be connected to the PCI Express receiver differential pair on the system board, and the PCI Express transmitter pair on the add-in card

ML555 Engineering Rev04 (4th eng. spin) will be Production Rev01 for customer Release

ML555 PCB:

Latest Schematics Revision:

Rev01_10-30-06

Xilinx PCB Schematic Number: 0381219

Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		1 of 37	10-30-2006_10:43

ML555 Schematic Sheet List

Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

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DAVID NAYLOR		2 of 37	8-30-2006_8:06

PCI EDGE CONNECTOR 3.3V 32-bit SECTION

EDGE_JTAG

P1

B1	-12V		TRST#	A1	
B2	TCK		+12V	A2	
B3	GND	GND	TMS	A3	
B4	TDO		TDI	A4	
B5	+5V	VCC5	+5V	A5	VCC5
B6	+5V	VCC5	INTA#	A6	EDGE_INTA_B
B7	INTB#	EDGE_INTB_B	INTC#	A7	EDGE_INTC_B
B8	INTD#	EDGE_INTD_B	+5V	A8	VCC5
B9	PRSNT1#		RESERVED	A9	
B10	RESERVED	EDGE_PRSNT1_B	+IOV	A10	
B11	PRSNT2#	EDGE_PRSNT2_B	RESERVED	A11	
	KEY		KEY		
	KEY		KEY		
B14	RESERVED		+AUXV	A14	AUXV_A14
B15	GND	GND	RST#	A15	EDGE_RST_B
B16	CLK	CLK_FROM_EDGE	+IOV	A16	
B17	GND	GND	GNT#	A17	EDGE_GNT_B
B18	REQ#	EDGE_REQ_B	GND	A18	GND
B19	+IOV		PME#	A19	EDGE_PME_B
B20	AD[31]	EDGE_AD31	AD[30]	A20	EDGE_AD30
B21	AD[29]	EDGE_AD29	+3.3V	A21	
B22	GND	GND	AD[28]	A22	EDGE_AD28
B23	AD[27]	EDGE_AD27	AD[26]	A23	EDGE_AD26
B24	AD[25]	EDGE_AD25	GND	A24	GND
B25	+3.3V		AD[24]	A25	EDGE_AD24
B26	C/BE#[3]	EDGE_CBE3	IDSEL	A26	EDGE_IDSEL
B27	AD[23]	EDGE_AD23	+3.3V	A27	
B28	GND	GND	AD[22]	A28	EDGE_AD22
B29	AD[21]	EDGE_AD21	AD[20]	A29	EDGE_AD20
B30	AD[19]	EDGE_AD19	GND	A30	GND
B31	+3.3V		AD[18]	A31	EDGE_AD18
B32	AD[17]	EDGE_AD17	AD[16]	A32	EDGE_AD16
B33	C/BE#[2]	EDGE_CBE2	+3.3V	A33	
B34	GND	GND	FRAME#	A34	EDGE_FRAME_B
B35	IRDY#	EDGE_IRDY_B	GND	A35	GND
B36	+3.3V		TRDY#	A36	EDGE_TRDY_B
B37	DEVSEL#	EDGE_DEVSEL_B	GND	A37	GND
B38	PCIXCAP	EDGE_PCIXCAP	STOP#	A38	EDGE_STOP_B
B39	LOCK#		+3.3V	A39	
B40	PERR#	EDGE_PERR_B	SMBCLK	A40	
B41	+3.3V		SMBDAT	A41	
B42	SERR#	EDGE_SERR_B	GND	A42	GND
B43	+3.3V		PAR	A43	EDGE_PAR
B44	C/BE#[1]	EDGE_CBE1	AD[15]	A44	EDGE_AD15
B45	AD[14]	EDGE_AD14	+3.3V	A45	
B46	GND	GND	AD[13]	A46	EDGE_AD13
B47	AD[12]	EDGE_AD12	AD[11]	A47	EDGE_AD11
B48	AD[10]	EDGE_AD10	GND	A48	GND
B49	M66EN	EDGE_M66EN	AD[09]	A49	EDGE_AD9
B50	GND		GND	A50	
B51	GND		GND	A51	
B52	AD[08]	EDGE_AD8	C/BE#[0]	A52	EDGE_CBE0
B53	AD[07]	EDGE_AD7	+3.3V	A53	
B54	+3.3V		AD[06]	A54	EDGE_AD6
B55	AD[05]	EDGE_AD5	AD[04]	A55	EDGE_AD4
B56	AD[03]	EDGE_AD3	GND	A56	GND
B57	GND	GND	AD[02]	A57	EDGE_AD2
B58	AD[01]	EDGE_AD1	AD[00]	A58	EDGE_AD0
B59	+IOV		+IOV	A59	
B60	ACK64#	EDGE_ACK64_B	REQ64#	A60	EDGE_REQ64_B
B61	+5V	VCC5	+5V	A61	VCC5
B62	+5V	VCC5	+5V	A62	VCC5

EDGE_PCI_3V3

P6 DNA

PCI_VCC

R239 100R

R238 15R

R240 100R

EDGE_RST_I_B

P7

EDGE_PME_B

FPGA_EDGE_PME_B

to U10 LX50T Bank 5

P8 JUMPERS:
NO JUMPER = PCI-X 133MHz capable
JUMPER 1-2 = PCI-X 66MHz capable
JUMPER 2-3 = NOT PCI-X capable, PCI Mode Only

R1 10K

PCIXCAP_PD

P8

EDGE_PCIXCAP

C12 0.01UF

REMOVE JUMPER FOR 66Mhz

P9

EDGE_M66EN

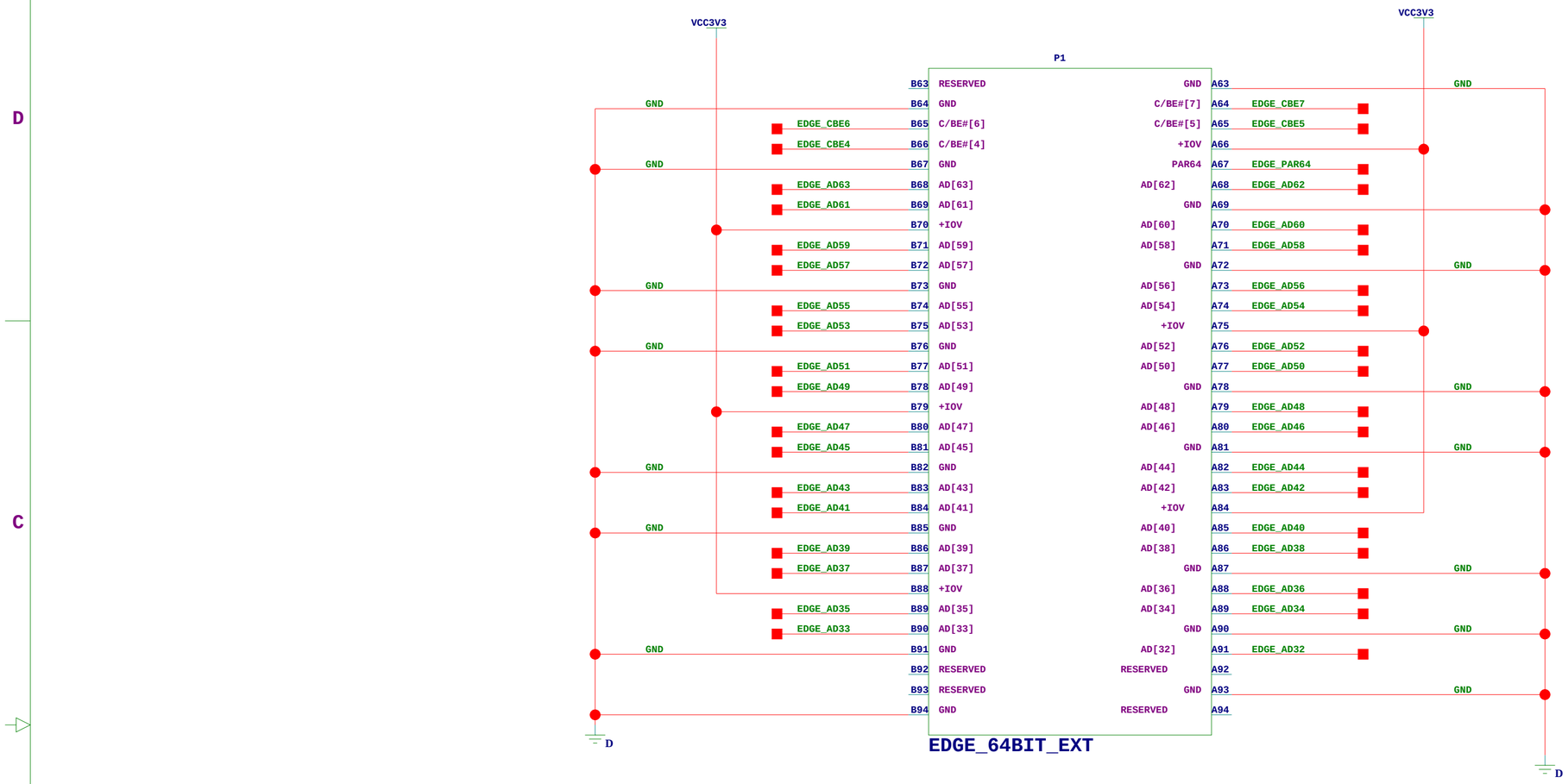
C13 0.01UF

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

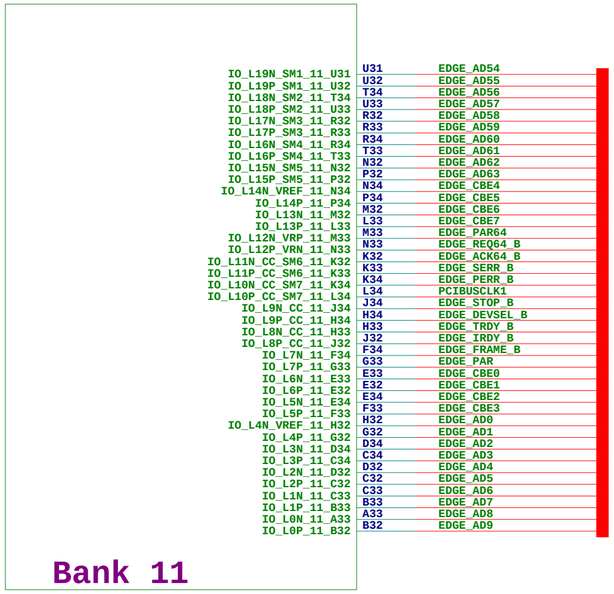
DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		3 of 37	6-8-2006_19:07

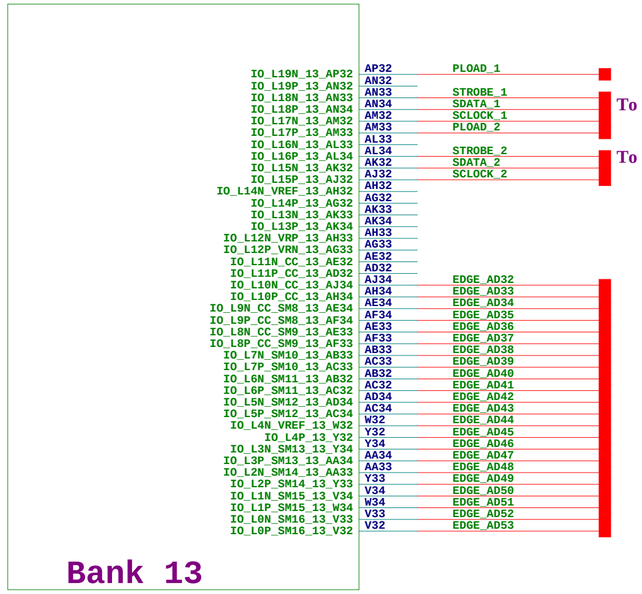


PCI EDGE CONNECTOR 3.3V 64-bit EXTENSION

Xilinx

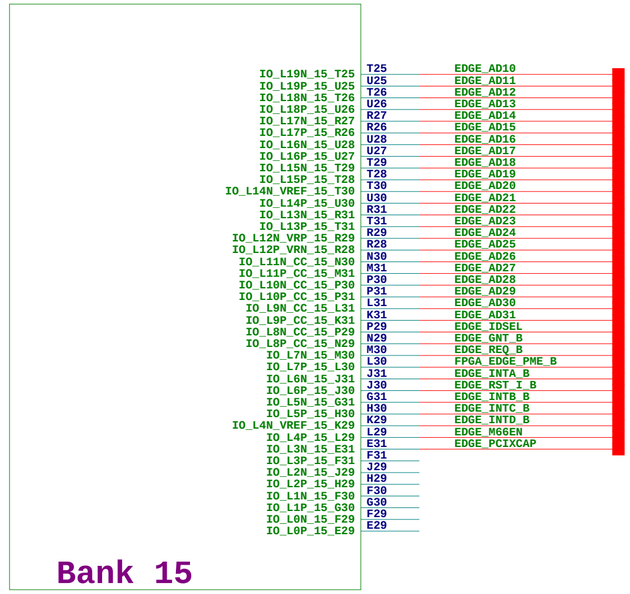
TITLE	SCHEM, ML555 PCIE PCI PCI-X PCB,1280389	
SIZE: C	DWG NO: 0381219	REV: 01
DRAWN BY: DAVID NAYLOR	SCALE	SHEET 4 of 37
5-30-2006_18:44		



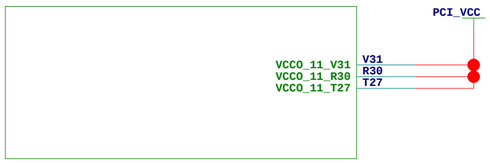


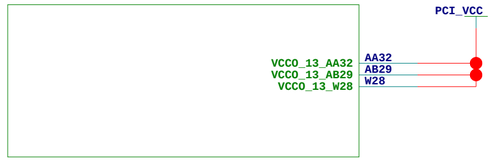
To Sheet24 U8

To Sheet25 U7

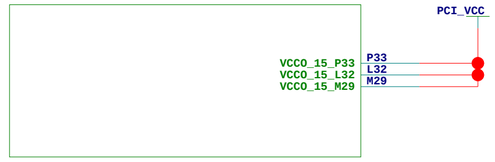


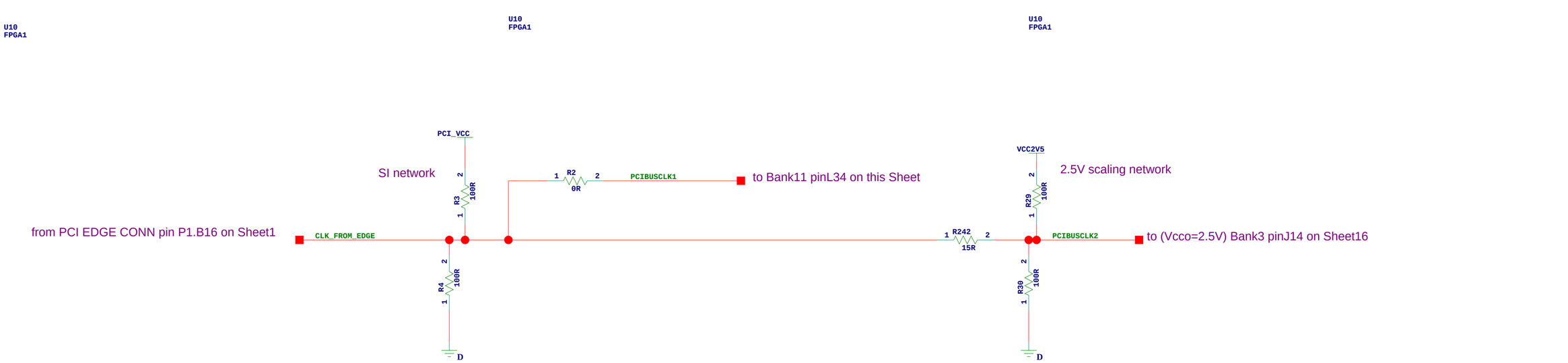
PCI 32-bit I/F





PCI 64-bit EXTENSION I/F





Banks 11,13,15

PCI 32&64 bit EDGE Connector Bank I/F

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

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DAVID NAYLOR		5 of 37	8-30-2006_8:06

P1.B11&P1.A11 to scaling resistors on Sheet15

X0Y0

U10 FPGA1 5VLX50T FF1136

MGTTXP1_122_AN4 AN4 MGTX0Y0_TX1_P
MGTTXN1_122_AN3 AN3 MGTX0Y0_TX1_N
MGTREFCLKP_122_AL5 AL5 MGT_122_AL5_REFCLKP
MGTRXP1_122_AP3 AP3 PER7_P
MGTREFCLKN_122_AL4 AL4 MGT_122_AL4_REFCLKN
MGTRXN1_122_AP2 AP2 PER7_N
MGTRXN0_122_AM1 AM1 PER6_N
MGTRXP0_122_AL1 AL1 PER6_P
MGTTXN0_122_AL2 AL2 MGTX0Y0_TX0_N
MGTTXP0_122_AK2 AK2 MGTX0Y0_TX0_P

C426 0.1UF PET7_P
C425 0.1UF PET7_N
C344 0.1UF MGT_X0Y3_RCLKP — From Sheet25 U7
C343 0.1UF MGT_X0Y3_RCLKN
C427 0.1UF PET6_N
C428 0.1UF PET6_P

X0Y1

U10 FPGA1 5VLX50T FF1136

MGTTXP1_118_AJ2 AJ2 MGTX0Y1_TX1_P
MGTTXN1_118_AH2 AH2 MGTX0Y1_TX1_N
MGTREFCLKP_118_AF4 AF4 MGT_X0Y1_REFCLKP
MGTRXP1_118_AH1 AH1 PER3_P
MGTREFCLKN_118_AF3 AF3 MGT_X0Y1_REFCLKN
MGTRXN1_118_AG1 AG1 PER3_N
MGTRXN0_118_AF1 AF1 PER2_N
MGTRXP0_118_AE1 AE1 PER2_P
MGTTXN0_118_AE2 AE2 MGTX0Y1_TX0_N
MGTTXP0_118_AD2 AD2 MGTX0Y1_TX0_P

C429 0.1UF PET3_P
C430 0.1UF PET3_N
C448 0.1UF MGT_X0Y1_RCLKP — From Sheet24 U8
C449 0.1UF MGT_X0Y1_RCLKN
C431 0.1UF PET2_N
C432 0.1UF PET2_P

X0Y2

U10 FPGA1 5VLX50T FF1136

MGTTXP1_114_AC2 AC2 MGTX0Y2_TX1_P
MGTTXN1_114_AB2 AB2 MGTX0Y2_TX1_N
MGTREFCLKP_114_Y4 Y4
MGTRXP1_114_AB1 AB1 PER1_P
MGTREFCLKN_114_Y3 Y3
MGTRXN1_114_AA1 AA1 PER1_N
MGTRXN0_114_Y1 Y1 PER0_N
MGTRXP0_114_W1 W1 PER0_P
MGTTXN0_114_W2 W2 MGTX0Y2_TX0_N
MGTTXP0_114_V2 V2 MGTX0Y2_TX0_P

C433 0.1UF PET1_P
C434 0.1UF PET1_N
C450 0.1UF PCIE250M_P — From U16 This Page
C451 0.1UF PCIE250M_N
C435 0.1UF PET0_N
C436 0.1UF PET0_P

X0Y3

U10 FPGA1 5VLX50T FF1136

MGTTXP1_112_U2 U2 MGTX0Y3_TX1_P
MGTTXN1_112_T2 T2 MGTX0Y3_TX1_N
MGTREFCLKP_112_P4 P4 SMA_GTPCLK_P4_P
MGTRXP1_112_T1 T1 PER5_P
MGTREFCLKN_112_P3 P3 SMA_GTPCLK_P3_N
MGTRXN1_112_R1 R1 PER5_N
MGTRXN0_112_P1 P1 PER4_N
MGTRXP0_112_N1 N1 PER4_P
MGTTXN0_112_N2 N2 MGTX0Y3_TX0_N
MGTTXP0_112_M2 M2 MGTX0Y3_TX0_P

C437 0.1UF PET5_P
C438 0.1UF PET5_N — SMAs J12&J13 Sheet10
C439 0.1UF PET4_N
C440 0.1UF PET4_P

U10 FPGA1 5VLX50T FF1136

VCC3V3
R50 10R
PCI_VCC
R54 4.7K
C105 0.01UF
F_SEL2

PCIE_GCLK_N
PCIE_GCLK_P
To Sheet16 Bank3 PinsJ16(P)&J17(N)

PCIE250M_P
PCIE250M_N
MR
F_SEL0
F_SEL1
To Sheet13 CPLD U6

U16
ICS874003-02 TSSOP20
QA1 NQA1 VDDO_1 VDDO_2 QA0 QB1 NQA0 NQB1 MR F_SEL2 F_SEL0 OEB NC GND VDDA NCLK F_SEL1 CLK VDD OEA

PCIE_REFCLKN
PCIE_REFCLKP
OEA
P13.A13 & A14 THIS PAGE

C102 0.01UF
C103 10UF C0805
C104 0.01UF
R450 0R
R451 0R
R51 100R
R52 49.9R
R53 49.9R
Place close to U16.12&13

Note: U16 and R450/R451 are MUTUALLY EXCLUSIVE. The resistors are located beneath the body of U16

VCC3V3 PCIE_VCC12 — PCIE_VCC12 VCC3V3

P13

B1	+12V	PRSNT#1	A1
B2	+12V	+12V	A2
B3	+12V	+12V	A3
B4	GND	GND	A4
B5	SMCLK	JTAG2/TCK	A5
B6	SMDAT	JTAG3/TDI	A6
B7	GND	JTAG4/TDO	A7
B8	+3.3V	JTAG5/TMS	A8
B9	JTAG1/TRST#	+3.3V	A9
B10	+3.3Vaux	+3.3V	A10
B11	WAKE#	PERST	A11
	KEY	KEY	
B12	RESERVED	GND	A12
B13	GND	REFCLK+	A13
B14	PETp0	REFCLK-	A14
B15	PETn0	GND	A15
B16	GND	PERp0	A16
B17	PRSNT#2	PERn0	A17
B18	GND	GND	A18
B19	PETp1	RESERVED	A19
B20	PETn1	GND	A20
B21	GND	PERp1	A21
B22	GND	PERn1	A22
B23	PETp2	GND	A23
B24	PETn2	GND	A24
B25	GND	PERp2	A25
B26	GND	PERn2	A26
B27	PETp3	GND	A27
B28	PETn3	GND	A28
B29	GND	PERp3	A29
B30	RESERVED	PERn3	A30
B31	PRSNT#2	GND	A31
B32	GND	RESERVED	A32
B33	PETp4	RESERVED	A33
B34	PETn4	GND	A34
B35	GND	PERp4	A35
B36	GND	PERn4	A36
B37	PETp5	GND	A37
B38	PETn5	GND	A38
B39	GND	PERp5	A39
B40	GND	PERn5	A40
B41	PETp6	GND	A41
B42	PETn6	GND	A42
B43	GND	PERp6	A43
B44	GND	PERn6	A44
B45	PETp7	GND	A45
B46	PETn7	GND	A46
B47	GND	PERp7	A47
B48	PRSNT#2	PERn7	A48
B49	GND	GND	A49

PCIE_PRSNT_B
PCIE_PERST_B
PCIE_REFCLKP
PCIE_REFCLKN
PET0_P PET0_N PET1_P PET1_N PET2_P PET2_N PET3_P PET3_N PET4_P PET4_N PET5_P PET5_N PET6_P PET6_N PET7_P PET7_N
PER0_P PER0_N PER1_P PER1_N PER2_P PER2_N PER3_P PER3_N PER4_P PER4_N PER5_P PER5_N PER6_P PER6_N PER7_P PER7_N
PCIE_PRSNT_X1
PCIE_PRSNT_X4
PCIE_PRSNT_X8

PCIE_8LANE_EDGE

P45
X8 X4 X1
HEADER3X2

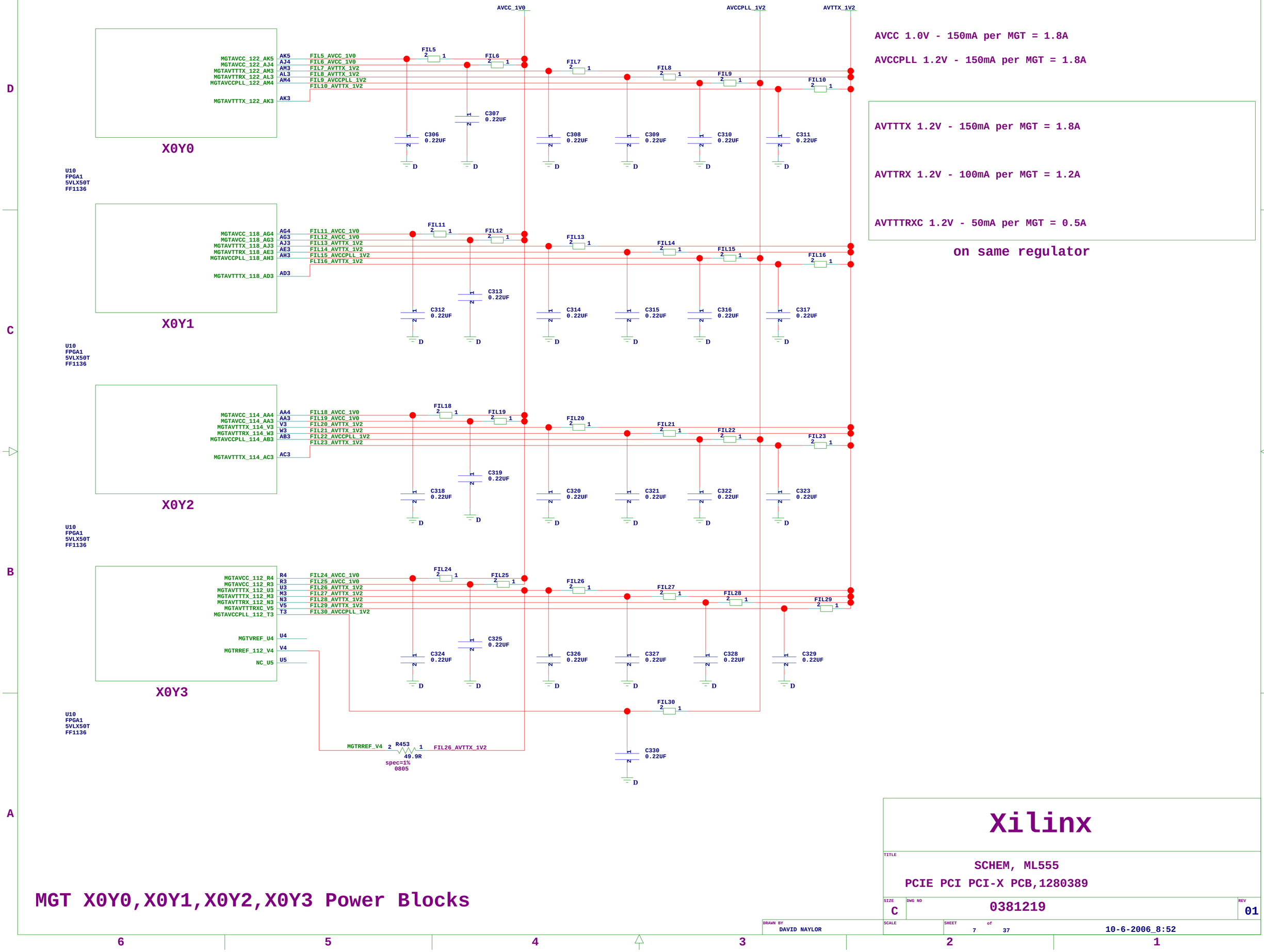
Lane Size Select

Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		6 of 37	11-14-2006_13:51



AVCC 1.0V - 150mA per MGT = 1.8A

AVCCPLL 1.2V - 150mA per MGT = 1.8A

AVTTTX 1.2V - 150mA per MGT = 1.8A

AVTTRX 1.2V - 100mA per MGT = 1.2A

AVTTTRXC 1.2V - 50mA per MGT = 0.5A

on same regulator

MGT X0Y0,X0Y1,X0Y2,X0Y3 Power Blocks

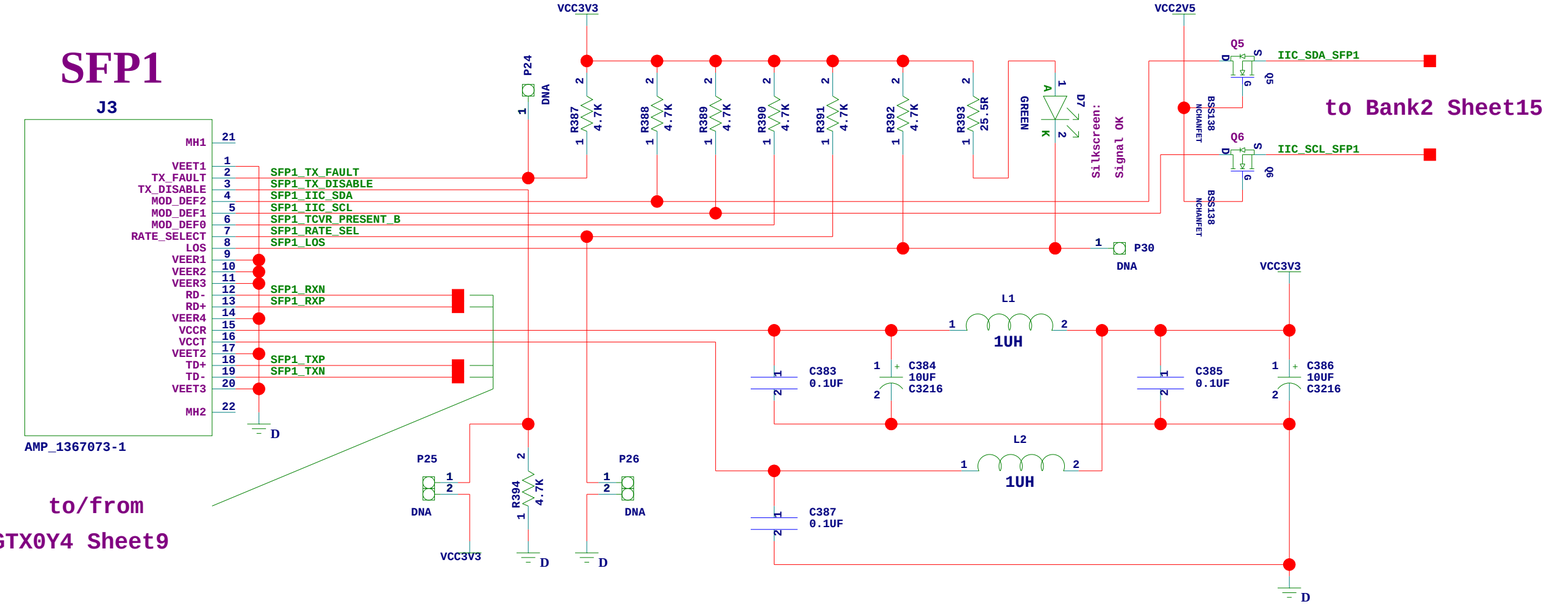
Xilinx

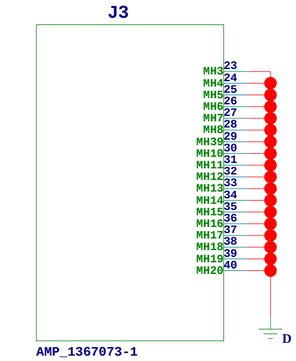
TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

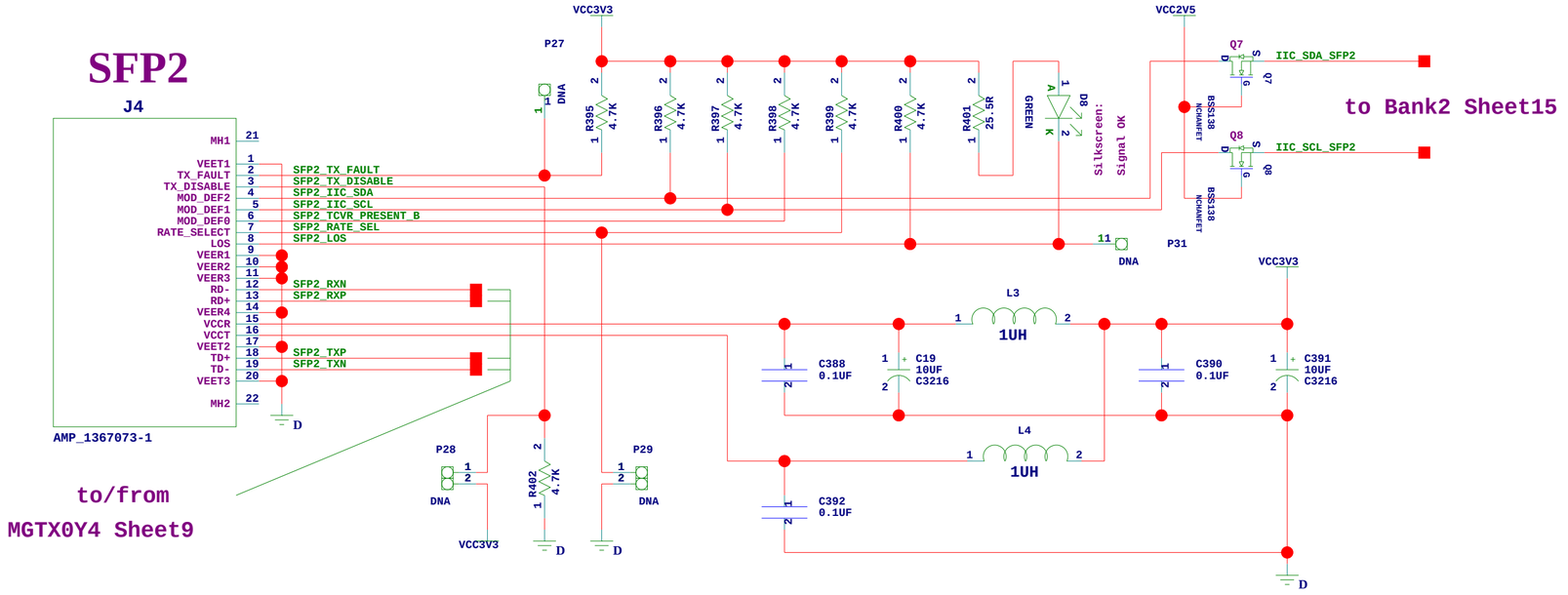
DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		7	37	10-6-2006_8:52

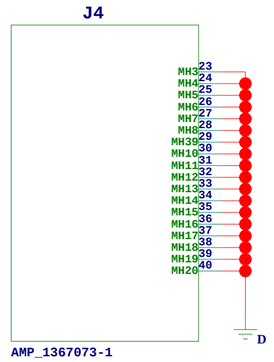
SFP1





SFP2





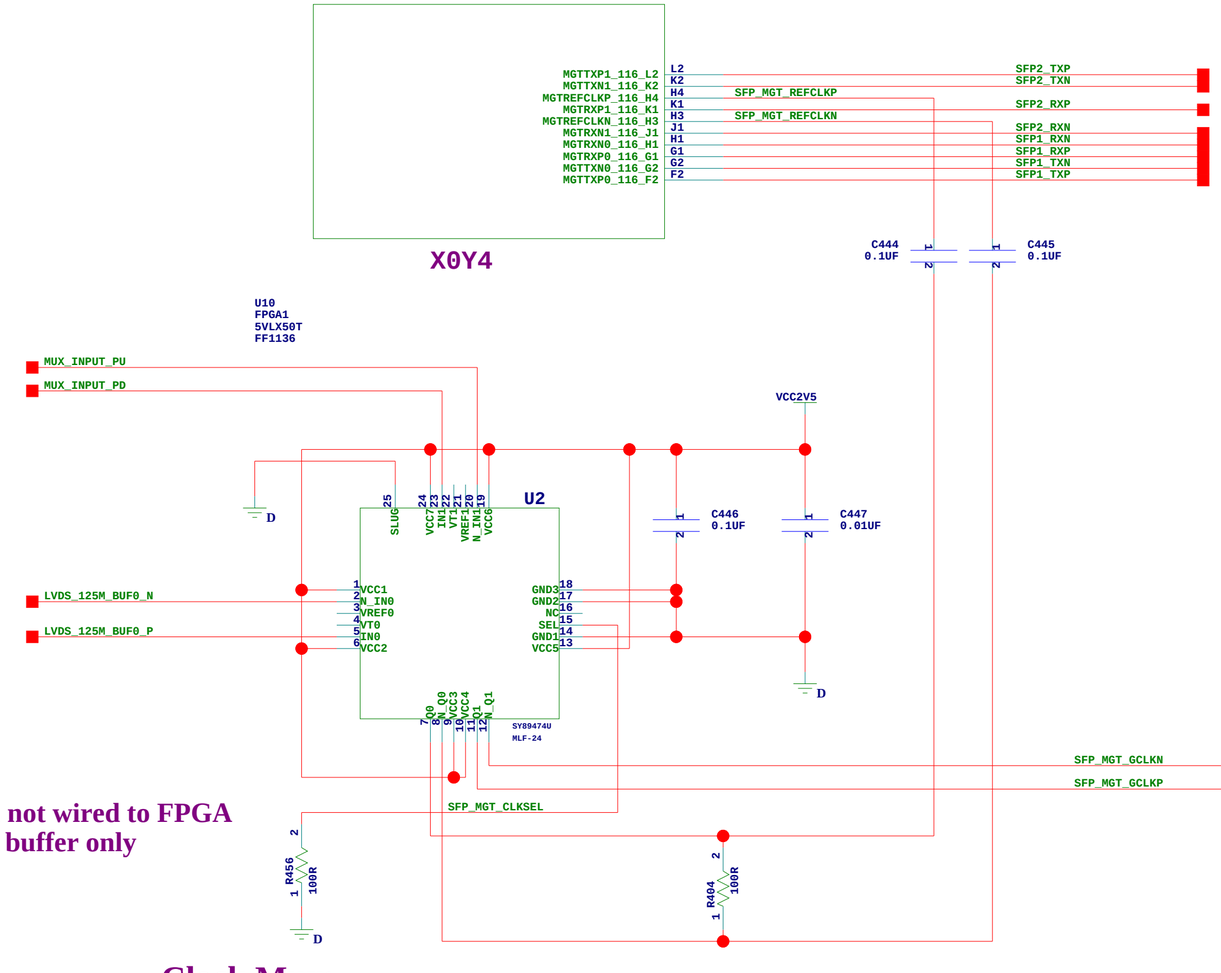
2xSFP

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		8 of 37	8-30-2006_7:58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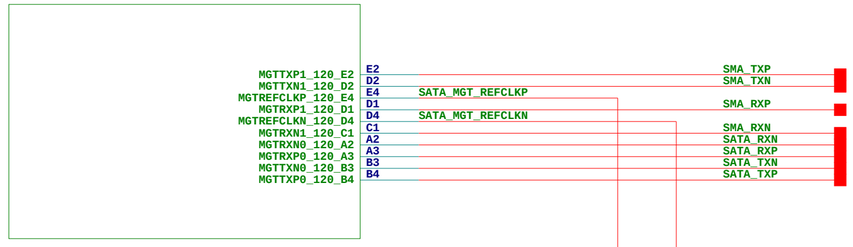
MGTTXN1_116_K2
MGTREFCLKP_116_H4
MGTRXP1_116_K1
MGTREFCLKN_116_H3
MGTRXN1_116_J1
MGTRXN0_116_H1
MGTRXP0_116_G1
MGTTXN0_116_G2
MGTTXP0_116_F2
L2
K2
H4
K1
H3
J1
H1
G1
G2
F2
SFP2_TXP
SFP2_TXN
SFP_MGT_REFCLKP
SFP2_RXP
SFP_MGT_REFCLKN
SFP2_RXN
SFP1_RXN
SFP1_RXP
SFP1_TXN
SFP1_TXP
to SFP1&2 Sheet8
X0Y4
C444
0.1UF
C445
0.1UF
U10
FPGA1
5VLX50T
FF1136
IN1 pulled down
From Sheet11 R42/43
MUX_INPUT_PU
MUX_INPUT_PD
VCC2V5
U2
SLUG
VCC7
IN1
VT1
VREF1
IN0
VCC6
C446
0.1UF
C447
0.01UF
From Sheet11 U11
LVDS_125M_BUF0_N
LVDS_125M_BUF0_P
VCC1
N_IN0
VREF0
VT0
IN0
VCC2
GND3
GND2
NC
SEL
GND1
VCC5
Q0
N_Q0
VCC3
VCC4
N_Q1
SY89474U
MLF-24
SFP_MGT_GCLKN
SFP_MGT_GCLKP
To Bank3 GCLK Sheet16
SFP_MGT_CLKSEL not wired to FPGA
U2 used as clock buffer only
SFP_MGT_CLKSEL
R456
100R
R404
100R
Clock Mux:
Sel: Q0 Out:
0 LVDS_125M (default)
1 IN1 tied to static levels via p/u & p/d resistors
AVCC_1V0
AVCCPLL_1V2
AVTTX_1V2
MGTAVCC_116_J4
MGTAVCC_116_J3
MGTAVTTTX_116_L3
MGTAVTTRX_116_G3
MGTAVCCPLL_116_K3
MGTAVTTTX_116_F3
J4
J3
L3
G3
K3
F3
FIL31_AVCC_1V0
FIL32_AVCC_1V0
FIL33_AVTTX_1V2
FIL34_AVTTX_1V2
FIL35_AVCCPLL_1V2
FIL36_AVTTX_1V2
FIL31
FIL32
FIL33
FIL34
FIL35
FIL36
C331
0.22UF
C332
0.22UF
C333
0.22UF
C334
0.22UF
C335
0.22UF
C336
0.22UF
X0Y4
U10
FPGA1
5VLX50T
FF1136
MGT X0Y4 SFP I/F & Power Block
Xilinx
TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389
SIZE
C
DWG NO
0381219
REV
01
DRAWN BY
DAVID NAYLOR
SCALE
SHEET
9
of
37
6-6-2006_10:29



C441 0.1UF C442 0.1UF

U10
FPGA1
5VLX50T
FF1136

From Sheet25 U7

LVDSCLKMOD2_N
LVDSCLKMOD2_P

VCC2V5

U3

C443 0.1UF C421 0.01UF

From Sheet11 U11

LVDS_125M_BUF1_N
LVDS_125M_BUF1_P

SY89474U
MLF-24

SATA_MGT_CLKSEL wired to FPGA

SATA_MGT_CLKSEL

Bank1 pin K14 Sheet 16

R459 4.7K
R458 DNA
R6 100R

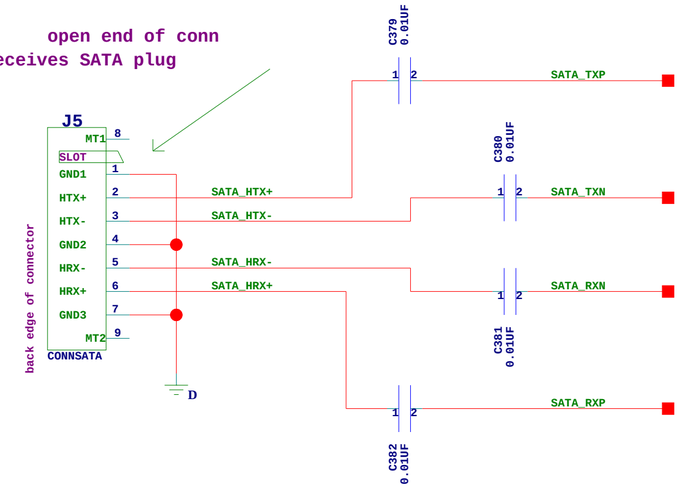
SATA_MGT_GCLKN
SATA_MGT_GCLKP

To Bank3 GCLK Sheet16

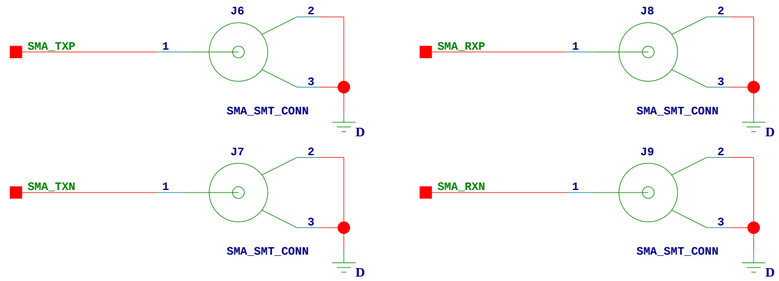
Clock Mux:

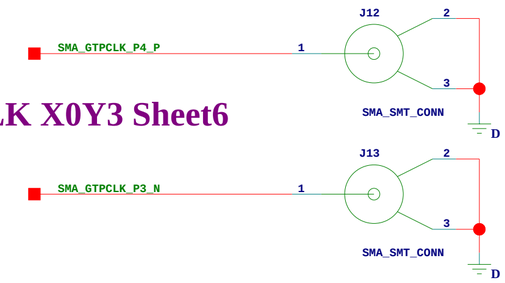
Sel:	Q0 Out:
0	LVDS_125M
1	LVDSCLKMOD2 (default)

open end of conn
which receives SATA plug

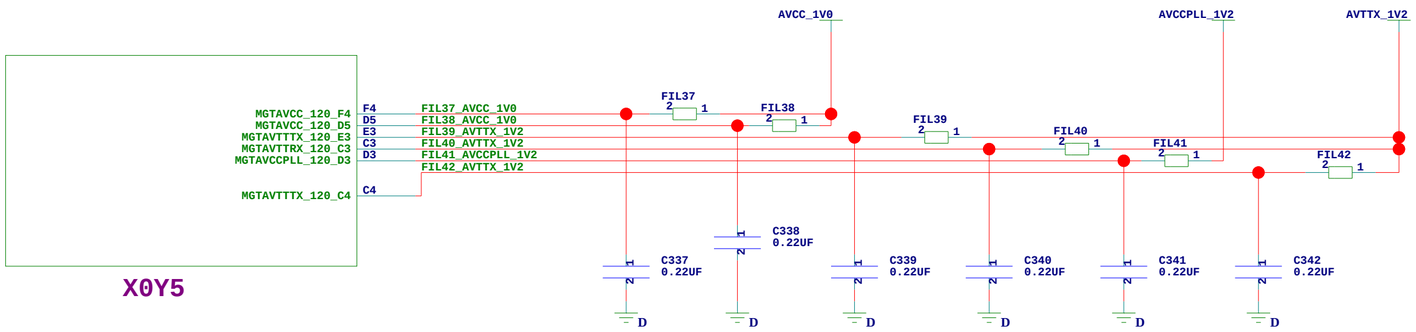


SMA TX and RX





SMA_GTPCLK X0Y3 Sheet6



U10
FPGA1
5VLX50T
FF1136

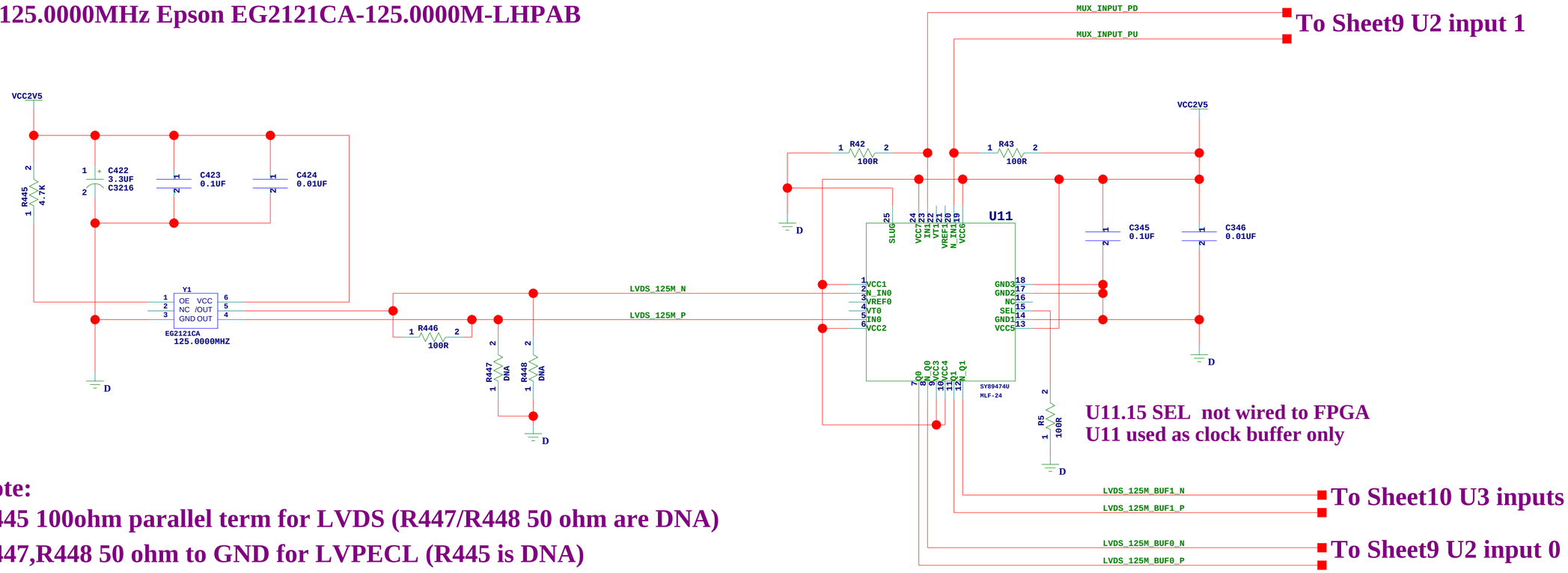
SATA Conn,4xSMA,MGT X0Y5 & Power Block

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		10	37	9-6-2006_15:09



Note:
R445 100ohm parallel term for LVDS (R447/R448 50 ohm are DNA)
R447,R448 50 ohm to GND for LVPECL (R445 is DNA)

Clock Mux:

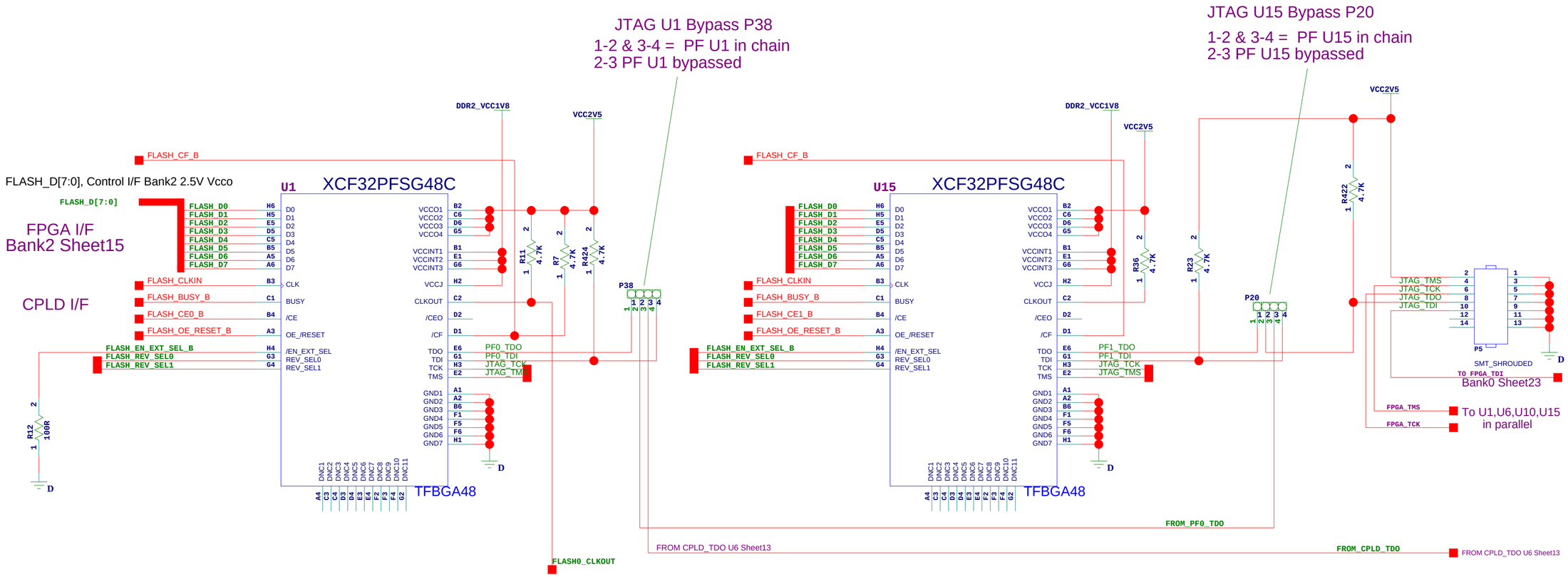
Sel:	Q0 Out:
0	LVDS_125M (default)
1	IN1 tied to static levels via p/u & p/d resistors

125MHz Osc Y1 & LVDS Clock Mux U11
200MHz Osc Y3 LVPECL

Xilinx

TITLE	SCHEM, ML555 PCIE PCI PCI-X PCB,1280389	
SIZE: C	DWG NO: 0381219	REV: 01
DRAWN BY: DAVID NAYLOR	SCALE	SHEET: 11 of 37 — 6-6-2006_10:30

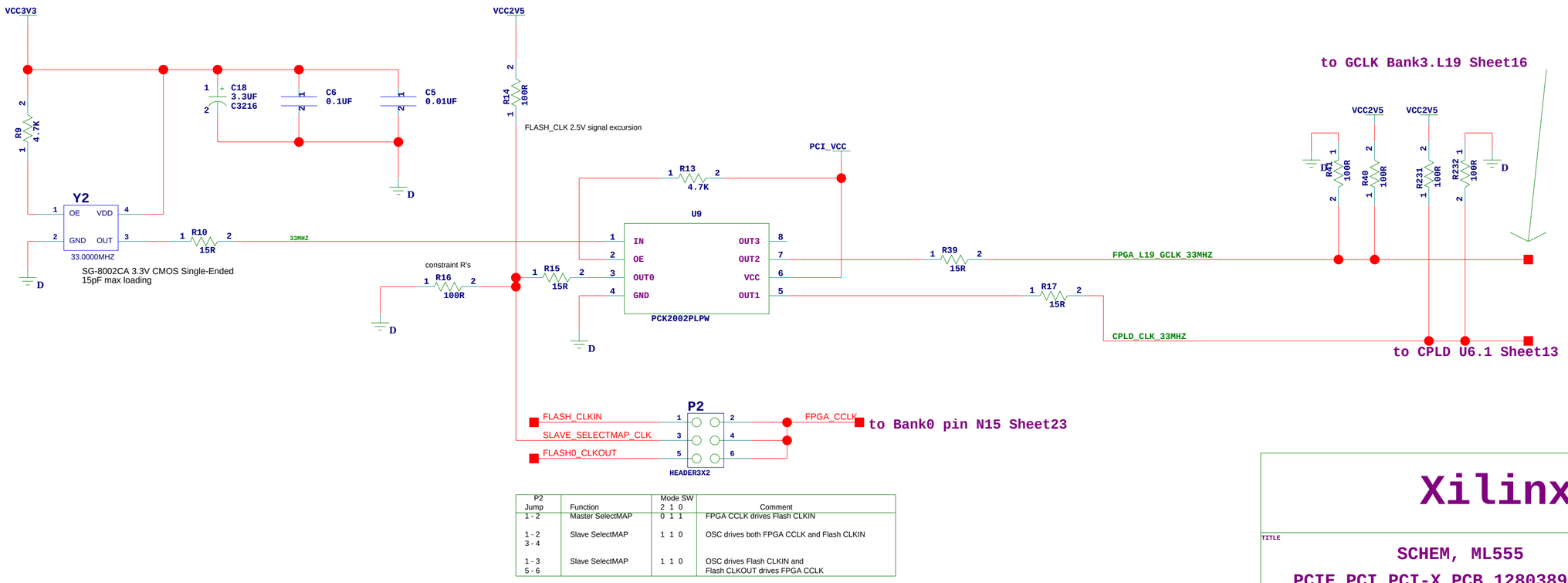
Platform Flash, JTAG I/F



(Bypassable) (Bypassable) (Bypassable)

Loop=JTAG P5=>LX50T U10=>CPLD U6=>PF0 U1=>PF1 U15=>JTAG P5

P5 2mm JTAG conn. is Xilinx Parallel Cable IV or Platform USB Cable compatible



P2 Jump	Function	Mode SW 2 1 0	Comment
1 - 2	Master SelectMAP	0 1 1	FPGA CCLK drives Flash CLKIN
1 - 2 3 - 4	Slave SelectMAP	1 1 0	OSC drives both FPGA CCLK and Flash CLKIN
1 - 3 5 - 6	Slave SelectMAP	1 1 0	OSC drives Flash CLKIN and Flash CLKOUT drives FPGA CCLK

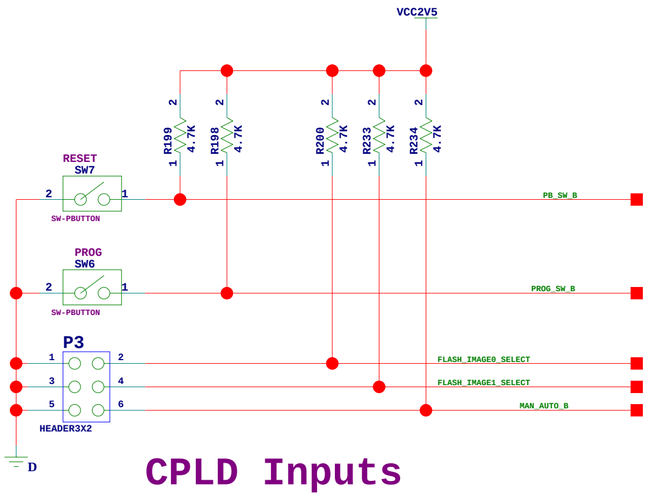
Platform Flash Clock Select

Xilinx

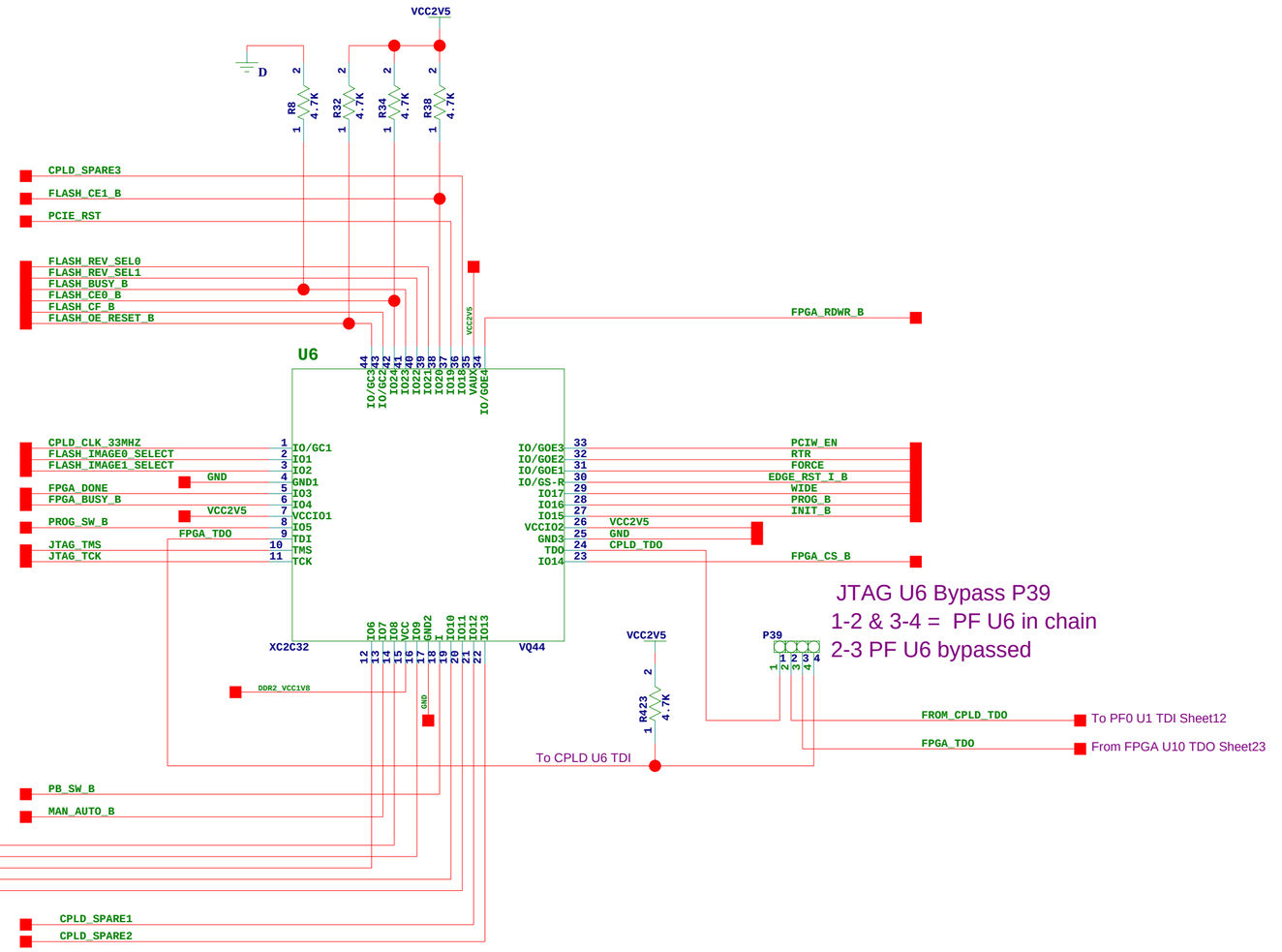
TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		12 of 37	9-8-2006_14:28

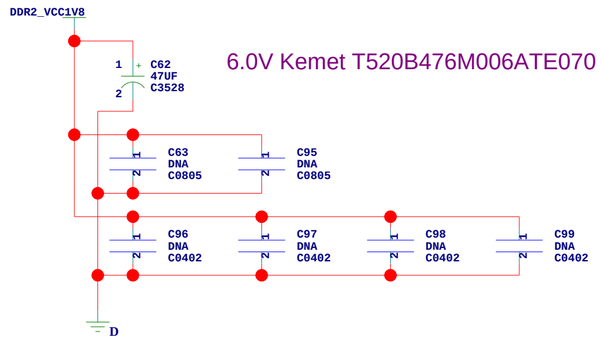


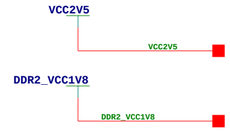
CPLD Inputs



To Sheet6 U16

1.8V CPLD





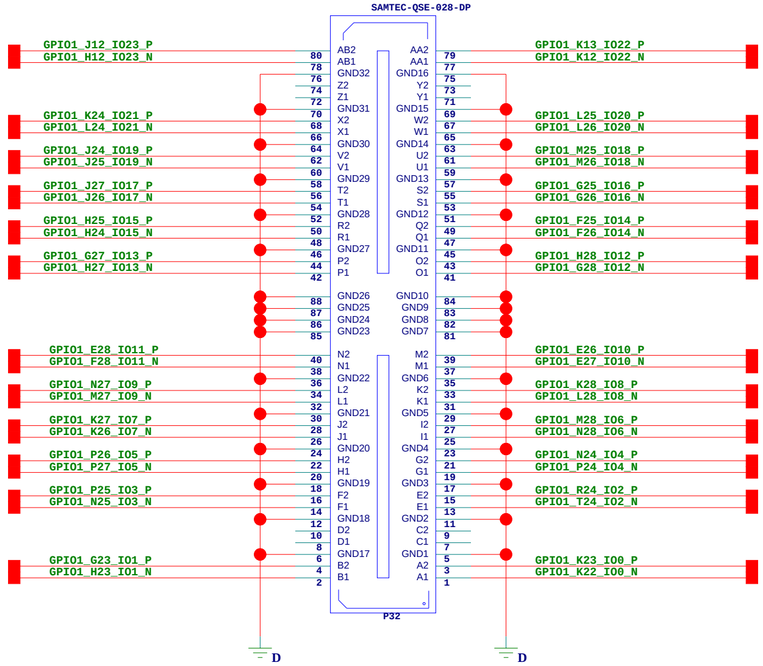
Dynamic Reconfig. CPLD

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

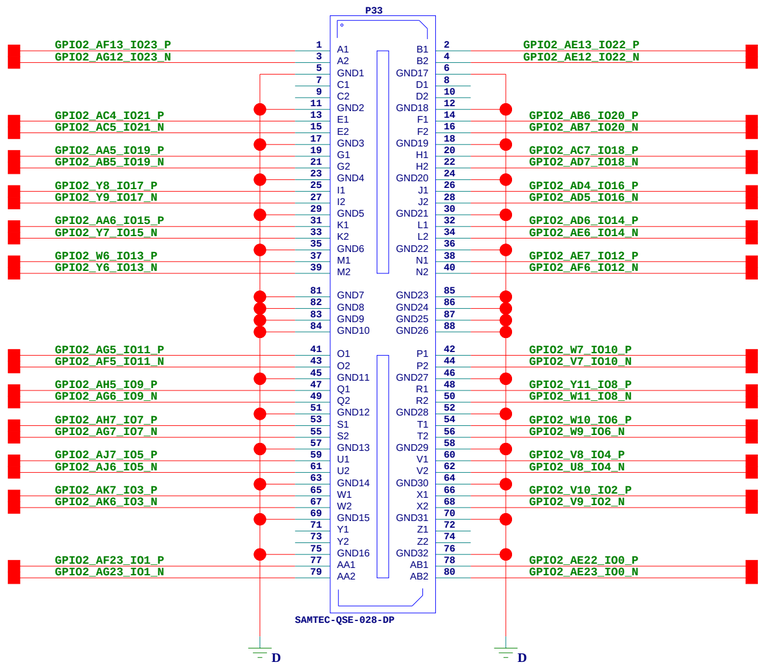
SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		13 of 37	9-12-2006_12:22



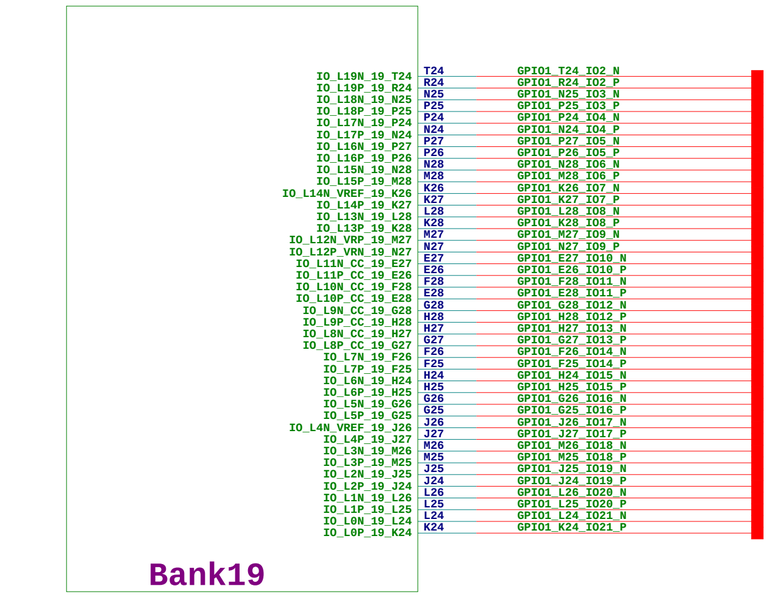
GPIO1

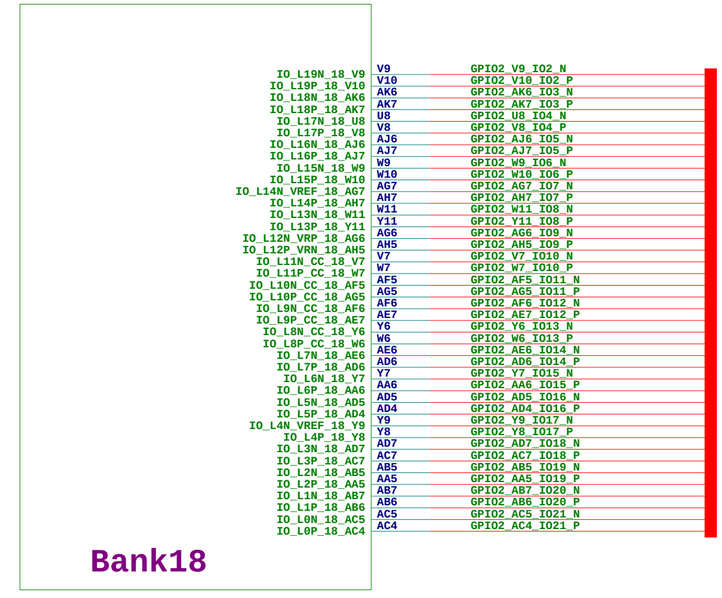
GPIO1_[21:02] P32 <=> Bank19
GPIO1_[23,22,01,00] P32 <=> Bank1

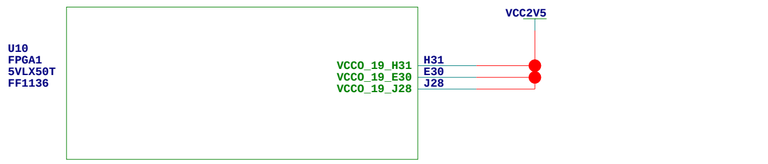


GPIO2

GPIO2_[21:02] P33 <=> Bank18
GPIO2_[23,22,01,00] P33 <=> Bank2







U10
FPGA1

U10
FPGA1

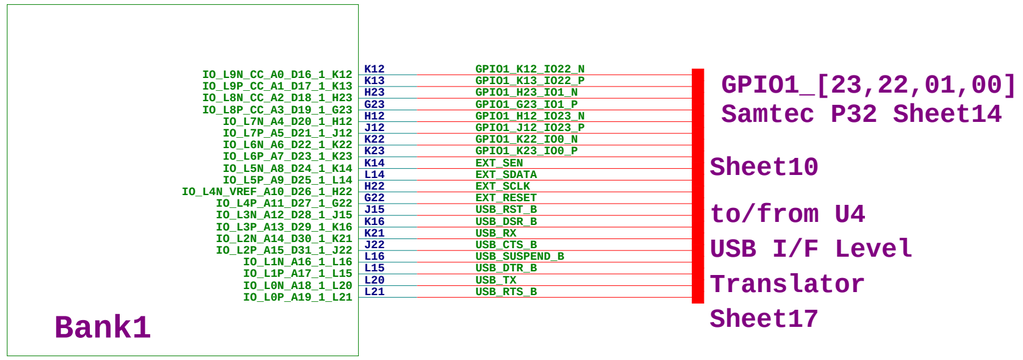
GPIO - 2xQSE SamtecDP Connector

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		14	37	7-11-2006_6:37



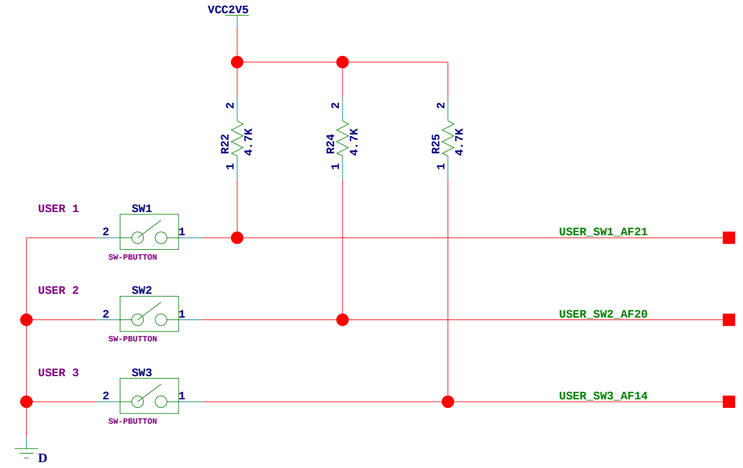
GPIO1_[23,22,01,00]
Samtec P32 Sheet14

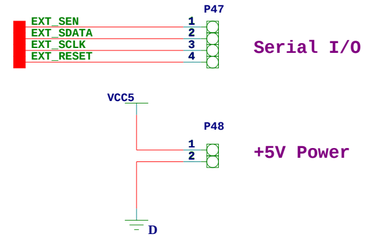
Sheet10

to/from U4
USB I/F Level
Translator
Sheet17

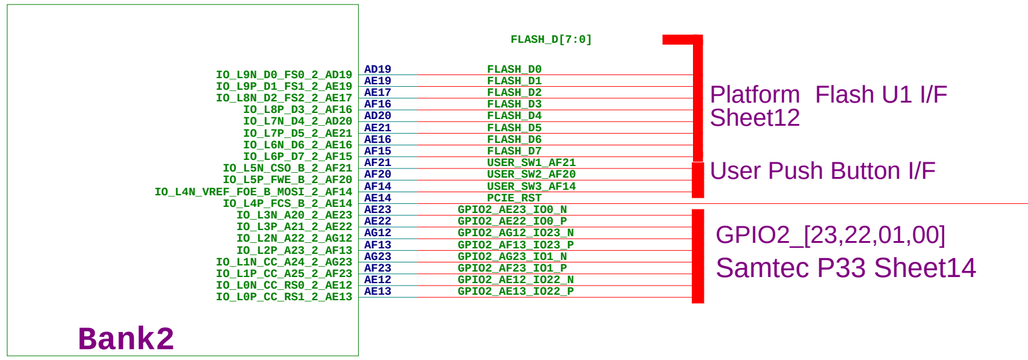
U10
FPGA1
5VLX50T
FF1136

U10
FPGA1





Samtec Mezzanine Board Support



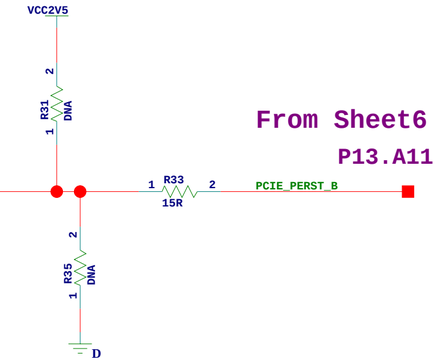
Platform Flash U1 I/F
Sheet12

User Push Button I/F

GPIO2_[23,22,01,00]
Samtec P33 Sheet14

U10
FPGA1
5VLX50T
FF1136

U10
FPGA1



Also to Sheet13 CPLD U6.37

Bank1 USB-UART I/F,GPIO1

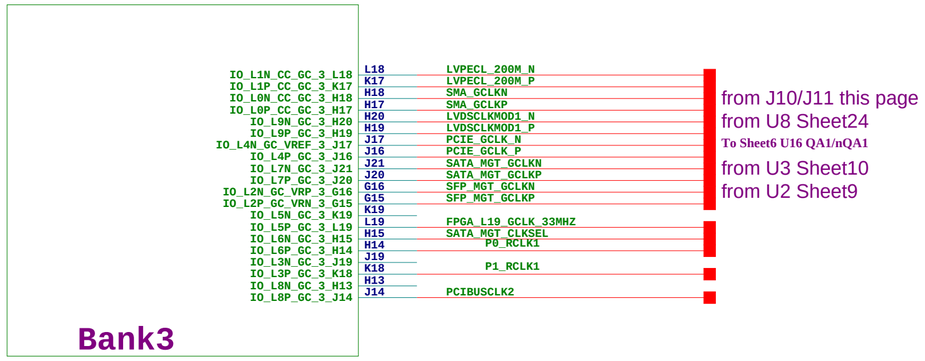
Bank2 PF U1 I/F,GPIO2,UserPB

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

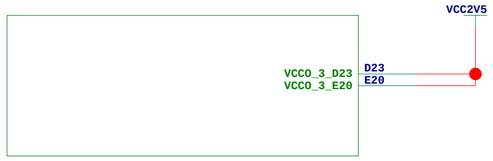
SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		15 of 37	9-24-2006_11:34



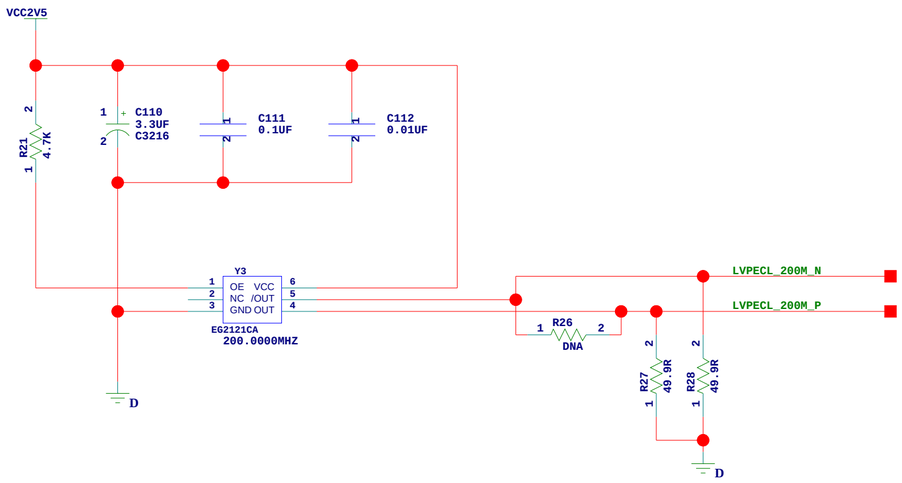
from J10/J11 this page
from U8 Sheet24
To Sheet6 U16 QA1/nQA1
from U3 Sheet10
from U2 Sheet9

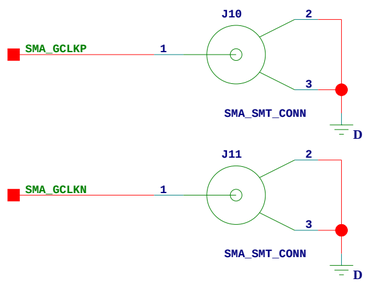
U10
FPGA1



U10
FPGA1

200.0000MHz Epson EG2121CA-200.0000M-PHPAB





Bank3 Global Clock

Bank3 Clocks

Xilinx

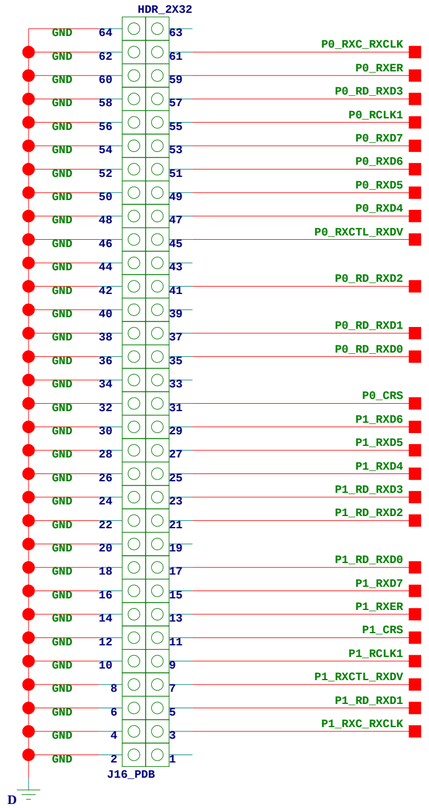
TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

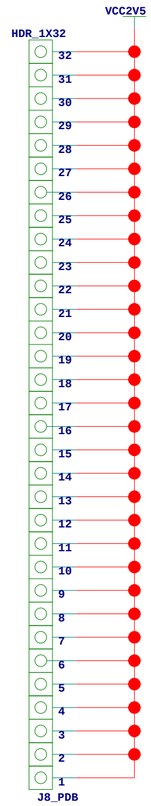
SIZE	DWG NO	REV
C	0381219	01

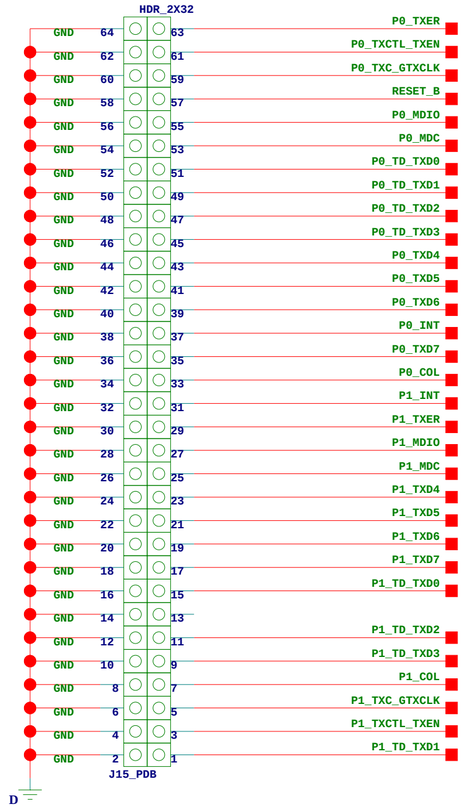
DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		16	37	9-11-2006_16:57

HW-AFX-BERG-EPHY Interface

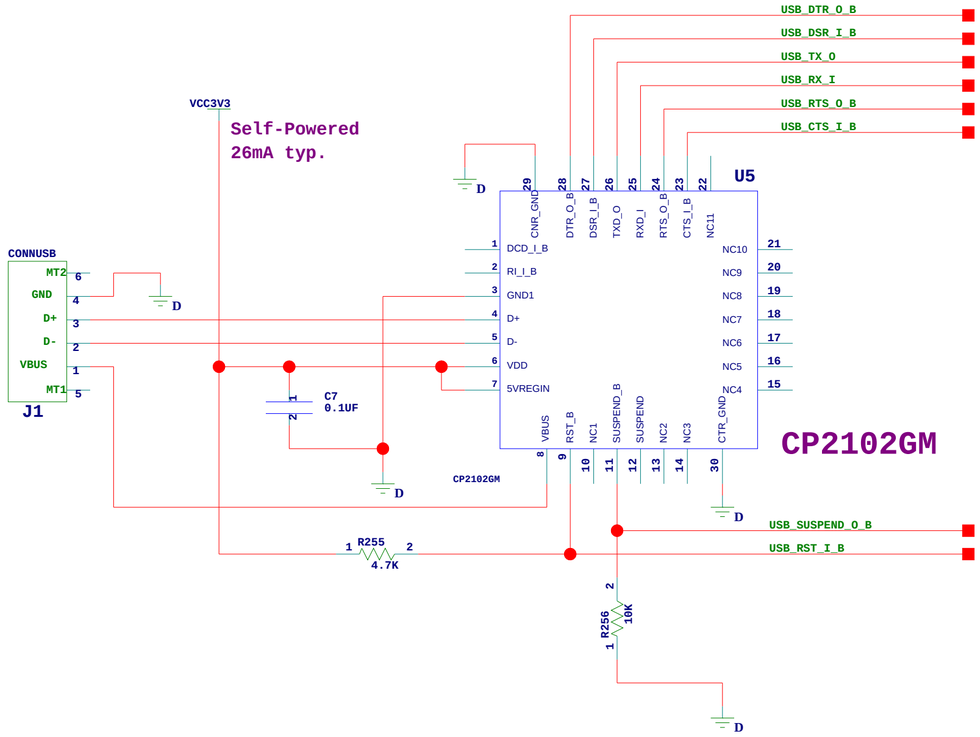
Bank12 Sheet18

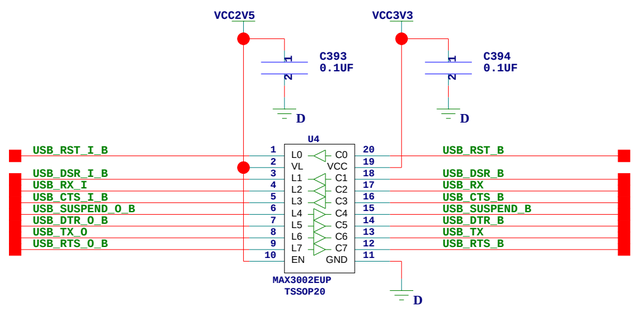






Bank20 Sheet18





To/From FPGA
Bank1 Sheet16

USB to RS232 Converter
(full UART interface implementation)

BERG EPHY Header

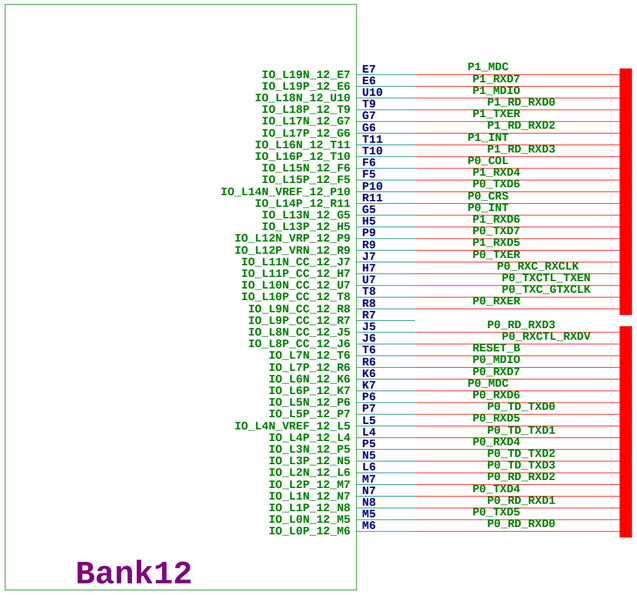
USB to RS232 Converter

Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

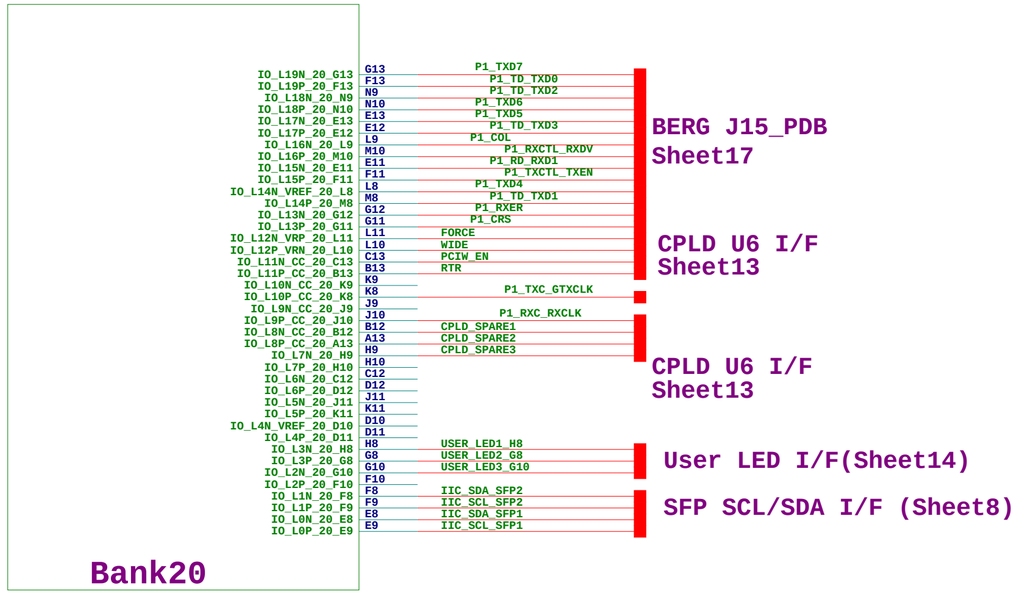
SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		17 of 37	9-6-2006_11:43



BERGJ15_PDB Sheet17

BERGJ16_PDB Sheet17



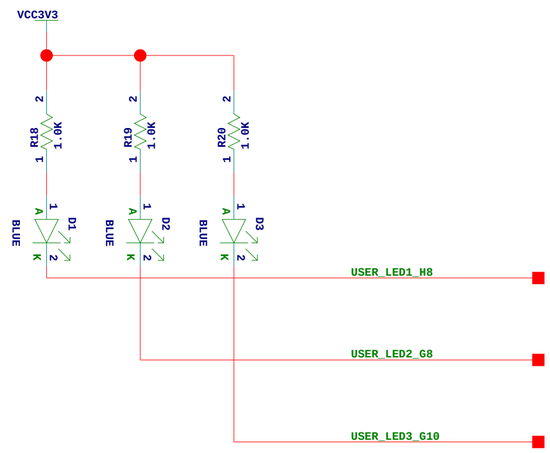
BERG J15_PDB Sheet17

CPLD U6 I/F Sheet13

CPLD U6 I/F Sheet13

User LED I/F(Sheet14)

SFP SCL/SDA I/F (Sheet8)



Bank12 BERG I/F

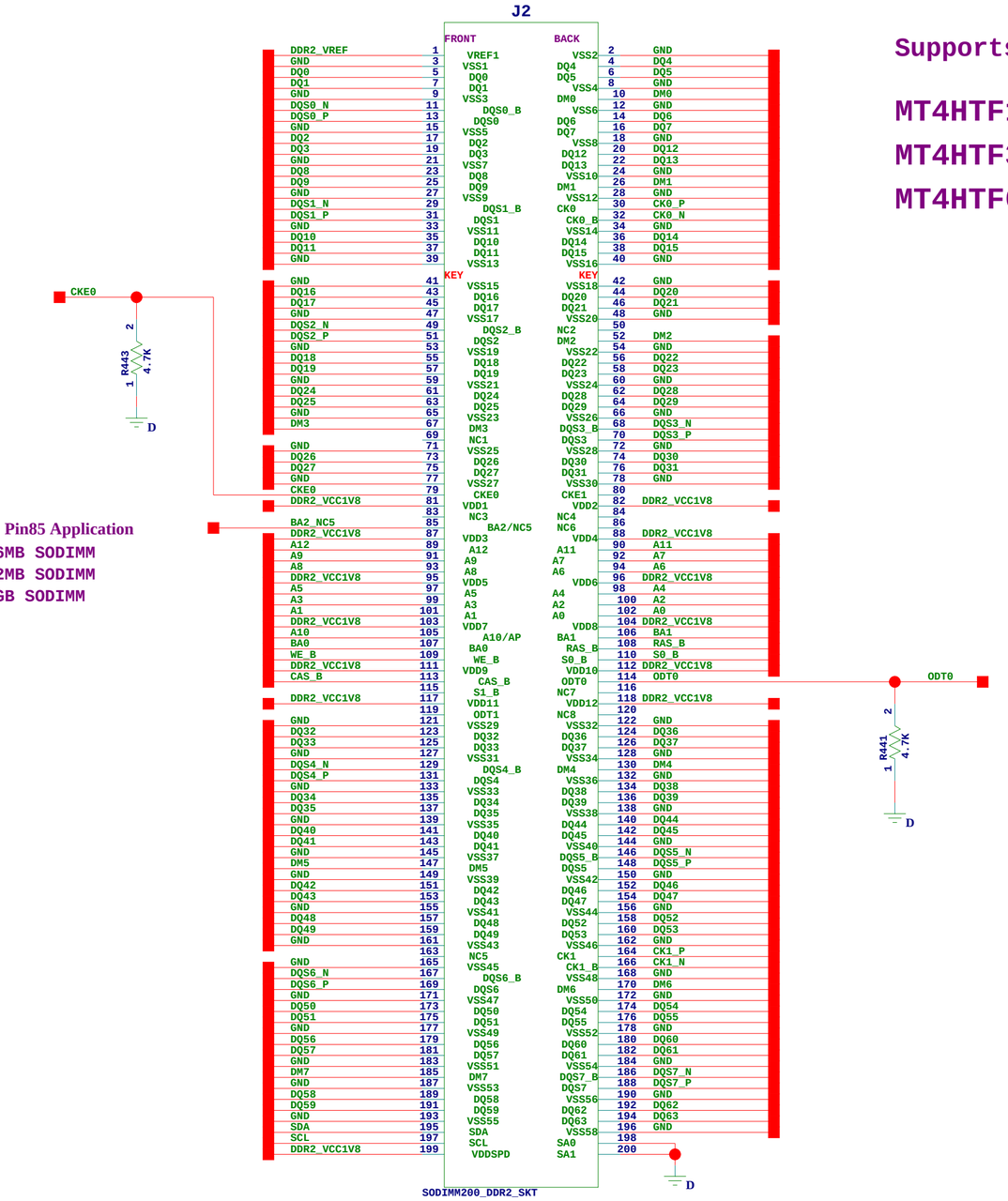
Bank20 BERG HDR, CPLD, PF I/F

Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE: C | DWG NO: 0381219 | REV: 01

DRAWN BY: DAVID NAYLOR | SCALE: | SHEET: 18 of 37 | 8-30-2006_8:08



Pin85 Application

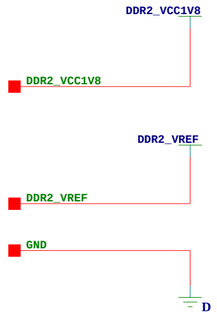
- NC for 256MB SODIMM
- NC for 512MB SODIMM
- BA2 for 1GB SODIMM

Supports Micron single rank SODIMMs:

MT4HTF1664HY-667 128MB

MT4HTF3264HY-667 256MB

MT4HTF6464HY-53E 512MB



SODIMM DDR-2 200-pin 1.8V memory socket

121 pin interface

Xilinx

TITLE

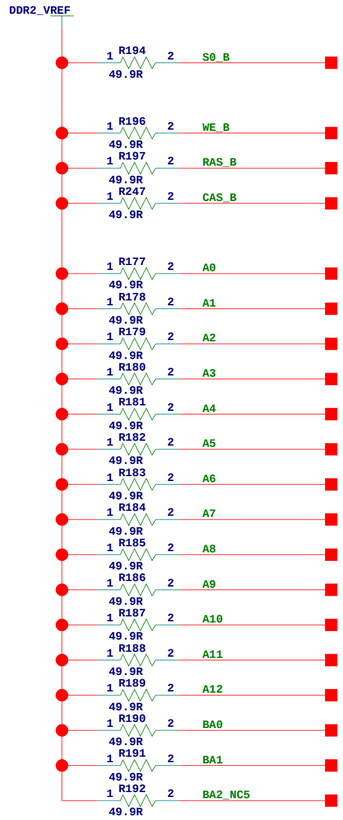
SCHEM, ML555

PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

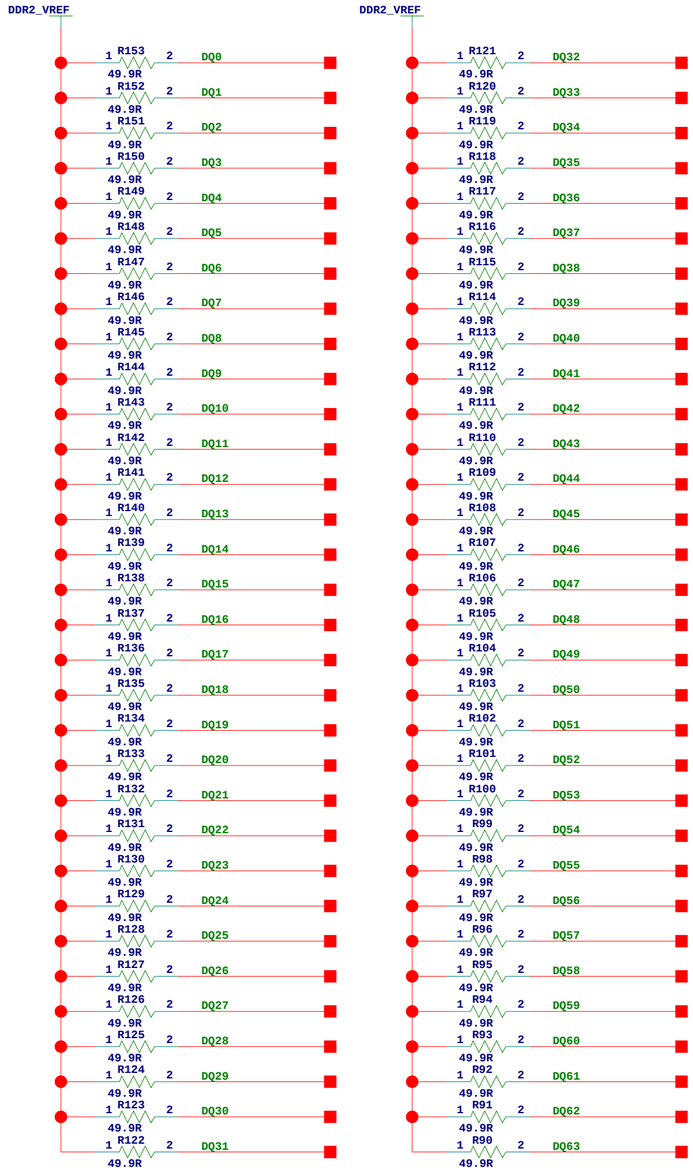
DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		19	37	9-14-2006_6:09

SODIMM End of bus



For DQS, ODT active on the memory module

FPGA End of bus



For DQS, FPGA will implement DIFF_SSTL18_II

DDR-2 SODIMM Terminations

Xilinx

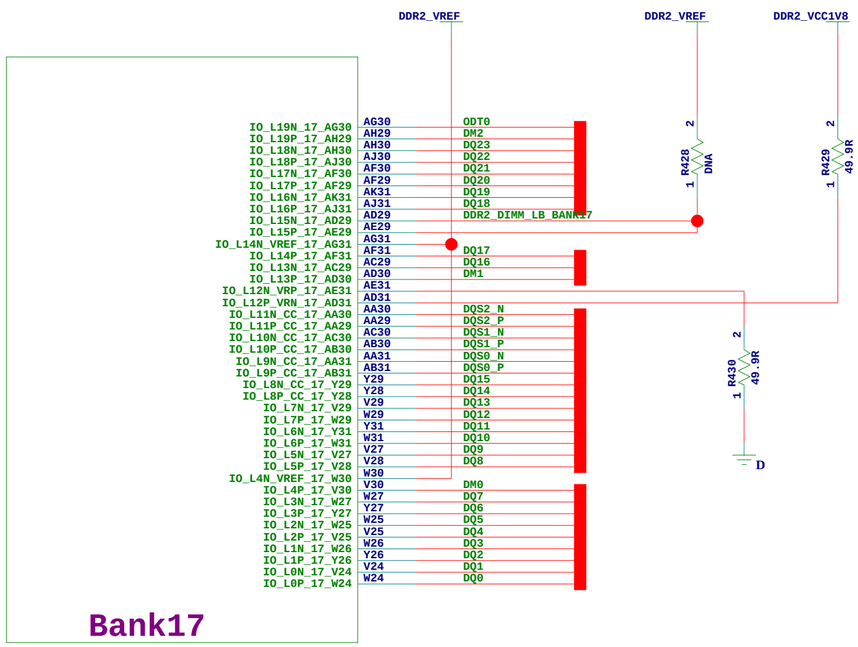
TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		20 of 37	5-30-2006_18:44

CK0: DQ[31:0]

LOOP LENGTH = SUM (CK0 + DQS0)

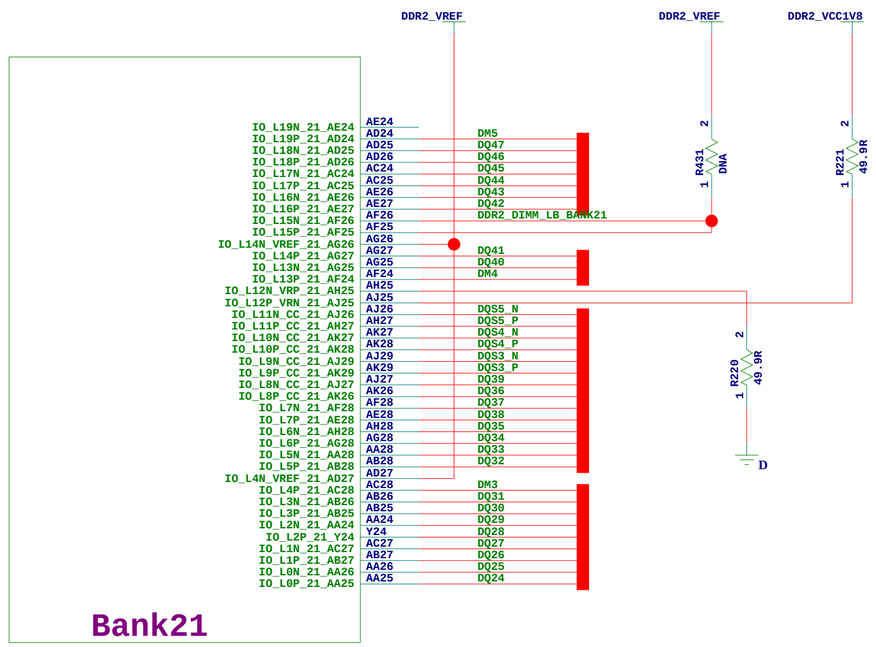


U10
FPGA1
5VLX50T
FF1136

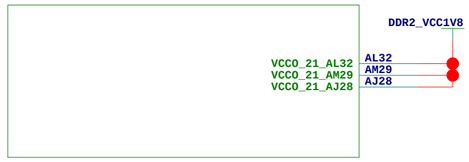
U10
FPGA1

CK0: DQ[31:0] CK1: DQ[63:32]

LOOP LENGTH = SUM (CK1 + DQS4)



U10
FPGA1
5VLX50T
FF1136



U10
FPGA1

Banks 17,21 DDR2 SODIMM I/F to Sheet19

Xilinx

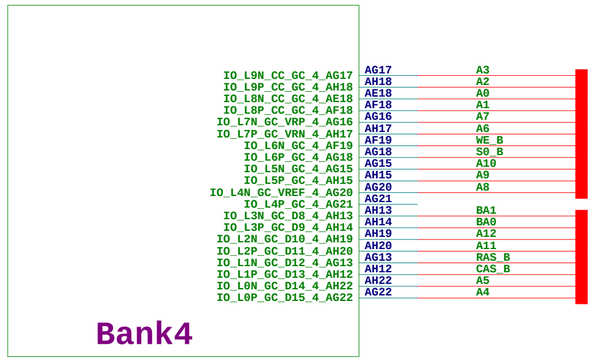
TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

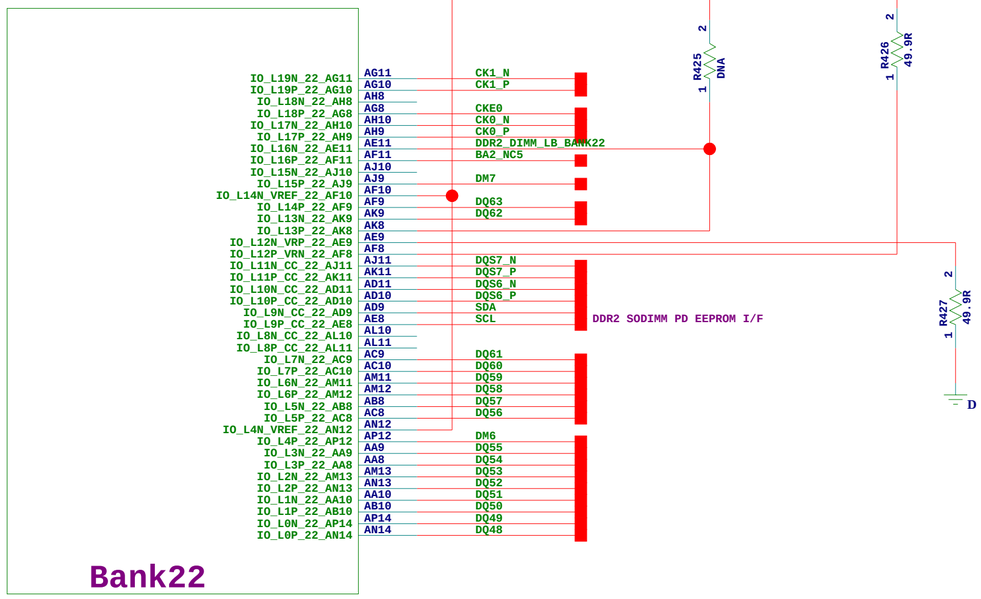
DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		21	37	9-2-2006_10:39

CK1: DQ[63:32]

LOOP LENGTH = SUM (CK1 + DQS6)



U10
FPGA1



U10
FPGA1
5VLX50T
FF1136

U10
FPGA1

U10
FPGA1

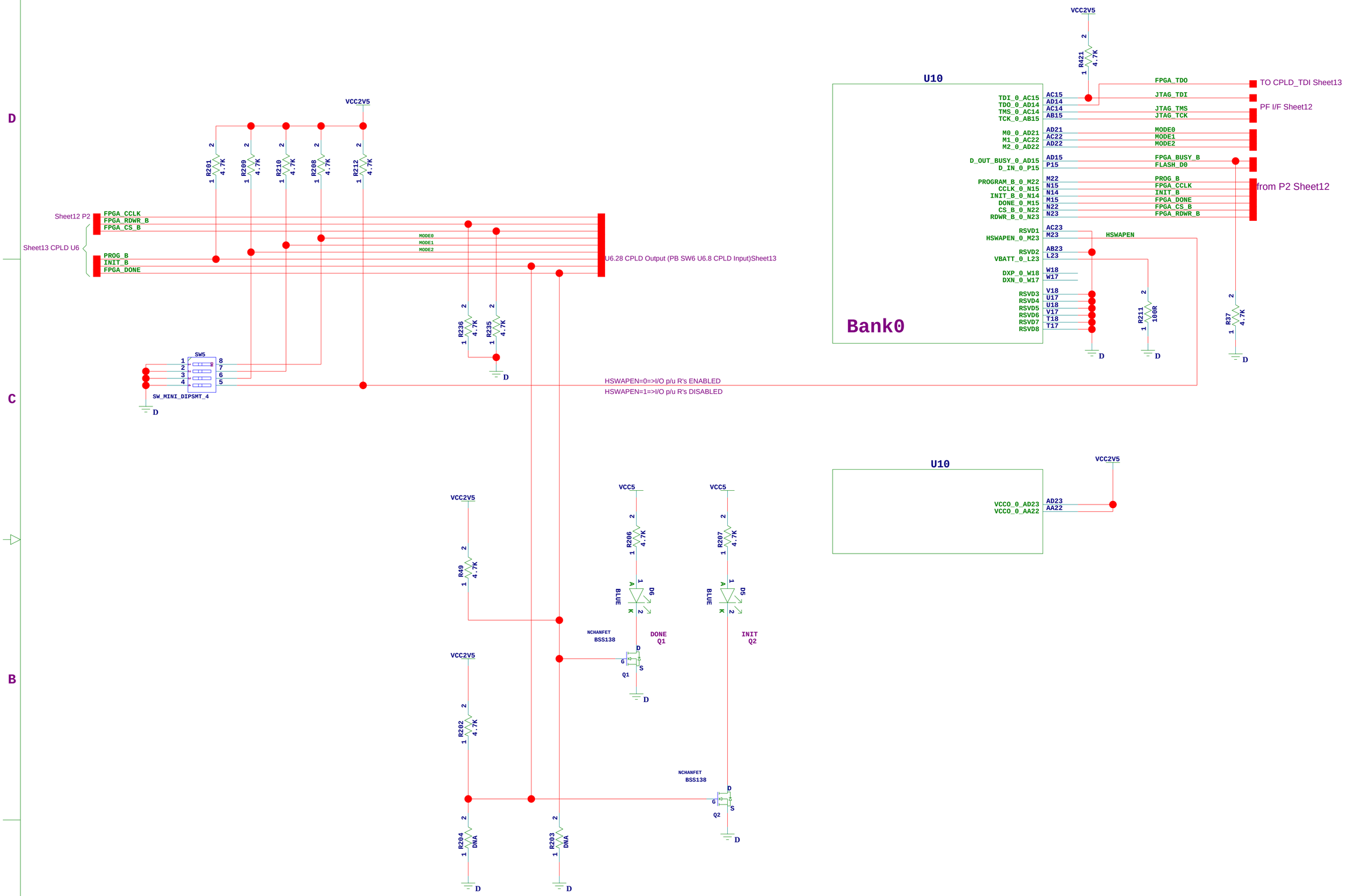
Banks 4,22 DDR2 SODIMM I/F

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		22 of 37	9-13-2006_9:09



Bank0 CONFIGURATION I/F

Xilinx

TITLE	SCHEM, ML555 PCIE PCI PCI-X PCB,1280389
SIZE	C
DWG NO	0381219
REV	01
DRAWN BY	DAVID NAYLOR
SCALE	
SHEET	23 of 37
	6-13-2006_17:32

Freq. Load Button

Xtal Sel

VCO Sel

Parallel Freq. Set

Programmable ICS "Clock_1" 31.25MHz - 700MHz

to Sheet25 SW17.9

to Sheet16
Bank3 GCLK SODIMM I/F

to Sheet6
MGT X0Y1 MGTREFCLK

ICS8442AY

Xilinx	
TITLE	SCHEM, ML555 PCIE PCI PCI-X PCB,1280389
SIZE	C
DWG NO	0381219
REV	01
DRAWN BY	DAVID NAYLOR
SCALE	
SHEET	24 of 37
	8-31-2006_16:25

Freq. Load Button

Xtal Sel

VCO Sel

Parallel Freq. Set

SW11
SW-PBUTTON
CM2_FREQ_LD_PB_N
R433 4.7K
R434 4.7K
R435 4.7K
Q4
NCHANFET
BSS138
PLOAD_2
R437 1.0K
C17 22PF
C14 22PF
X2
MA-505
25MHZ
25MHz
CM2_25M_XTAL_OUT
CM2_25M_XTAL_IN
P16
P21
CM2_XTAL_SEL
CM2_VCO_SEL
VCC3V3
C15 22NF
SW12
SW_MINI_DIPSMT_8
CM2_M0
CM2_M1
CM2_M2
CM2_M3
CM2_M4
CM2_M5
CM2_M6
CM2_M7
CM2_M8
CM2_N0
CM2_N1
U7
ICS8442AY
XTAL_OUT
TST_CLK
XTAL_SEL
VDDA
S_LOAD
S_DATA
S_CLK
MR
CM1_N1
from Sheet24
R438 4.7K
R439 4.7K
STROBE_2
SDATA_2
SCLOCK_2
LVDSCLKMOD2_N
LVDSCLKMOD2_P
SMTPAD3
SMTPAD2
SMTPAD1
to Sheets 9&10
SATA+SMA MGT
and SFP MGT
'Scope Trigger Tap
FIL3
R440 10R
C378 10UF C3216
C370 22NF
C371 220PF
R359 4.7K
R361 100R
R363 100R
R367 4.7K
R365 4.7K
R358 4.7K
R360 100R
R362 100R
R366 4.7K
R368 4.7K
R364 4.7K
FIL4
C372 22NF
C373 220PF
C374 22NF
C375 47UF C3528
C376 22NF
C377 220PF
MGT_X0Y3_RCLKN
MGT_X0Y3_RCLKP
to Sheet6
MGT X0Y3 MGTREFCLK

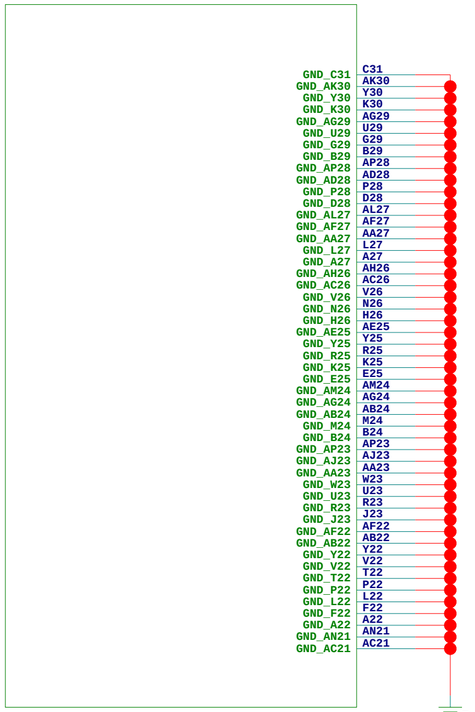
Programmable ICS "Clock_2" 31.25MHz - 700MHz

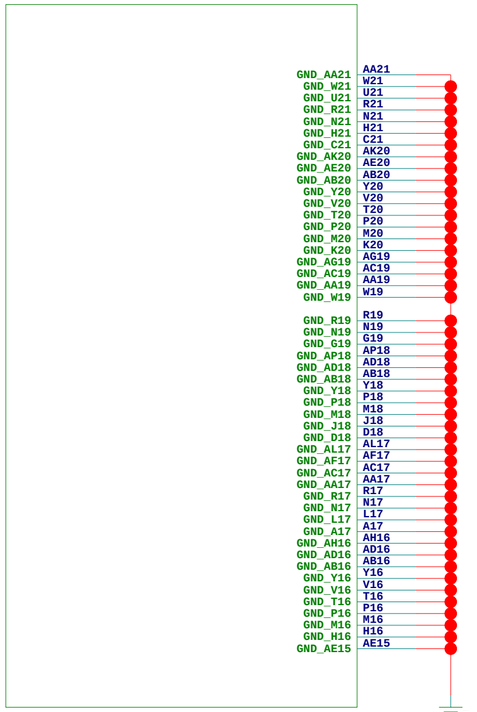
Xilinx

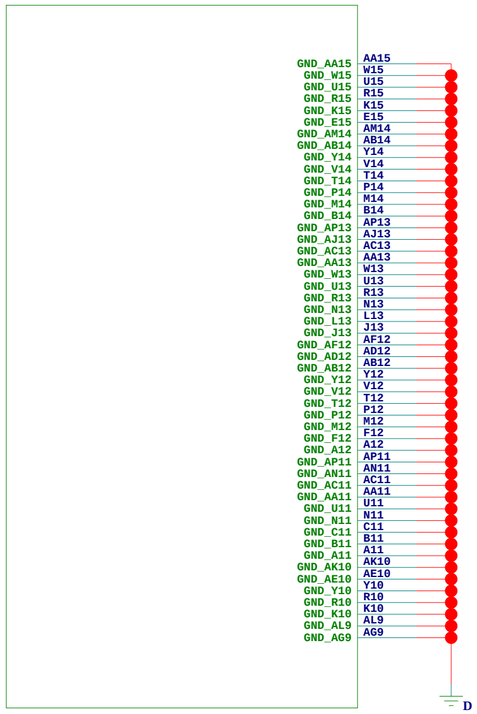
TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

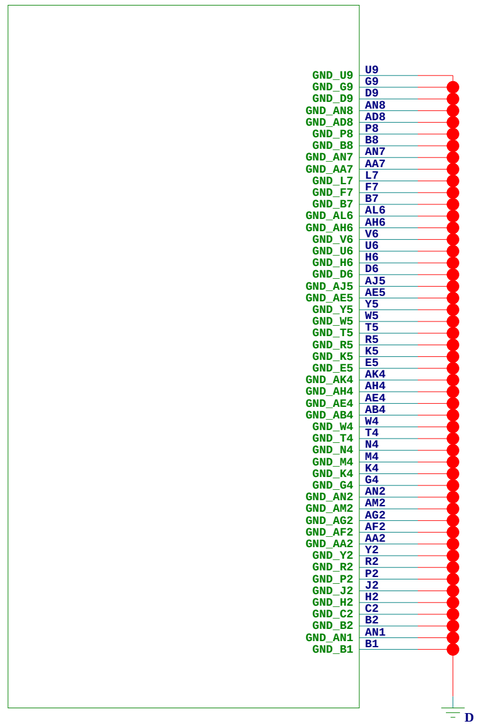
SIZE	DWG NO	REV
C	0381219	01

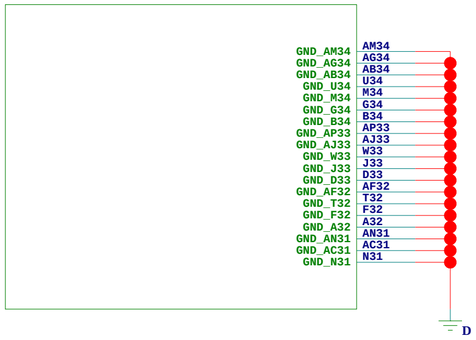
DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		25 of 37	9-5-2006_6:09

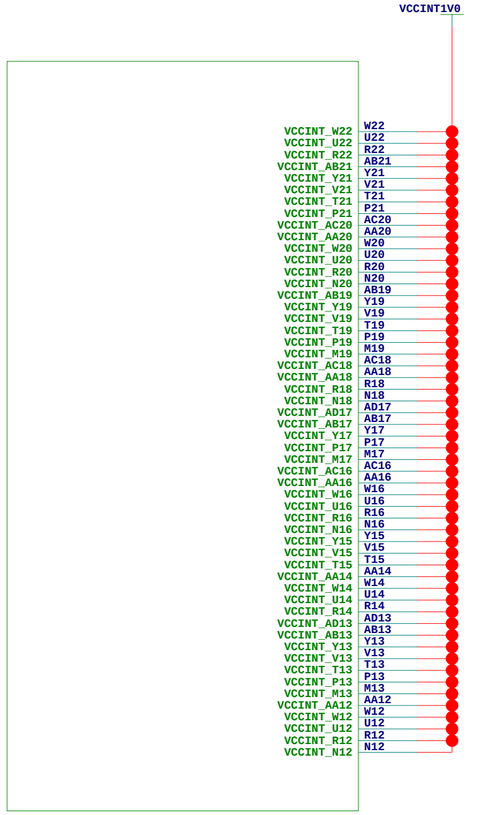


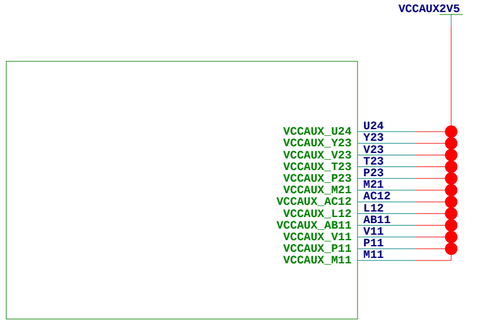












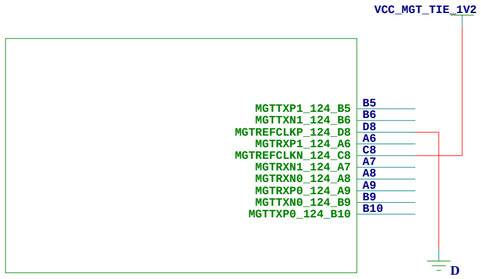
FPGA Core Power, and GND

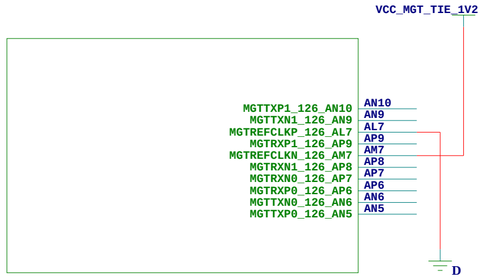
Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

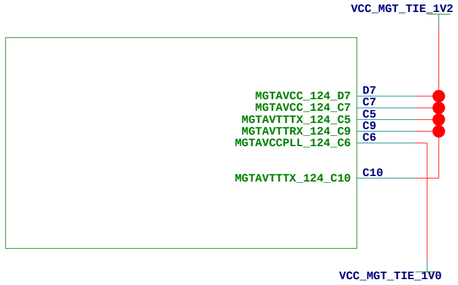
SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		26	37	5-30-2006_18:44

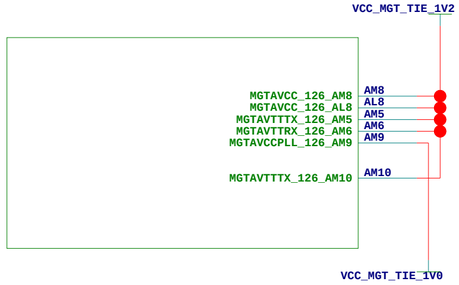




U10
FPGA1
5VLX50T
FF1136



U10
FPGA1
5VLX50T
FF1136



U10
FPGA1
5VLX50T
FF1136

GTP TIE OFF TAPS

Unused MGTs

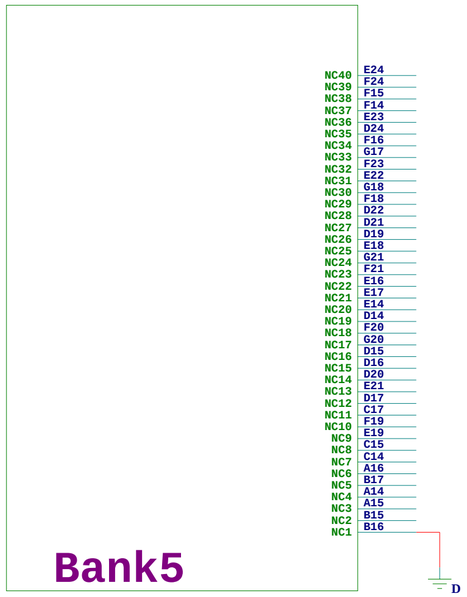
(5vlx110tff1136)

Xilinx

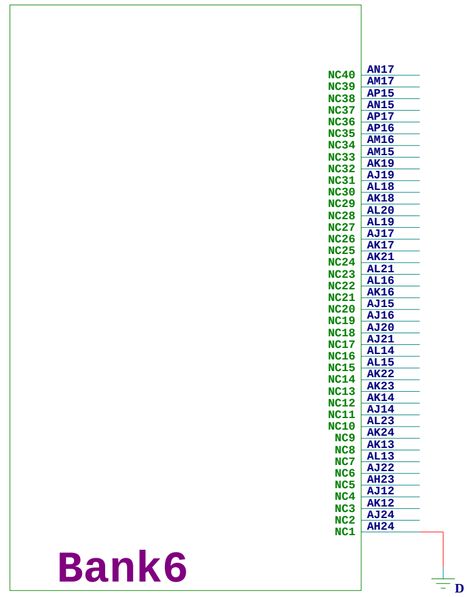
TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

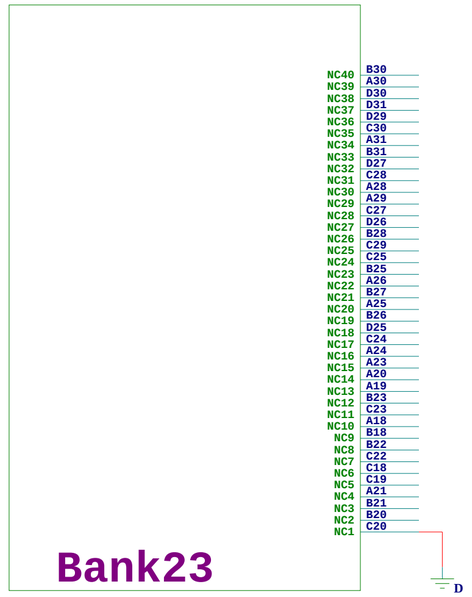
DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		27 of 37	6-5-2006_9:28



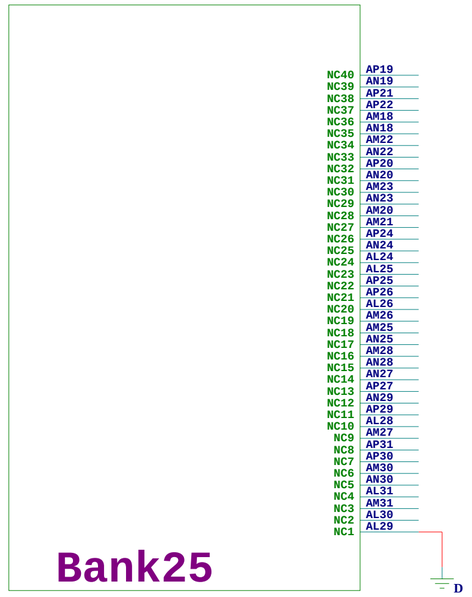
U10
FPGA1
5VLX50T
FF1136



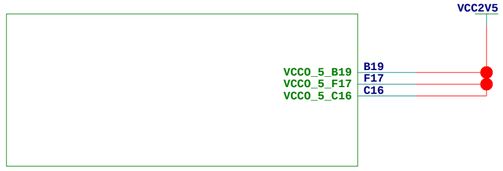
U10
FPGA1



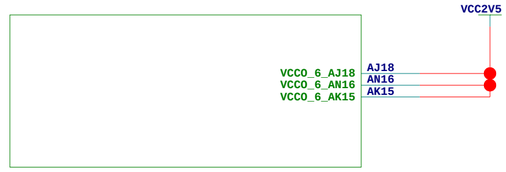
U10
FPGA1
5VLX50T
FF1136



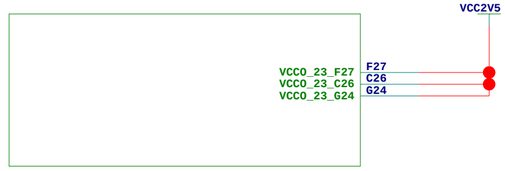
U10
FPGA1



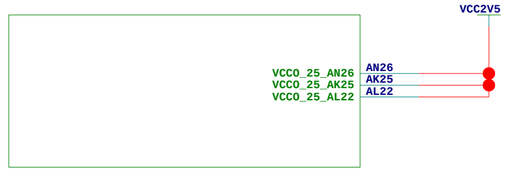
U10
FPGA1



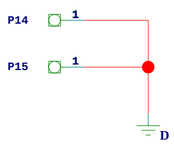
U10
FPGA1



U10
FPGA1



GND TP



Fiducials

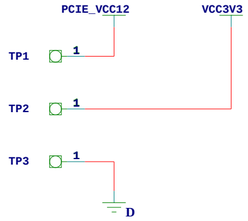
Comp Side

FID1
FID2
FID3

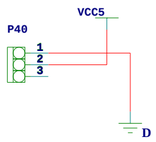
Solder Side

FID4
FID5
FID6

Stand-Alone Power Taps



PTH Holes to solder wire into



Radian INF35001-16
Fan Heat Sink Power

Metal Bracket Mounting Holes

(0.116" 4-40 clearance)

MH1
MH2

EPHY Daughter Card Standoff Mounting Holes

(0.144" 6-32 clearance)

MH3
MH4

Banks 5,6,23,25 are N/C in 5VLX50T-FF1136

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

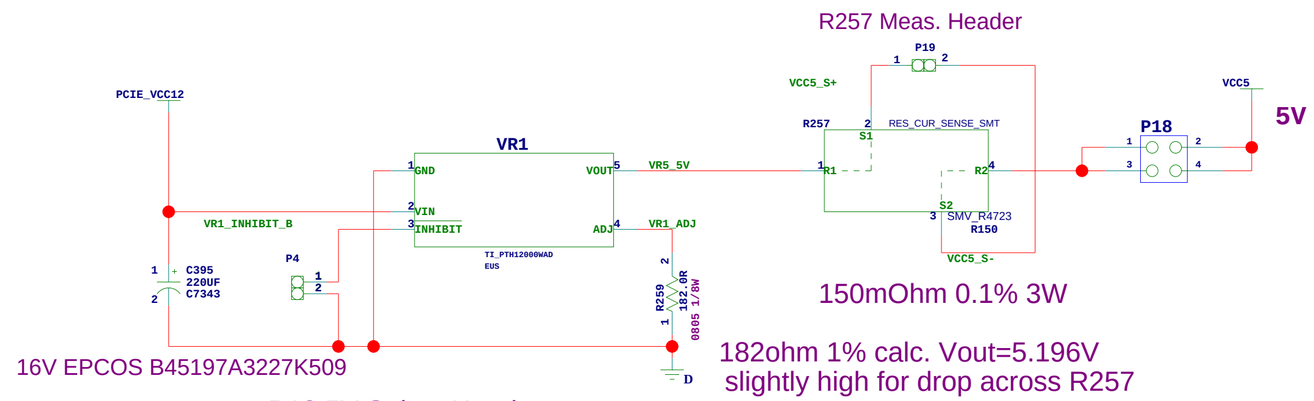
SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		28 of 37	7-17-2006_9:18

PCIe 12V input conversion to VCC5

PCIe 12.0V @ 5.5A (75W Slot)
PCIe 3.3V @ 3.0A (75W Slot)

PCI   5.0V @ 5.0A (25W Slot)
PCI   3.3V @ 7.6A (25W Slot)



16V EPCOS B45197A3227K509

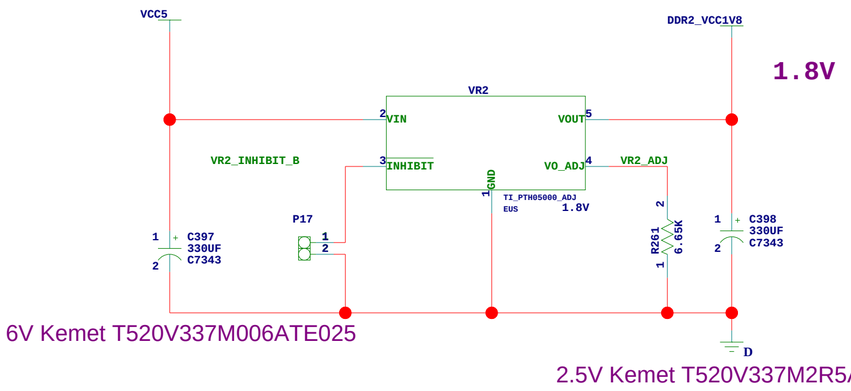
182ohm 1% calc. Vout=5.196V
slightly high for drop across R257
(typ. VCC5 = 5.08V)

P18 5V Select Header

1-2 & 3-4 ON = PCIe Mode

1-2 & 3-4 OFF = PCI/PCI-X Mode

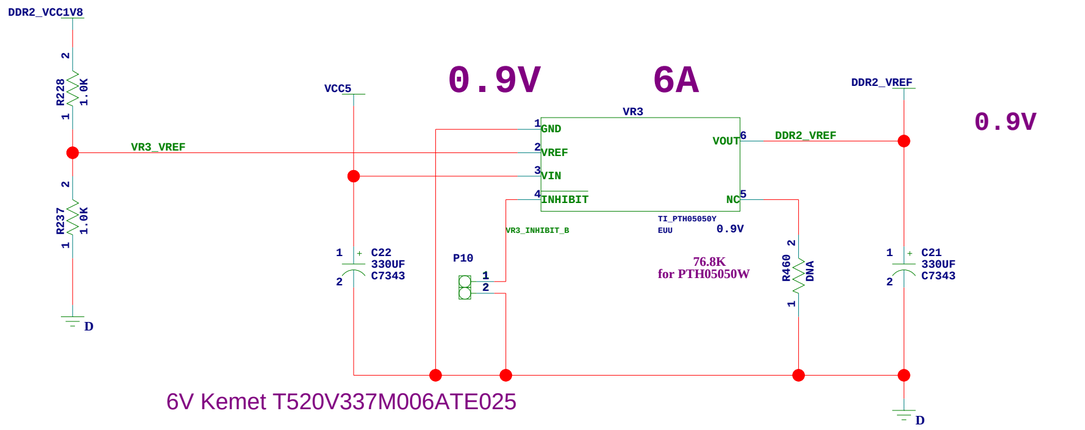
5V input to DDR2 1.8V output



6V Kemet T520V337M006ATE025

2.5V Kemet T520V337M2R5ATE025

1.8V DDR2 reference input to 0.9V DDR-2 Vtt



6V Kemet T520V337M006ATE025

2.5V Kemet T520V337M2R5ATE025

VR1 PTH12000 12Vin-to-5Vout

VR2 PTH05000 5Vin-to-1.8Vout

VR3 PTH05050 1.8V/2 in-to-0.90V out

Power Regulators - Sheet 1

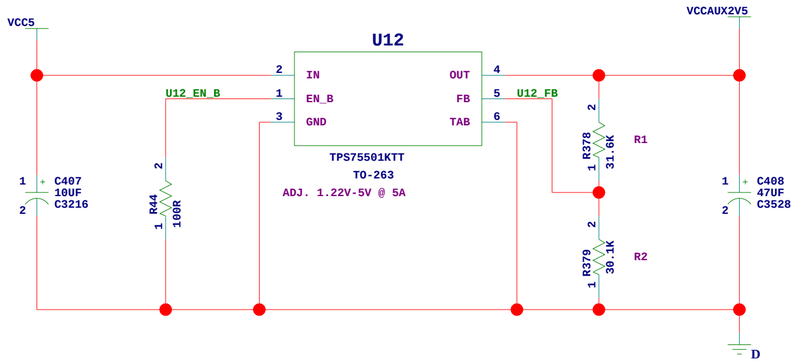
Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE: C | DWG NO: 0381219 | REV: 01

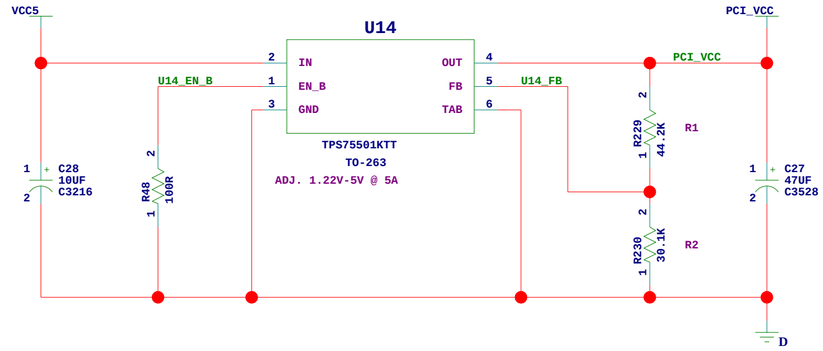
DRAWN BY: DAVID NAYLOR | SCALE: | SHEET: 29 of 37 | 10-4-2006_11:33

2.5089V @5A
U12 2.5V Vccaux



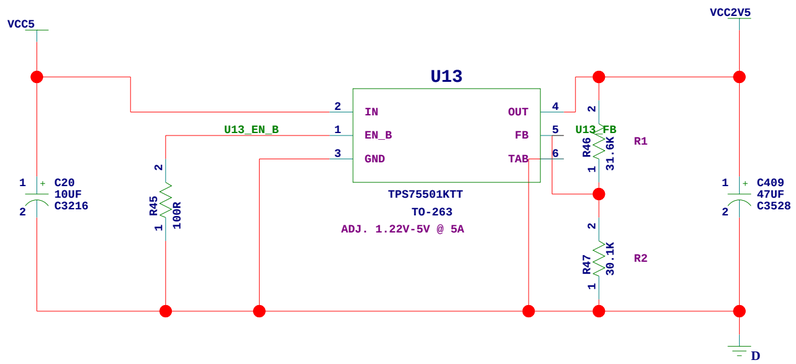
6.0V Kemet T520B476M006ATE070

3.0214V @5A
U14 3.0V PCI_VCC



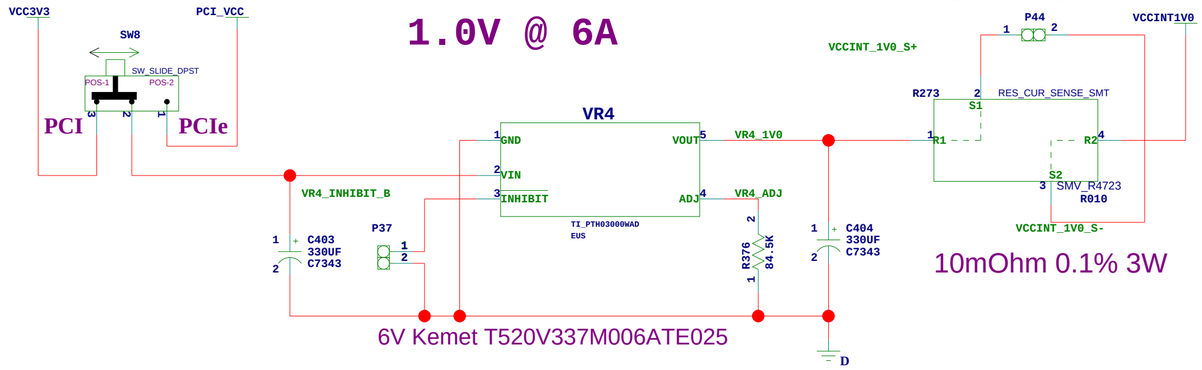
6.0V Kemet T520B476M006ATE070

2.5089V @5A
U13 2.5V Vcco



6.0V Kemet T520B476M006ATE070

3.0V input to FPGA Vccint 1.0V @ 6A



6V Kemet T520V337M006ATE025

Bus Mode	SW8 Position	VCCNIT_1V0 via VR4 from
PCIe	2	U14 PCI_VCC 3.0V Regulator
PCI/PCI-X	1	PCI Bus 3.3V

VR4 PTH03000 3.3Vin-to-1.0Vout (Vccint)

U12 TPS75501 5Vin-to-2.5Vout (Vccaux)
U13 TPS75501 5Vin-to-2.5Vout (Vcco)
U14 TPS75501 5Vin-to-3.0Vout (PCI_VCC)

1Vx4A=4W

4W/3V=1.33A

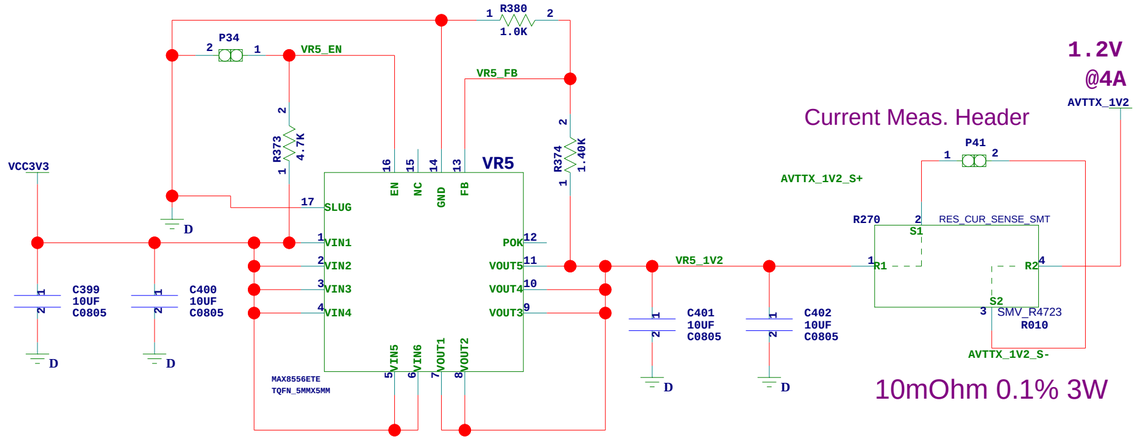
Power Regulators - Sheet 2

Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE: C | DWG NO: 0381219 | REV: 01

DRAWN BY: DAVID NAYLOR | SCALE: | SHEET 30 of 37 | 9-6-2006_12:04



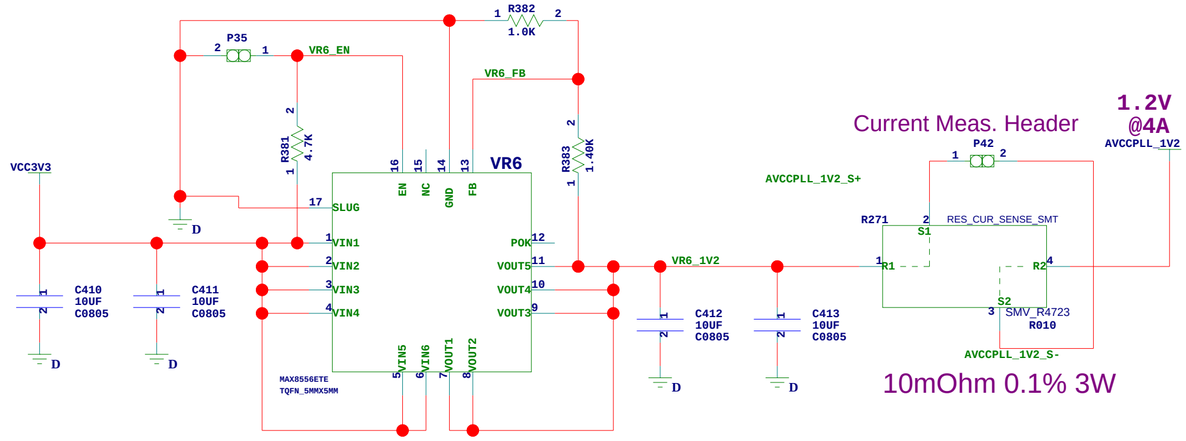
5VLX50T MGT Supply#1/3

AVTTX 1.2V - 150mA per MGT = 1.8A

AVTTRX 1.2V - 100mA per MGT = 1.2A

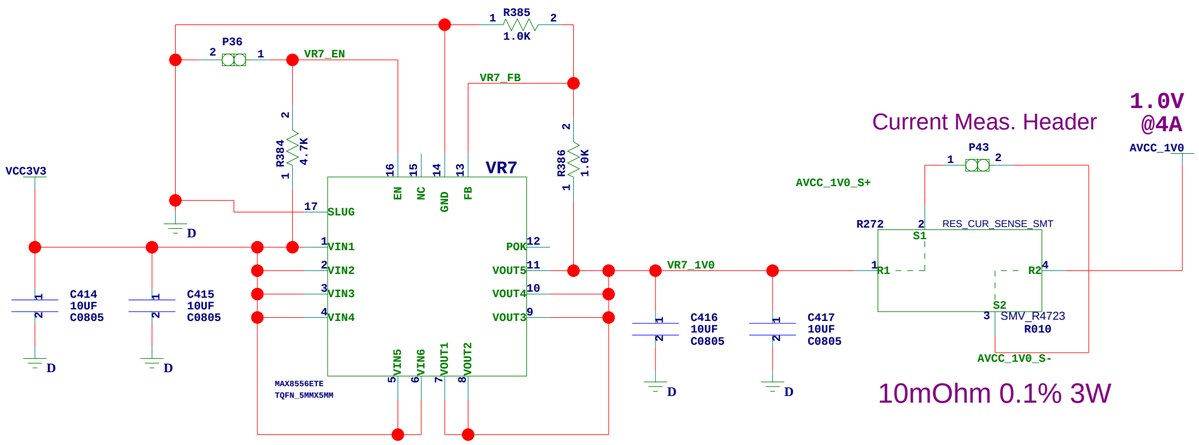
VVTTRXC 1.2V - 50mA per MGT = 0.5A

on same regulator



5VLX50T MGT Supply#2/3

AVCCPLL 1.2V - 150mA per MGT = 1.8A



5VLX50T MGT Supply#3/3

AVCC 1.0V - 150mA per MGT = 1.8A

Power Regulators - Sheet 3

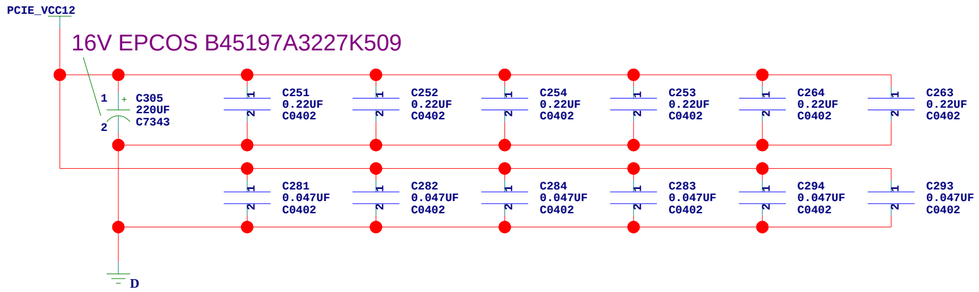
Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

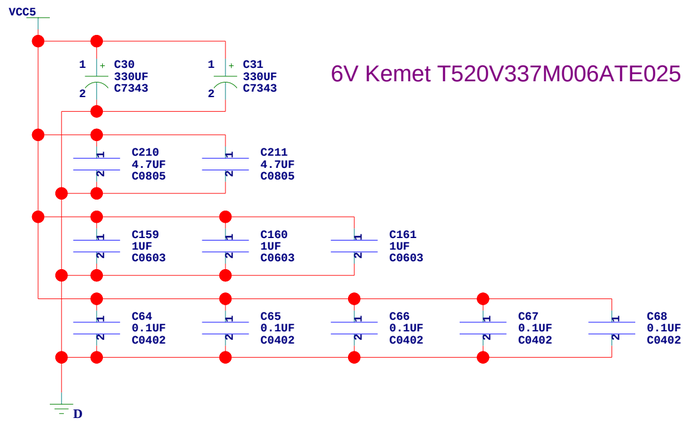
SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		31	37	9-6-2006_11:46

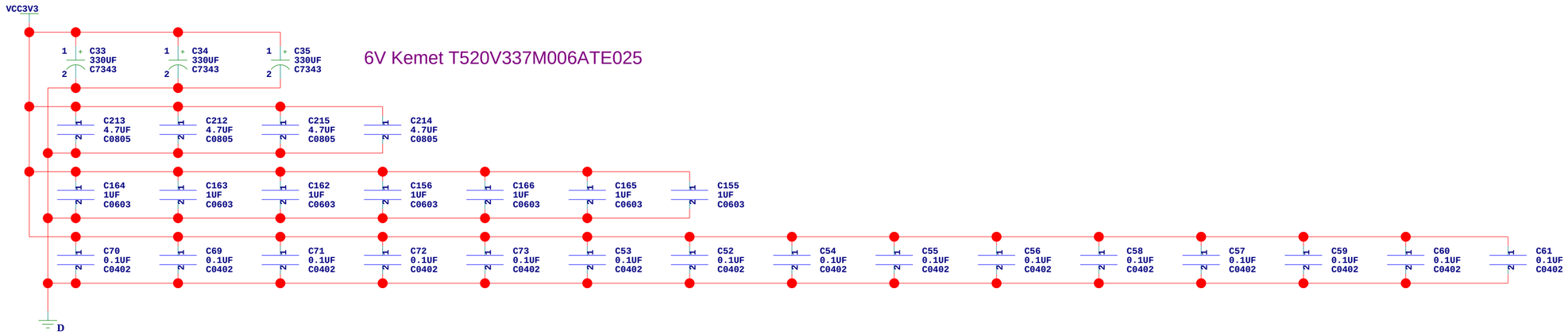
+12V from PCIe Edge Conn P13



5V VR1 Output + PCI Edge Conn P1



PCIe/PCI Edge +3.3V



Decoupling CAPS Page 1:

Decoupling CAPS for PCI Edge Conn.:

+12V(PCIe),+5V(PCI),+3.3V(both)

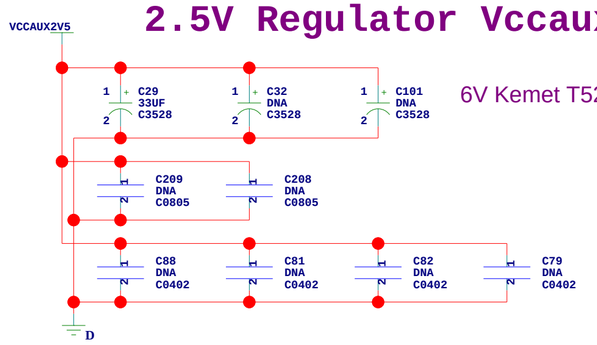
Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

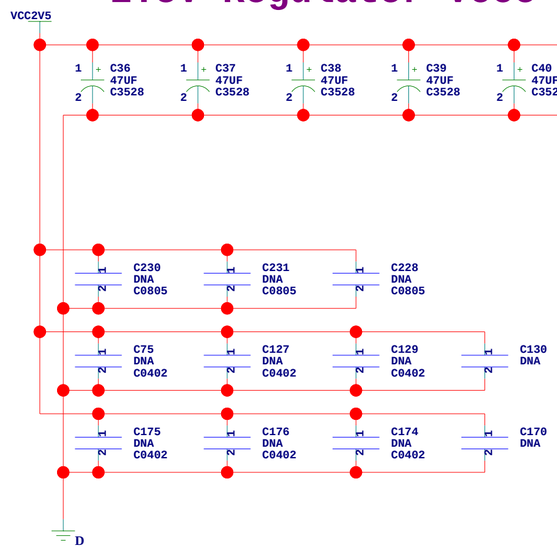
DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		32 of 37	8-29-2006_17:41

2.5V Regulator Vccaux



6V Kemet T520V336M006ATE040

2.5V Regulator Vcco



6.0V Kemet T520B476M006ATE070

Additional LX110T decoupling
deleted, not enough room on ML555

Reference Sheet 1, Note 4:
PCIe CEM Spec, Pg. 56 footnotes:

MGTs X0Y0,X0Y1,X0Y2,X0Y3 PCIe
8-Lane Edge Connector I/F

Decoupling CAPS Page 2:

Decoupling Caps for:

2.5V Regulator Vcco

2.5V Regulator Vccaux

Xilinx

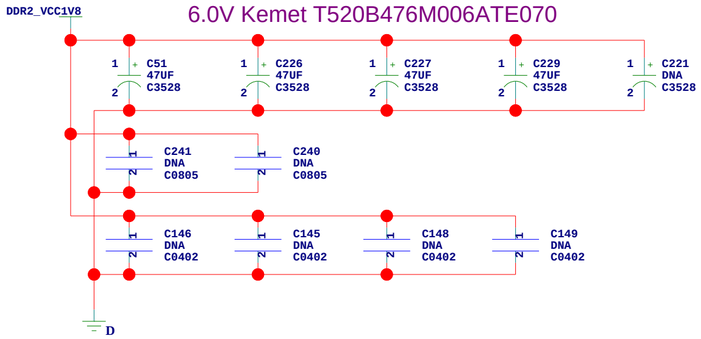
TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		33 of 37	9-12-2006_12:12

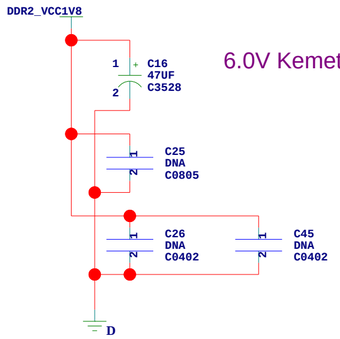
1.8V FPGA Vcco (Mem I/F)

6.0V Kemet T520B476M006ATE070



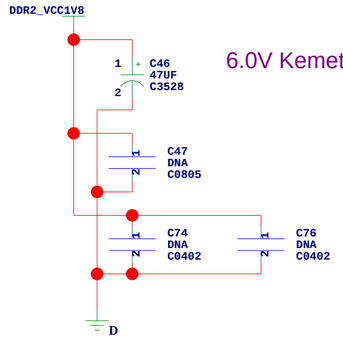
1.8V PF U1 Vccint

6.0V Kemet T520B476M006ATE070



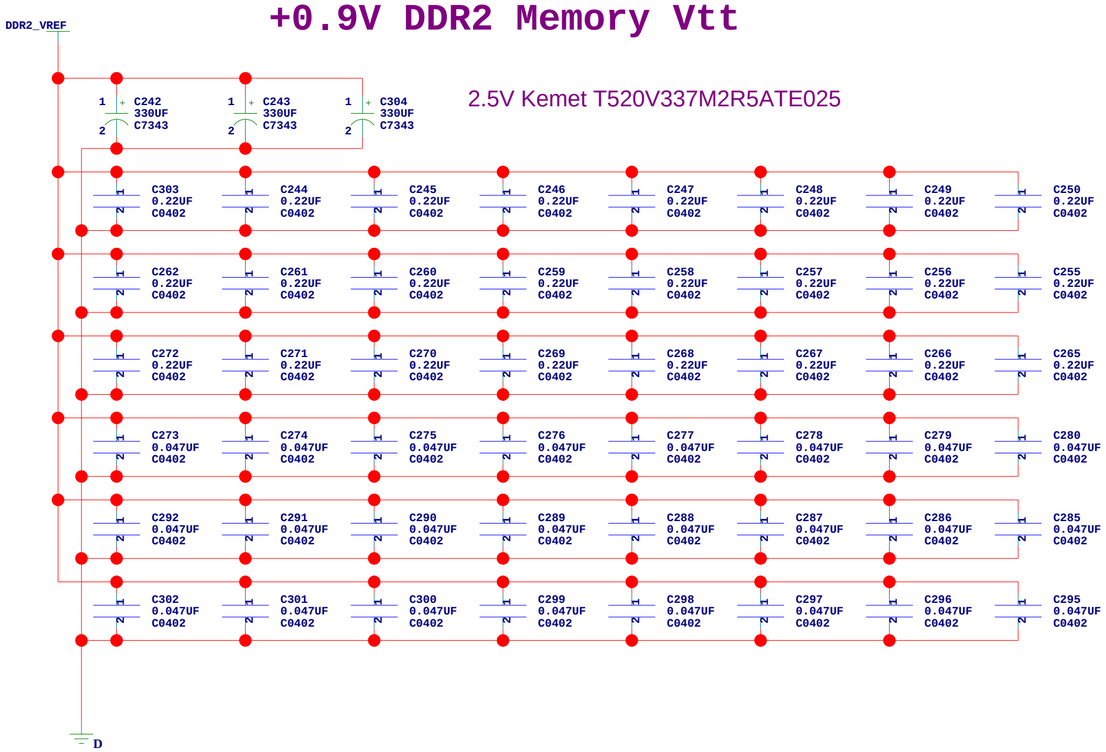
1.8V PF U15 Vccint

6.0V Kemet T520B476M006ATE070



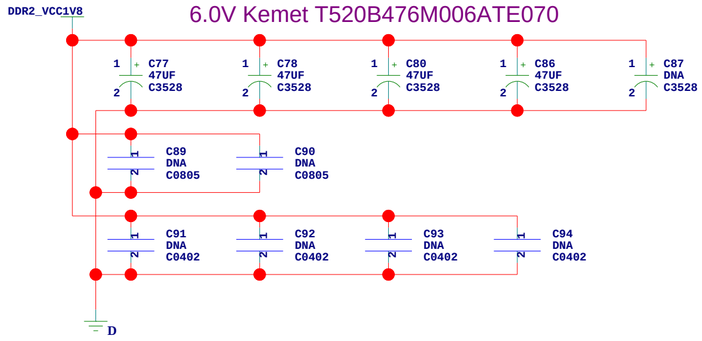
+0.9V DDR2 Memory Vtt

2.5V Kemet T520V337M2R5ATE025



1.8V Mem SODIMM

6.0V Kemet T520B476M006ATE070



Decoupling CAPS Page 3:

Decoupling Caps for:

1.8V Reg.Mem.SODIMM+FPGA Bank Vcco

1.8V Reg.PF Vccint

0.9VRegulator Vtt (84 PullUp R's on Sht20)

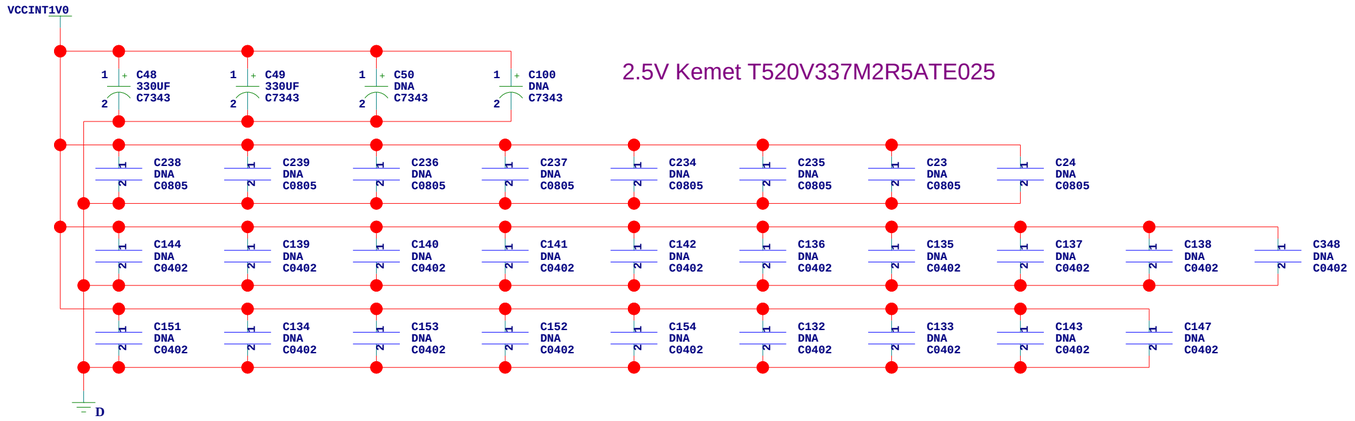
Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

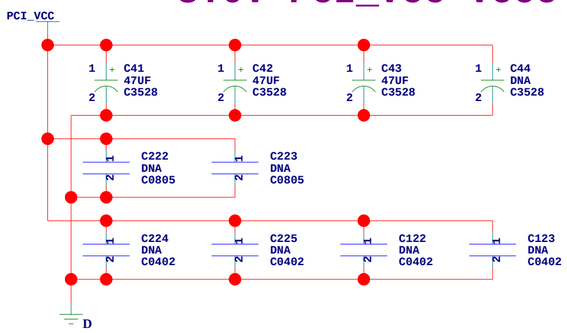
SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		34 of 37	6-30-2006_14:11

1.0V FPGA Vccint



3.0V PCI_VCC Vcco



Decoupling CAPS Page 4:

Decoupling Caps for:

- 1.0V Regulator FPGA Vccint
- 3.0V Regulator PCI_VCC Vcco

Xilinx

TITLE: SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	01

DRAWN BY	SCALE	SHEET	
DAVID NAYLOR		35 of 37	6-30-2006_14:11

VR5 MAX8556/7
AVTTTX/RX 1.2V
4A
MGT Supply

P34 Inhibit

VR6 MAX8556/7
AVCCPLL 1.2V
4A
MGT Supply

P35 Inhibit

VR7 MAX8556/7
AVCC 1.0V
4A
MGT Supply

P36 Inhibit

P4 Inhibit

VR1 PTH12000
PCIe12V=>VCC5
6A

P18

1 2 3 4

Jumper = on for PCIe
Jumper = off for PCI/PCI-X

VR2 PTH05000
DDR2_1V8
6A

P17 Inhibit

1.8V DDR2 SODIMM

0.9V DDR2 Vref

VR3 PTH05050
DDR2_VREF
6A

P10 Inhibit

0.9V DDR2 Vref

U14 TPS75501
PCI_VCC (3.0V)
5A

FPGA Vcco
3.0V PCI I/F

U13 TPS75501
VCCO_2V5
5A

FPGA Vcco

U12 TPS75501
VCCAUX_2V5
5A

FPGA Vccaux

PCIe POS-2
SW8
PCI POS-1

1 2 3

VR4 PTH03000
VCCINT_1V0
6A

FPGA Vccint

Motherboard PCIe Slot/Conn. Sources 3.3V and 12V

PCIe 3.3V@3.0A

PCIe 12V@5.5A

PCI 3.3V@7.6A

Motherboard PCI Slot/Connector Sources 3.3V and 5V

PCI 5V@5.0A

Voltage Regulator Topology

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	E8

DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		36	37	6-8-2006_14:03

PCI/PCI-X 64-bit Edge Connector

SFP#1

SFP#2

Platform Flash
&
CPLD

5vlx50t-ff1136

PTH03000
Vout=1.0V/6A

PTH05000
Vout=1.8V/6A

PTH05050
Vout=0.9V/6A

HW-AFX-BERG-EPHY I/F

DDR2 SODIMM

HW-AFX-BERG-EPHY Outline

SATA

MGT SMA I/F

JTAG Conn.

CLKIN SMA I/F

GTPCLK SMA I/F

USB "B"

USB/UART
+Level Shifter

Samtec#1

Samtec#2

PTH12000
Vout=5V/6A

PCIe 8-Lane Edge Connector

GTP Power Regs

3 X MAX8557
on back of board

ML555 Block Diagram, PCB Component Side

Xilinx

TITLE
SCHEM, ML555
PCIE PCI PCI-X PCB,1280389

SIZE	DWG NO	REV
C	0381219	E8

DRAWN BY	SCALE	SHEET	of	
DAVID NAYLOR		37	37	7-13-2006_10:19