Virtex-5 LXT Development Kit for PCI Express –
ML555 Board Overview

XILINX®

Agenda

- Overview
- ML555 Features
- Block Diagram
- PCI Express
- PCI and PCI-X
- System Power Configuration
- Clocking
- DDR2 Memory
- Ethernet Support
- GTP Interfaces
- SMA Peripherals
- USB Interface
- Configuration

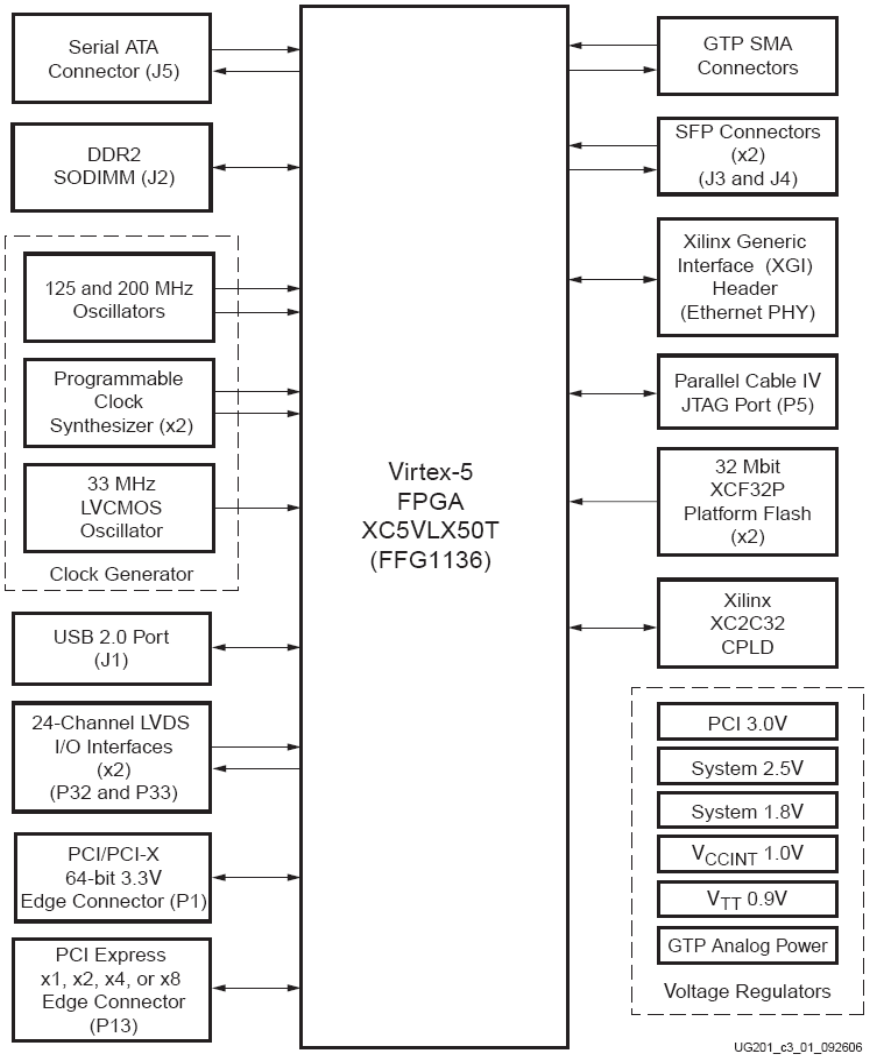
Overview

- Produce a development board for parallel & serial PCI
  - Support soft IP cores: PCI and PCI-X
  - Support Virtex-5 LXT PCIe Endpoint Block and GTP transceiver
    - Endpoints: x1, x2, x4 and x8
    - PCIe Endpoint Block and PCIe Endpoint Block Plus LogiCORE designs
- Support 10/100/1000 Mbps hard & soft Ethernet MAC IP
  - HW-AFX-BERG-EPHY adapter (sold separately)
  - Two SFP cages (optics not included)
  - 1000BASE-X PCS/PMA with GTP and SFP module
- Support GTP (12 interfaces)
  - PCI Express: x1, x2, x4 or x8 endpoint
  - Two SFP cages
  - One Serial ATA port
  - One SMA port for off-board expansion

ML555 Features

- 5VLX50T-FFG1136
  - 480 SelectIO
- Form factor: 4.70” x 10.5”
  - 3.3V PCI(-X) add-in card
  - PCI Express Endpoint add-in card
- 256MB DDR2 SDRAM
  - 200-pin SODIMM interface
  - 400 MT/s
  - 1.8V I/O (SSTL_18)
  - DDR2 on die termination (ODT)
- Clocking options
  - 33 MHz, 125 MHz & 200MHz
  - PCI clocks: regional & global
  - Clock synthesizers
    - For SODIMM and GTP
- DC power input
  - 12V & 3.3V PCIe connector
  - 5V & 3.3v PCI-X connector
  - Power monitoring (GTP +Vccint)
- SAMTEC connectors for LVDS I/O
- Ethernet support
  - Xilinx BERG expansion header
  - HW-AFX-BERG-EPHY
  - MII, GMII, RGMII, SGMII
- GTP support
  - x1, x2, x4 or x8 PCIe Endpoint
  - 2 SFP interfaces (optics not included)
  - 1 set of SMA connectors
  - 1 Serial ATA port
- USB 2.0 to RS232 bridge
- User pushbuttons/LEDS (3 sets)
- Device Configuration
  - JTAG: PC IV or Platform Cable USB
  - Platform Flash (multi-image)
    - Multiple 5VLX50T images supported
  - Static and dynamic device reconfiguration

Block Diagram

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PCI Express Support

- PCI Express Endpoint: x1, x2, x4 or x8
  - ML555 uses 8 lane PCIe add-in card connector
  - x1 and x2 lane interface requires adapter
  - Not all systems with 8 lane connector are wired for 8 lanes!
- COREGen PCIe reference designs in kit
  - X4 and x8 lane endpoints in Platform Flash U1 image 0 & 1
    - PCI Express Endpoint Block LogiCORE
  - See CDROM for demo and design information
- PCIe REFCLK connects to GTP X0Y2 MGTREFCLK
  - 100MHz spread spectrum REFCLK supported
    - PCIe reference designs support 100MHz REFCLK

ML555 PCI Express Connectivity

- Timing optimized for 8 lane PCI Express designs
  - PCI Express Lanes 0 & 1 <= GTP_DUAL X0Y2
  - PCI Express Lanes 2 & 3 <= GTP_DUAL X0Y1
  - PCI Express Lanes 4 & 5 <= GTP_DUAL X0Y3
  - PCI Express Lanes 6 & 7 <= GTP_DUAL X0Y0

CORE Generator optimally places the GTP_DUALs

Follow these GTP placements to simplify timing!!!

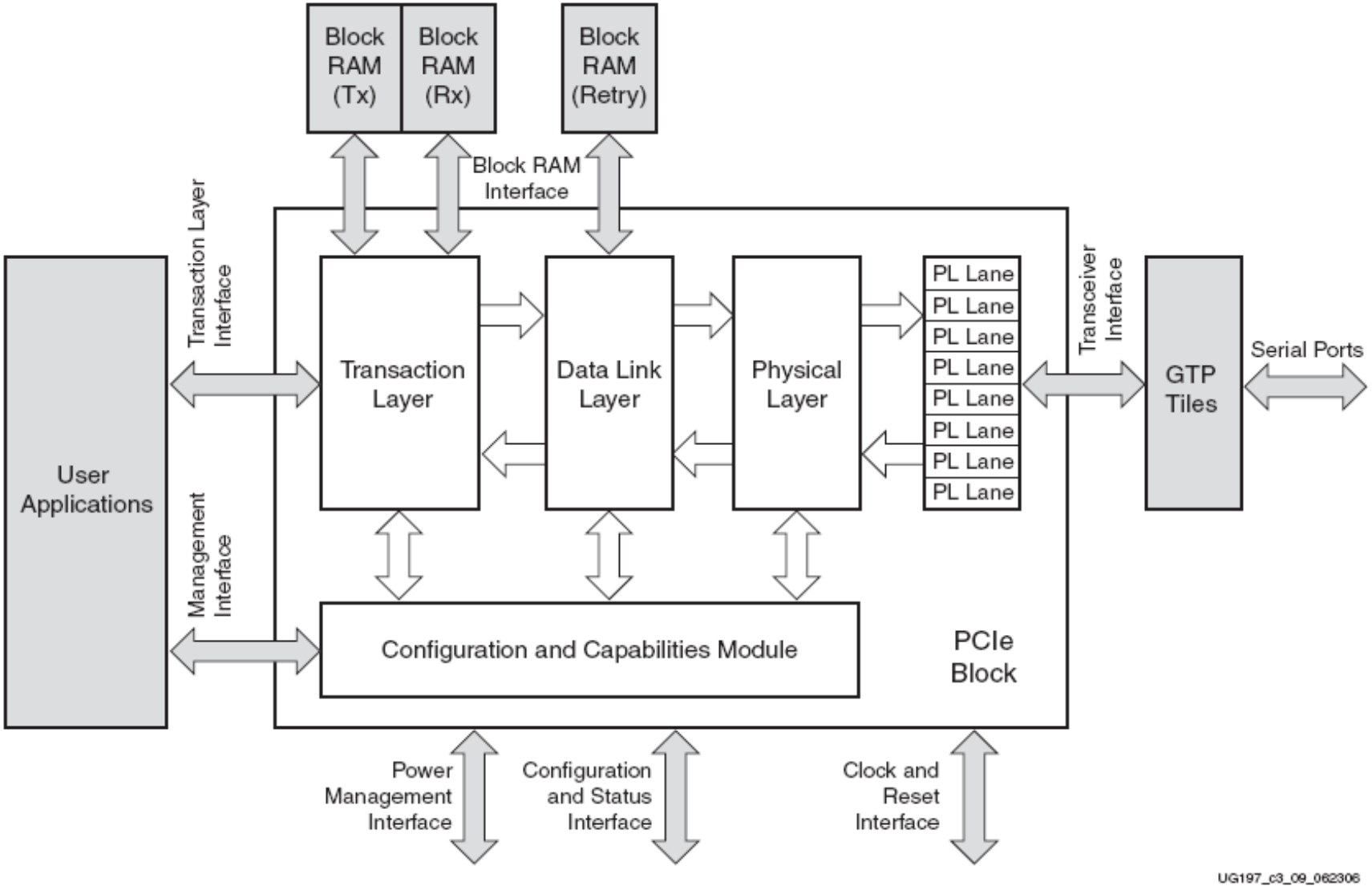


Figure 3-9: **PCIe Block Connections/Customization Before Using Wrapper**

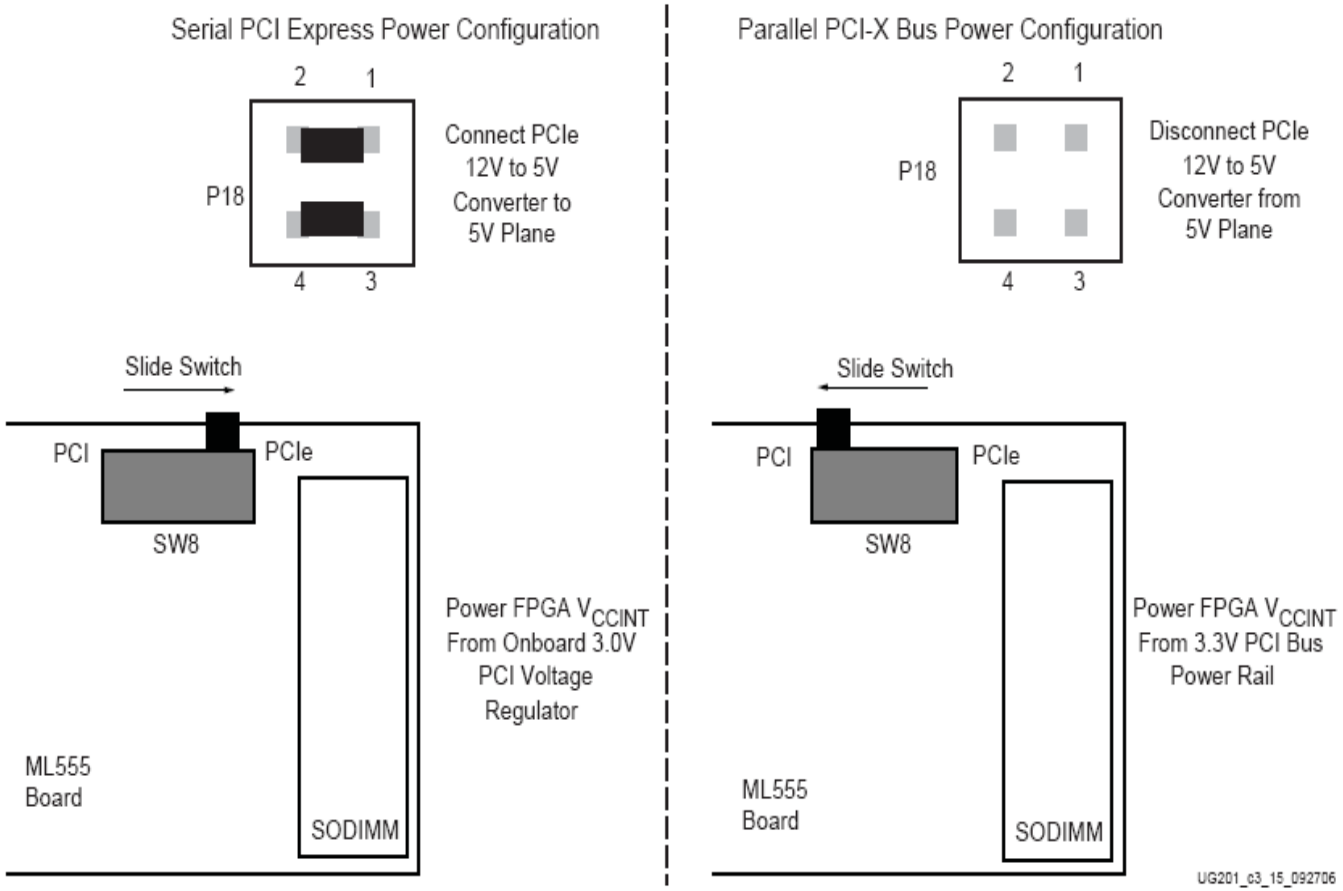
PCI and PCI-X support

- Standard length card: 4.376” x 12.283” (max)
  - Actual board measurements, post layout: 4.7” x 10.50”
  - Slightly higher than standard form factor: dual connector design
- Supports PCI and PCI-X IP cores
  - Version 4.1 (PCI) and 6.1 (PCI-X)
  - Global clock versions
- ML555 uses 3V regulator for 3.3V I/O support
  - Same solution as V-II Pro and V4
- Platform Flash supports four LX50T FPGA device images
  - 33MHz PCI and 133MHz PCI-X design images included
  - See speaker notes

PCI and PCI-X Design

- Simple design included as BIT files on CDROM
  - Same design as generated by COREGen
  - Platform Flash contains 2 PCI and 2 PCIe designs
  - PCI 33MHz and PCI-X 133MHz designs
    - 66MHz PCI not supported at this time
    - Check PCI Product lounge for product/support updates
- One memory BAR and one I/O BAR
  - 16 deep memory behind memory BAR
  - Read/write access supported

ML555 DC Power Configuration

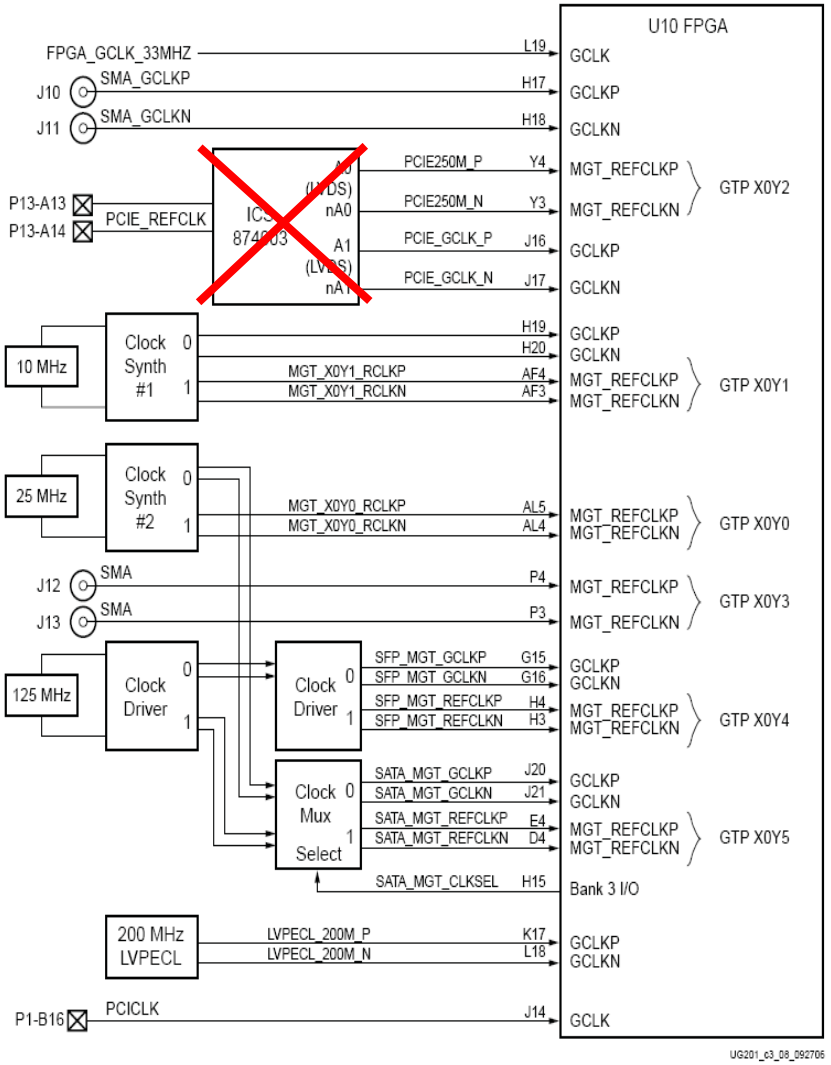


Always check ML555 Power configuration before plugging into a system unit!

Clocks

- PCI and PCI-X bus: global and regional clock inputs
- ICS874003-02 PCI Express Jitter Attenuator Clock
  - 100MHz, 125MHz or 250MHz REFCLK input to GTP tile X0Y2
    - Footprint provided on board for customer installation
    - Not required for V5-LXT PCI Express applications. Xilinx does not provide this component on the ML555 boards. Two zero ohm resistors bypass the device. See UG201 for details. Contact IDT for pricing and availability of components.
    - AC coupled input to GTP tile X0Y2
- Two clock synthesizers (10 & 25 MHz input clocks)
  - One primarily for DDR2 memory
  - Wide range of frequency synthesis: 31MHz to 700MHz
- 125MHz for EMAC reference clock
- 200MHz reference clock for IDELAY / ODELAY
- LVDS SMA global clock input and LVDS SMA GTP MGTREFCLK inputs
- 33MHz for Platform Flash and FPGA user clock

Clocking Block Diagram



GTP Clocking

GTP Tile LOC	FPGA Pins	Clock Source	GTP Connection
X0Y0	AL5, AL4	Clock Synthesizer 2	PCIe Lanes 6 & 7
X0Y1	AF4, AF3	Clock Synthesizer 1	PCIe Lanes 2 & 3
X0Y2	Y4, Y3	PCI Express Clock	PCIe Lanes 0 & 1
X0Y3	P4, P3	SMA GTP REFCLK	PCIe Lanes 4 & 5
X0Y4	H4, H3	125 MHz LVDS oscillator	SFP1 & SFP2
X0Y5	E4, D4	Selectable 125MHz oscillator or Clock Synthesizer 2	Serial ATA and SMA

DDR2 Memory

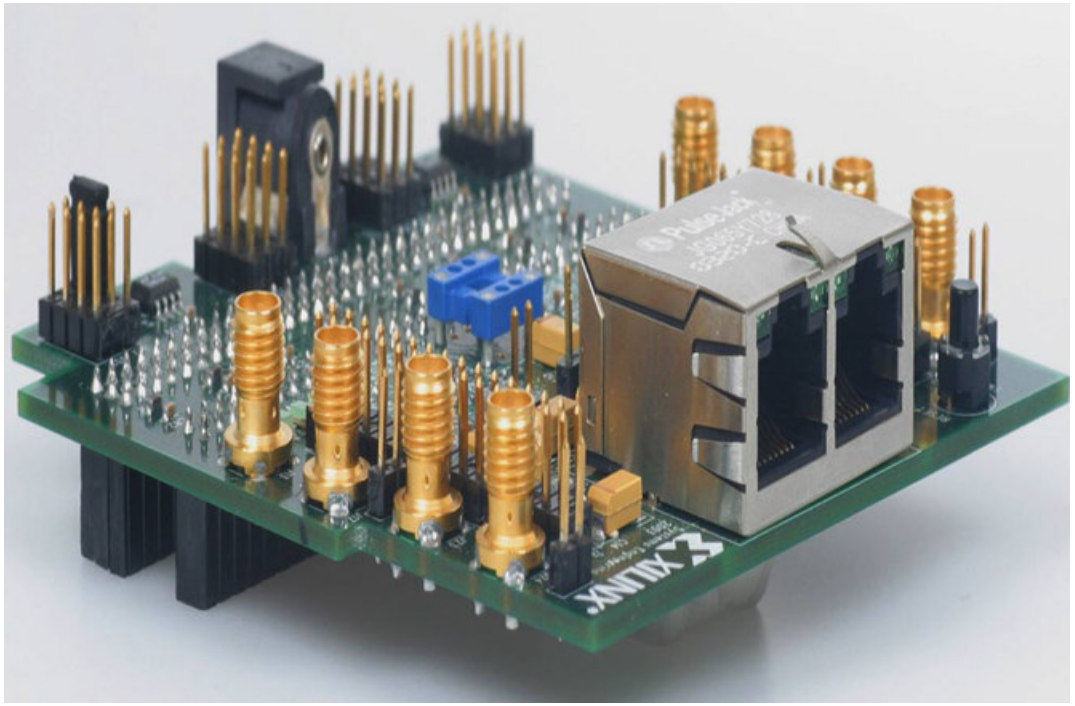
- 200-pin SODIMM (lead free) with 64-bit data path
  - MT4HTF3264HY-40E (or equivalent) single rank
  - Achieves smallest form factor with SODIMM
  - 1.8V SSTL_18 interface
- Support 128MB, 256MB and 512MB SODIMM
  - Non-registered interface
  - Included 256MB density in development kit
  - On die termination of memory interface
  - Dual rank NOT supported
  - FPGA speedgrade (-1) limits DDR2 performance, see V5-LXT datasheet
- Support 400 MT/s or 533 MT/s or 667 MT/s
  - CAS latency 3 (400)/ 4 (533)/ 5(667)
  - Use ICS clock synthesizer to generate clock frequencies
    - BIT file for DDR2 memory interface included on CDROM image
    - Latest Memory Applications Engineering design technique for Virtex-5

Ethernet Support

- Support hard and soft EMAC IP
- On board 125MHz EMAC reference clock
- Xilinx Generic Interface (XGI) BERG connector
  - Attach HW-AFX-BERG-EPHY
    - NOT included with ML555 PCI/PCI Express Development Kit
    - Dual Marvell Alaska 88E1111 PHY on daughter card
  - GMII, MII, SGMII and RGMII standards
- Two SFP interfaces for 1G/2G electrical/optical connectivity
  - 1000 BASE-X PCS/PMA mode
  - SFP modules NOT included with kit
  - Ethernet or Fibre Channel support (must be same standard)
- One port SMA connector to HW-AFX-SMA-SFP

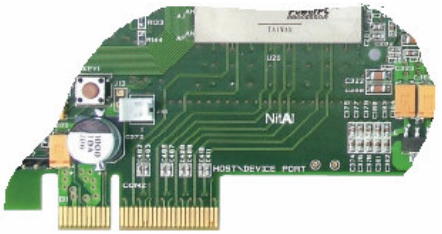
HW-AFX-BERG-EPHY

Support dual 10/100/1000 Ethernet interfaces
GMII, MII, SGMII and RGMII support
Plug-in to Xilinx Generic Interface (XGI) BERG connector on ML555
Xilinx product inventory **@$499.00** retail



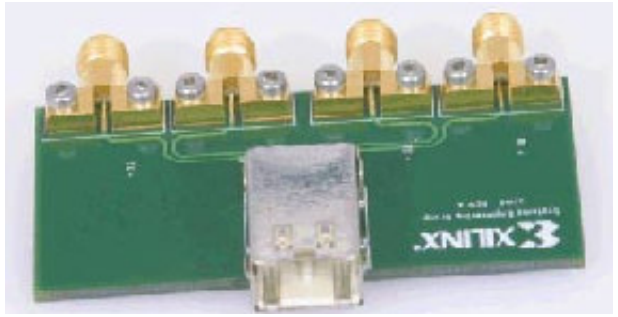
GTP Interfaces

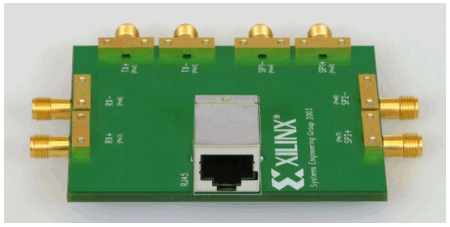
- Twelve GTP devices available on LX50
- Eight ports to PCI-e connector (Gen 1)
  - Support x1, x2, x4 or x8 endpoint designs
- One set of SMA connectors
  - Cable to external SMA to SATA/SFP/HSSDC2 boards
- Two ports for SFP module interface
- One port Serial ATA
  - ASIC World Services SATA IP core support



SMA Peripheral Support

- Cable ML555 SMA to external SMA adapter boards
- Doesn't burden ML555 kit with costs of interfaces
  - Customer orders exactly what they need for their design
- Products available through Xilinx on Board program:
  - **$149**: HW-AFX-SMA-SFP
  - **$199**: HW-AFX-SMA-SATA
  - **$279**: HW-AFX-SMA-RJ45
  - **$249**: HW-AFX-SMA-HSSDC2





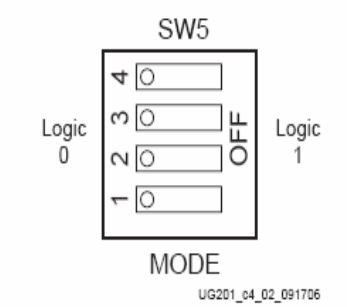
USB Interface

- Replace RS232 interface with USB 2.0
- Use Silicon Laboratories CP2102 device
  - Single chip USB to UART bridge
    - USB 2.0 compliant (12 Mbps)
    - External interface USB
    - FPGA interface RS232 (no level translators)
  - Royalty free distribution license: Virtual COM port driver
    - Install driver on system unit (not XLNX demo board)
- Works with existing COM port PC applications
  - Don't have to rewrite existing Xilinx demo/functional test code
  - Windows and Linux support available

Configuration

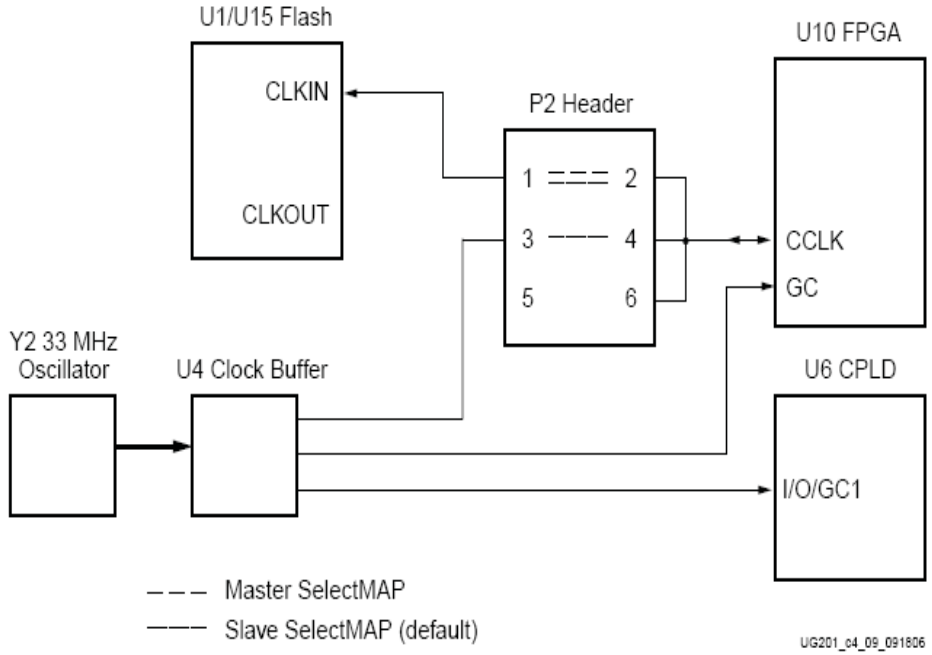
- JTAG Header
- Two Platform Flash devices XCF32P
  - Two LX50T images per device
  - CPLD controls image selection from header P3
- Master SelectMAP
  - Eight bit parallel or serial (PROMGEN option)
  - CCLK frequency selected as BITGEN option
- Slave SelectMAP
  - 33MHz onboard oscillator for CCLK

SelectMAP Mode SW5



Mode SW5 Position	Master SelectMAP	Slave SelectMAP
1 (M0)	ON	ON
2 (M1)	ON	OFF
3 (M2)	OFF	OFF
4 (HSWAPEN)	X	X

SelectMAP CCLK Source



Install shunts on P2-1 to P2-2 for Master SelectMAP
Install shunts on P2-1 to P2-2 AND P2-3 to P2-4 for Slave SelectMAP

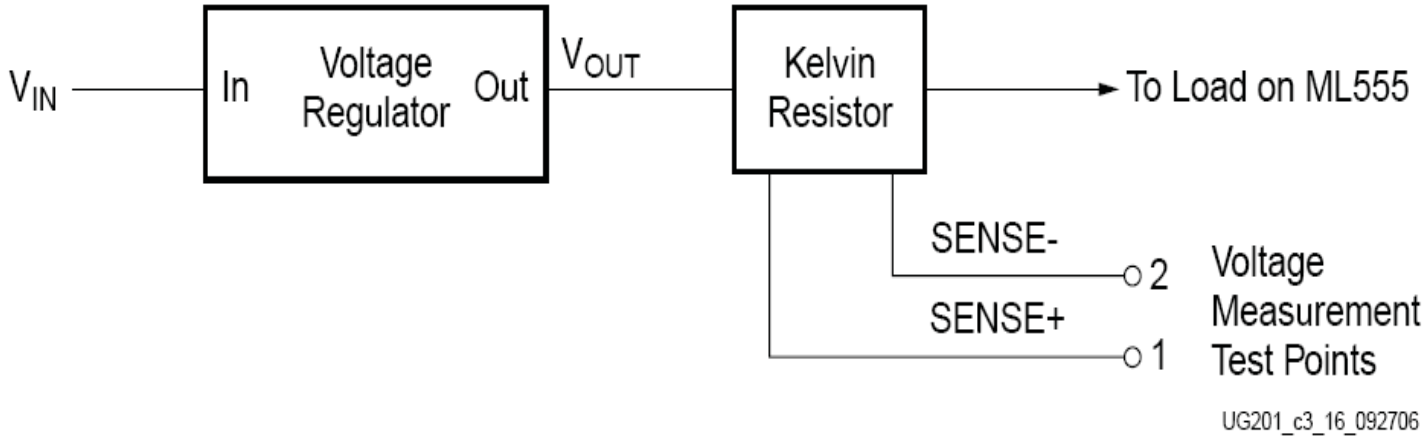
Image Selection Header P3

Platform Flash Image	P3-1 to P3-2 Shunt	P3-3 to P3-4 Shunt
U1 Image 0 PCIe 4 lane Endpoint Block	ON	ON
U1 Image 1 PCIe 8 lane Endpoint Block	OFF	ON
U15 Image 0 PCI 33MHz Memory BAR	ON	OFF
U15 Image 1 PCI-X 133MHz Memory BAR	OFF	OFF

Platform Flash devices are U1 and U15 (two LX50 images per device)
Always install shunt on header P3-5 to P3-6

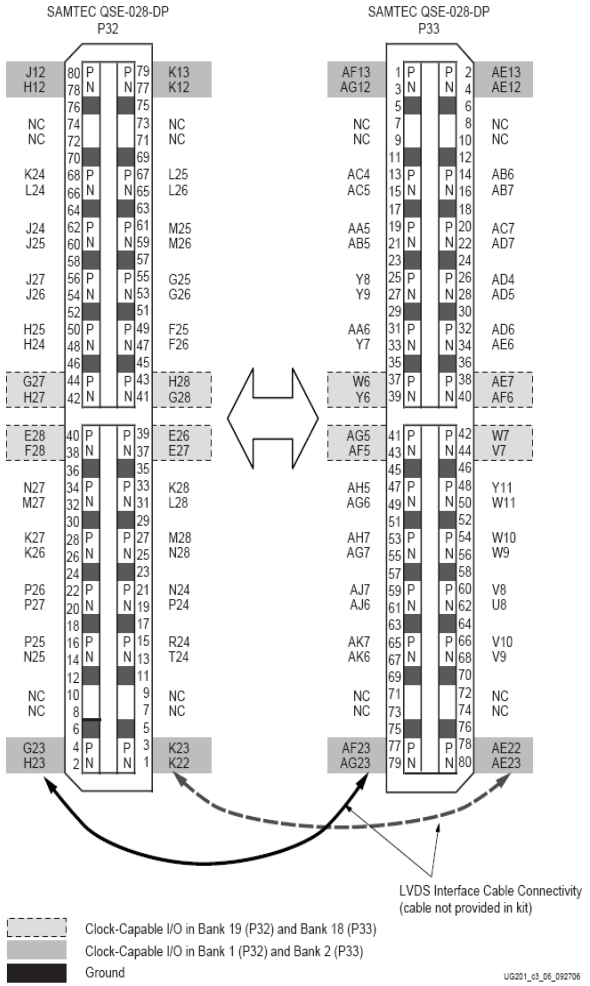
Power Measurements

- Measure power consumption for total 5V power (PCIe mode), FPGA Vccint, GTP analog supplies
- See UG201 for details and component measurement points



LVDS Interface

- 24 LVDS channels per connector
- Two connectors



Thank You