SPEF Format

So, this has been due for long time. May be because of tight tape out deadlines, this very important piece of Physical Design flow just got missed. And I am sure, like me, many might be curious to know what is the IEEE SPEF format, what does various attributes of SPEF file represent, etc...

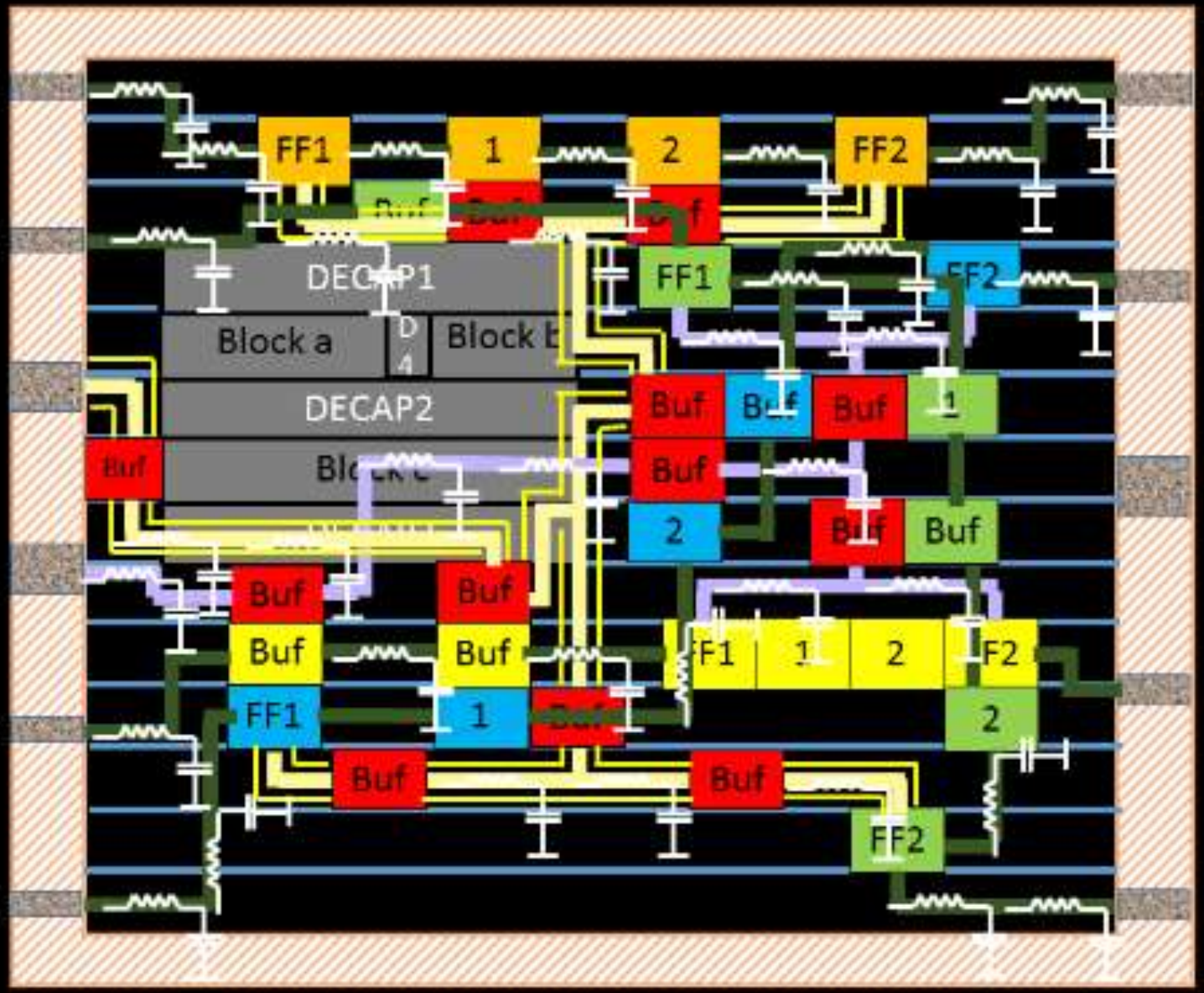
So, here you go. Finally got time to make video on IEEE SPEF format. Let's nail this down, with below example design, which I have been using on Udemy

7) Parasitics Extraction

Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999



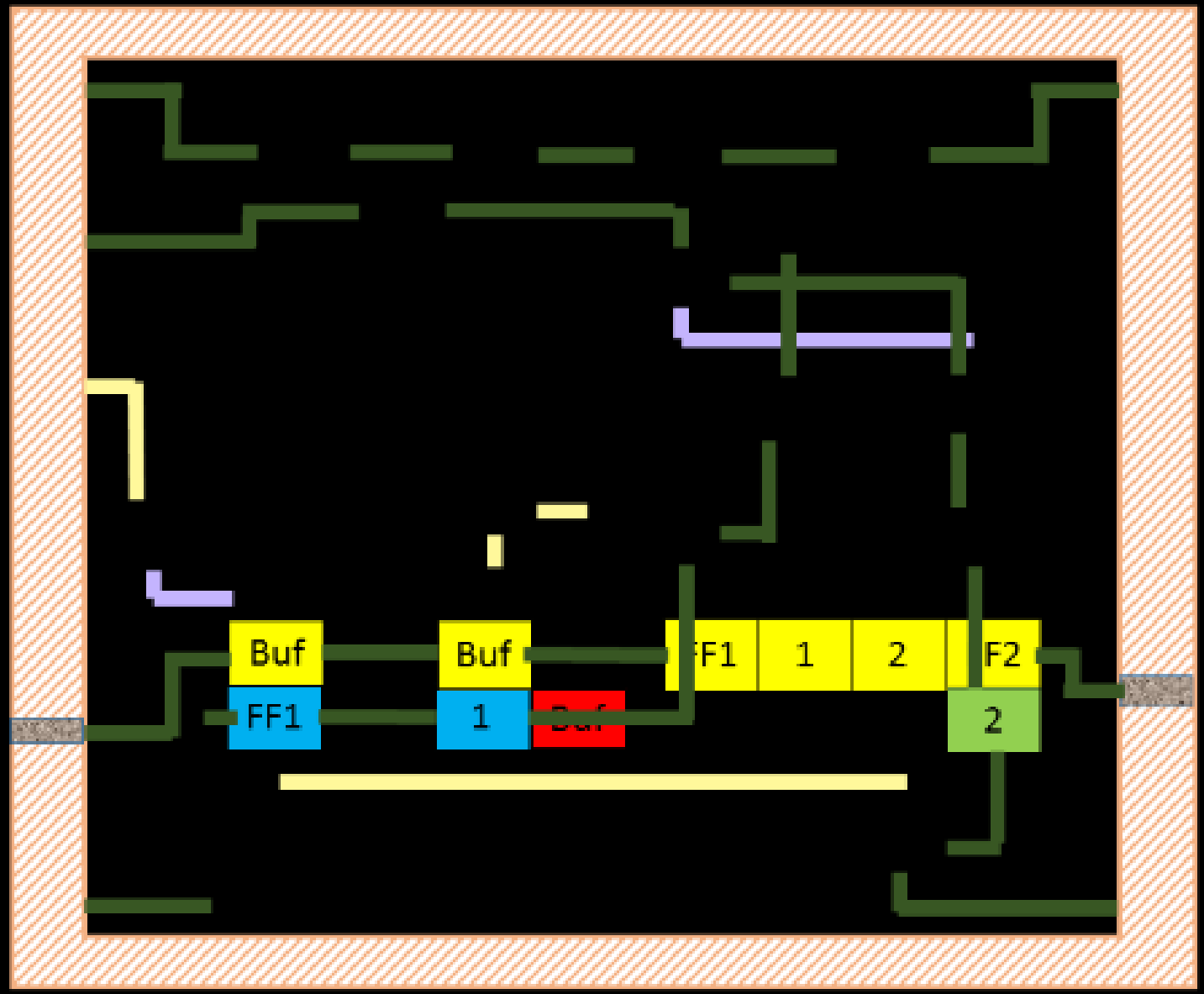
We will take a piece of the circuit and write the SPEF file for a piece of input port and net

7) Parasitics Extraction

Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999



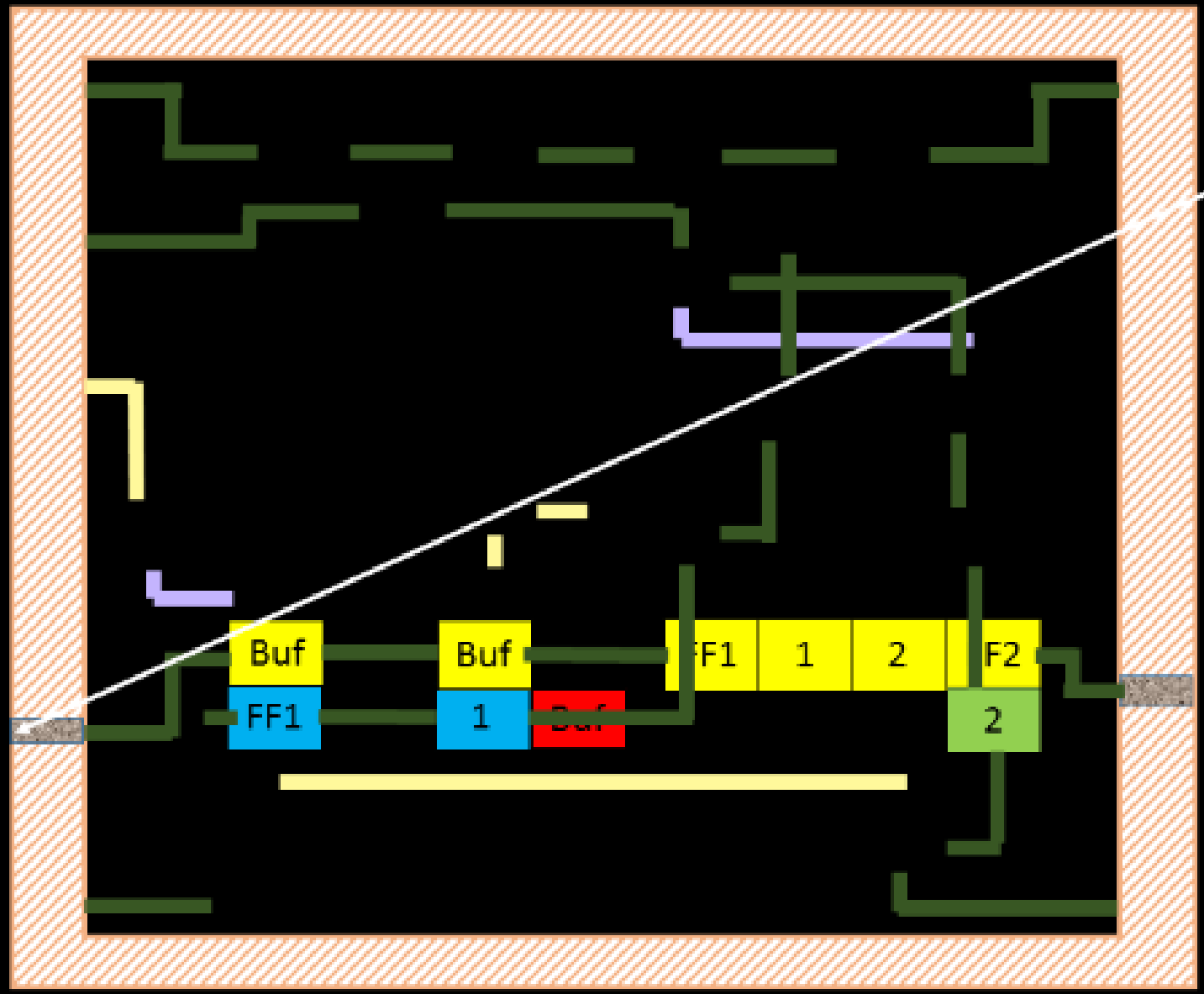
Let's write down the path components of Input port Din2 in SPEF format, which will also be a part of large SPEF file

7) Parasitics Extraction

Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999

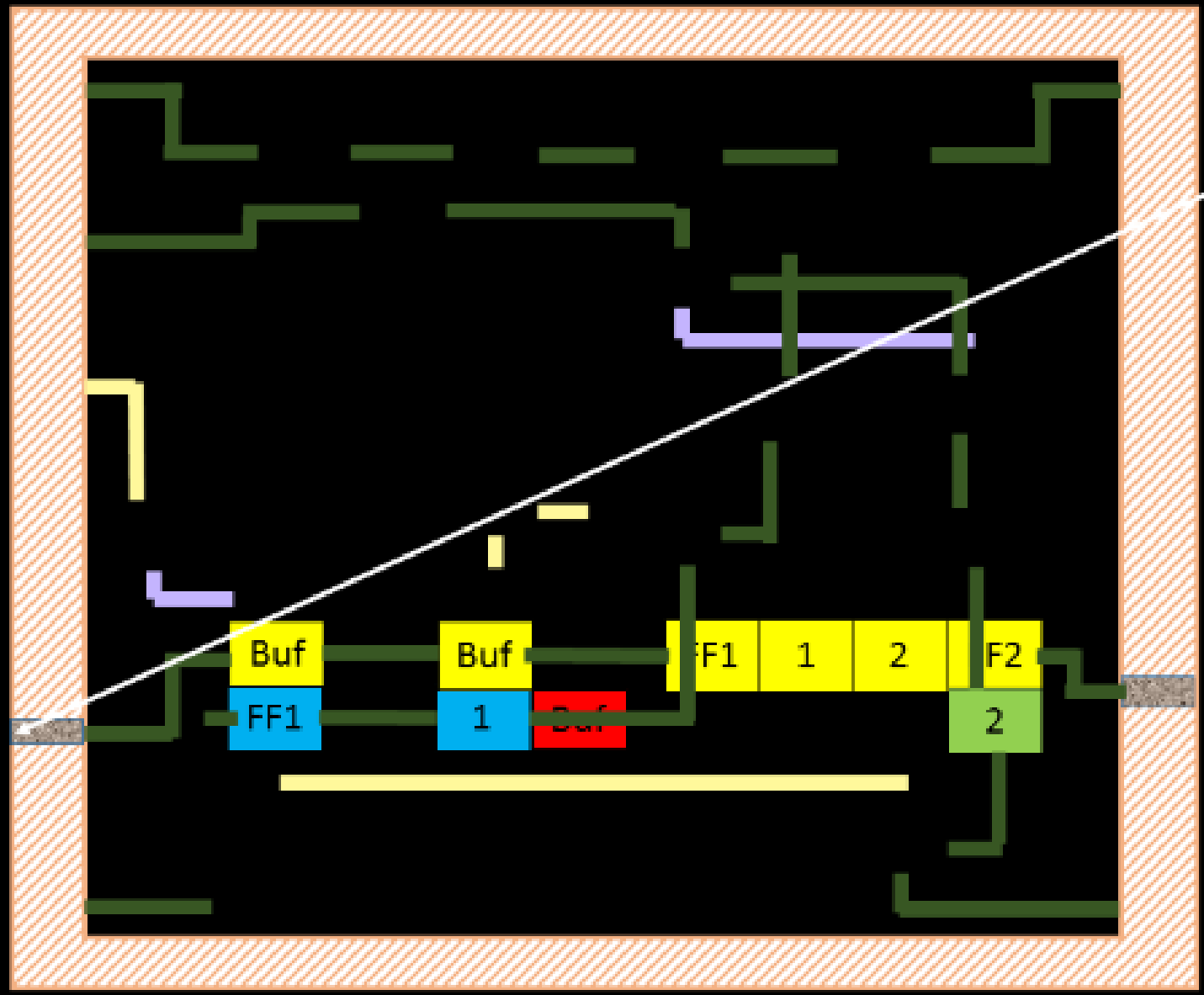


7) Parasitics Extraction

Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999

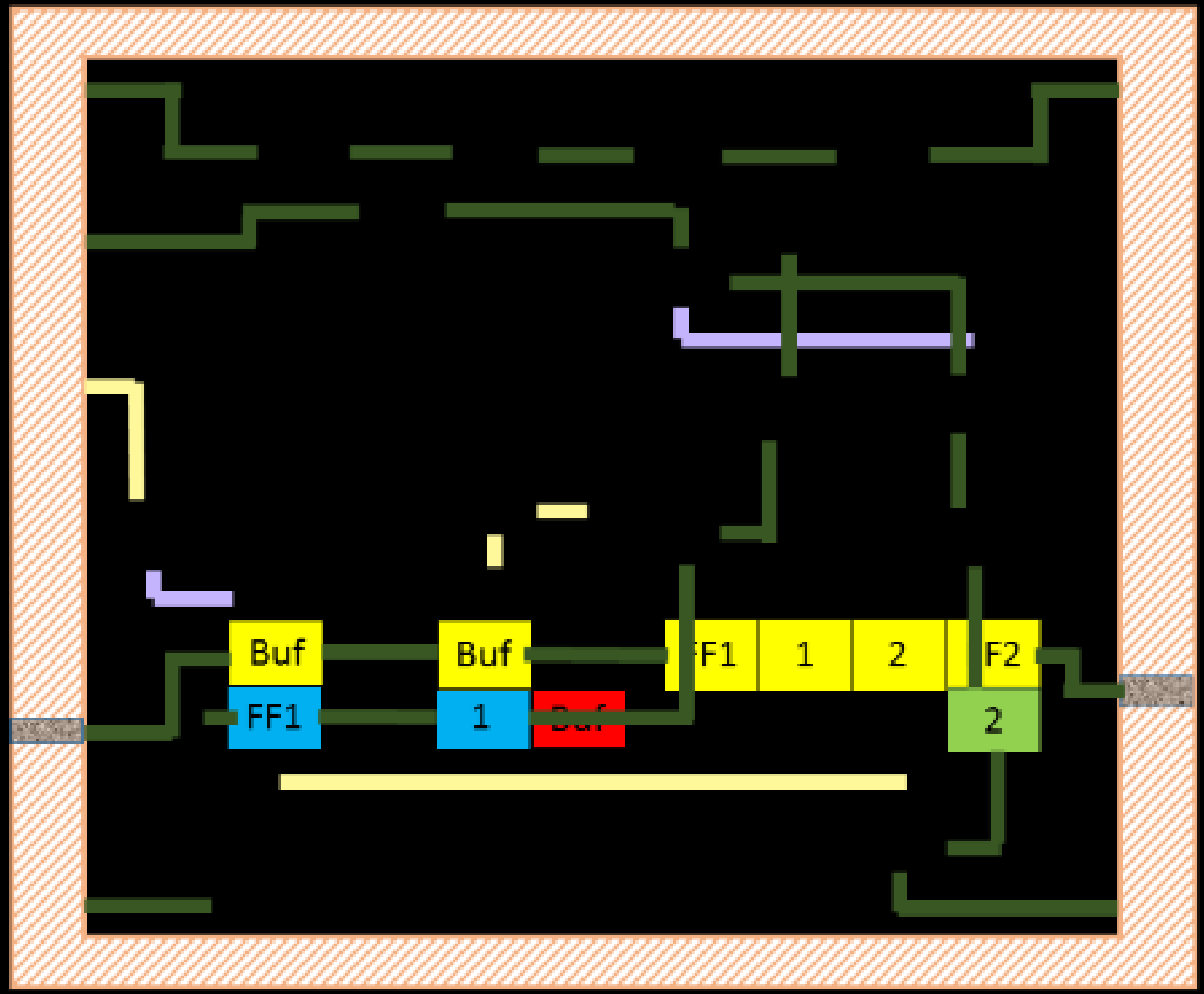


Path Components :

Din2 : Input Port

- Load (Capacitance, *SPEF : *L*)
- Co-ordinate (Location, *SPEF : *C*)
- Driver (*SPEF : *D*)
- Waveform Shape (rise/fall slew, *SPEF : *S*)

7) Parasitics Extraction



Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999

Path Components :

Din2 : Input Port

- Load (Capacitance, *SPEF : *L*)
- Co-ordinate (Location, *SPEF : *C*)
- Driver (*SPEF : *D*)
- Waveform Shape (rise/fall slew, *SPEF : *S*)

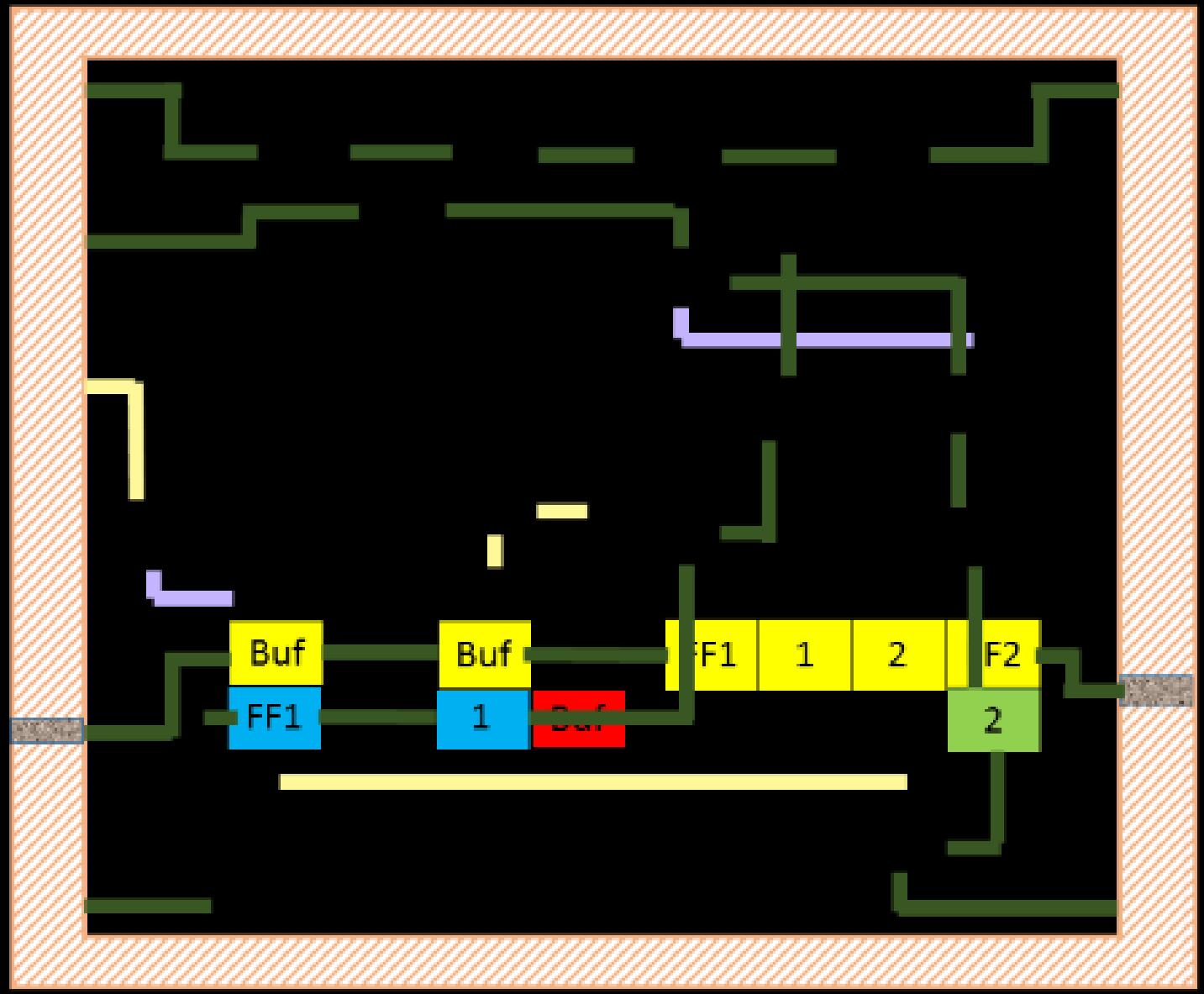
SPEF Equivalent

*PORTS

Din2 I *L 0.05 *S 100 100

In the above SPEF equivalent "I" represents input port
We can also map the Din2 port with a number, (say *1, as in below example), and use *1 as reference for Input Port Din2. So, wherever, we have *1 in SPEF file, it is nothing but Din2 port. This technique greatly reduces SPEF file size

7) Parasitics Extraction



Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999

Path Components :

Din2 : Input Port

- Load (Capacitance, *SPEF : *L*)
- Co-ordinate (Location, *SPEF : *C*)
- Driver (*SPEF : *D*)
- Waveform Shape (rise/fall slew, *SPEF : *S*)

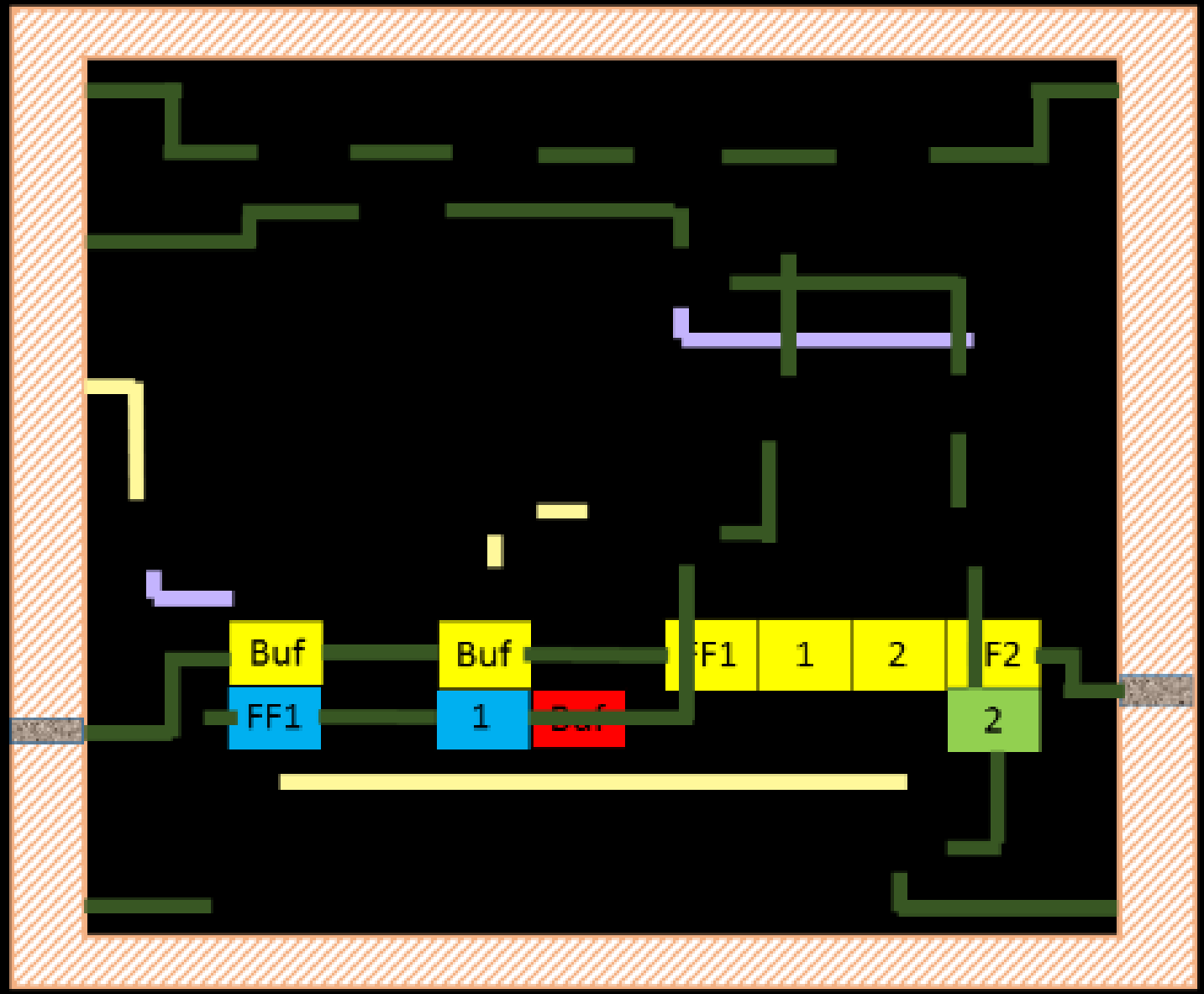
SPEF Equivalent

```
*PORTS
Din2 I *L 0.05 *S 100 100
```

OR

```
*NAME_MAP
*1 Din2
```

7) Parasitics Extraction



Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999

Path Components :

Din2 : Input Port

- Load (Capacitance, *SPEF : *L*)
- Co-ordinate (Location, *SPEF : *C*)
- Driver (*SPEF : *D*)
- Waveform Shape (rise/fall slew, *SPEF : *S*)

SPEF Equivalent

```
*PORTS
Din2 I *L 0.05 *S 100 100
```

OR

```
*NAME_MAP
*1 Din2

*PORTS
*1 I *L 0.05 *S 100 100
```

This becomes one part of the SPEF file

7) Parasitics Extraction

```
*NAME_MAP
*1 Din2

*PORTS
*1 I *L 0.05 *S 100 100
```

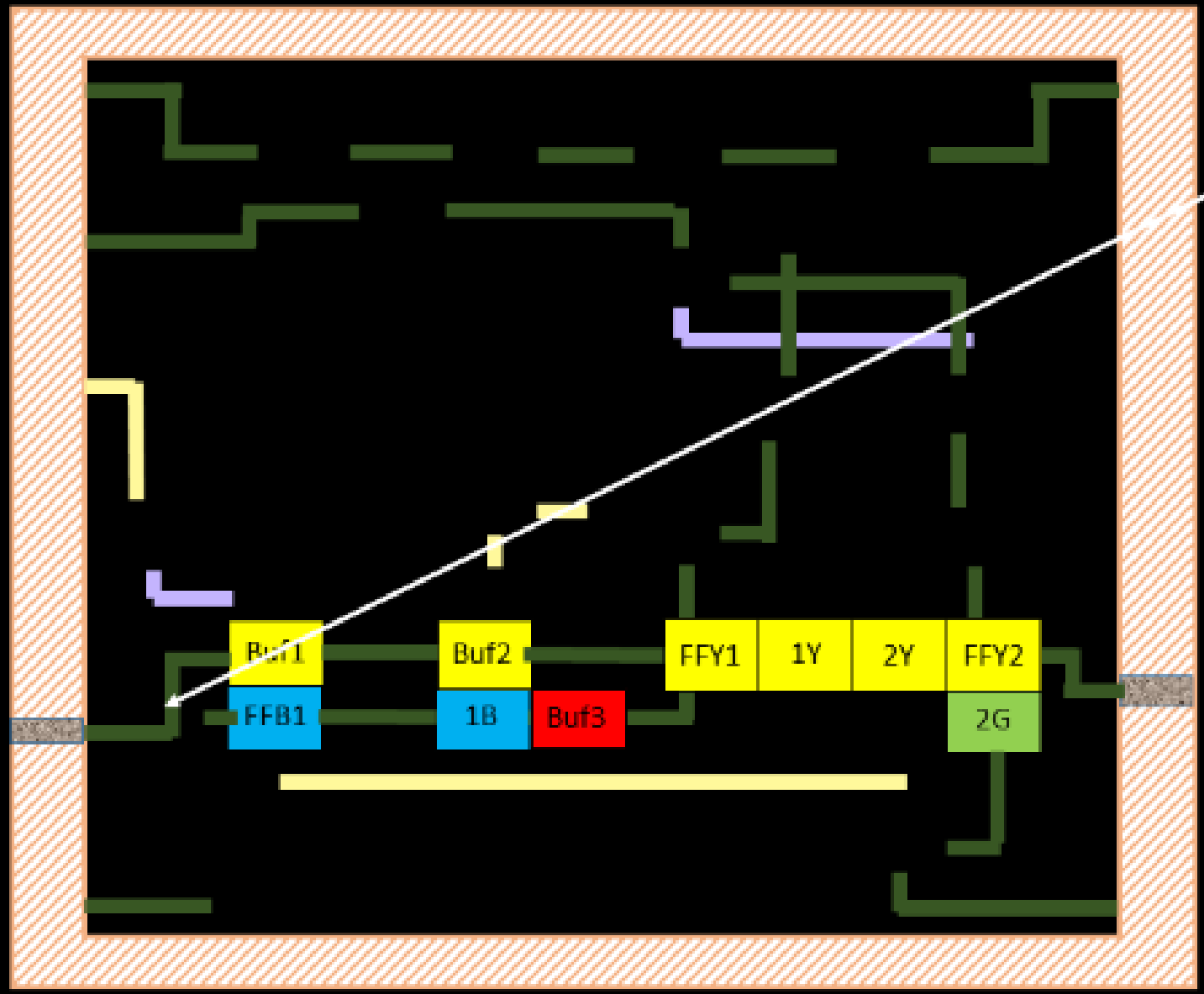
Further, we will extract the net connected to Din2 (shown below) and write a SPEF format of the same

7) Parasitics Extraction

Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999



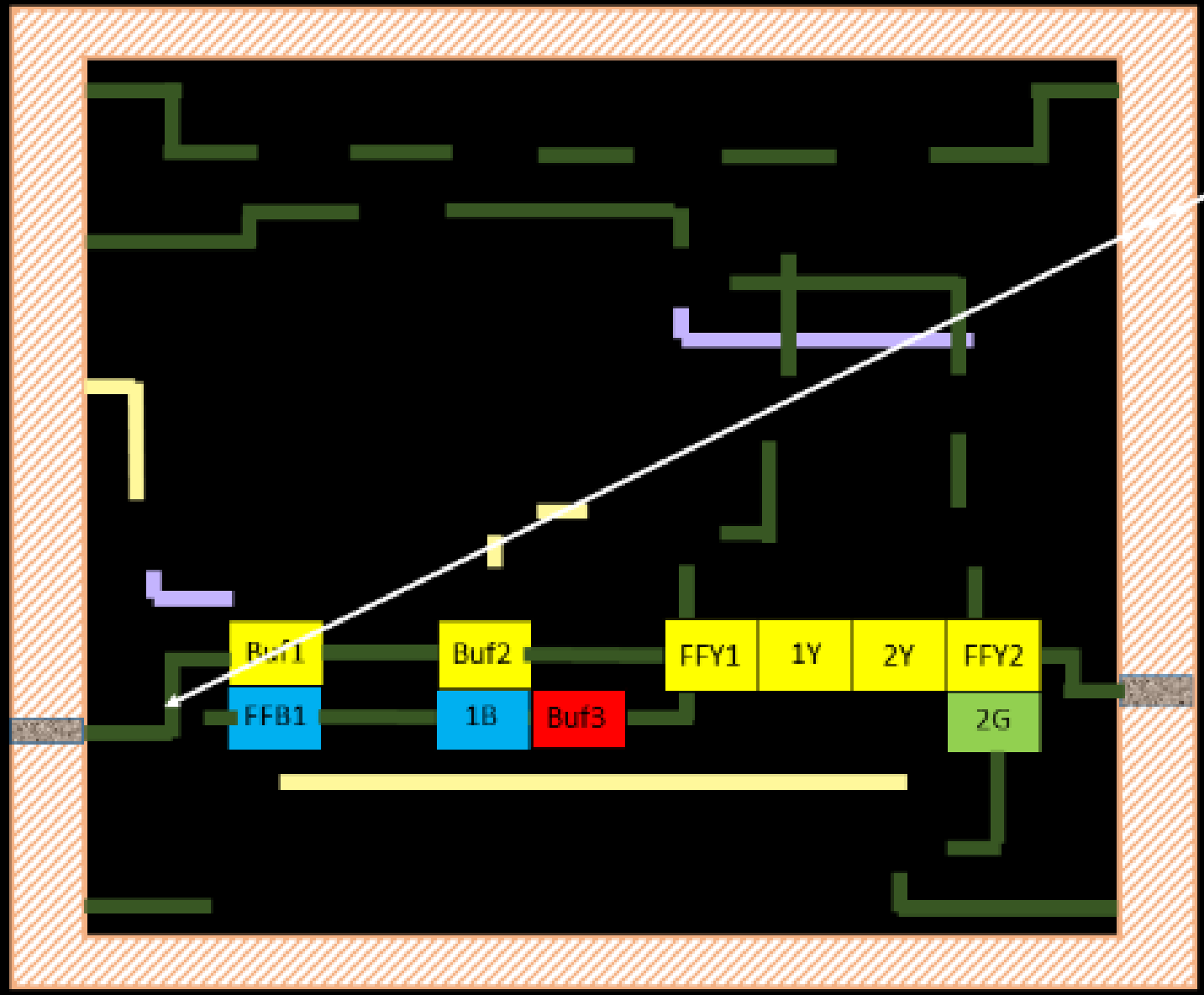
Let's move on with identifying the path components of net connected to Din2 port shown below

7) Parasitics Extraction

Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999



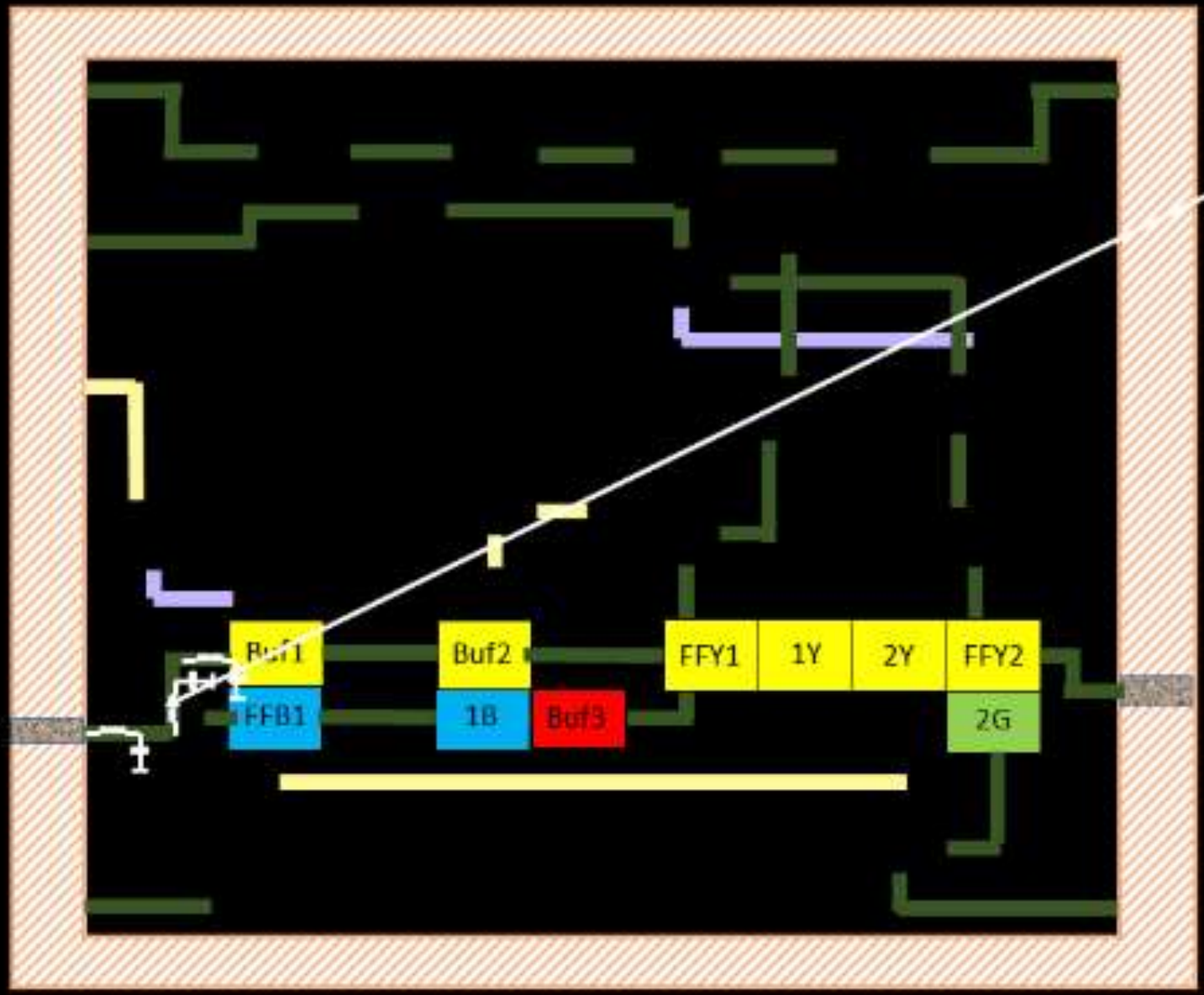
Path Components :

Din2_net : Wire/Net (*SPEF : *D_NET*)

- Driver : Port "Din2" (*SPEF : *P*)
- Driver Type : Not Specified (*SPEF : *D*)
- Receiver : Internal Pin "Buf1/a" (*SPEF : *I*)

For now, let's have a distributed RC network representation of the net (shown below). We do have another way of representing RC network in reduced format. I will come back to that in a moment

7) Parasitics Extraction



Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999

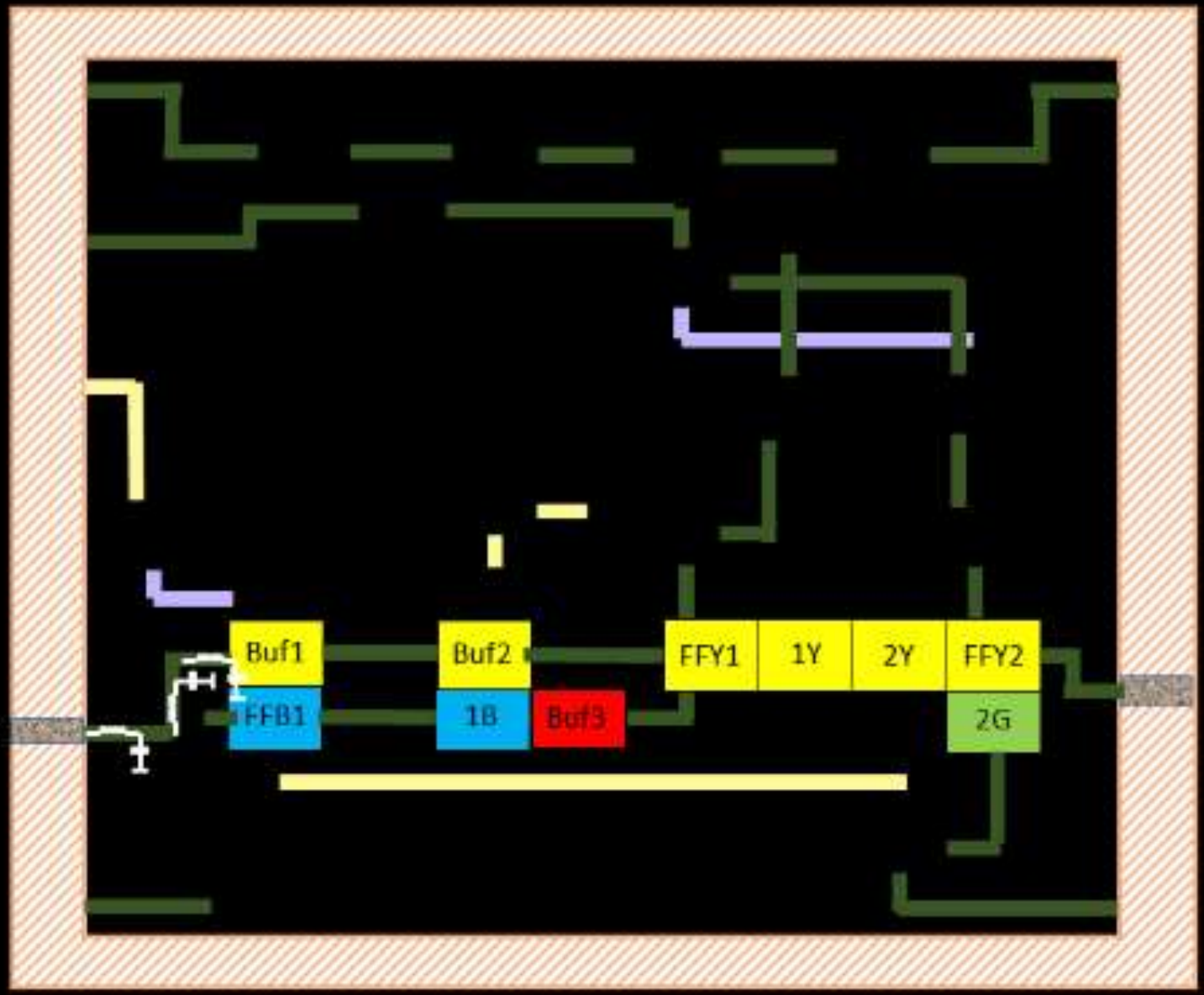
Path Components :

Din2_net : Wire/Net (*SPEF : *D_NET*)

- Driver : Port "Din2" (*SPEF : *P*)
- Driver Type : Not Specified (*SPEF : *D*)
- Receiver : Internal Pin "Buf1/a" (*SPEF : *I*)
- Lumped Capacitance
- 3 Distributed Resistance (*SPEF : *RES*)
- 3 Distributed Capacitance (*SPEF : *CAP*)

Now that we know the components of Din2_net, lets write down the SPEF equivalent of this net. Firstly, we will map the name "Din2_net" as "*2" and use "*2" hence forth, to refer to Din2_net.

7) Parasitics Extraction



Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999

Path Components :

Din2_net : Wire/Net (*SPEF : *D_NET*)

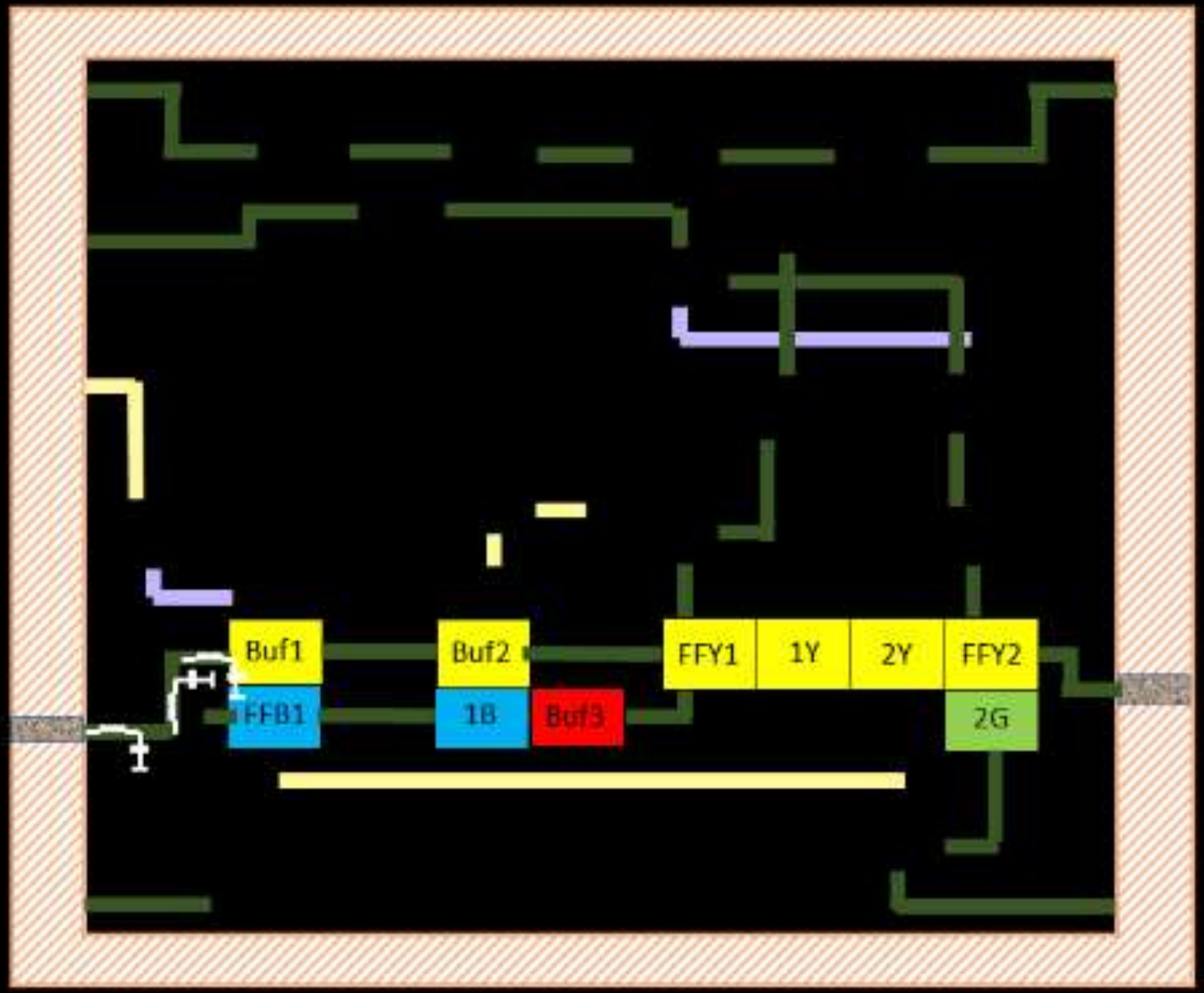
- Driver : Port "Din2" (*SPEF : *P*)
- Driver Type : Not Specified (*SPEF : *D*)
- Receiver : Internal Pin "Buf1/a" (*SPEF : *I*)
- Lumped Capacitance
- 3 Distributed Resistance (*SPEF : *RES*)
- 3 Distributed Capacitance (*SPEF : *CAP*)

SPEF Equivalent

```
*NAME_MAP
*1 Din2
*2 Din2_net

*D_NET *2 0.15
```

We will come back to how do we calculate the load value of "0.15". *D_NET denotes "distributed net". If we had used a reduced format of the nets, with only single value of resistance and capacitance, it would had been called as "*R_NET". Now lets write down the connectivity information of "Din2_net" or "*2". *CONN section defines connectivity of *2

7) Parasitics Extraction



Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999

Path Components :

Din2_net : Wire/Net (*SPEF : *D_NET*)

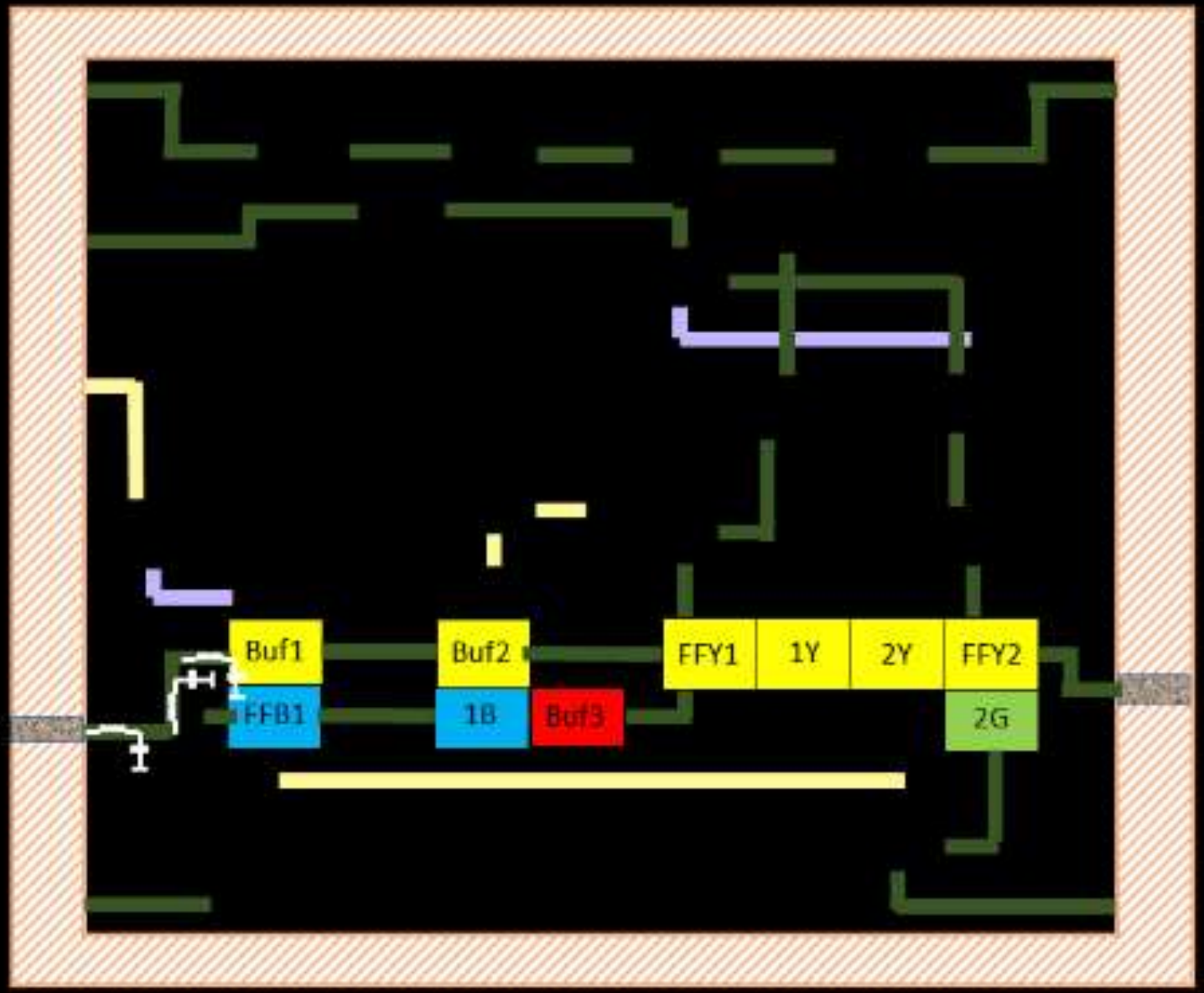
- Driver : Port "Din2" (*SPEF : *P*)
- Driver Type : Not Specified (*SPEF : *D*)
- Receiver : Internal Pin "Buf1/a" (*SPEF : *I*)
- Lumped Capacitance
- 3 Distributed Resistance (*SPEF : *RES*)
- 3 Distributed Capacitance (*SPEF : *CAP*)

SPEF Equivalent

```
*NAME_MAP
*1 Din2
*2 Din2_net

*D_NET *2 0.15

*CONN
```

The below says. ***2*** (Din2_net) is connected to external port (***P***), named ***1*** (port Din2), which has direction "input" (**I**)

7) Parasitics Extraction



Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999

Path Components :

Din2_net : Wire/Net (*SPEF : *D_NET*)

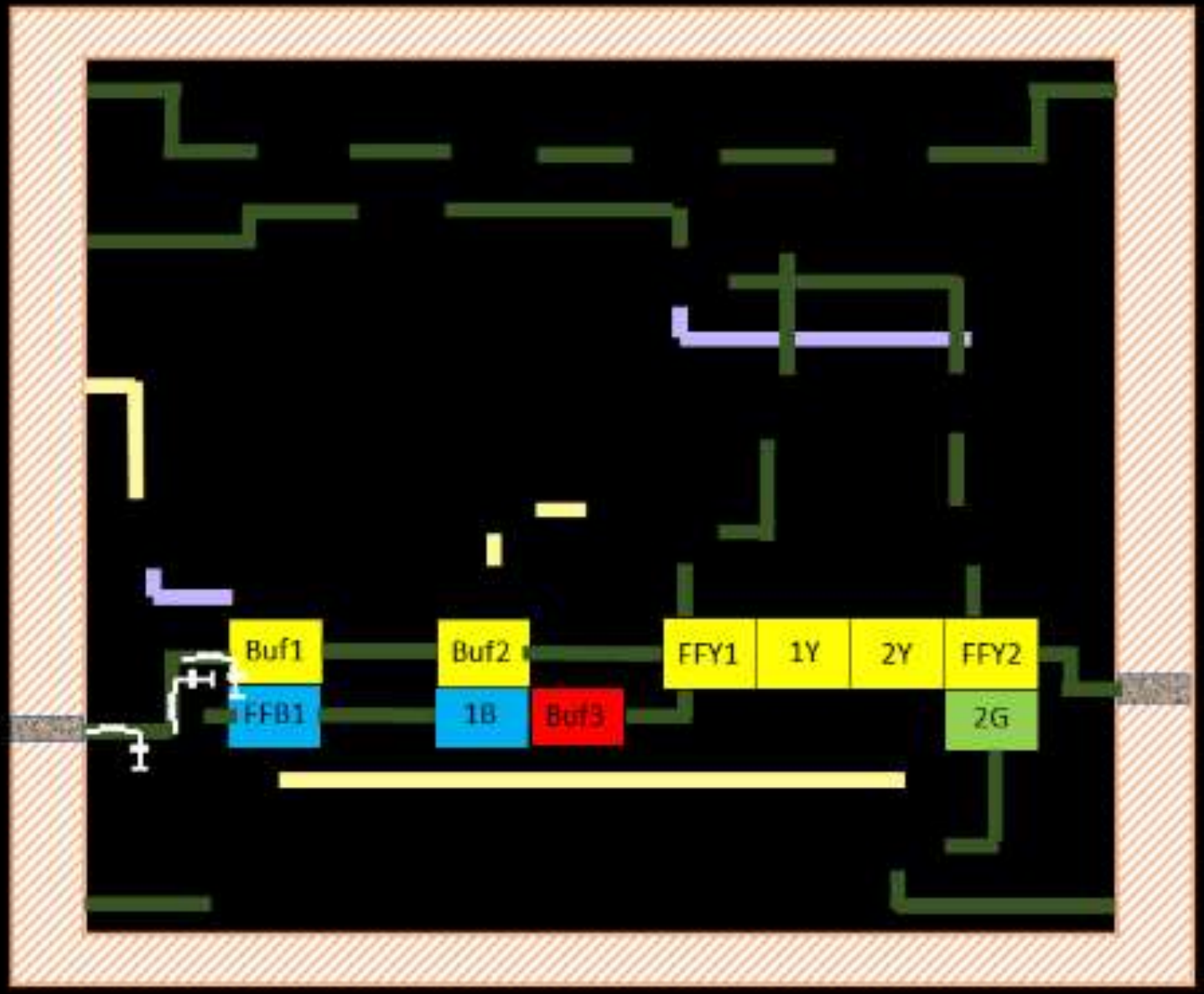
- Driver : Port "Din2" (*SPEF : *P*)
- Driver Type : Not Specified (*SPEF : *D*)
- Receiver : Internal Pin "Buf1/a" (*SPEF : *I*)
- Lumped Capacitance
- 3 Distributed Resistance (*SPEF : *RES*)
- 3 Distributed Capacitance (*SPEF : *CAP*)

SPEF Equivalent

```
*NAME_MAP
*1 Din2
*2 Din2_net

*D_NET *2 0.15

*CONN
*P *11
```

The other end of net "***2**" is connected to internal pin "**Buf1:a**" and having a load (***L**) of 0.15 units. I will come back later on the "units" section, in my following post

7) Parasitics Extraction



Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999

Path Components :

Din2_net : Wire/Net (*SPEF : *D_NET*)

- Driver : Port "Din2" (*SPEF : *P*)
- Driver Type : Not Specified (*SPEF : *D*)
- Receiver : Internal Pin "Buf1/a" (*SPEF : *I*)
- Lumped Capacitance
- 3 Distributed Resistance (*SPEF : *RES*)
- 3 Distributed Capacitance (*SPEF : *CAP*)

SPEF Equivalent

```
*NAME_MAP
*1 Din2
*2 Din2_net

*D_NET *2 0.15

*CONN
*P *1 I
*I Buf1:a *L 0.15
```

This becomes a part of the SPEF file, so lets put it in a file, that we were maintaining from last post

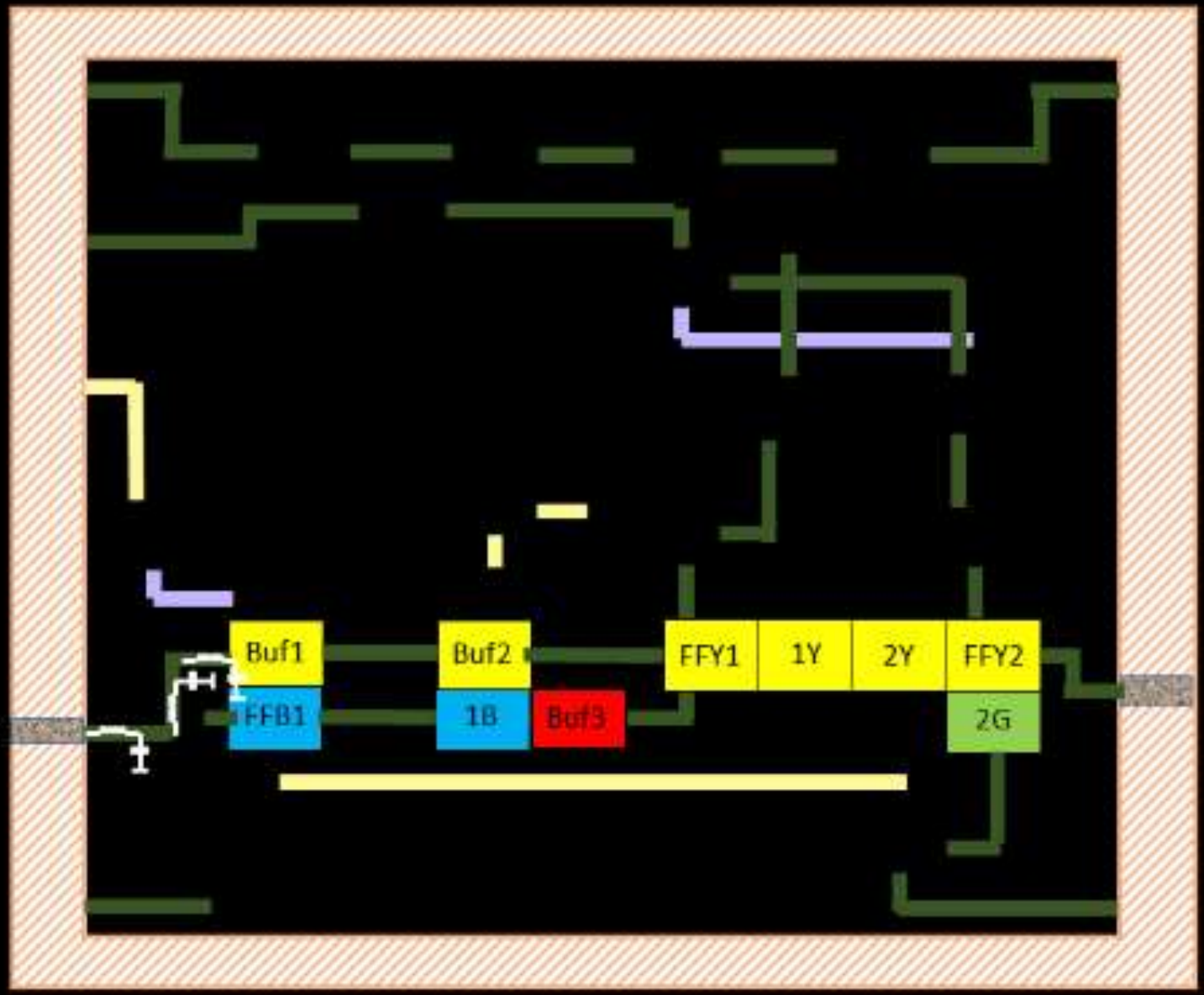
7) Parasitics Extraction

```
*NAME_MAP
*1 Din2
*2 Din2_net

*PORTS
*1 I *L 0.05 *S 100 100

*D_NET *2 0.15

*CONN
*P *1 I
*I Buf1:a *L 0.15
```


```
*NAME_MAP
*1 Din2
*2 Din2_net

*D_NET *2 0.15

*CONN
*P *1 I
*I Buf1:a *L 0.15
```

Notice, we have 3 capacitances and 3 resistances on the net. So the way to represent them is in below image. The numbers "121", "122", etc. are the line numbers, *2:1, *2:2.... are the respective capacitances. I will get back on *2 and *1 and the beginning and end of the cap section. Broadly, this is to denote the start and end section of *CAP

7) Parasitics Extraction



Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999

Path Components :

Din2_net : Wire/Net (*SPEF : *D_NET*)

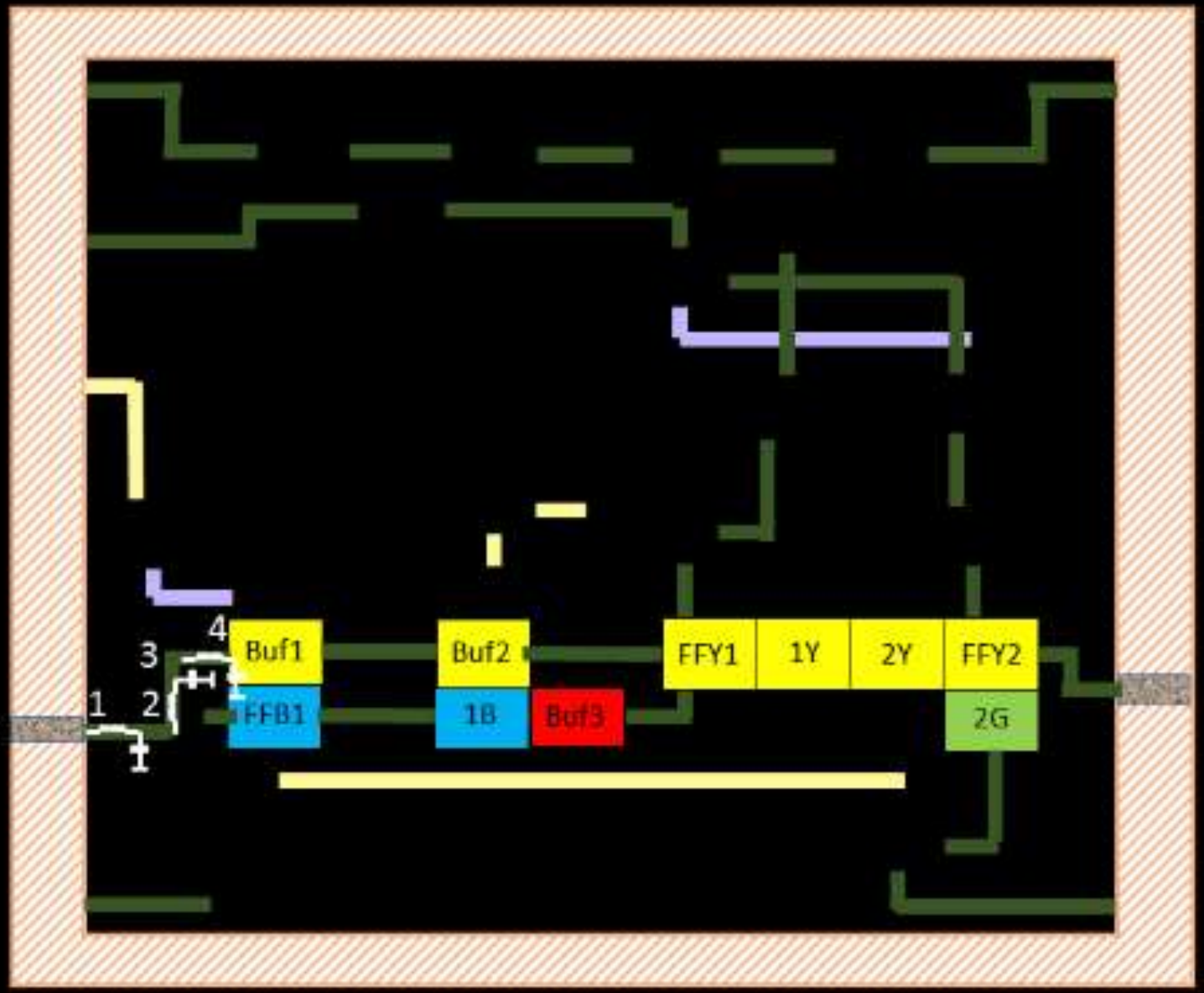
- Driver : Port "Din2" (*SPEF : *P*)
- Driver Type : Not Specified (*SPEF : *D*)
- Receiver : Internal Pin "Buf1/a" (*SPEF : *I*)
- Lumped Capacitance
- 3 Distributed Resistance (*SPEF : *RES*)
- 3 Distributed Capacitance (*SPEF : *CAP*)

SPEF Equivalent

```
*CONN
*P *1 I
*I Buf1:a *L 0.15

*CAP
121 *2 0
122 *2:1 0.05
123 *2:2 0.05
124 *2:3 0.05
125 *1 0
```

Now, we have 4 nodes, and within a pair of node, we have a resistance, like below

7) Parasitics Extraction



Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999

Path Components :

Din2_net : Wire/Net (*SPEF : *D_NET*)

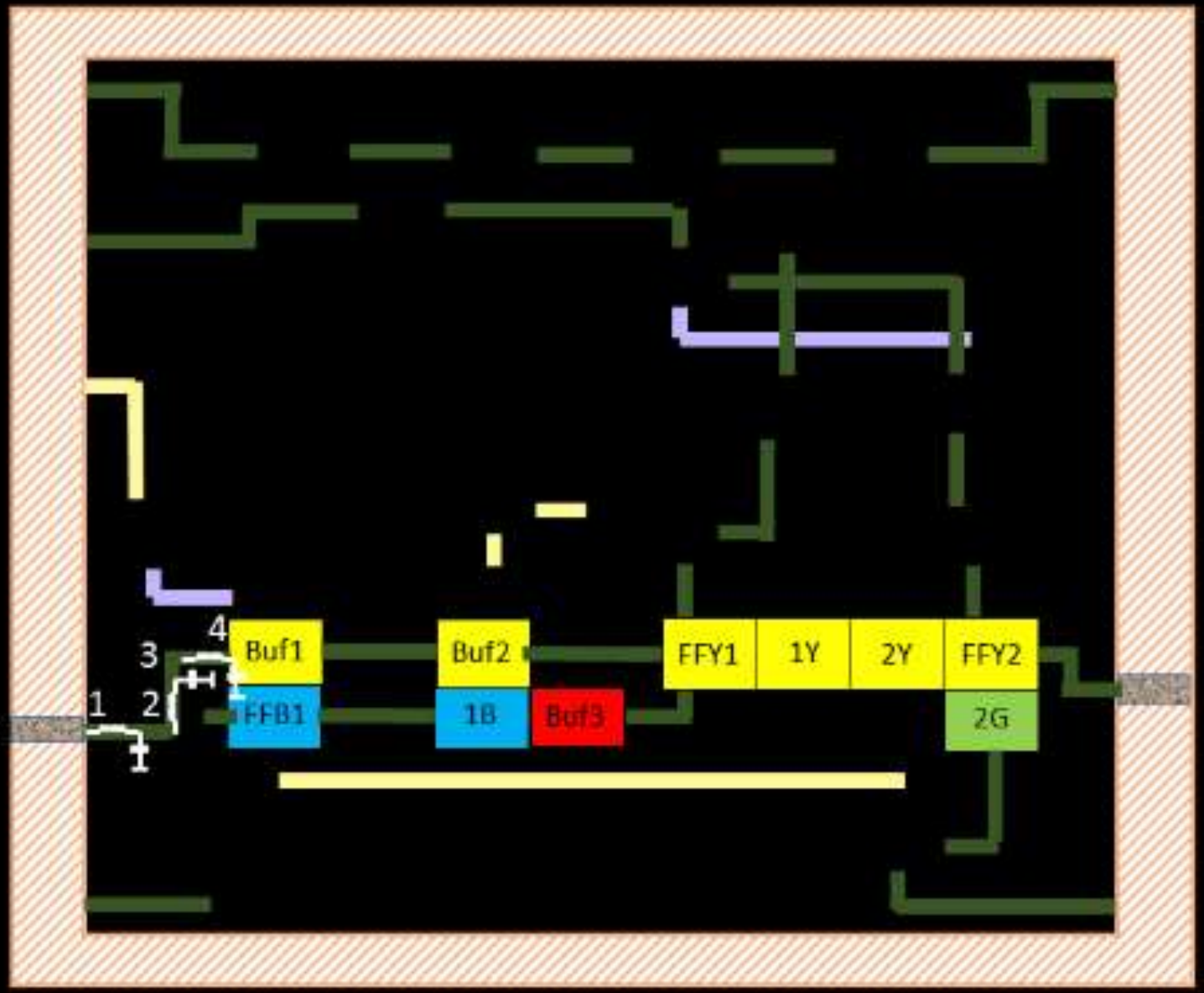
- Driver : Port "Din2" (*SPEF : *P*)
- Driver Type : Not Specified (*SPEF : *D*)
- Receiver : Internal Pin "Buf1/a" (*SPEF : *I*)
- Lumped Capacitance
- 3 Distributed Resistance (*SPEF : *RES*)
- 3 Distributed Capacitance (*SPEF : *CAP*)

SPEF Equivalent

*CONN
*P *1 I
*I Buf1:a *L 0.15

With the introduction of nodes, the representation of resistance has now become fairly simple, like below

7) Parasitics Extraction



Representation Format

SPEF : Standard Parasitics Exchange Format

IEEE 1481-1999

Path Components :

Din2_net : Wire/Net (*SPEF : *D_NET*)

- Driver : Port "Din2" (*SPEF : *P*)
- Driver Type : Not Specified (*SPEF : *D*)
- Receiver : Internal Pin "Buf1/a" (*SPEF : *I*)
- Lumped Capacitance
- 3 Distributed Resistance (*SPEF : *RES*)
- 3 Distributed Capacitance (*SPEF : *CAP*)

SPEF Equivalent

```
*CONN
*P *1 I
*I Buf1:a *L 0.15

*RES
323 *2:1 *2:2 65
324 *2:2 *2:3 76
325 *2:3 *2:4 55

*END
```

These set of lines for distributed resistance and capacitance, will become a part of the SPEF file, we were maintaining. So let;s add it there

7) Parasitics Extraction

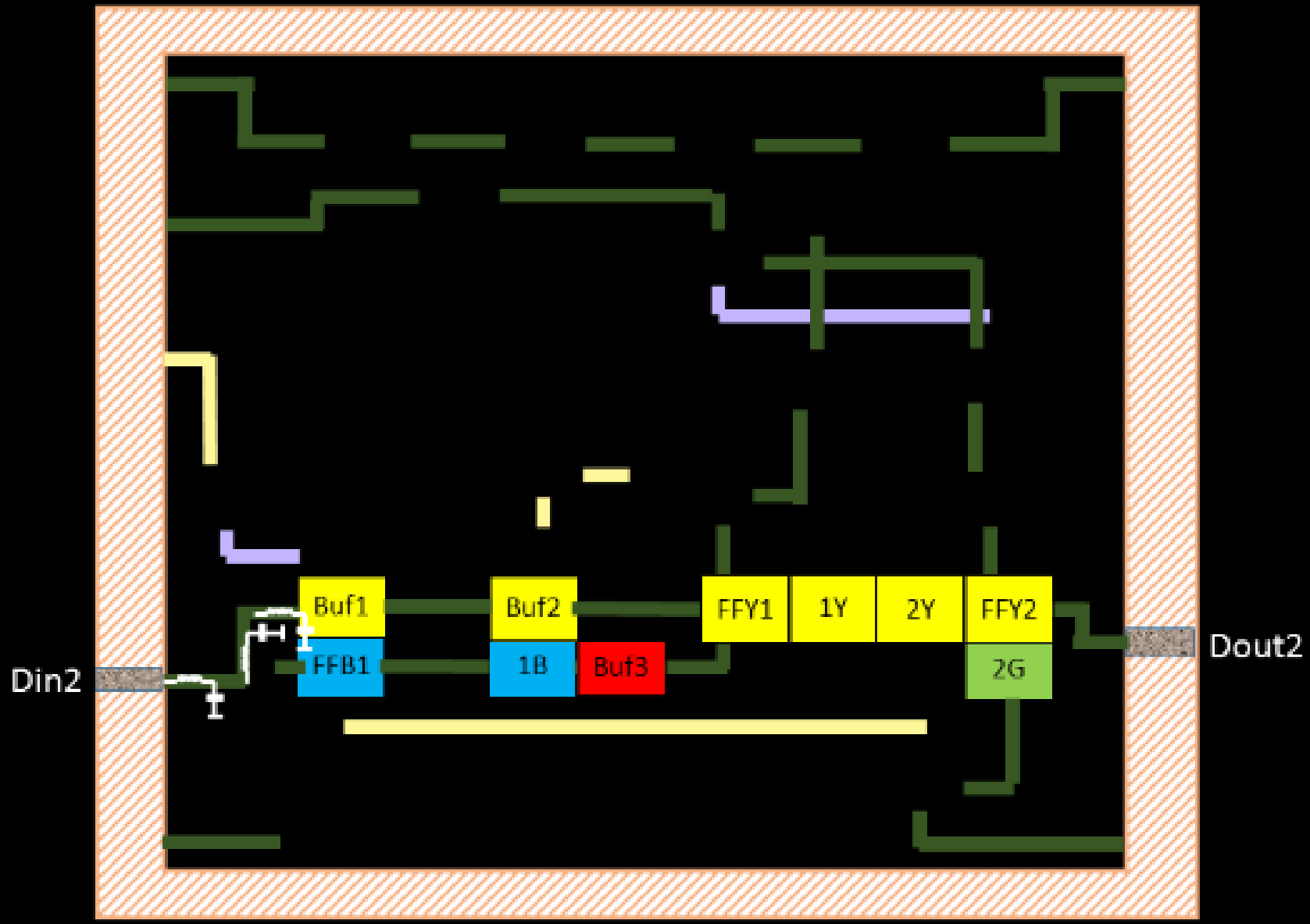
```
*NAME_MAP
*1 Din2
*2 Din2_net

*PORTS
*1 I *L 0.05 *S 100 100

*D_NET *2 0.15

*CONN
*P *1 I
*I Buf1:a *L 0.15

*CAP
121 *2 0
122 *2:1 0.05
123 *2:2 0.05
124 *2:3 0.05
125 *1 0

*RES
323 *2:1 *2:2 65
324 *2:2 *2:3 76
325 *2:3 *2:4 55

*END
```

```
*CONN
*P *1 I
*I Buf1:a *L 0.15

*RES
323 *2:1 *2:2 65
324 *2:2 *2:3 76
325 *2:3 *2:4 55

*END
```

These couple of lines (about 20), now represents a small net and a port. Just imagine, how many lines it will be to extract parasitics for the complete circuit, below. Its HUGE. I think, now we nail the reason for having *NAME_MAP. The SPEF file size greatly reduces, by name mapping. A 10 character net or port name can be reduced to a 2~3 character net name and can be referred and reused in the whole SPEF file. These people are really Smart :)

7) Parasitics Extraction

```
*NAME_MAP
*1 Din2
*2 Din2_net

*PORTS
*1 I *L 0.05 *S 100 100

*D_NET *2 0.15

*CONN
*P *1 I
*I Buf1:a *L 0.15

*CAP
121 *2 0
122 *2:1 0.05
123 *2:2 0.05
124 *2:3 0.05
125 *1 0

*RES
323 *2:1 *2:2 65
324 *2:2 *2:3 76
325 *2:3 *2:4 55

*END
```



Remember, I had mentioned, I will get back on units. So here we go. We have a header file that defines all of the them. Firstly, the design name, vendor name, version, etc.

7) Parasitics Extraction

```
*NAME_MAP
*1 Din2
*2 Din2_net

*PORTS
*1 I *L 0.05 *S 100 100

*D_NET *2 0.15

*CONN
*P *1 I
*I Buf1:a *L 0.15

*CAP
121 *2 0
122 *2:1 0.05
123 *2:2 0.05
124 *2:3 0.05
125 *1 0

*RES
323 *2:1 *2:2 65
324 *2:2 *2:3 76
325 *2:3 *2:4 55

*END
```

SPEF Header

```
*SPEF "IEEE 1481-1999"
*DATE "09:04:44  Thursday March 08, 2015"
*DESIGN "vending_machine"
*VENDOR "vendor XXX"
*PROGRAM "RC gen"
*VERSION "3.4.5"
```

Then, the delimiter. Usually, in any report, we see, it as "/". In SPEF you can have your own delimiter, by defining something like below

7) Parasitics Extraction

```
*NAME_MAP
*1 Din2
*2 Din2_net

*PORTS
*1 I *L 0.05 *S 100 100

*D_NET *2 0.15

*CONN
*P *1 I
*I Buf1:a *L 0.15

*CAP
121 *2 0
122 *2:1 0.05
123 *2:2 0.05
124 *2:3 0.05
125 *1 0

*RES
323 *2:1 *2:2 65
324 *2:2 *2:3 76
325 *2:3 *2:4 55

*END
```

SPEF Header

```
*SPEF "IEEE 1481-1999"
*DATE "09:04:44  Thursday March 08, 2015"
*DESIGN "vending_machine"
*VENDOR "vendor XXX"
*PROGRAM "RC gen"
*VERSION "3.4.5"
*DELIMITER :
```

And the units, and power nets

7) Parasitics Extraction

```
*NAME_MAP
*1 Din2
*2 Din2_net

*PORTS
*1 I *L 0.05 *S 100 100

*D_NET *2 0.15

*CONN
*P *1 I
*I Buf1:a *L 0.15

*CAP
121 *2 0
122 *2:1 0.05
123 *2:2 0.05
124 *2:3 0.05
125 *1 0

*RES
323 *2:1 *2:2 65
324 *2:2 *2:3 76
325 *2:3 *2:4 55

*END
```

SPEF Header

```
*SPEF "IEEE 1481-1999"
*DATE "09:04:44  Thursday March 08, 2015"
*DESIGN "vending_machine"
*VENDOR "vendor XXX"
*PROGRAM "RC gen"
*VERSION "3.4.5"
*DELIMITER :
*T_UNIT 1 PS
*C_UNIT 1 PF
*R_UNIT 1 OHM
*L_UNIT 1 HENRY
```

7) Parasitics Extraction

```
*NAME_MAP
*1 Din2
*2 Din2_net

*PORTS
*1 I *L 0.05 *S 100 100

*D_NET *2 0.15

*CONN
*P *1 I
*I Buf1:a *L 0.15

*CAP
121 *2 0
122 *2:1 0.05
123 *2:2 0.05
124 *2:3 0.05
125 *1 0

*RES
323 *2:1 *2:2 65
324 *2:2 *2:3 76
325 *2:3 *2:4 55

*END
```

SPEF Header

```
*SPEF "IEEE 1481-1999"
*DATE "09:04:44  Thursday March 08, 2015"
*DESIGN "vending_machine"
*VENDOR "vendor XXX"
*PROGRAM "RC gen"
*VERSION "3.4.5"
*DELIMITER :
*T_UNIT 1 PS
*C_UNIT 1 PF
*R_UNIT 1 OHM
*L_UNIT 1 HENRY

*POWER_NETS VDD
*GND_NETS VSS
```

Below is the SPEF file, for one net and one port

7) Parasitics Extraction

SPEF File

```
*SPEF "IEEE 1481-1999"
*DATE "09:04:44 Thursday March 08, 2015"
*DESIGN "vending_machine"
*VENDOR "vendor XXX"
*PROGRAM "RC gen"
*VERSION "3.4.5"
*DELIMITER :
*T_UNIT 1 PS
*C_UNIT 1 PF
*R_UNIT 1 OHM
*L_UNIT 1 HENRY

*POWER_NETS VDD
*GND_NETS VSS

*NAME_MAP
*1 Din2
*2 Din2_net

*PORTS
*1 I *L 0.05 *S 100 100

*D_NET *2 0.15

*CONN
*P *1 I
*I Buf1:a *L 0.15

*CAP
121 *2 0
122 *2:1 0.05
123 *2:2 0.05
124 *2:3 0.05
125 *1 0

*RES
323 *2:1 *2:2 65
324 *2:2 *2:3 76
325 *2:3 *2:4 55

*END
```

So, next time, when you look at the SPEF, just make sure to open it, and see, if what we discussed in all SPEF format posts, does make sense.

And, In Lady Windemere's Fan, Oscar Wilde had Lord Darlington quip that a cynic was '***a man who knows the price of everything and the value of nothing***.'

Let's value SPEF files :)

For more, please refer to below courses

Circuit design & SPICE simulations
https://www.udemy.com/vlsi-academy-circuit-design/?couponCode=forSlideshare

Physical design flow
https://www.udemy.com/vlsi-academy-physical-design-flow/?couponCode=forSlideshare

Clock tree synthesis
https://www.udemy.com/vlsi-academy-clock-tree-synthesis/?couponCode=forSlideshare

Signal integrity
https://www.udemy.com/vlsi-academy-crosstalk/?couponCode=forSlideshare

VLSI – Essential concepts and detailed interview guide
https://www.udemy.com/vlsi-academy/?couponCode=forSlideshare

THANK YOU