# Supplementary B1: Full Vivado Xilinx Block Diagram of Cortex-M0 Microprocessor

\*\*Parent Project\*\*: Innovative Hardware Accelerator Architecture for FPGA-Based General-Purpose RISC Microprocessors (Article)

\*\*Author\*\*: Dr. Ehsan Ali

\*\*Email\*\*: <ehssan.aali@gmail.com>

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\*\*URL: https://github.com/ehsan-ali-th/cortex\_m0\_MA/tree/master/Supplementaries

bus\_matrix\_0



clk\_wiz\_0

cortex\_m0\_HRDATA[31:0]

CLK\_IN1\_D

reset

CLK

locked

Clocking Wizard

clk reset

cortex\_m0\_HADDR[31:0] cortex\_m0\_HWDATA[31:0] cortex\_m0\_HWRITE cortex\_m0\_HSIZE[2:0] code\_bram\_DOUTA[31:0]

data\_bram\_DOUTA[31:0]

code\_bram\_ADDRA[17:0] code\_bram\_DINA[31:0] code\_bram\_ENA code\_bram\_WEA[3:0] data\_bram\_ADDRA[14:0] data\_bram\_DINA[31:0] data\_bram\_ENA

data\_bram\_WEA[3:0]

BRAM\_32KB\_DATA

BRAM\_PORTA

addra[14:0] clka dina[31:0] douta[31:0] ena wea[3:0]

bus\_matrix\_v1\_0

Block Memory Generator

cortex\_m0\_core\_0

BRAM\_256KB\_CODE

dout[0:0]

Constant

constant\_0\_16bit

HADDR[31:0] HBURST[2:0] HMASTLOCK HPROT[3:0] HSIZE[2:0] HTRANS[1:0] HWDATA[31:0] HWRITE LOCKUP SLEEPING SYSTESETREQ

TXEV

accel\_code\_bram\_DINB[31:0] accel\_code\_bram\_ADDRB[31:0] accel\_code\_bram\_ENB accel\_code\_bram\_WEB[3:0]

xlslice\_0

Din[31:0]

Dout[15:0]

HCLK

constant\_1

dout[0:0]

Constant

HRESETn HRDATA[31:0] HREADY HRESP

NMI IRQ[15:0] RXEV

accel\_code\_bram\_DOUTB[31:0]

Slice

xlconcat\_0

xlconstant\_0

In0[15:0]

In1[1:0]

dout[17:0]

dout[1:0]

constant\_0 Constant

Concat

BRAM\_PORTA

addra[17:0] clka dina[31:0] douta[31:0] ena wea[3:0]

BRAM\_PORTB

addrb[17:0] clkb dinb[31:0] doutb[31:0] enb web[3:0]

Block Memory Generator

dout[15:0]

cortex\_m0\_core\_v1\_0

Constant

clk\_300mhz reset

LED0

LED1