# Supplementary B2: Simplified Vivado Xilinx Block Diagram of Cortex-M0 Microprocessor

\*\*Parent Project\*\*: Innovative Hardware Accelerator Architecture for FPGA-Based General-Purpose RISC Microprocessors (Article)

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\*\*Last update\*\*: 26th October, 2024.

\*\*URL: https://github.com/ehsan-ali-th/cortex\_m0\_MA/tree/master/Supplementaries

A diagram of a software server

Description automatically generated with medium confidence