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\* Supplementary F: Cortex-M0 Verification Flowchart

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\* Last Update: 4th Nov. 2024

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\* Used in Article: Innovative Hardware Accelerator Architecture

\* for FPGA-Based General-Purpose RISC Microprocessors

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\* URL: https://github.com/ehsan-ali-th/cortex\_m0\_MA/tree/master/Supplementaries

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A diagram of a software process

Description automatically generated with medium confidence