



**Shahid Beheshti University**  
**Faculty of Computer Science and Engineering**

**Computer Aided Digital System Design**  
**Homework No. 1**

1. Sketch the waveform of the output and internal signals.

<pre> ENTITY excercise\ IS     PORT ( a, b : IN bit;            y   : OUT bit); END test; ARCHITECTURE test OF excercise\ IS     SIGNAL n\ : bit; BEGIN     n\ &lt;= NOT b AFTER 5 ns;     y &lt;= a AND n\ AFTER 5 ns; END test;         </pre>	<div style="text-align: center; margin-bottom: 10px;">             10ns   15ns   20ns   25ns   30ns   35ns   40ns         </div>
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2. Sketch the waveform of the output and internal signals.

<pre> ENTITY excercise\ IS     PORT ( a, b, c, d, e : IN bit;            y               : OUT bit); END test; ARCHITECTURE test OF excercise\ IS     SIGNAL n1, n2, n3 : bit; BEGIN     n1 &lt;= a AND b;     n2 &lt;= d AND e;     n3 &lt;= n1 OR c AFTER 5 ns;     y &lt;= n3 XOR n2 AFTER 1 ns; END test;         </pre>	<div style="text-align: center; margin-bottom: 10px;">             5ns   10ns   15ns   20ns   25ns   30ns   35ns   40ns         </div>
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۳. Sketch the waveform of the output and internal signals.

<pre>ENTITY excercise۳ IS END test; ARCHITECTURE test OF excercise۳ IS     SIGNAL y : bit; BEGIN     y &lt;= NOT y AFTER ۳ ns; END test;</pre>	
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۴. Sketch the waveform of the output and internal signals.

<pre>ENTITY excercise۴ IS END test; ARCHITECTURE test OF excercise۴ IS     SIGNAL y : bit; BEGIN     y &lt;= NOT y; END test;</pre>	
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**Ali Jahanian**