Master's Thesis- Preliminary

Design and Implementation of OFDM System on FPGA

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The orthogonal frequency division multiplexing (OFDM) technology provides a high transmission data rate in wireless and mobile communications where multipath fading is a severe issue in degradation of the quality. Managing feasible coherent bandwidth to overcome Inter-Symbol Interference, OFDM enhances communication performance at a relatively small bandwidth cost. The improvement can be reached by interactive proper channel estimation and compensation which needs synchronization of transmitter and receiver. A *Discrete Fourier Transform* (DFT) algorithm- based configuration simplified the digital implementation of OFDM system on field programmable gate array (FPGA) as a highly flexible solution, which provide prominent performance.
In this thesis, steps to design a base-band OFDM system with channel estimation and timing synchronization upto implemented on FPGA are studied. It is a prototype based on the *IEEE 802.11a* standard and the signals is transmitted and received using a bandwidth of 20 MHz. Focusing on the quadrature phase shift keying (QPSK) modulation, the system can achieve a throughput of 24 Mbps. For the coarse estimation of timing, a modified maximum-normalized correlation (MNC) scheme is investigated and imple-

mented. Starting from theoretical study, this thesis in detail describes the system design and verification on the basis of both MATLAB simulation and hardware implementation. Bit error rate (BER) verses bit energy to noise spectral density (E_b/N_0) is presented in the case of different channels. In the meanwhile, comparison is made between the simulation and implementation results, which verifies system performance from the system level to the register transfer level (RTL).
First of all, the entire system is modeled in MATLAB and a floating-point model is established. Then, the fixed-point model is created with the help of Xilinxs System Generator for DSP (XSG) and Simulink. Subsequently, the system is synthesized and implemented within Xilinxs Integrated Software Environment (ISE) tools and targeted to Xilinx Zynq board. What is more, a hardware co-simulation is devised to reduce the processing time while calculating the BER for the fixed-point model.
Some time-based standards on IEEE 802.11a are discussed and optimum implementation of on FPGA, for instance Cross-Correlation and algebraic machine, will be introduced. Besides, we will demonstrate an engineering steps for choosing the radio board and the processor software implementations.

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Part I.
Introduction

1. Background

High quality of services (QoS) and reaching to high data rate communication to overcome the necessities in multimedia services, telecommunications industry is working currently toward the forth generation (4G) wireless communication systems. The orthogonal frequency division multiplexing (OFDM), is the most promising technology to meet the requirement as a mechanism in rapid development of digital signal processing techniques.

The first introduction of OFDM dated back 1960s as a parallel data transmitting scheme. There are many realization proposals although the foundations are fixed generally. The basic idea is to divide a single high rate data stream into a number of lower-rate data streams. Each of these data streams is modulated on a specific carrier, which is called subcarrier, and transmitted simultaneously. Robustness will be preserve against multipath fading effect. Moreover, spectrum efficiency is enhanced in comparison to conventional multi-carrier transmission. OFDM considered as a frequency division multiplexing (FDM) where the data stream carried by each sub-carrier separated.

Traditional methods used in single-carrier modulation require a number of sinusoidal subcarrier oscillators in the modulator side and multipliers and correlators in the demodulator. Introduction of Discrete Fourier Transform (DFT) until 1971 made a revolution in the complexity development. The DFT block simplified the two side processes and helped to implement the baseband in the digital manner.
Since 1990s, OFDM has been employed in wideband data transmission. Applications of OFDM technology include asymmetric digital subscriber line (ADSL), high-bit-rate digital subscriber line (HDSL), and very-high-speed digital subscriber line (VDSL) in wired systems, and digital audio broadcasting (DAB), digital video broadcasting (DVB) in wireless systems. Furthermore, it has also been recognized as the basis of the wireless local area network (WLAN) standards, among which the IEEE 802.11a standard is one of the most important ones.

Two main topics in wireless and mobile communications are high data rate and high QoS, which cause communication systems be adaptive to fast varying channel conditions and providing a steady environment to various kinds of users at a high speed of data transmission.

Due to its capabilities of providing high data rate and less sensitivity to fast channel fading, OFDM technology, in combination with other powerful techniques such as the multiple-input, multiple-output (MIMO) technique, has been the mainstream of wireless and mobile networks. It has been used in various applications, such as wireless fidelity (Wi-Fi), worldwide interoperability for microwave access (WiMAX), and the third generation partnership project (3GPP) long term evolution (LTE).

Recent development of digital integrated circuits, the high flexibility and low complexity of digital implementation of OFDM modem has accelerated its application. In competition of the technologies, field programmable gate array (FPGA) has attracted the most attention in recent years due to its superior performance and high flexibility. As a flexible general-purpose technology, FPGA is an array of gates that can be reconfigured by the designer as a versatile design platform. It is developed based on the programmable logic devices (PLDs) and the logic cell array (LCA) concept. By providing a two-dimensional array of configurable logic blocks (CLBs) and programming the interconnection that connects the configurable resources, FPGA can implement a wide range of arithmetic and logic functions. Compared to other popular IC technologies such as application specific integrated circuits (ASICs) and digital signal processors (DSPs), FPGA has the following advantages:

Performance: Inherently parallel architecture, FPGA has the ability to overcome the speed limit of sequential execution technologies and is able to process data at a much higher speed than DSP processors and whose performance is estimated by the system clock rate. Therefore, it can achieve much higher performance in various applications that requires large arithmetic resources, such as OFDM. However, DSP processors are still developing as an alternative.

Reliability: The high isolation and high parallelism mechanism not only minimize the reliability concerns, but also reduce the deterministic hardware dedicated to every task. Besides, there are mechanism in testing and verification of the system dynamically which are developing exponentially.

Cost: Because of its re-programmable nature, FPGA is a cost-effective solution for system development although the purchase cost are normally more than DSP processors which the architecture is fixed. It can be easily customized and reconfigured so that effectively versatile functionality can be realized using FPGA and there is no need to kick off design for each application. Normally, the products are tested and design and implement on the FPGA initially and after successful output it worth to transfer design into ASIC for mass production.

Flexibility: The most prominant functionality of FPGA is that the design can be changed rapidly in the prototype process. Recently, some other options like partial reconfiguration let the designer to look for more dynamic mechanisms. This let the manufacturers to have better performance in the time to market issues.
There is also some trends like IP core programs which help the big short-cuts in the designs but it very depends on the initial cost which should be decided very carefully.

2. Motivation

Practically, the signal is attenuated and distorted by multipath effect in real channel transmission. Fading estimation and equalization of the channel in wireless technology is inevitable to have a reliable communication. Implementation an OFDM system on FPGA with capability of channel estimation and synchronization is the final goal of this thesis.
There are many techniques and mechanism to implement OFDM wireless communication on FPGA. In ... the authors helped OFDM transceiver on certain topics in the receiver design, such as the synchronization, packet detection, channel estimation and equalization. Moreover, OFDM transceivers are designed for the AWGN channel have been presented in ..... However, there are not a comprehensive work presenting a complete development of OFDM system with channel estimation and synchronization using the FPGA technology.

A top-down approach and demonstrative system performance in baseband OFDM is done in this thesis. System synchronization will also be discussed in this thesis. In addition, we focus on the design and implementation of channel estimation and equalization, while a verification at system level is performed. The detailed objectives include:

- To design, model and implement after proper simulation a baseband OFDM system including both the transmitter and the receiver, and to analyze the system performance.
- To prototype an OFDM system based on a specific wireless communication standard.
- To implement the synchronization and channel estimation system for the receiver and provide system evaluation under different channel conditions.

3. Methodology

It is tried to explain the theoretical concepts firstly and then to show some facts in the simulation based on extracted models. Finally, the issues is examined on hardware.
The hardware chosen is consisted a Zynq board which is an FPGA with two embedded ARM processors and the radio board which is FMCOMMS1.

4. Contribution

Part II. Theory, Design and Simulation

5. OFDM System Architecture

Generally, an OFDM signal is defines as a summation of many OFDM standard symbols, which can considered continous in the time domain.It can be defined as following:

$$s(t) = \sum_{k=-\infty}^{+\infty} s_k(t) \tag{1}$$

where $s_k(t)$ is the k-th OFDM symbol which starts at time $t = t_s$. An OFDM system is a multi-carrier transmission mechanism which the mathematical model is generalized by the summing a series of modulated subcarriers digitally. This modulation can be phase shift keying (PSK) or quadrature amplitude modulation (QAM) and transmitted in parallel. So, we can conclude:

$$s_k(t) = \begin{cases} Re\left(\sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1} d_{i+\frac{N}{2}} \exp[j2\pi(f_c - \frac{i+0.5}{T})(t - t_s)]\right), & t_s \leq t < t_s + T \\ 0, & \text{otherwise} \end{cases} \tag{2}$$

where T is the symbol duration, N is the number of subcarriers, f_c is the signal carrier frequency on the radio frequency (RF) band, and d_i is the complex value for PSK or QAM modulated symbol. We reach I_i and Q_i being the in-phase and quadrature part of d_i, respectively.
The complex envelope of an OFDM signal given by the following equation is used as the baseband notation:

$$s_k(t) = \begin{cases} Re\left(\sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1} d_{i+\frac{N}{2}} \exp[j2\pi \frac{i}{T}(t - t_s)]\right), & t_s \leq t < t_s + T \\ 0, & \text{otherwise} \end{cases} \tag{3}$$

The real and imaginary parts of 3 are the in-phase (I) and quadrature (Q) of the baseband OFDM signal. Consequently, they are multiplied by a cosine and a sine waveform with a carrier frequency to generate the passband OFDM. At the receiver, each subcarrier is down-converted with a subcarrier of the desired frequency and supported over the symbol period. For example, the complex value for the m-th subcarrier d_m is obtained equation 4, where the whole signal is multiplied by the frequency of $\frac{m}{T}$, and then integrated over the symbol period T:

$$
\begin{aligned}
\int_{t_s}^{t_s+T} s_k(t)\exp[-j2\pi\frac{m}{T}(t-ts)]dt &= \int_{t_s}^{t_s+T}\left(\sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1} d_{i+\frac{N}{2}}\exp[j2\pi\frac{i}{T}(t-t_s)]\right)\exp[-j2\pi\frac{m}{T}(t-ts)]dt \\
&= \sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1} d_{i+\frac{N}{2}}\int_{t_s}^{t_s+T}\left(\exp[j2\pi\frac{i-m}{T}(t-t_s)]\right)dt \\
&= Td_{m+\frac{N}{2}}
\end{aligned}
\tag{4}
$$

4 shows all the subcarriers over the integral region are zero except the desired one. The desired output for the signal demodulation, $d_{m+\frac{N}{2}}$ multiplied to a constant factor T, is exactly the integration for the m-th subcarrier. Since each subcarrier has an exact integer number of cycles within OFDM symbol duration, the orthogonality between subcarriers is guaranteed.
the mathematical model for discrete time signal is as below if the OFDM symbol is sampled with a sampling period $\frac{T}{N}$:

$$
s(n) = s_k(\frac{nT}{N}) = \sum_{i=0}^{N-1} d_i\exp(j2\pi\frac{in}{N}), n = 0, 1, ..., N-1 \tag{5}
$$

This represents an inverse DFT (IDFT) for PSK or QAM symbols.
According to the above analysis, the basic architecture for a baseband OFDM system that contains the essential parts is shown in Figure 5.

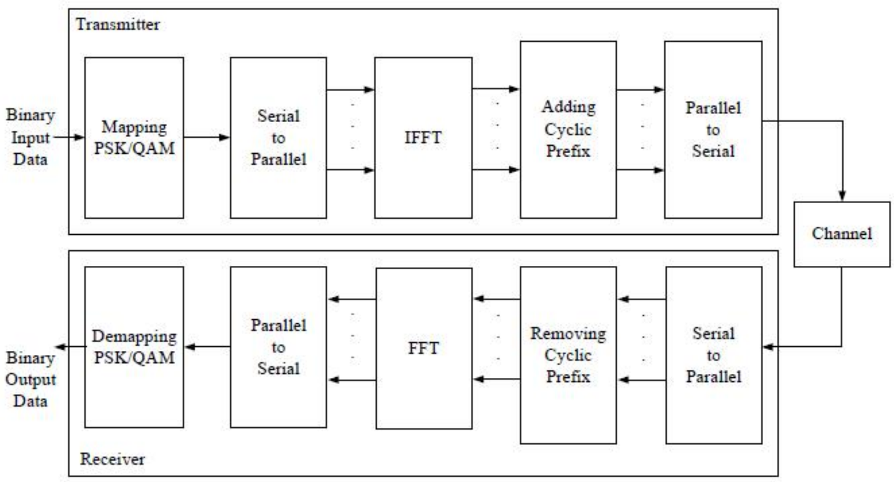


Figure 1: Basic baseband OFDM system

In practice, to prevent sharp transactions at the sample time boundaries, a windowing block is used for filter shaping. In conclusion, spectrum utilization is enhanced dramatically. Therefore, the baseband OFDM symbol can be written as below:

$$s_k(t) = \begin{cases} w(t-t_s) \sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1} d_{i+\frac{N}{2}} \exp[j2\pi \frac{i}{T}(t-t_s-Tg), & t_s \leq t < t_s + (1+\beta)T_{sym} \\ 0, & \text{otherwise} \end{cases} \quad (6)$$

where T_g is the guard interval duration, $T_{sym} = T + T_g$ is the OFDM symbol period, symbol starting time $t_s = kT_{sym}$, and $w(t - t_s)$ is the pulse shaping window, which is usually a raised cosine filter, and β is the roll-off factor.

6. OFDM Specifications in IEEE 802.11a Standard

6.1. System Design

In reality, having an anti-aliasing configuration, oversampling is performed before passing the digital signal to digital-to-analog converter. There are many other blocks in standards like channel coding, symbol interleaving and channel estimation.

In comparison to the fundamental architecture shown in Figure 000, some other building blocks are added in a practical IEEE 802.11 design shown in Fig 00, marked with blue and dashed on line. At the transmitter, several ”null” subcarriers or tones are reserved besides of the data subcarriers in order to perform oversampling of the transmitted signal. In this context, ”null” means the symbol carried on this subcarrier has a value of zero. Besides, some other subcarriers used as pilot for channel estimation are also inserted. The subcarriers are allocated at the input of the IFFT block to generate a phase shift. The windowing for pulse shaping is achieved after CP extension.

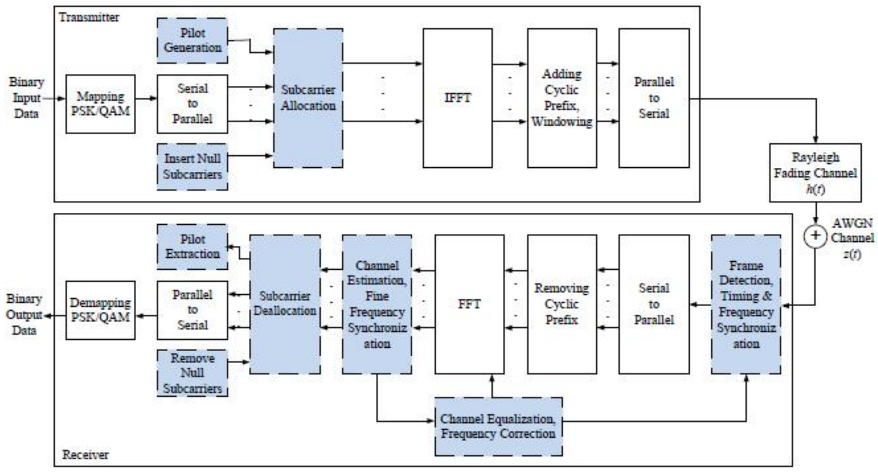


Figure 2: Architecture of an OFDM system

At the receiver side, the frame synchronization and detection for both timing and frequency is performed in the first stage. Channel estimation is performed after the FFT block outputs the preambles in the frequency domain. The result is fed back to the FFT block for the equalization, which eliminates the effects of fading channel, while the fine synchronization for both timing and frequency is also added to further improve the system performance.
At least these basic parameters should be specified for a system design:
1) Delay spread expected for the channel (300 ns)
2) Guard duration (800 ns) which describes symbol duration (4.0 μs)
3) Available bandwidth
4) Data rate

For indoor environment a delay spread less than 300 ns expected. We consider the guard duration 800 ns, which effectively protects the signal from ISI in the indoor environment and some of the outdoor wireless communication environments. Five times the guard duration for limiting the power and bandwidth loss is regarded for the symbol duration, and is set to 4.0 μs in our case. Hence, the OFDM symbol rate is 0.25 mega symbol per second (Mbaud).
Keep in mind, the useful OFDM symbol duration without the guard interval is 3.2 μs. So, the subcarrier spacing, which is the reciprocal of the useful symbol duration, can be determined as 312.5 kHz. Assuming that there is a bandwidth of 20 MHz available, the number of subcarriers is calculated to be 64. This is exactly the same as the specification defined in IEEE 802.11a standard.
As mentioned, some tones are reseved for pilot subcarries (channel estimation), null subcarriers (realizing oversampling to avoid aliasing) and windowing (reduce the out-of-band spectral energy).

In our design we chose 48 data tones and 4 pilot subcarriers. So, 52 subcarries are occupied. Applying a raised-cosine window with roll-off factor β= 0.02 the total occupied bandwidth is

$$(1 + 0.02) \times (52 \times 312.5kHz) \approx 16.6MHz$$

To accomplish Oversampling, some zeros before and after the data vector are appended in the frequency domain as shown below.

$$\overbrace{0, 0, \ldots, 0}^{1/2 \text{ appended zeros}},\ \underbrace{d_{-\frac{N_d}{2}}, d_{-\frac{N_d}{2}+1}, \ldots, d_{-1}}_{\text{Negative subcarriers}},\ \underbrace{d_1, d_2, \ldots, d_{\frac{N_d}{2}}}_{\text{Positive subcarriers}},\ \overbrace{0, 0, \ldots, 0}^{1/2 \text{ appended zeros}}$$

The nonzero data values are mapped onto the subcarriers around 0 Hz, and the zeros are mapped onto frequencies around sampling rate.

Basically, in the BPSK modulation is applied on each subcarrier, each symbol for an individual subcarrier has one bits. The bit rate achieves without channel coding:

$$\frac{1}{4.0\mu s} \times 48 \times 1 = 12Mbps$$

The same calculation can be perform for QPSK to reach 24Mbps. But, channel coding will reduce this values. Variation of coding rates and modulation methods, In the 802.11a standard, the data rate ranges from 6 Mbps to 54 Mbps.

Table 1: System parameters defined for the proposed OFDM system

Parameter	Description	Value
B_w	Available channel bandwidth	$20MHz$
σ_τ	Delay spread of the channel	$< 300ns$
T_g	Guard interval duration	$0.8\mu s$
T_{sym}	OFDM symbol period	$4.0\mu s$
T	Effective symbol duration (FFT period)	$3.2\mu s(= T_g - T_{sym})$
T	Effective symbol duration (FFT period)	$3.2\mu s(= T_g - T_{sym})$
Δf	Subcarrier spacing	$312.5kHz(= 1/T)$
N_g	Number of guard samples	16
N	FFT size	$64 = B/\Delta fs$
N_d	Number of data subcarriers	48
N_p	Number of pilot sucarriers	4
N_u	Number of used subcarriers	52
B_u	Signal occupied bandwidth	$16.6MHz$
	Modulation type	$BPSK, QPSK$
R_b	Data rate without coding	$12Mbps, 24Mbps$

6.2. IEEE 802.11a Standard in Time and Frequency

A packet of OFDM will be described here. In an OFDM frame, a preamble which carries no data is transmitted first, followed by the signal field which give some information about data and transmitted data. As indicated in Figure 00, an OFDM frame has the general form as below:

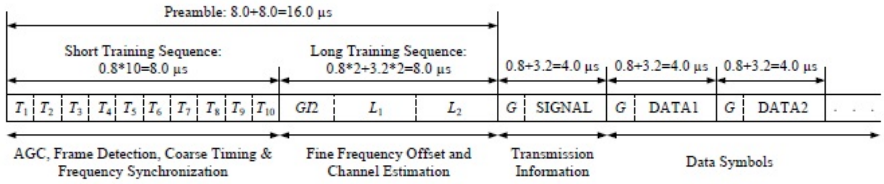
$$s_{OFDM}(t) = s_{preamble}(t) + s_{signal}(t - T_{preamble}) + s_{data}(t - T_{preamble} - T_{signal})$$

where

$$s_{preamble}(t) = s_{short}(t) + s_{long}(t - T_{short})$$

The preamble starts with 10 short training symbols (STSs) from T1 to T10, followed by a guard interval (GI2) and two long training symbols (LTSs) L1 and L2. Both the short and long training sequences have an 8 μs duration and the entire preamble lasts for 16 μs. Then, a 3.2 μs signal symbol, as well as 800 ns guard interval is transmitted. This field bears some information necessary for the data symbols, such as the coding rate and length. Finally the various data symbols that carry user information are transmitted. Each data symbol has a duration of 4.0 μs, within which there is a 800 ns CP, as already described.

The application of STS and LTS for training are different. STS used for AGC, frame detection, coarse timing and frequency synchronization. Each symbol in this sequence has a duration of 800 ns and contains 16 samples, and is identical to one another. It will be shown in a professional system, auto-correlation will apply to this portion to perform such the operations. After the short training sequence is transmitted, a 1.6 μs guard interval that contains 32 samples is introduced. The LTS is cyclically extended within this interval. Then two identical LTSs with the same duration of 4.0 μs are followed. The LTS is used for fine frequency offset and channel estimation. It will be described that a cross-correlation with a stored array is done for extraction of the offset.



As we already analyzed, 52 subcarriers are used for an OFDM data symbol and pilot. Oversampling is achieved by adding 12 null subcarriers in order to eliminate aliasing which might occur during digital to analog conversion. Because FFT shift is performed, the null subcarriers with a value of zero are located in the middle of the input vector for the IFFT block. Note that dc carrier is not used to transmit data. The short and long training sequences can also be applied to this mapping rule, since they both have a length of 52 samples with frequency index from -26 to +26.

7. Hardware Introduction

7.1. Processor

Figure 3: Xilinx Zynq-7000 SoC ZC706 Evaluation Kit

7.2. Radio Board

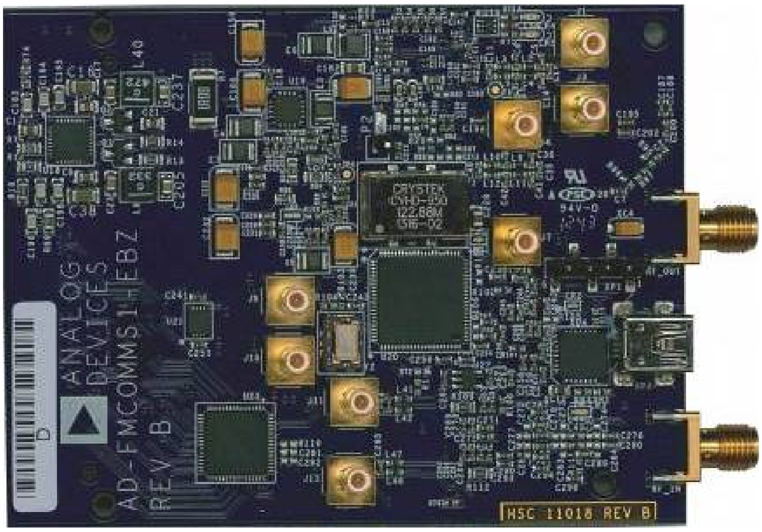


Figure 4: AD-FMCOMMS1-EBZ (Radio Board)

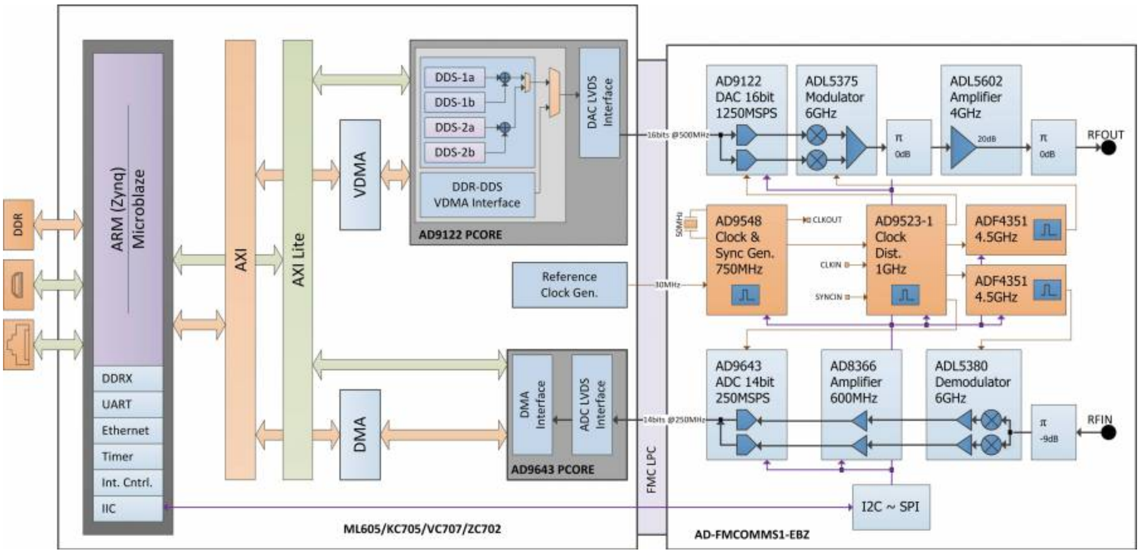


Figure 5: AD-FMCOMMS1-EBZ Block Diagram

7.3. Clock Chain on FMCOMMS1

Now, we discuss more about the clock chain and distribution mechanism on the board to find some meaningful number. As you can see in the figure, we configure the board and internal FPGA architecture to generate a 30MHz clock to the RF board. This 30MHz is just chosen because a relevant crystal mounted on the Zynq board and the all generated clock is supposed to be in-phased with it. This 30MHz is an input for AD9548 as a clock generator/synchronizer which has a very precise PLL inside to generate a 20MHz.

The AD9548 generates an output clock synchronized to one of up to four differential or eight single-ended external input references. The digital PLL allows for reduction of input time jitter or phase noise associated with the external references. The AD9548 continuously generates a clean (low jitter), valid output clock even when all references have failed by means of a digitally controlled loop and holdover circuitry. AD9548 is a very complicated device to generate 20MHz with maximum precision.

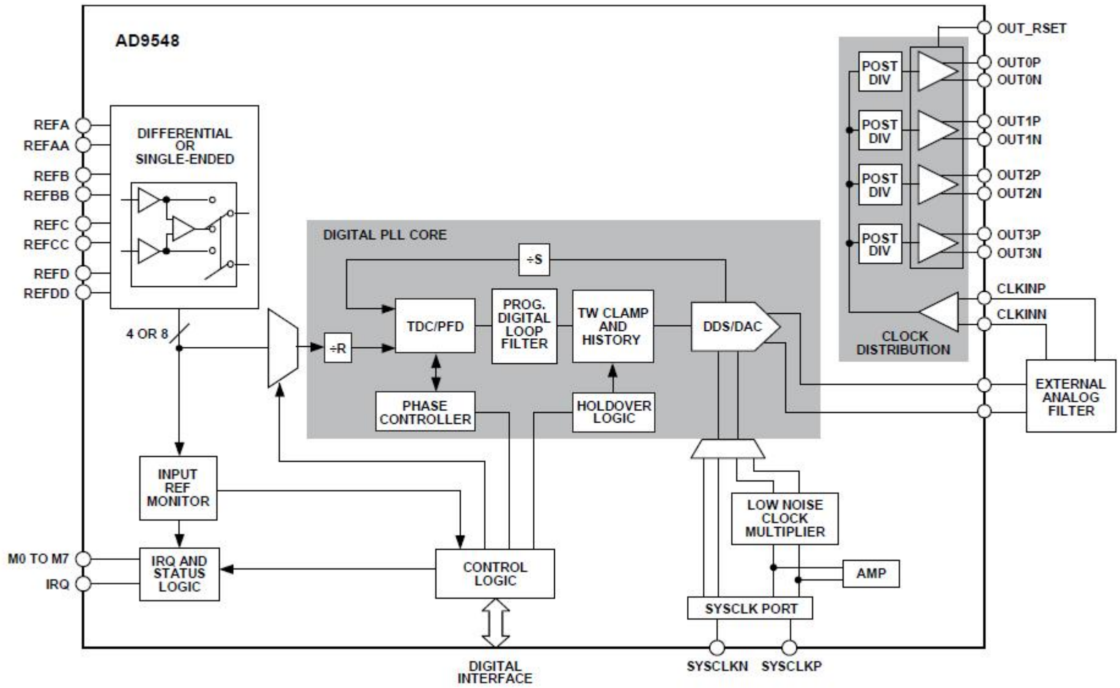


Figure 6: AD9548 Block Diagram

The next IC in the clock chain is AD9523-1 which is Low Jitter Clock Generator. The AD9523-1 provides a low power, multi-output, clock distribution function with low jitter performance, along with an on-chip PLL and VCO with two VCO dividers. The on-chip VCO tunes from 2.94 GHz to 3.1 GHz. The AD9523-1 is defined to support the clock requirements for long term evolution (LTE) and multicarrier GSM base station designs. It relies on an external VCXO to provide the reference jitter cleanup to achieve the restrictive low phase noise requirements necessary for acceptable data converter SNR performance.

The input receivers, oscillator, and zero delay receiver provide both single-ended and differential operation. When connected to a recovered system reference clock and a VCXO, the device generates 14 low noise outputs with a range of 1 MHz to 1 GHz, and one dedicated buffered output from the input PLL (PLL1). The frequency and phase of one clock output relative to another clock output can be varied by means of a divider phase select function that

serves as a jitter-free, coarse timing adjustment in increments that are equal to half the period of the signal coming out of the VCO.
In our chain we have a 80MHz VCXO connected to AD9523-1. It is supposed to generated 40MHz for ADC, DAC and also the main OFDM architecture FPGA program. You can see the specification of the crystal oscillator in ....

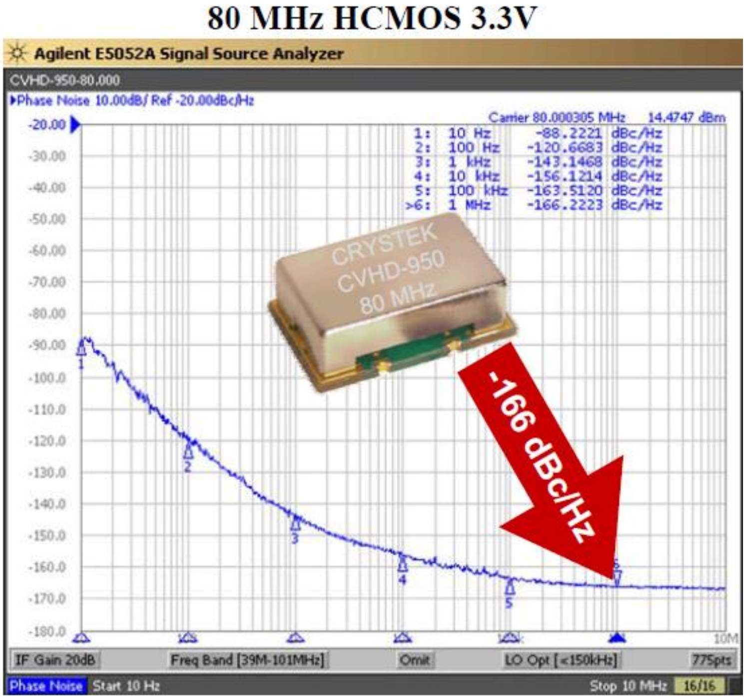


Figure 7: CVHD-950 Ultra Low Phase Noise Oscillator

8. Expectations for CFO on FMCOMM1

In implementation of an OFDM chain, we should have good understanding the range of carrier frequency offsets which can be expected on our hardware platform. Our RF board foundation is based on FMCOMMS1. As a result, the elements in term of phase -noise and CFO should be studied. The main RF frequency refrence is a Crystek CVHD-950 (VCXO). This VCXO provides a clock signal at a nominal frequency of 80 MHz. Actual output frequency varies as a function of multiple factors, and is only specified by the manufacturer with some tolerance. The CVHD-950 is specified with a frequency tolerance of ± 4 ppm. Thus, we must design for a reference frequency of 80 ± 0.000320 MHz. Imagine our target RF carrier frequency is 2452 MHz which implies 2400 MHz± 4 ppm (or 2400 ± 0.009600 MHz).
The worst case CFO will occur when the transmit and receive nodes operate at opposite ends of this range. Thus, for operation in the 2.4 GHz band

our OFDM transceiver design must be ready to handle any carrier frequency offset up to ≈20 kHz.

9. Time Domain CFO Correction

Prevention of the degradation of CFO, the receiver should estimate and correct the offset in the time domain before the FFT block. The FFT block translates the received signal into the frequency. Regarding to the variety issue of OFDM, many estimation algorithms have been proposed.

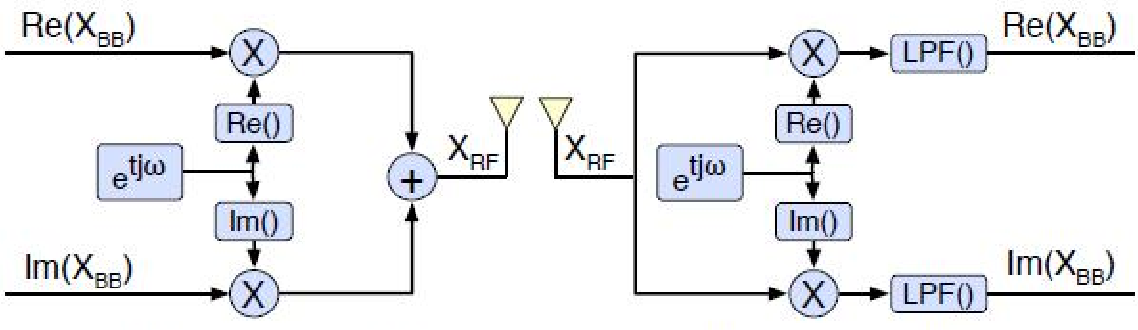
10. System Analysis by Simulation

11. Carrier Frequency Offsets

As a result of the frequency variation between local oscillators of the transmitter and the receiver nodes that generate the carrier signals, carrier frequency offsets (CFO) is happened. It causes when the baseband signal is going to be translated to RF. The issue is understood well but the impact to overcome CFO and suppression this phenomena is always depend on the specific parameters of the given transceiver and the hardware.
The origin of the CFO effect is studied in this section. We explore in a specific scenario of OFDM and the impact on the hardware design. Both simulation and experiments will be demonstrated and the CFO estimation and compensation is described.

11.1. Origin of CFO

A simple model of a radio transmitter and receiver can depict the basis of the CFO source.



(a) Transmitter model (b) Receiver model

Figure 8: General models of a direct conversion RF

In Figure 8, ω is The carrier frequency and X_{BB} is the complex baseband signal, X_{RF} is a real-valued RF signal. These models simplified many other operations in a real RF transceivers although none of these affect the up/down-conversion processes as they relate to CFO.
These equations about transmit and receive processes can be written in equation (7):

$$\begin{aligned} X_{RF} &= TX(X_{BB}) \\ &= Re(X_{BB})\cos(\omega t) - Im(X_{BB})\sin(\omega t) \\ &= \frac{1}{2}(X_{BB}e^{jt\omega} + X_{BB}^{*}e^{-jt\omega}) \end{aligned} \tag{7}$$

$$\begin{aligned} X_{BB} &= RX(X_{RF}, \omega) \\ &= LPF(X_{RF}e^{j\omega t}) \end{aligned}$$

Assume a signal S_{BB} transmitted with carrier frequency ω_S which is received with carrier frequency ω_D. we can express the received baseband signal D_{BB} in terms of the transmitted baseband signal S_{BB} and the carrier frequencies. Then:

$$\begin{aligned} D_{BB} &= LPF(\frac{(S_{BB}e^{jt\omega_S} + S_{BB}^{*}e^{-jt\omega_S})e^{jt\omega_D}}{2}) \\ &= S_{BB}(e^{jt(\omega_S - \omega_D)}) \end{aligned} \tag{8}$$

The received baseband signal is equal to the original baseband signal modulated by a complex sinusoid. In the frequency domain, this gives a received spectrum equal to the transmitted one, only shifted away from DC by the difference in the carrier frequencies of the transmitter and receiver (i.e. $\omega_S - \omega_D$). This shift of the received signal is the baseband manifestation of carrier frequency offset.

11.2. Impact of CFO

There are two destructive impacts on an OFDM system. Firstly, the phase offset across subcarriers in an symbol which can be estimated and corrected in frequency domain to prevent errors in a constant rotated constellation. Some subcarriers are allocated as pilot tones which receiver can estimate phase errors.
The second effect of CFO is the degradation of orthogonality between subcarriers in receiver's FFT which causes inter-carrier interference (ICI). ICI acts

an effective SNR reduction as a result of CFO increasing. [...]
The impact is displayed in Figure 9 which is shown simulated OFDM system uses 10 MHz bandwidth and 64 subcarriers, 48 of on a random 16-QAM data symbols. CFO and AWGN are applied between the transmitter and receiver. The receiver model uses perfect knowledge of the CFO to correct the phase offset in each OFDM symbol, but does not implement any correction for ICI.

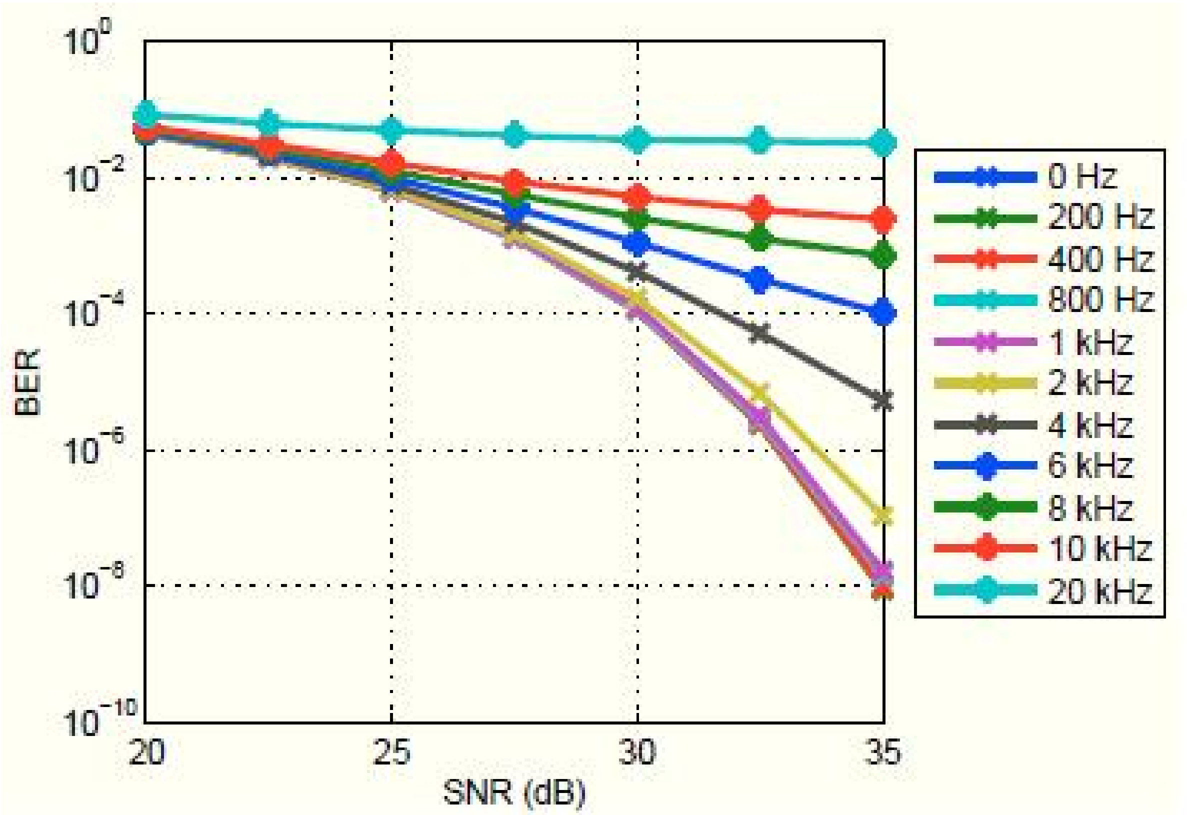


Figure 9: OFDM performance loss due to CFO-induced ICI.

The results shows that for large CFOs errors caused by ICI dominate performance, even at high SNR. It is also clear that for small CFOs performance is dominated by SNR. Specifically, for frequency offsets smaller than 1 kHz, the performance degradation due to ICI is negligible.

Part III.
FPGA Implementation

An OFDM structure from modulator to demodulator is studied. The aim is to investigate the characteristics of the system in different conditions and comparing the behavior with the single carrier configuration. The simulation conditions change in the cyclic prefix size, a Non-Linear Amplifier (NLA), multipath and equalizer activation.
Optimization on the cost function for the system is done. Semi-Analysis calculation for noise for a target Bit Error Rate (BER) of 10^{-3} are done. OFDM simulation is based on the characteristic of Fast Fourier Transform.
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With activated NLA with fixed $\beta = 10$ the E_b/N_0 has to be amplified by almost $0.8dB$ in order to reach the target BER.
The optimized back-off of $\beta = 8$ improves this value by $14dB$ when equalization block is activated.

12. Introduction

An OFDM communication system is simulated. Different characteristics of the system are examined and parameters are adjusted to study.
A block based signaling configuration is chosen for the implementation. As a result, the realization of the modulator is done thanks to IFFT computation characteristics. Cyclic prefixes are added to the resulting OFDM symbols as well as guard time filling. On the demodulator an FFT block recreates the initial input of the system.
An optimization is performed on the input back-off of a Non-Linear Amplifier (NLA). The back-off of the NLA is normally more than in a single carrier system because of better performance of the inter symbol interference (ISI) thanks to smaller coherent bandwidth which let us work on less power.
A description of the the system is given in section 13. Section 18 describes the varied parameters and analysis values while in section 19 observations on the simulation are presented and characteristics of the system are shown. Before the conclusion in section **??**, section **??** describes the optimization of

the system.

13. System Model

Figure 10 presents the OFDM system block diagram. Basic steps of the praxis are realized in blocks in the simulation. Additionally is shown how the composition of data changes in the single steps of the system.
The first block represents the data source. They are the bits which an application may send. In the simulation it is realized by a random bit generator. The following QPSK modulation block converts this bits into symbols, which are complex numbers. Each symbol carries several bits. The third block is the first one actually relevant for OFDM. The serial symbol stream is converted into a channel and OFDM symbol structure. In the simulation it is represented in a matrix shape where the rows are different channels and each column is an OFDM symbol. This means that each OFDM symbol, formed by c (#channels) serial symbols (complex numbers), is distributed over the c channels.
In the next step zero channels are added in order to separate well subsequent OFDM symbols. For the simulation structure zero rows are added in the middle of the matrix. The following block interprets each symbol (complex number) of an OFDM symbol as a orthogonal frequency and converts each OFDM symbol per IFFT into a vector of time discrete values of the same length. As sixth step the cyclic prefix insertion is done. In order to maintain orthogonality of the frequencies but prevent ISI, an amount of *guard values* are copied from the end of each OFDM symbol to its beginning. The number of rows in the simulation matrix grows by that by the number of *guard values*.
The following block is the NLA which depends on the optimization parameter β (back-off). At this point the transmitter side ends. In order to simulate the multipath a convolution is made on each OFDM symbol with the delay filter. Since the simulation is made on each OFDM symbol separated, this operation works with a memory in order simulate a serial transmission.
The receiver side is just the opposite of the transmitter. In the cyclic prefix remover the copied values are deleted and the simulation matrix size decreases. The next block performs the FFT on each OFDM symbol which reconstructs the as frequencies interpreted complex numbers.
The following equalization block tries to remove the effect of the multipath. For the simulation a multiplication with the inverted transfer function of the multipath is operated. By this, only the phase of the complex symbols changes.
Finally, the zero channels are removed and the matrix structure is reconverted to a series of symbols. The following analysis is done on the received symbols and consequently they are not demodulated into a bitstream.

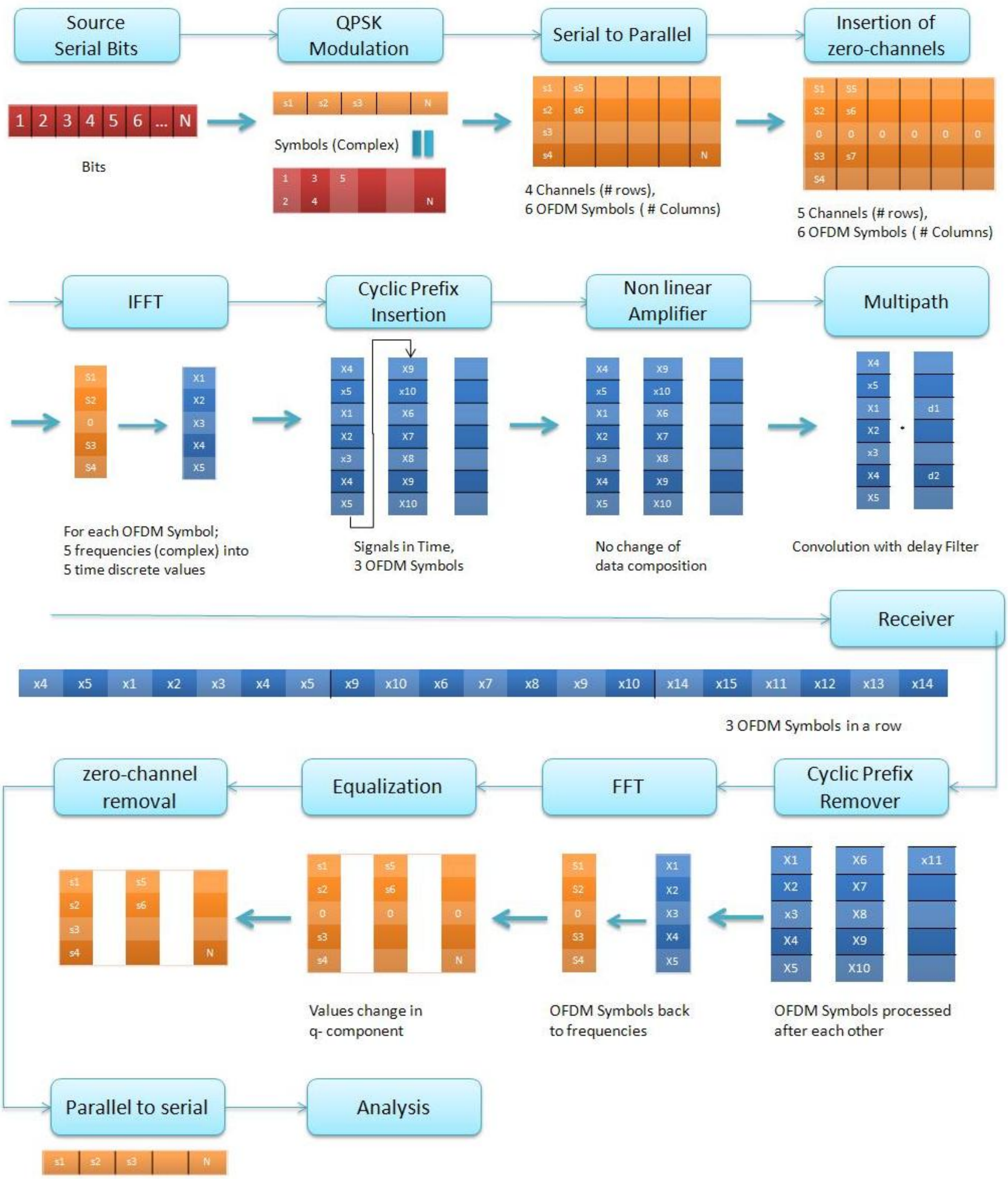

Figure 10: OFDM System Model

14. Simulation Structure

Fundamentally, we do block-by-block simulation thanks to IFFT for parallel processing. Simulation is done by (de)activation of the blocks on Figure 10. First, we study the noise semi-analysis by having only the basic blocks activated and also to examine the correctness of them. The basic blocks for our OFDM system are IFFT and FFT, Cyclic addition and removal and the semi-analyzer block. The theoretical equation of the BER for a QPSK channel is:

$$P_b(e) = \frac{1}{2}erfc(\sqrt{\frac{E_b}{N_0}})$$

It is discussed that the BER can be computed by considering the non-ideality which the two parameters *guard time* and *pilots* will inject into the result. The formulation would be:

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In the next step, the NLA block is activated and its effect is studied. We have chosen NLA number 3 and try to optimize its back-off. Later, the channel impulse response modeled by considering two multipaths with different delays is implemented by an FIR filter. This extended simulation will be compared with NLA in the scenario and also the equalizer. Finally, we optimize the system by adjusting the back-off parameter of NLA in an AWGN channel. When we study the equalization block we consider such equation for the received tones:

$$y_i = H_i\lambda_i + n_i$$

Without equalization the BER would be:

$$P_b(e) = \frac{1}{2}erfc(\frac{H_i\lambda_i}{\sqrt{2\sigma^2}})$$

Then, after the equalization, the formula will be changed to this:

$$y_i' = \lambda_i + \frac{n_i}{H_i}$$

and the BER to

$$P_b(e) = \frac{1}{2}erfc(\frac{\lambda_i}{\sqrt{2\sigma^2}})$$

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15. System Design in System Generator

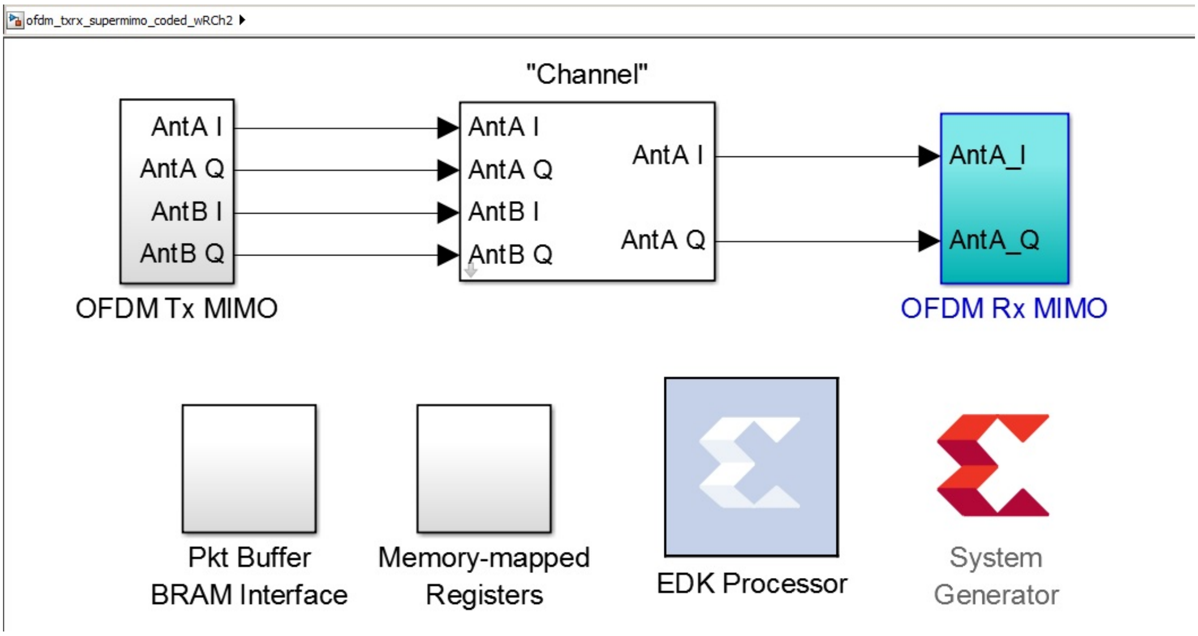

Figure 11: OFDM System.

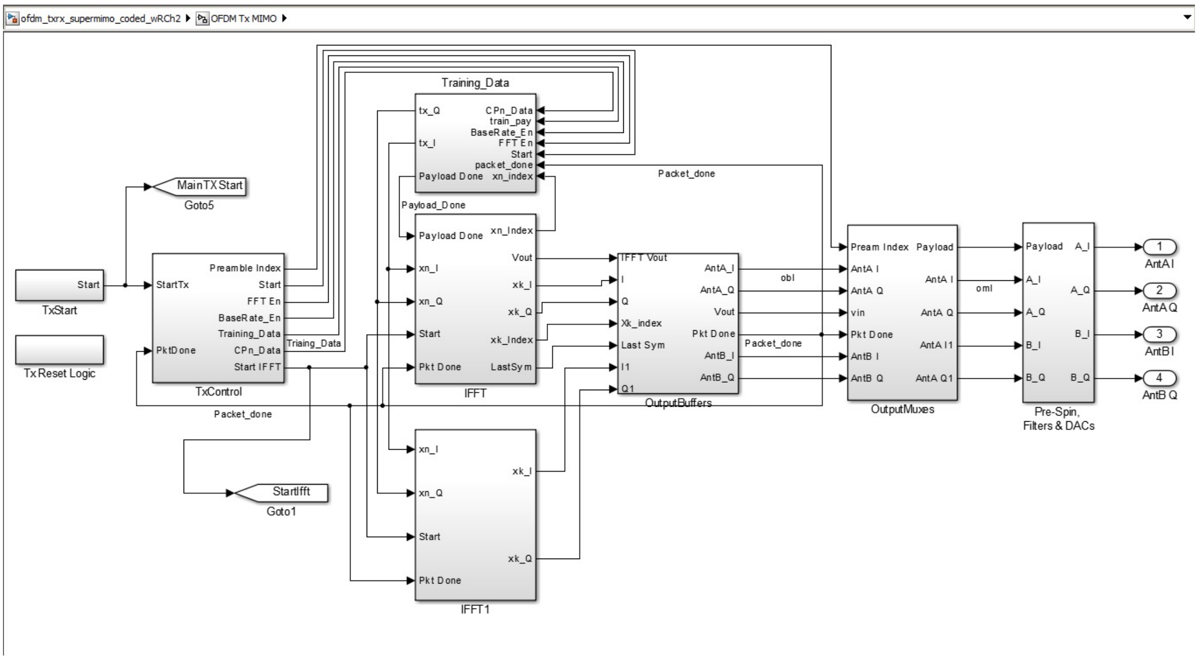

Figure 12: OFDM Transmitter Block.

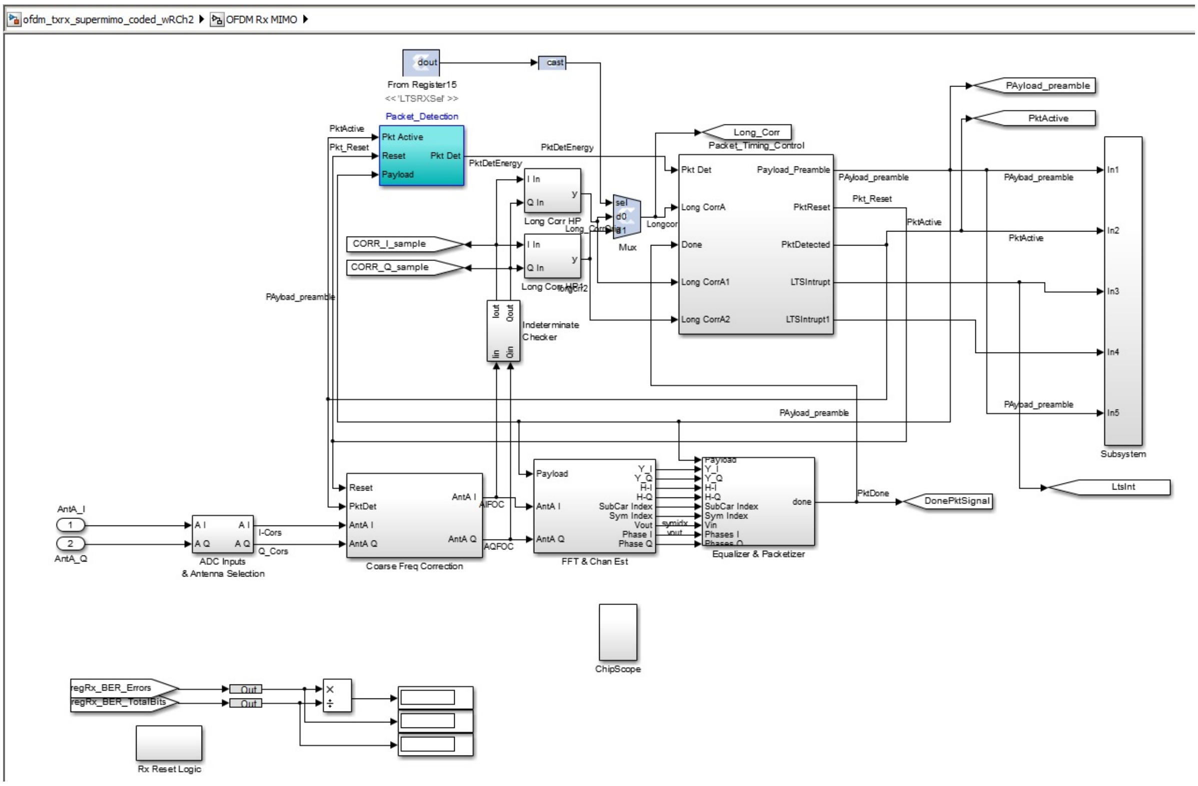

Figure 13: OFDM Receiver Block.

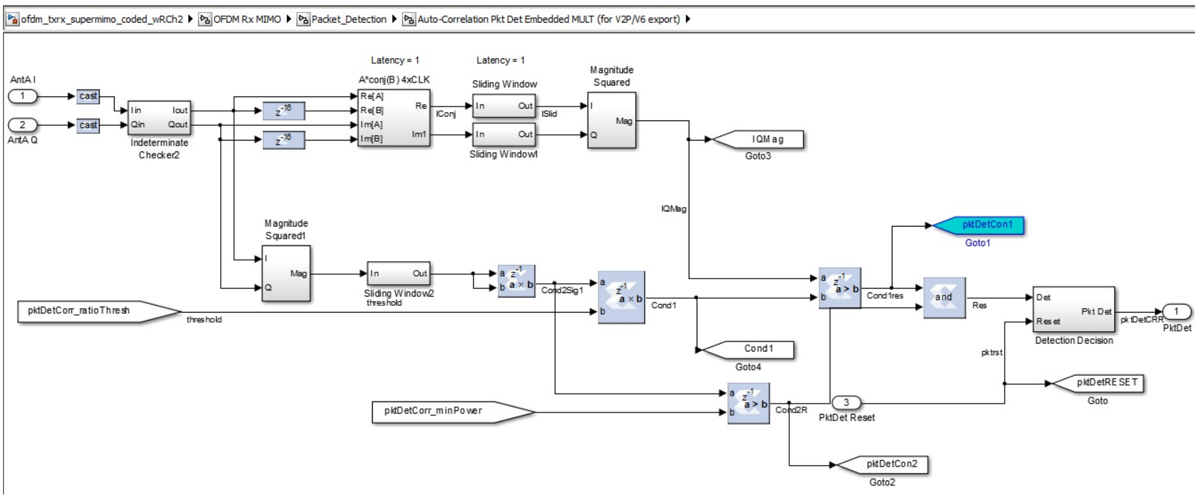

Figure 14: Auto-Correlation Block.

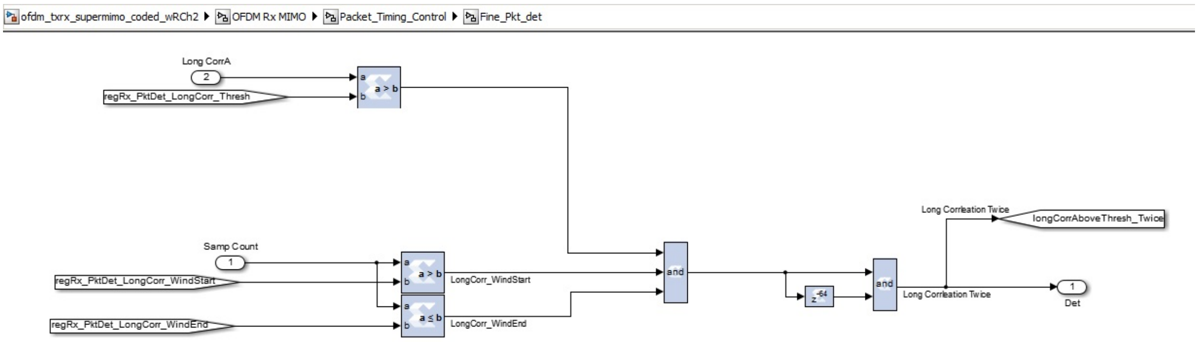

Figure 15: Fine Packet Detection Block.

16. Hardware Samples and Analysis

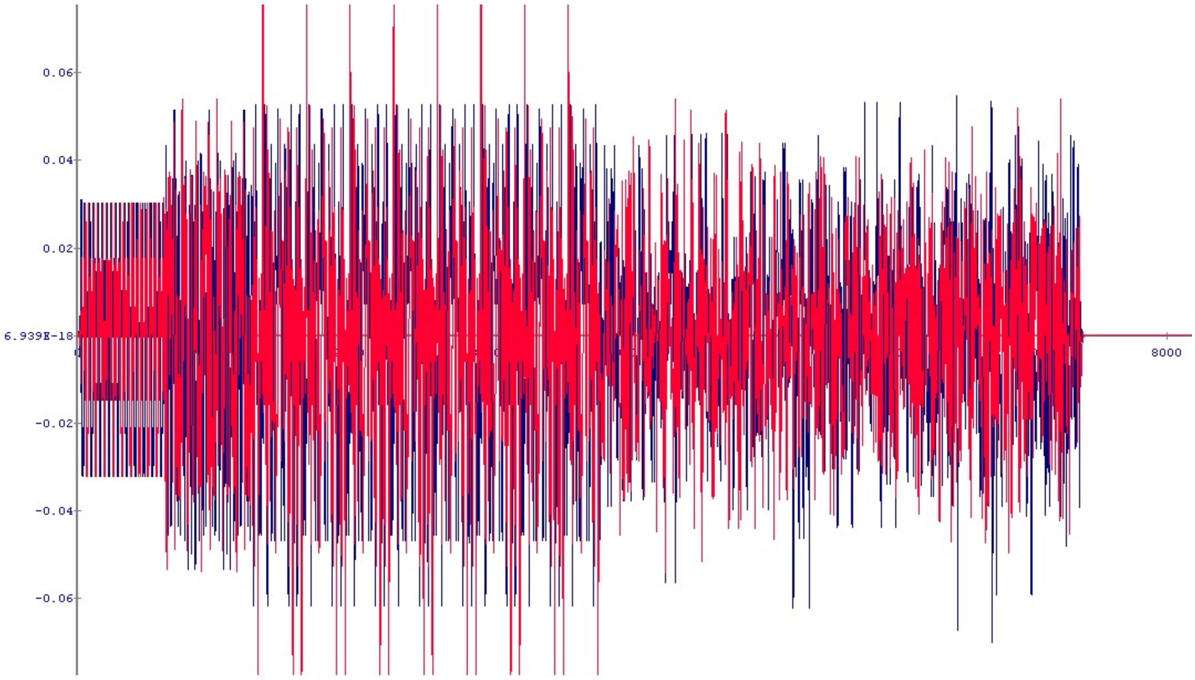

Figure 16: OFDM Frame (I/Q) detected in Chipscope.

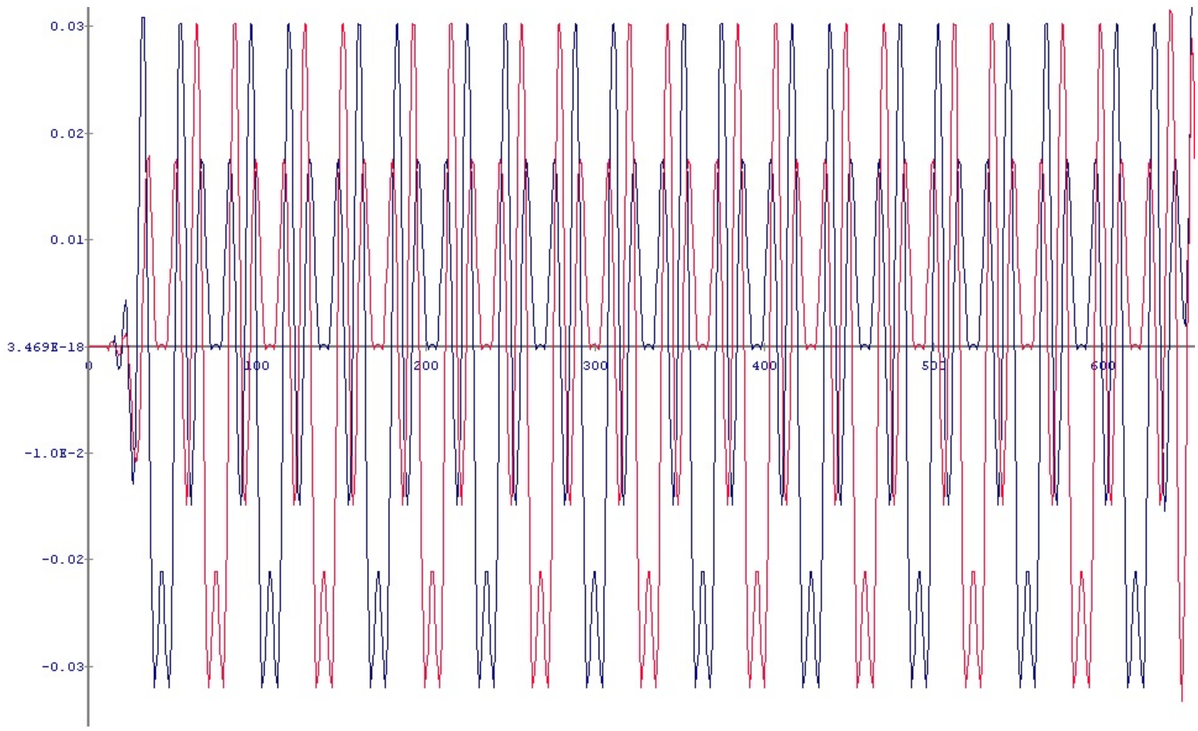

Figure 17: STS (I/Q) detected in Chipscope.

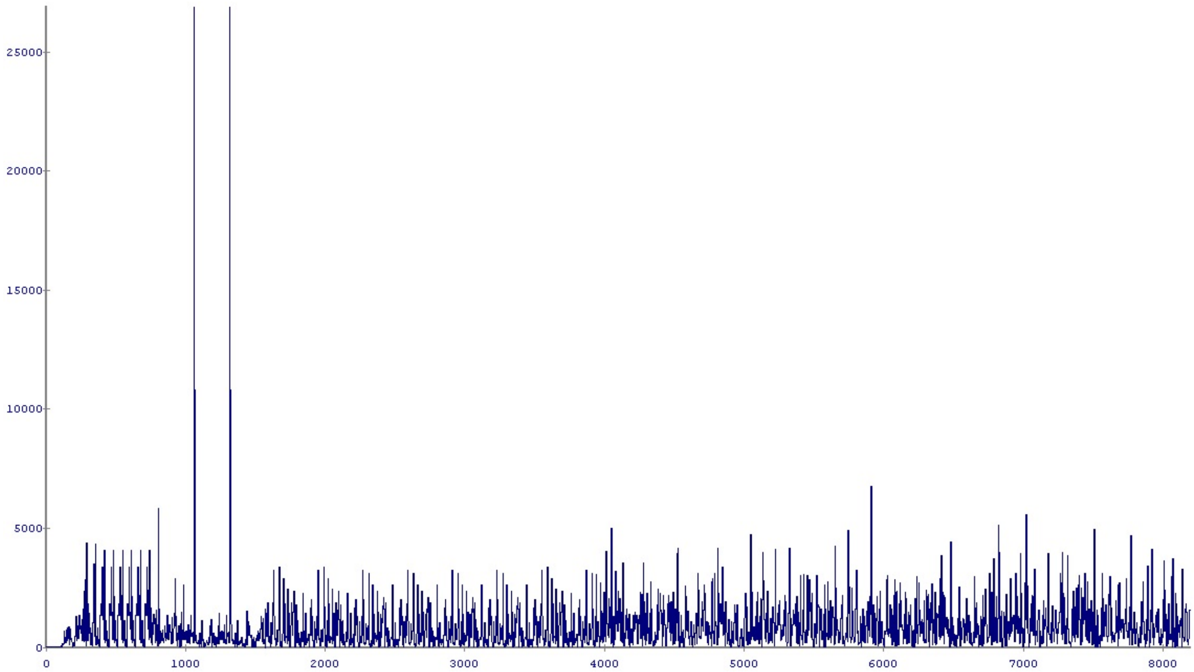

Figure 18: Cross-Correlation detected in Chipscope.

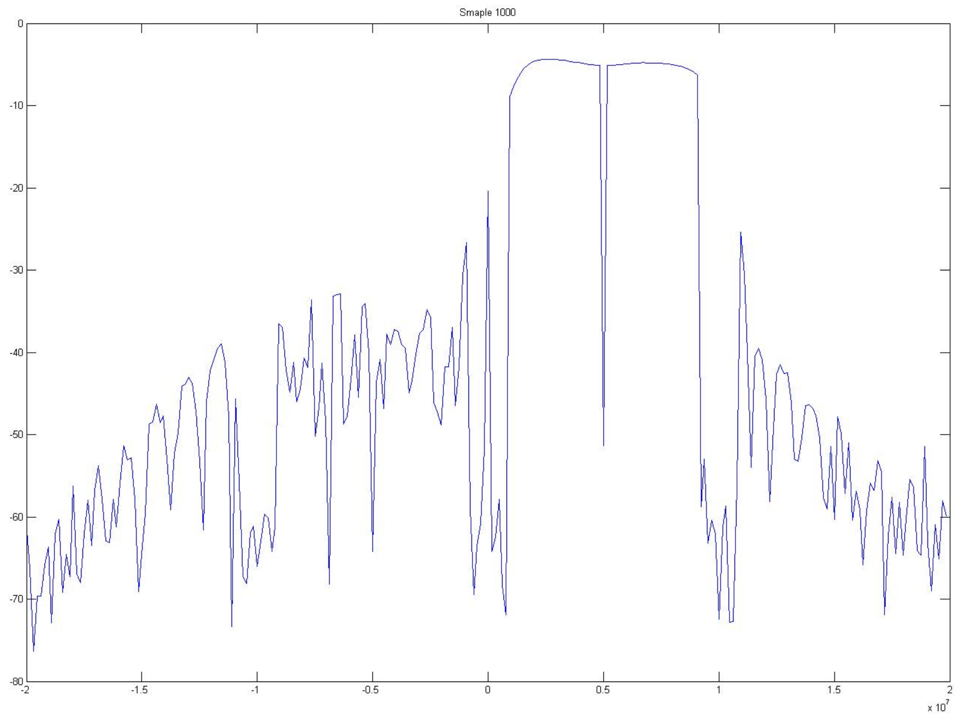

Figure 19: LTS Spectrum in Baseband chain (IF filter is enable)

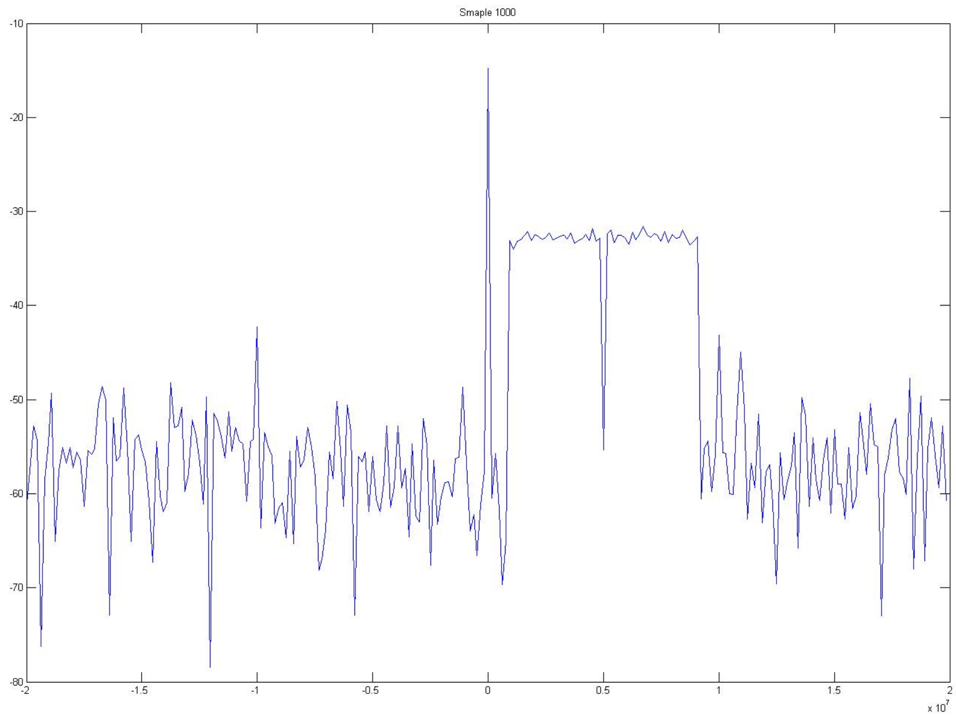

Figure 20: LTS Spectrum- passed RF chain (IF filter is enable)

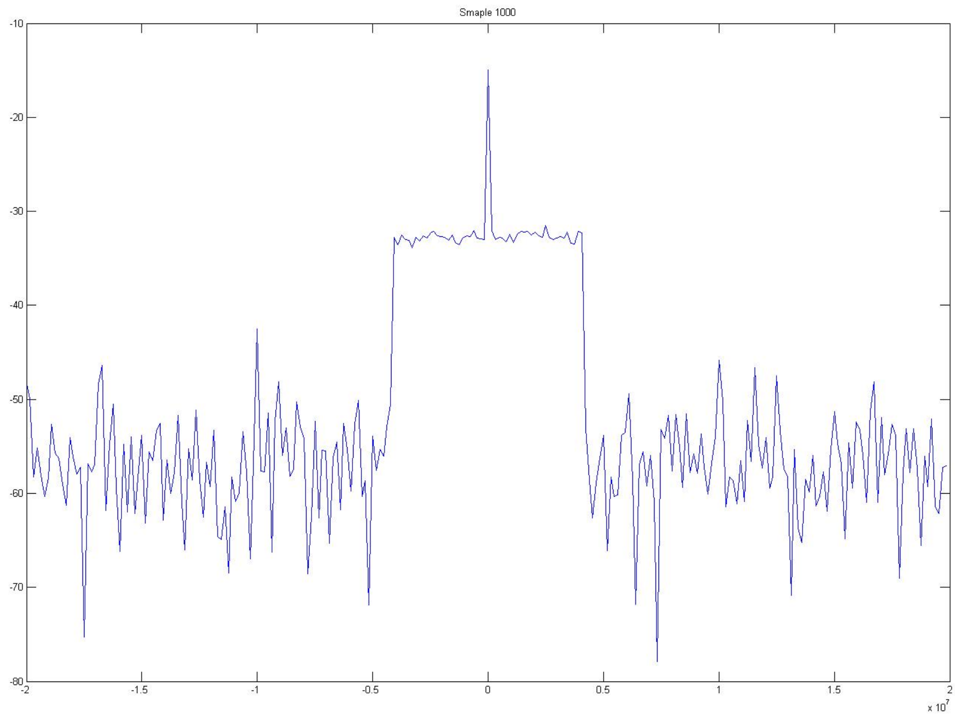

Figure 21: LTS Spectrum- passed RF chain (IF filter is disable)

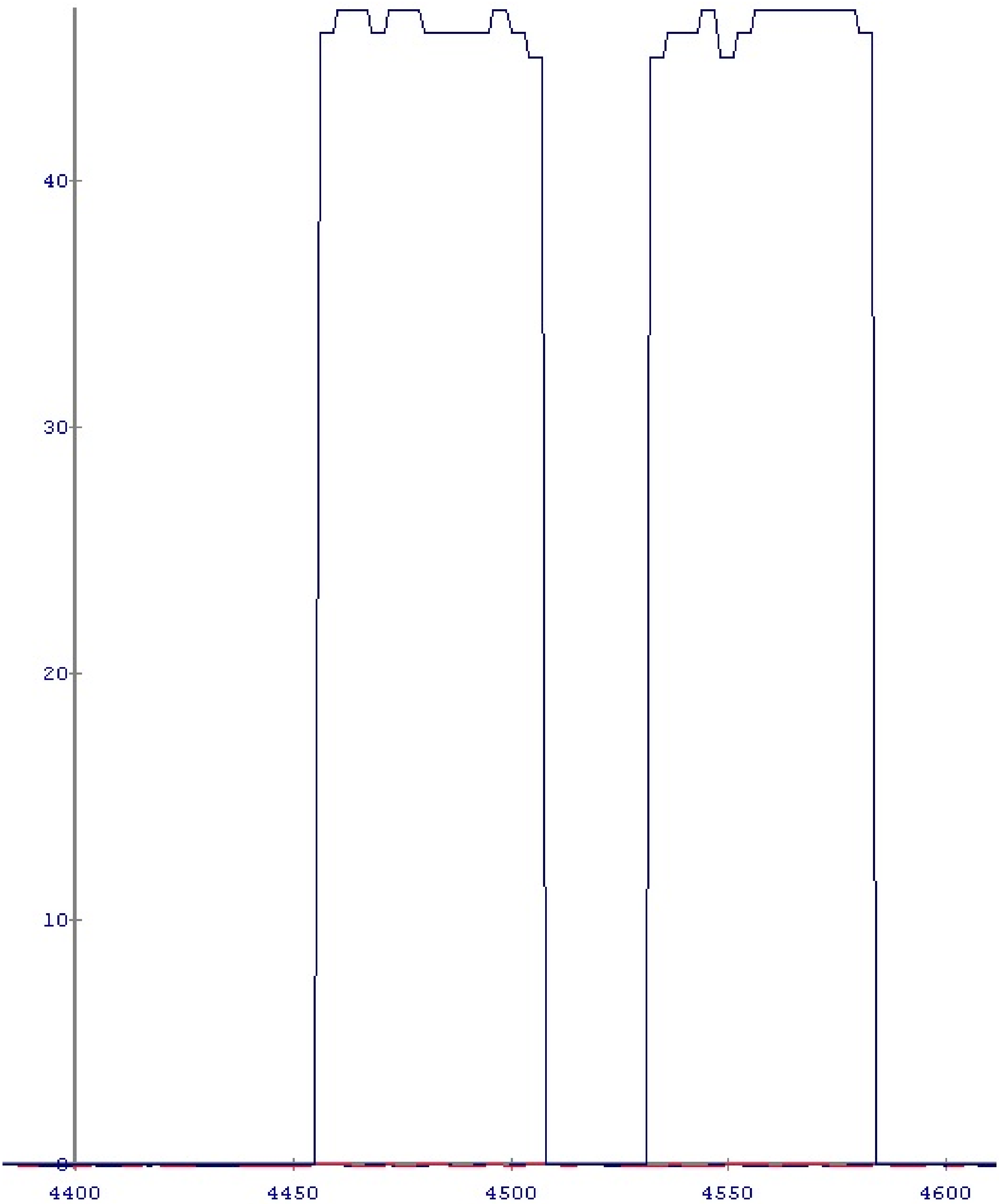

Figure 22: Frequency Response of a semi-perfect channel

Part IV. Conclusion and Future Works

An OFDM structure from modulator to demodulator is studied. The aim is to investigate the characteristics of the system in different conditions and comparing the behavior with the single carrier configuration. The simulation conditions change in the cyclic prefix size, a Non-Linear Amplifier (NLA), multipath and equalizer activation.
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19. System Analysis by Simulation