Design and Implementation of OFDM System on FPGA

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Outline

What is OFDM?

- Orthogonal Frequency Division Multiplexing is a modulation format that is being used for many of the latest wireless and telecommunications standards.
- OFDM is a form of multicarrier modulation. An OFDM signal consists of a number of closely spaced modulated carriers.
- Any non-linearity in receiving system will cause interference between the carriers as a result of inter-modulation distortion.

OFDM Characteristics

OFDM advantages:

- Immunity to selective fading
- Resilience to interference
- Spectrum efficiency
- Resilient to ISI
- Resilient to narrow-band effects
- Simpler channel equalisation

OFDM disadvantages:

- High peak to average power ratio
- Sensitive to carrier offset and drift

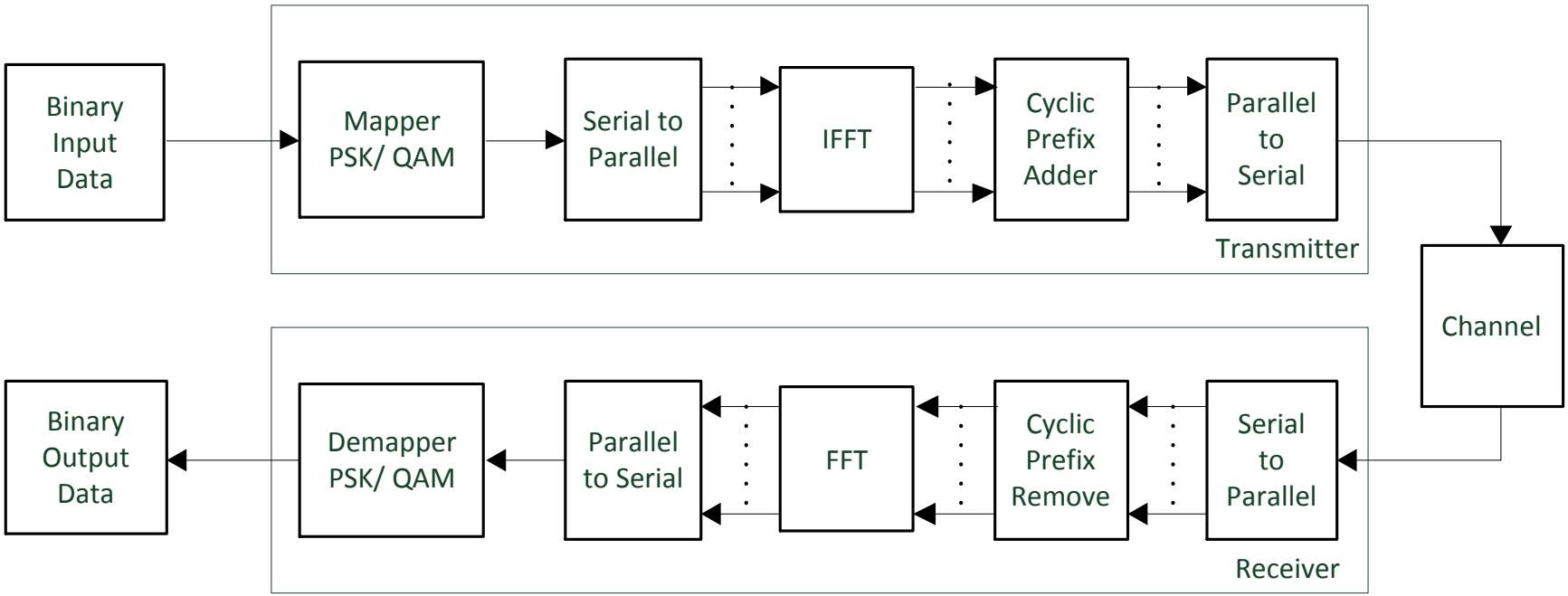
Thesis Goals

Motivation

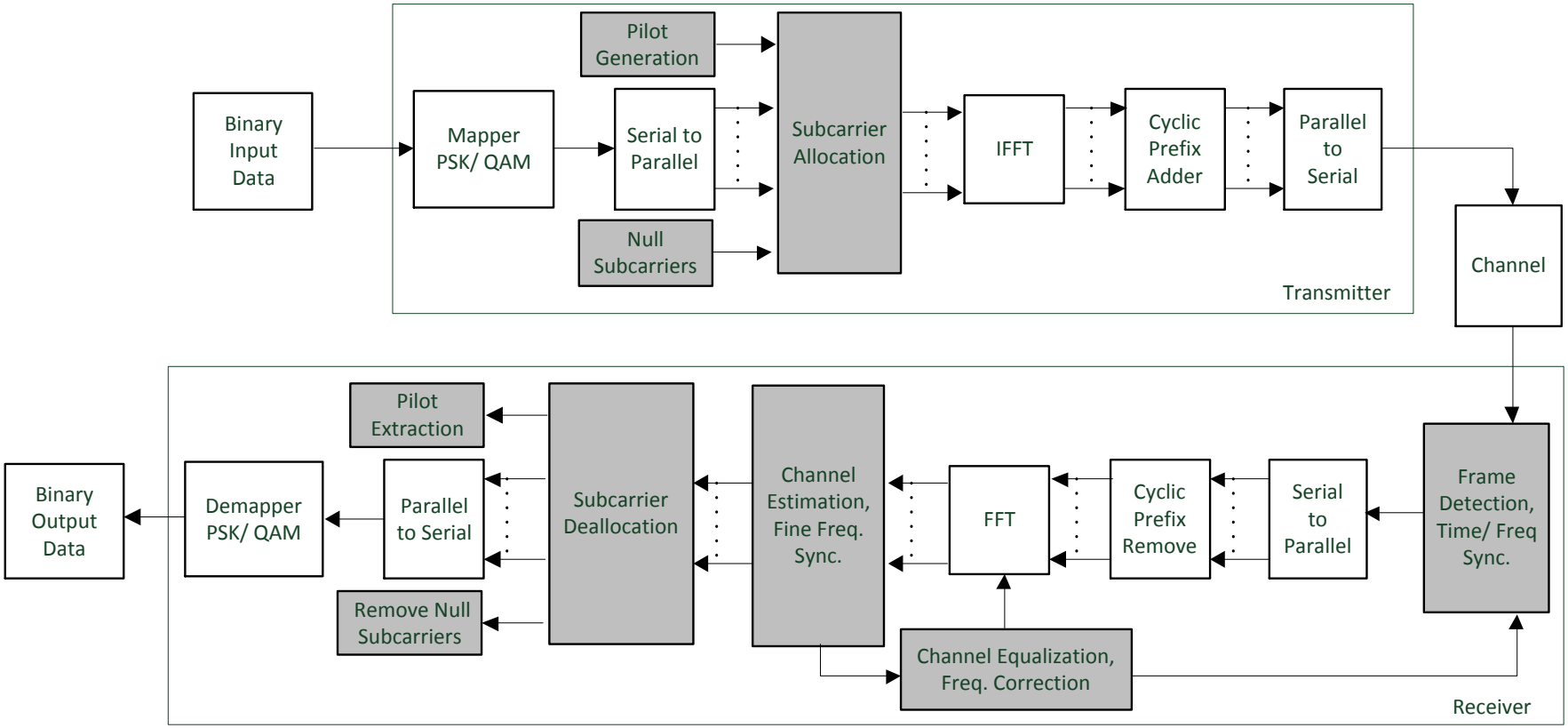
- Innovation in telecommunication concepts (Full-duplex communication, coding, etc); a standard platform is mandatory
- Implement a basic OFDM architecture (IEEE 802.11a) receiver/ transmitter in the logic side
- Processor side (peripherals, memories, connection to the logic, etc)
- Bridge between the logic and processor (BRAM, AXI bus, DMA, etc)
- A evaluation board for RF side should be selected and initialize in software (power amplifiers, clock chains, ADC/ DAC)
- A correct methodology to test all the system elements together should be chosen

Outline

Basic baseband OFDM system



Architecture of an OFDM system



Basic Parameters

- Delay spread expected for the channel ($300ns$)
- Guard duration ($800ns$) which describes symbol duration ($4.0\mu s$)
- Available bandwidth
- Data rate
- Number of Subcarriers 64 in 20 MHz
- Roll-off factor β= 0.02

System parameters defined for the proposed design

Parameter	Description	Value
B_w	Available channel bandwidth	$20MHz$
σ_τ	Delay spread of the channel	$< 300ns$
T_g	Guard interval duration (Cyclic Prefix)	$0.8\mu s$
T_{sym}	OFDM symbol period	4.0μ
T	Effective symbol duration (FFT period)	$3.2\mu s(= T_g - T_{sym})$
Δf	Subcarrier spacing	$312.5kHz(= 1/T)$
N_g	Number of guard samples	16
N	FFT size	$64 = B/\Delta fs$
N_d	Number of data subcarriers	48
N_p	Number of pilot sucarriers	4
N_u	Number of used subcarriers	52
B_u	Signal occupied bandwidth	$16.6MHz$
R_b	Data rate without coding	$12Mbps, 24Mbps$

Bit Error Rate

Theoretical equation of the BER for a QPSK:

$$P_b(e) = \frac{1}{2} erfc(\sqrt{\frac{E_b}{N_0}}) \tag{1}$$

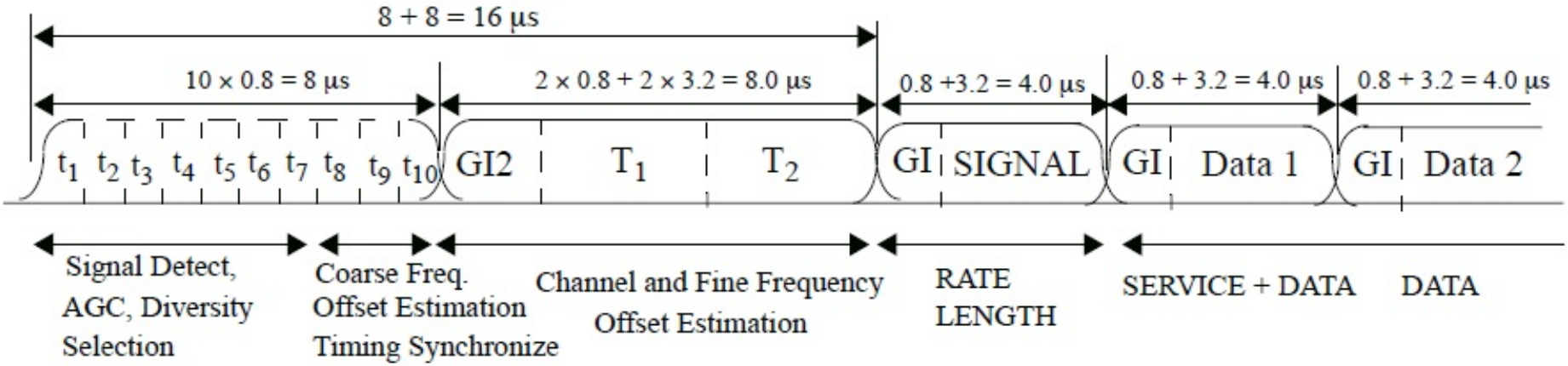
Non-ideality :

$$P_b(e) = \frac{1}{2} erfc(\sqrt{\frac{E_b}{N_0} \frac{T}{T + T_g} \frac{N_u}{N_u + N_p}}) \tag{2}$$

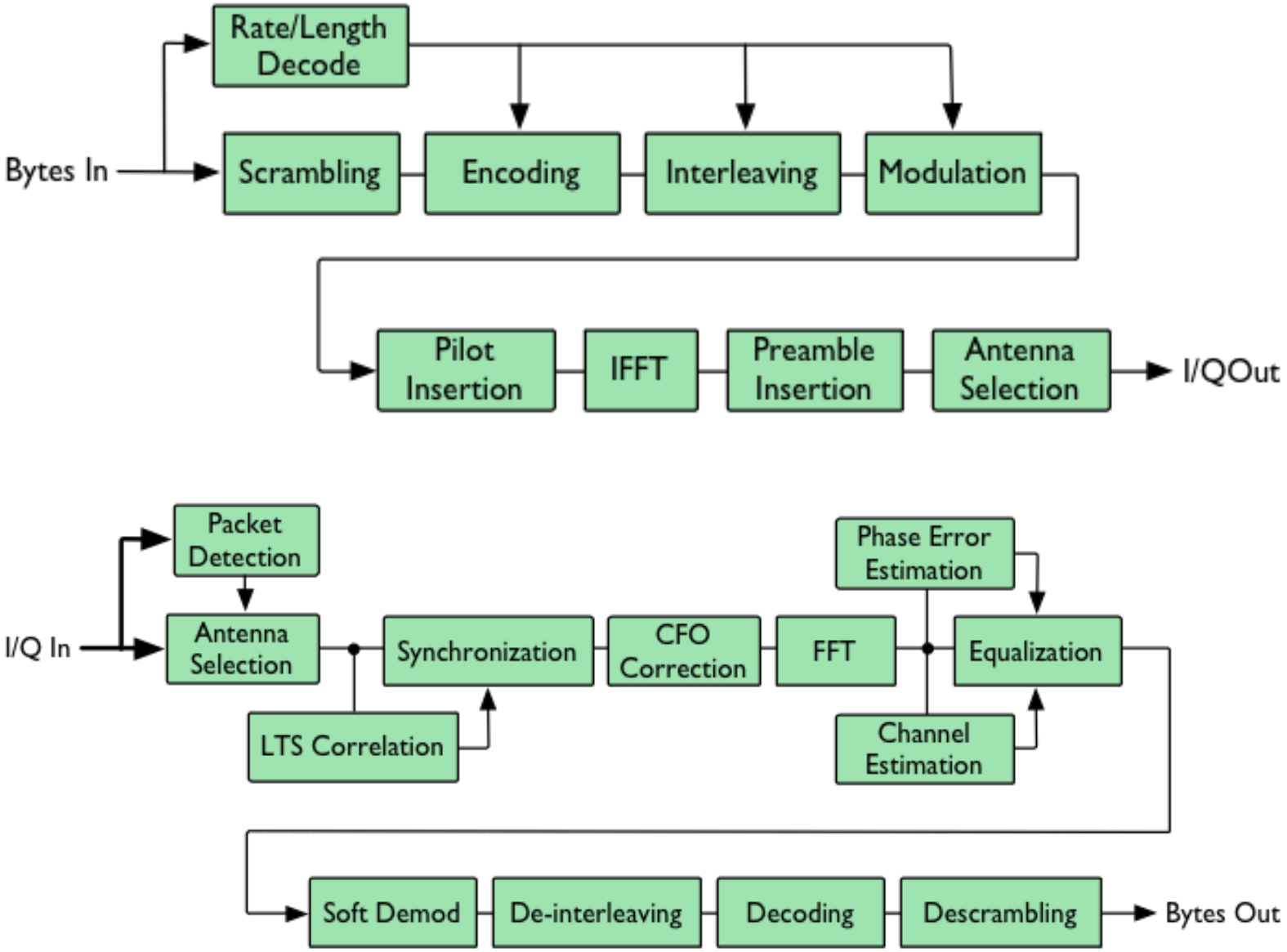
Replacement:

$$P_b(e) = \frac{1}{2} erfc(\sqrt{\frac{E_b}{N_0} 0.65}) \tag{3}$$

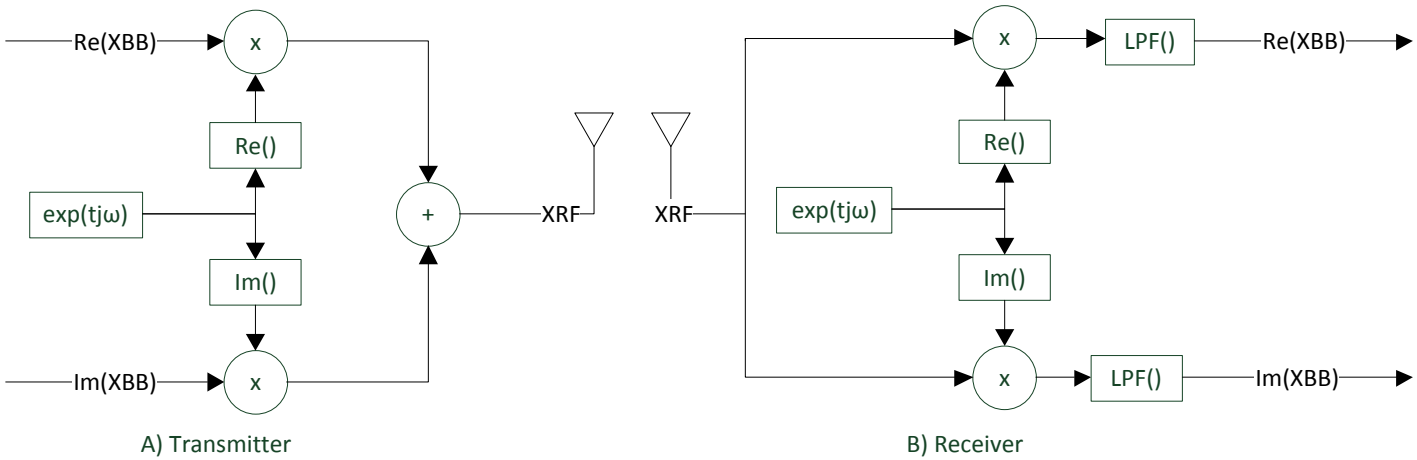
Preamble of IEEE 802.11



Design Block Diagram of OFDM PHY

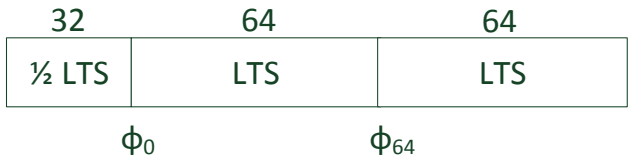


General models of a direct conversion RF



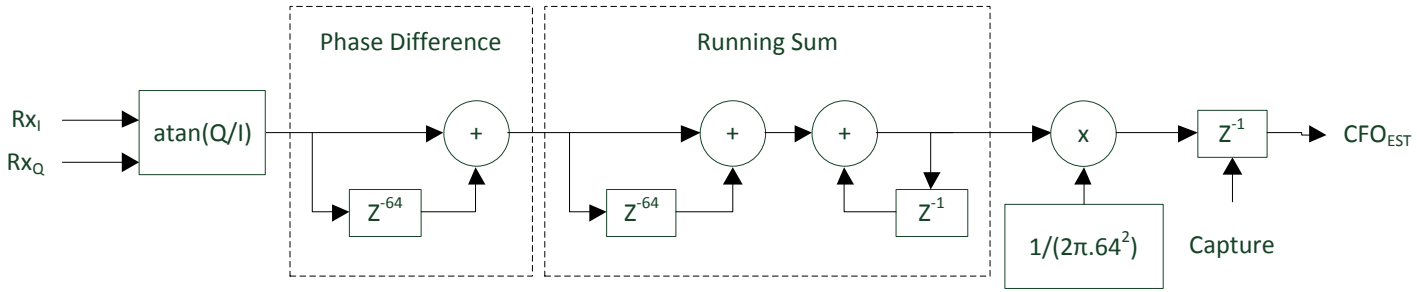
- Phase offset across subcarriers in an symbol which can be estimated by pilot tones and corrected in frequency domain
- Degradation of orthogonality between subcarriers in receiver's FFT which causes inter-carrier interference (ICI)

OFDM performance loss due to CFO-induced ICI



$$CFO \approx (\phi_{64} - \phi_0)$$

$$CFO_{EST} = \frac{f_s}{2\pi.64^2} \sum_{n=64}^{127} \phi_n - \phi_{(n-64)} \tag{4}$$



Synchronization

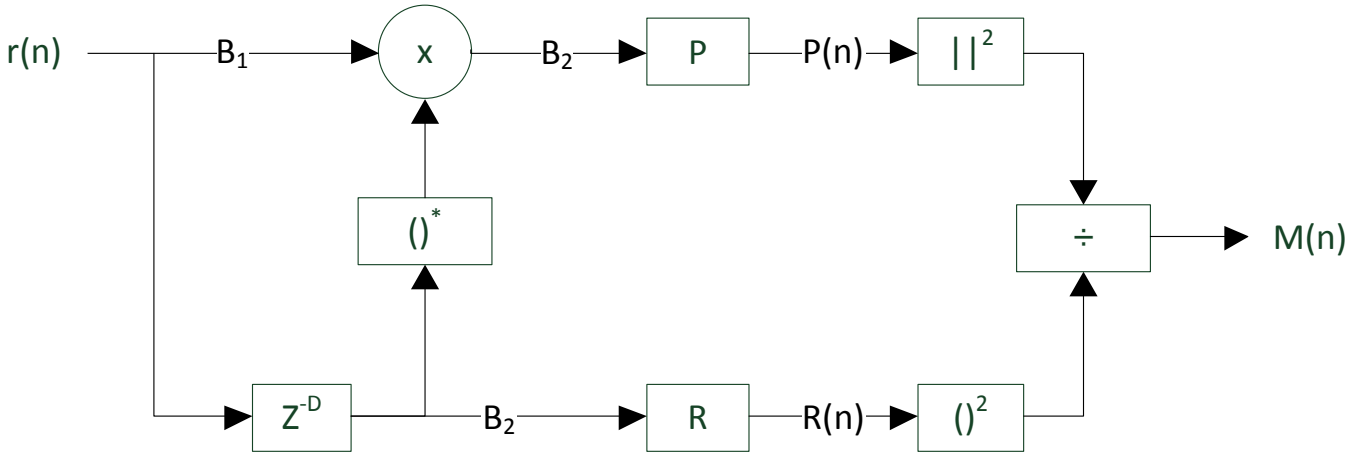
Cross-Correlation

$$P(n) = \sum_{m=0}^{L-1} r_{n+m} r^*_{n+m+D} \tag{5}$$

Auto-Correlation

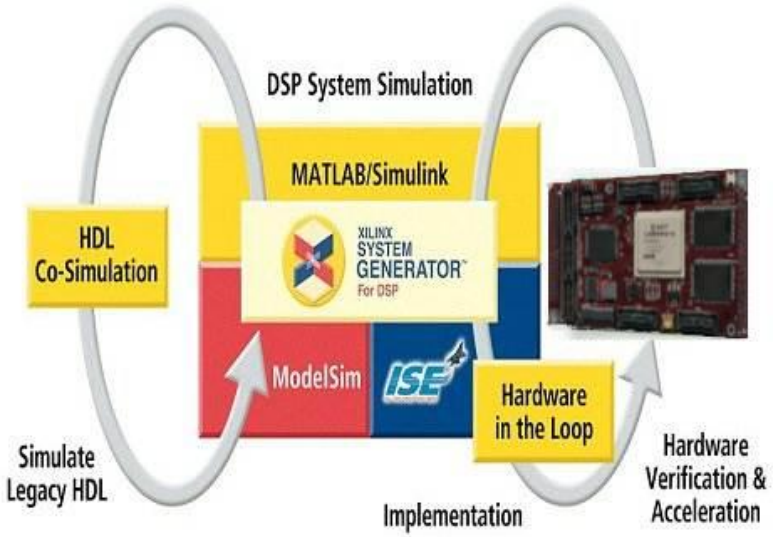
$$R(n) = \sum_{m=0}^{L-1} r_{n+m+D} r^*_{n+m+D} \tag{6}$$

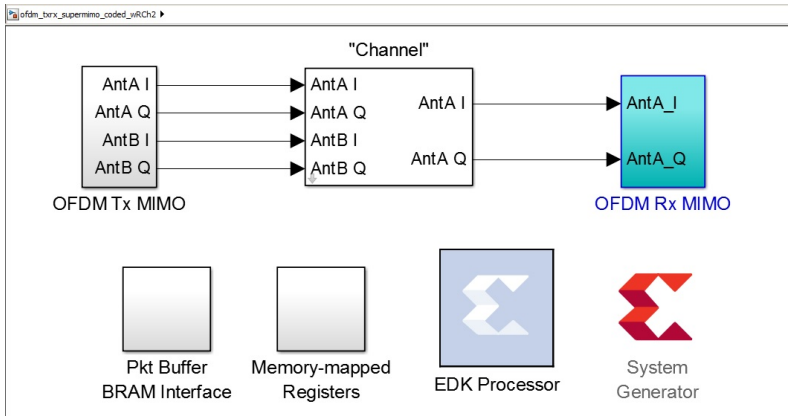
Schimdl and Cox Delay and Correlate Algorithm



Outline

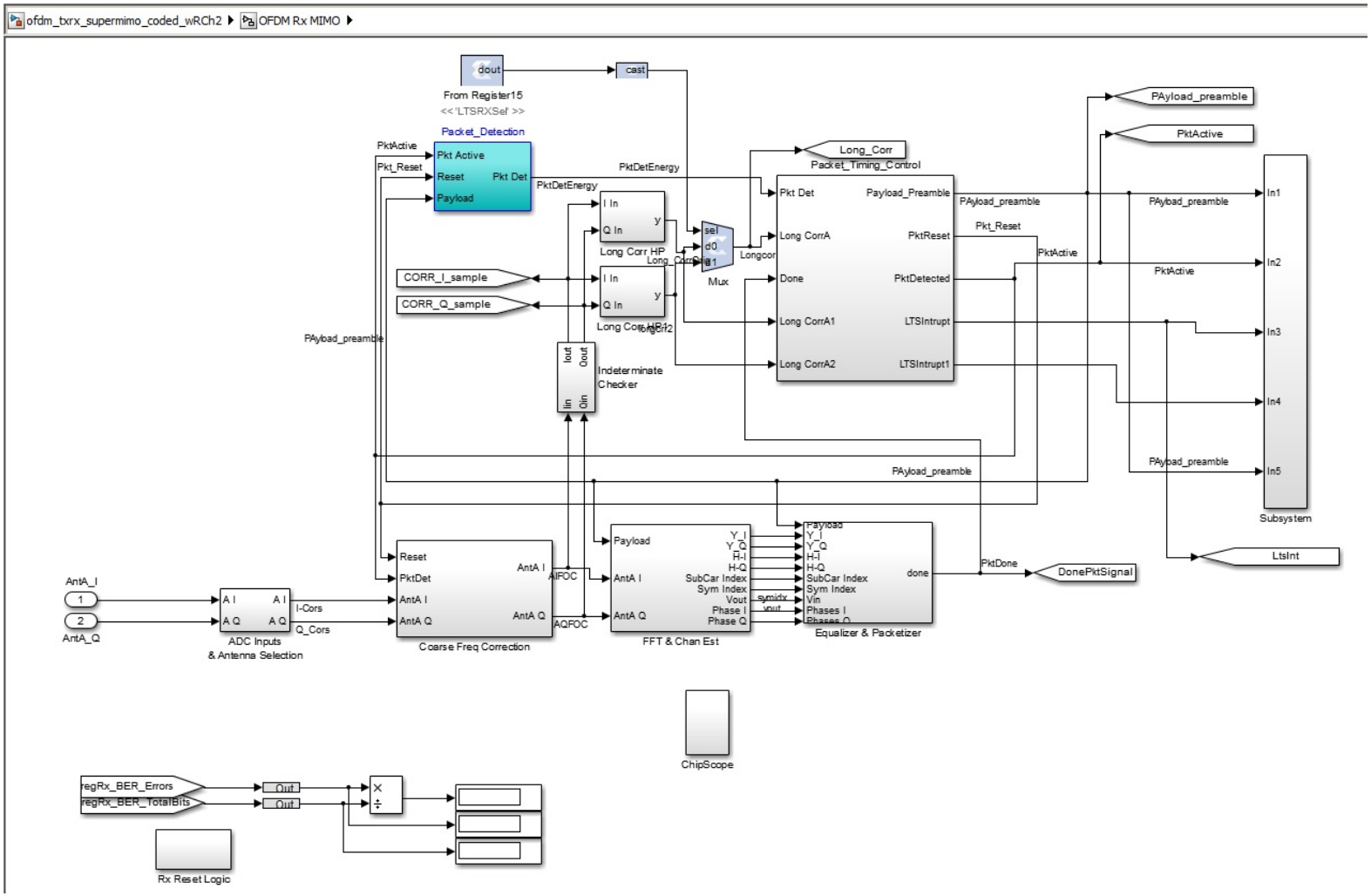
System Generator Cycle





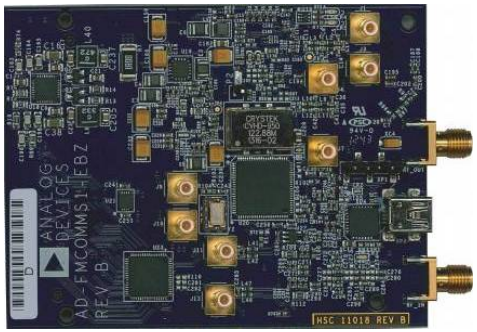
System Generator Sample

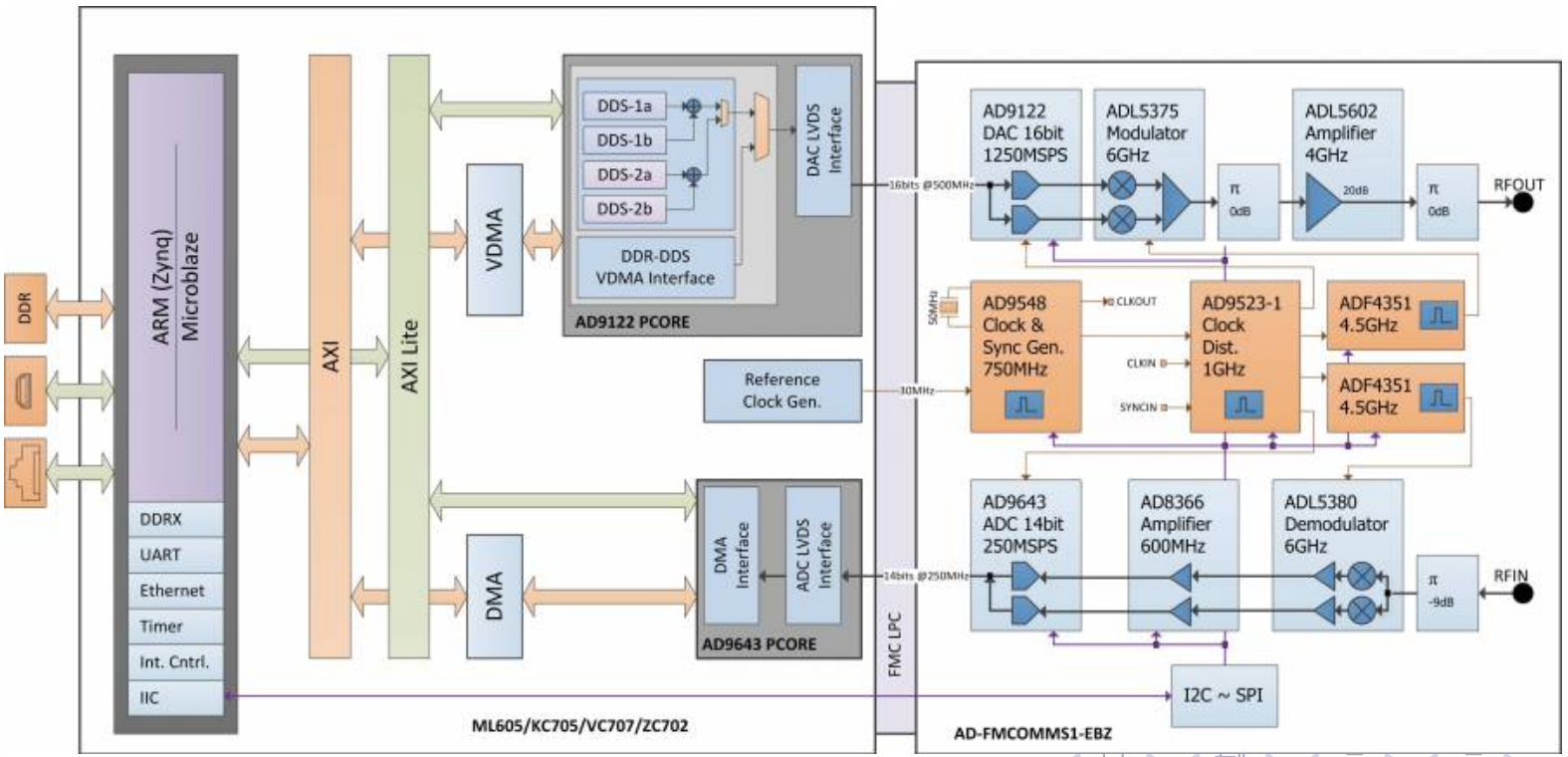
OFDM Receiver Block



Radio Board

AD-FMCOMMS1-EBZ





Board Elements

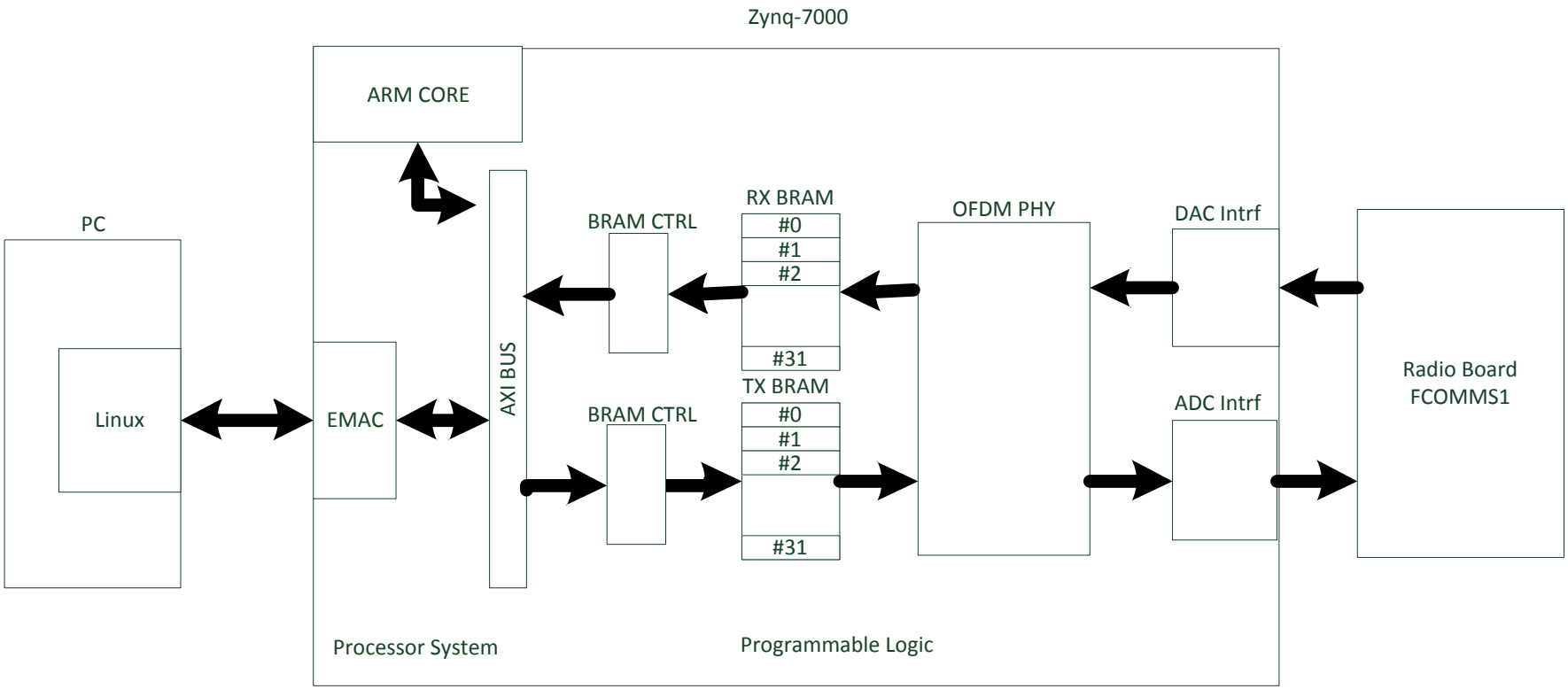
- Clock chain is re-programmed based on our necessities in the FPGA architecture design
- Clock synchronization blocks are studied to be in our design margin
- Non-linearity caused by the modems, amplifiers and ADC/DAC are studied

OFDM on FPGA?

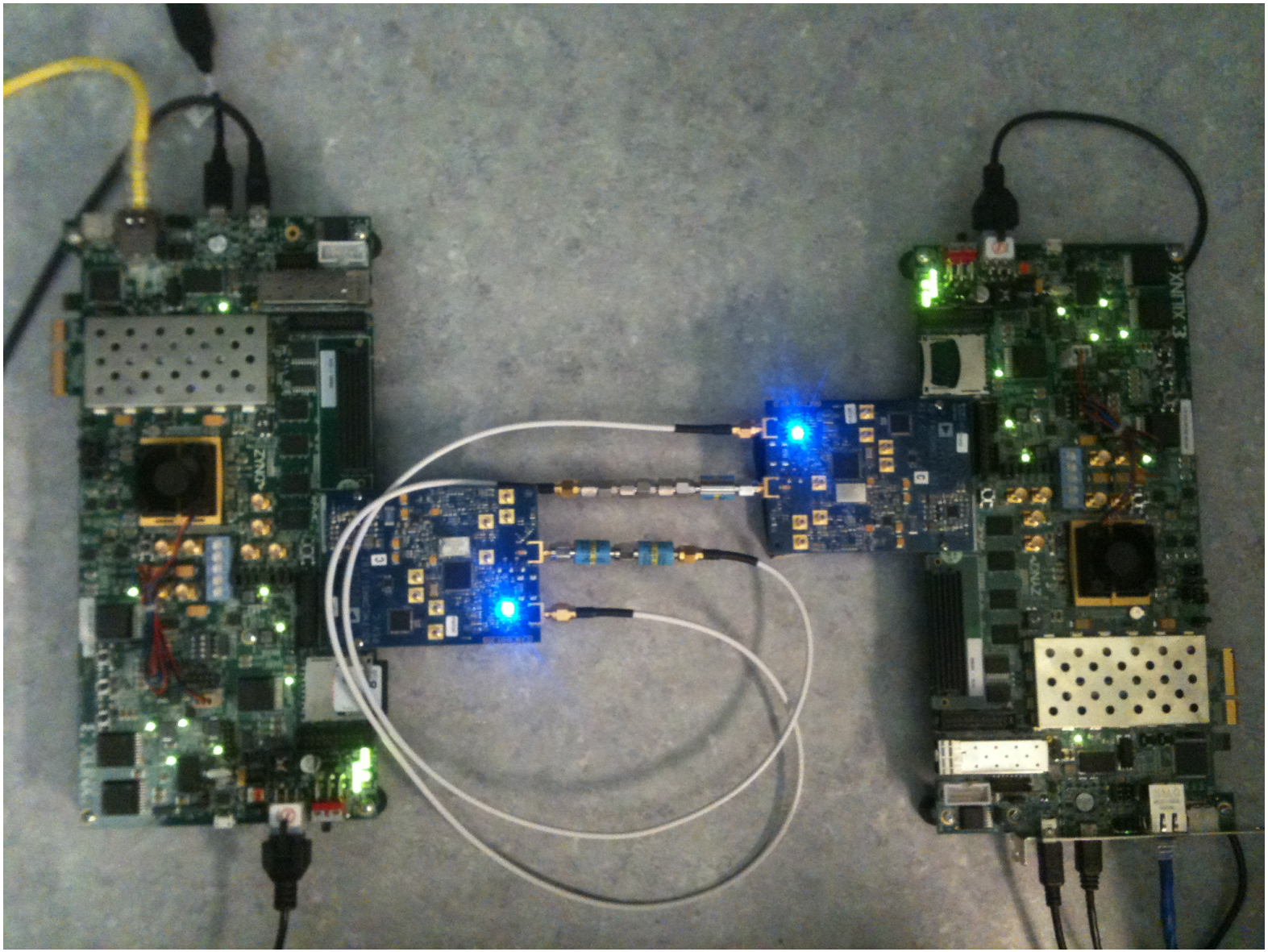
- Flexibility, re-configurable
- Parallel processing
- Re-use of the processing units (FFT, filters, etc)
- Triangle operations are not easy to implement!
- A processor on standard communication ports (UART, I2C, Ethernet)
- Reliable bridge between logic side and processor side

Design Block Diagram

Full Design with Processor

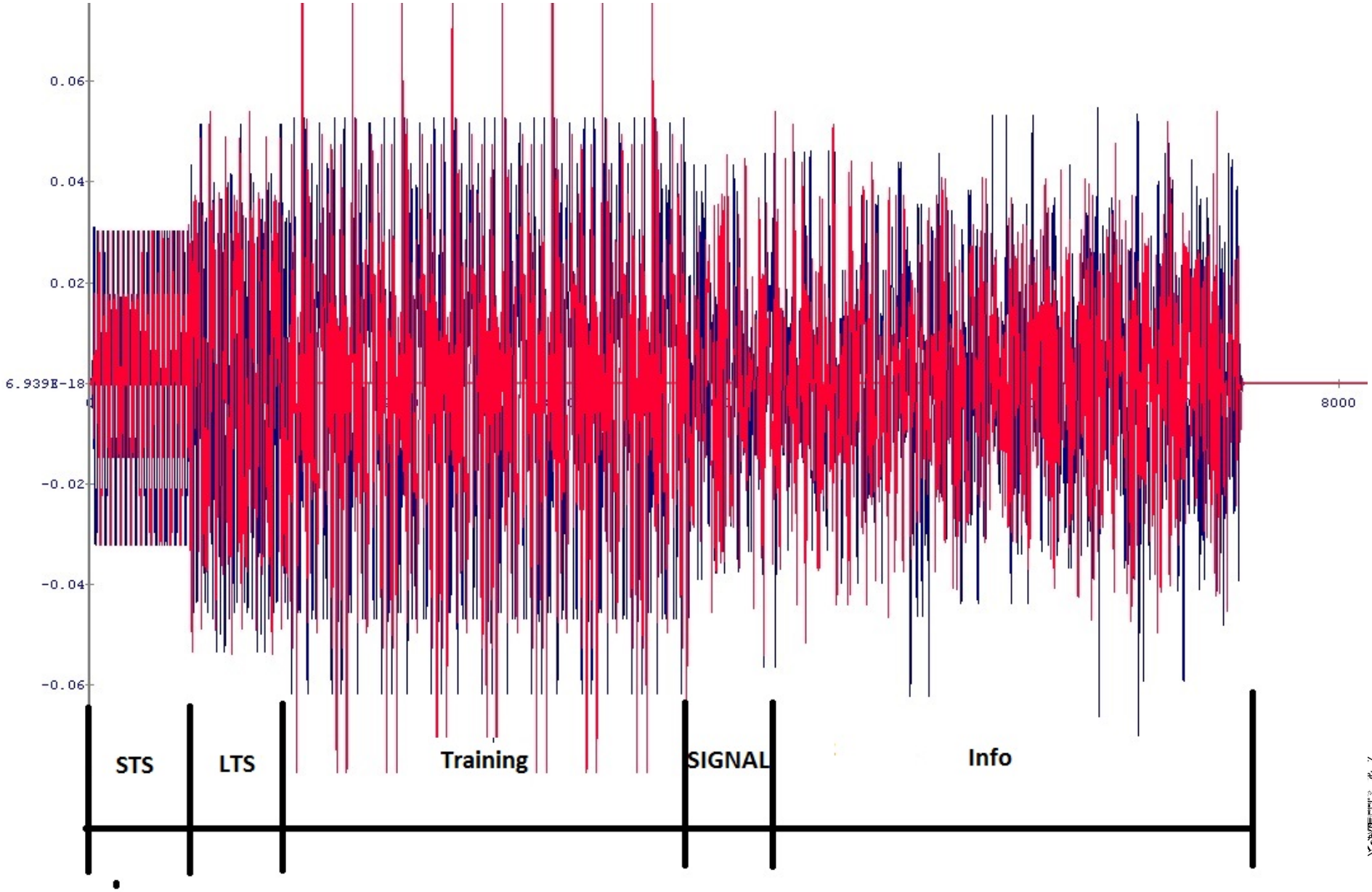


Hardware set-up



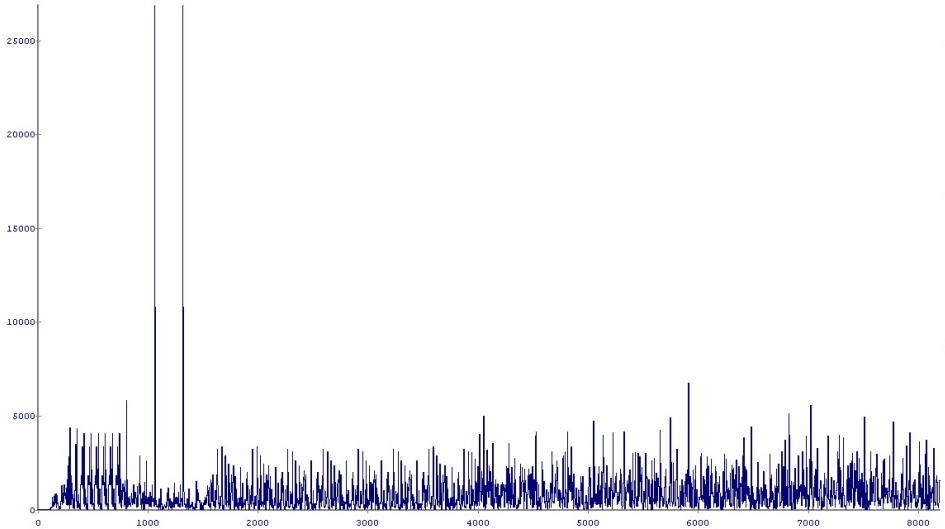
Outline

OFDM Frame (I/Q) detected in Chipscope

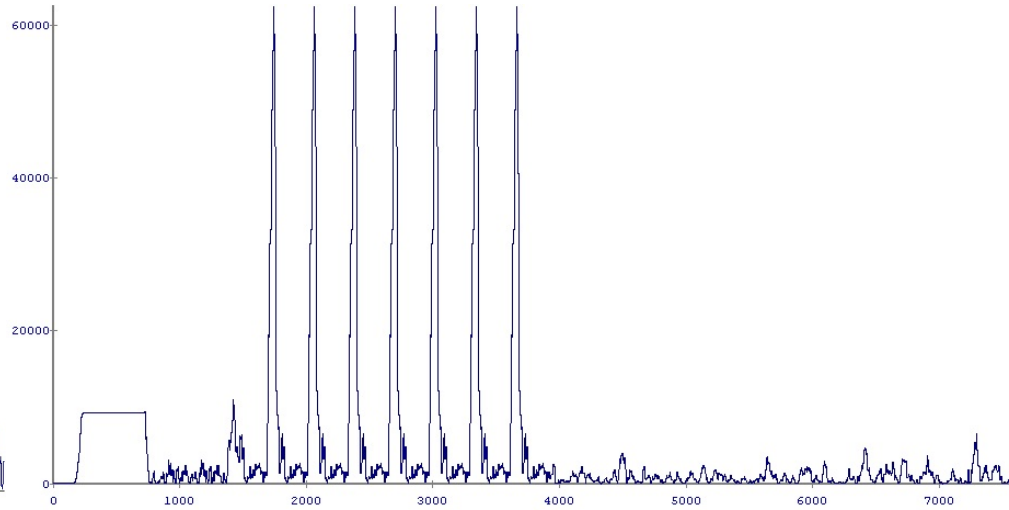


Chipscope samples

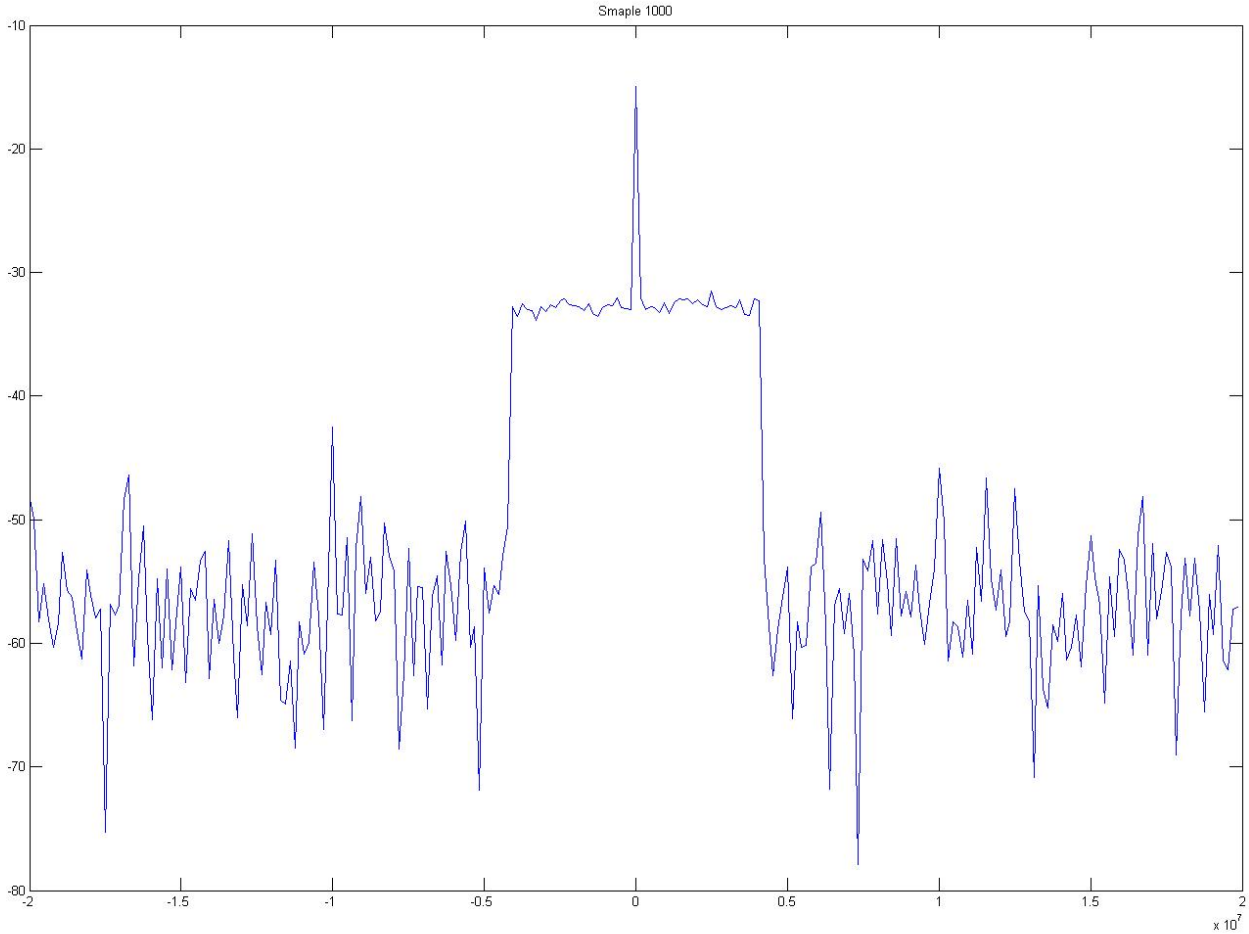
Cross Correlation on LTS



Auto Correlation on STS



LTS Spectrum- passed RF chain



Device Utilization Summary

XC7Z045-22FFG900C

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	42,703	437,200	9%
Number of Slice LUTs	59,787	218,600	27%
Number used as Memory	5,384	70,400	7%
Number of occupied Slices	21,749	54,650	39%
Number of DSP48E1s	149	900	16%

Summary

- The OFDM system is prototyped based on IEEE 802.11a standard and transmits/receives signals on a 20 MHz bandwidth (throughput of 24 Mbps).
- System Generator is not optimized. There are low-level techniques to manage the power, speed and area.

Thanks for your attention.