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Corso di Laurea in Electronic and Telecommunication Engineering

Tesi di Laurea

Design and Implementation of OFDM System on FPGA



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Summary

Acknowledgements

The orthogonal frequency division multiplexing (OFDM) technology provides a high transmission data rate in wireless and mobile communications where multipath fading is a severe issue in degradation of the quality. Managing feasible coherent bandwidth to overcome Inter-Symbol Interference, OFDM enhances communication performance at a relatively small bandwidth cost. The improvement can be reached by interactive proper channel estimation and compensation which needs synchronization of transmitter and receiver. A *Discrete Fourier Transform* (DFT) algorithm-based configuration simplified the digital implementation of OFDM system on field programmable gate array (FPGA) as a highly flexible solution, which provide prominent performance.

In this thesis, steps to design a base-band OFDM system with channel estimation and timing synchronization upto implemented on FPGA are studied. It is a prototype based on the *IEEE 802.11a* standard and the signals is transmitted and received using a bandwidth of 20 MHz. Focusing on the quadrature phase shift keying (QPSK) modulation, the system can achieve a throughput of $24Mbps$. For the coarse estimation of timing, a modified maximum-normalized correlation (MNC) scheme is investigated and implemented. Starting from theoretical study, this thesis in detail describes the system design and verification on the basis of both MATLAB simulation and hardware implementation. Bit error rate (BER) verses bit energy to noise spectral density (E_b/N_0) is presented in the case of different channels. In the meanwhile, comparison is made between the simulation and implementation results, which verifies system performance from the system level to the register transfer level (RTL).

First of all, the entire system is modeled in MATLAB and a floating-point model is established. Then, the fixed-point model is created with the help of Xilinxâs System Generator for DSP (XSG) and Simulink. Subsequently, the system is synthesized and implemented within Xilinxâs Integrated Software Environment (ISE) tools and targeted to Xilinx Zynq board. What is more, a hardware co-simulation is devised to reduce the processing time while calculating the BER for the fixed-point model. Some time-based standards on IEEE 802.11a are discussed and optimum implementation of on FPGA, for instance Cross-Correlation and algebraic machine, will be

introduced. Besides, we will demonstrate an engineering steps for choosing the radio board and the processor software implementations.

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Part I

Introduction

0.1 Background

High quality of services (QoS) and reaching to high data rate communication to overcome the necessities in multimedia services, telecommunications industry is working currently toward the forth generation (4G) wireless communication systems. The orthogonal frequency division multiplexing (OFDM), is the most promising technology to meet the requirement as a mechanism in rapid development of digital signal processing techniques.

The first introduction of OFDM dated back 1960s as a parallel data transmitting scheme. There are many realization proposals although the foundations are fixed generally. The basic idea is to divide a single high rate data stream into a number of lower-rate data streams. Each of these data streams is modulated on a specific carrier, which is called subcarrier, and transmitted simultaneously. Robustness will be preserve against multipath fading effect. Moreover, spectrum efficiency is enhanced in comparison to conventional multi-carrier transmission. OFDM considered as a frequency division multiplexing (FDM) where the data stream carried by each subcarrier separated.

Traditional methods used in single-carrier modulation require a number of sinusoidal subcarrier oscillators in the modulator side and multipliers and correlators in the demodulator. Introduction of Discrete Fourier Transform (DFT) until 1971 made a revolution in the complexity development. The DFT block simplified the two side processes and helped to implement the baseband in the digital manner. Since 1990s, OFDM has been employed in wideband data transmission. Applications of OFDM technology include asymmetric digital subscriber line (ADSL), high-bit-rate digital subscriber line (HDSL), and very-high-speed digital subscriber line (VDSL) in wired systems, and digital audio broadcasting (DAB), digital video broadcasting (DVB) in wireless systems. Furthermore, it has also been recognized as the basis of the wireless local area network (WLAN) standards, among which the IEEE 802.11a standard is one of the most important ones.

Two main topics in wireless and mobile communications are high data rate and high QoS, which cause communication systems be adaptive to fast varying channel conditions and providing a steady environment to various kinds of users at a high speed of data transmission.

Due to its capabilities of providing high data rate and less sensitivity to fast channel fading, OFDM technology, in combination with other powerful techniques such as the multiple-input, multiple-output (MIMO) technique, has been the mainstream of wireless and mobile networks. It has been used in various applications,

such as wireless fidelity (Wi-Fi), worldwide inter-operability for microwave access (WiMAX), and the third generation partnership project (3GPP) long term evolution (LTE).

Recent development of digital integrated circuits, the high flexibility and low complexity of digital implementation of OFDM modem has accelerated its application. In competition of the technologies, field programmable gate array (FPGA) has attracted the most attention in recent years due to its superior performance and high flexibility. As a flexible general-purpose technology, FPGA is an array of gates that can be reconfigured by the designer as a versatile design platform. It is developed based on the programmable logic devices (PLDs) and the logic cell array (LCA) concept. By providing a two-dimensional array of configurable logic blocks (CLBs) and programming the interconnection that connects the configurable resources, FPGA can implement a wide range of arithmetic and logic functions. Compared to other popular IC technologies such as application specific integrated circuits (ASICs) and digital signal processors (DSPs), FPGA has the following advantages:

Performance: Inherently parallel architecture, FPGA has the ability to overcome the speed limit of sequential execution technologies and is able to process data at a much higher speed than DSP processors and whose performance is estimated by the system clock rate. Therefore, it can achieve much higher performance in various applications that requires large arithmetic resources, such as OFDM. However, DSP processors are still developing as an alternative.

Reliability: The high isolation and high parallelism mechanism not only minimize the reliability concerns, but also reduce the deterministic hardware dedicated to every task. Besides, there are mechanism in testing and verification of the system dynamically which are developing exponentially.

Cost: Because of its re-programmable nature, FPGA is a cost-effective solution for system development although the purchase cost are normally more than DSP processors which the architecture is fixed. It can be easily customized and reconfigured so that effectively versatile functionality can be realized using FPGA and there is no need to kick off design for each application. Normally, the products are tested and design and implement on the FPGA initially and after successful output it worth to transfer design into ASIC for mass production.

Flexibility: The most prominent functionality of FPGA is that the design can be changed rapidly in the prototype process. Recently, some other options like partial reconfiguration let the designer to look for more dynamic mechanisms. This let the manufacturers to have better performance in the time to market issues.

There is also some trends like IP core programs which help the big short-cuts in the designs but it very depends on the initial cost which should be decided very carefully.

0.2 Motivation

Practically, the signal is attenuated and distorted by multipath effect in real channel transmission. Fading estimation and equalization of the channel in wireless technology is inevitable to have a reliable communication. Implementation an OFDM system on FPGA with capability of channel estimation and synchronization is the final goal of this thesis.

There are many techniques and mechanism to implement OFDM wireless communication on FPGA. In ... the authors helped OFDM transceiver on certain topics in the receiver design, such as the synchronization, packet detection, channel estimation and equalization. Moreover, OFDM transceivers are designed for the AWGN channel have been presented in However, there are not a comprehensive work presenting a complete development of OFDM system with channel estimation and synchronization using the FPGA technology.

A top-down approach and demonstrative system performance in baseband OFDM is done in this thesis. System synchronization will also be discussed in this thesis. In addition, we focus on the design and implementation of channel estimation and equalization, while a verification at system level is performed. The detailed objectives include:

- To design, model and implement after proper simulation a baseband OFDM system including both the transmitter and the receiver, and to analyze the system performance.
- To prototype an OFDM system based on a specific wireless communication standard.
- To implement the synchronization and channel estimation system for the receiver and provide system evaluation under different channel conditions.

0.3 Methodology

It is tried to explain the theoretical concepts firstly and then to show some facts in the simulation based on extracted models. Finally, the issues is examined on

hardware.

The hardware chosen is consisted a Zynq board which is an FPGA with two embedded ARM processors and the radio board which is FMCOMMS1.

0.4 Contribution

Part II

Theory, Design and Simulation

Abstract

The fundamental concepts of an OFDM design is described. A detailed block diagram is shown. A theoretical basic based band OFDM system is compared with IEEE 802.11 standard scheme. Influential parameters to are explained with guided us to have other parameters in Table

0.5 OFDM System Architecture

Generally, an OFDM signal is defined as a summation of many OFDM standard symbols, which can be considered continuous in the time domain. It can be defined as following:

$$s(t) = \sum_{k=-\infty}^{+\infty} s_k(t) \quad (1)$$

where $s_k(t)$ is the k -th OFDM symbol which starts at time $t = t_s$. An OFDM system is a multi-carrier transmission mechanism which the mathematical model is generalized by the summing a series of modulated subcarriers digitally. This modulation can be phase shift keying (PSK) or quadrature amplitude modulation (QAM) and transmitted in parallel. So, we can conclude:

$$s_k(t) = \begin{cases} Re \left(\sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1} d_{i+\frac{N}{2}} \exp[j2\pi(f_c - \frac{i+0.5}{T})(t - t_s)] \right), & t_s \leq t < t_s + T \\ 0, & \text{otherwise} \end{cases} \quad (2)$$

where T is the symbol duration, N is the number of subcarriers, f_c is the signal carrier frequency on the radio frequency (RF) band, and d_i is the complex value for PSK or QAM modulated symbol. We reach I_i and Q_i being the in-phase and quadrature part of d_i , respectively.

The complex envelope of an OFDM signal given by the following equation is used as the baseband notation:

$$s_k(t) = \begin{cases} Re \left(\sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1} d_{i+\frac{N}{2}} \exp[j2\pi \frac{i}{T}(t - t_s)] \right), & t_s \leq t < t_s + T \\ 0, & \text{otherwise} \end{cases} \quad (3)$$

The real and imaginary parts of

This represents an inverse DFT (IDFT) for PSK or QAM symbols.

Figure

In the next step zero channels are added in order to separate well subsequent OFDM symbols. For the simulation structure zero rows are added in the middle of the matrix. The following block interprets each symbol (complex number) of an OFDM symbol as a orthogonal frequency and converts each OFDM symbol per IFFT into a vector of time discrete values of the same length. As sixth step the

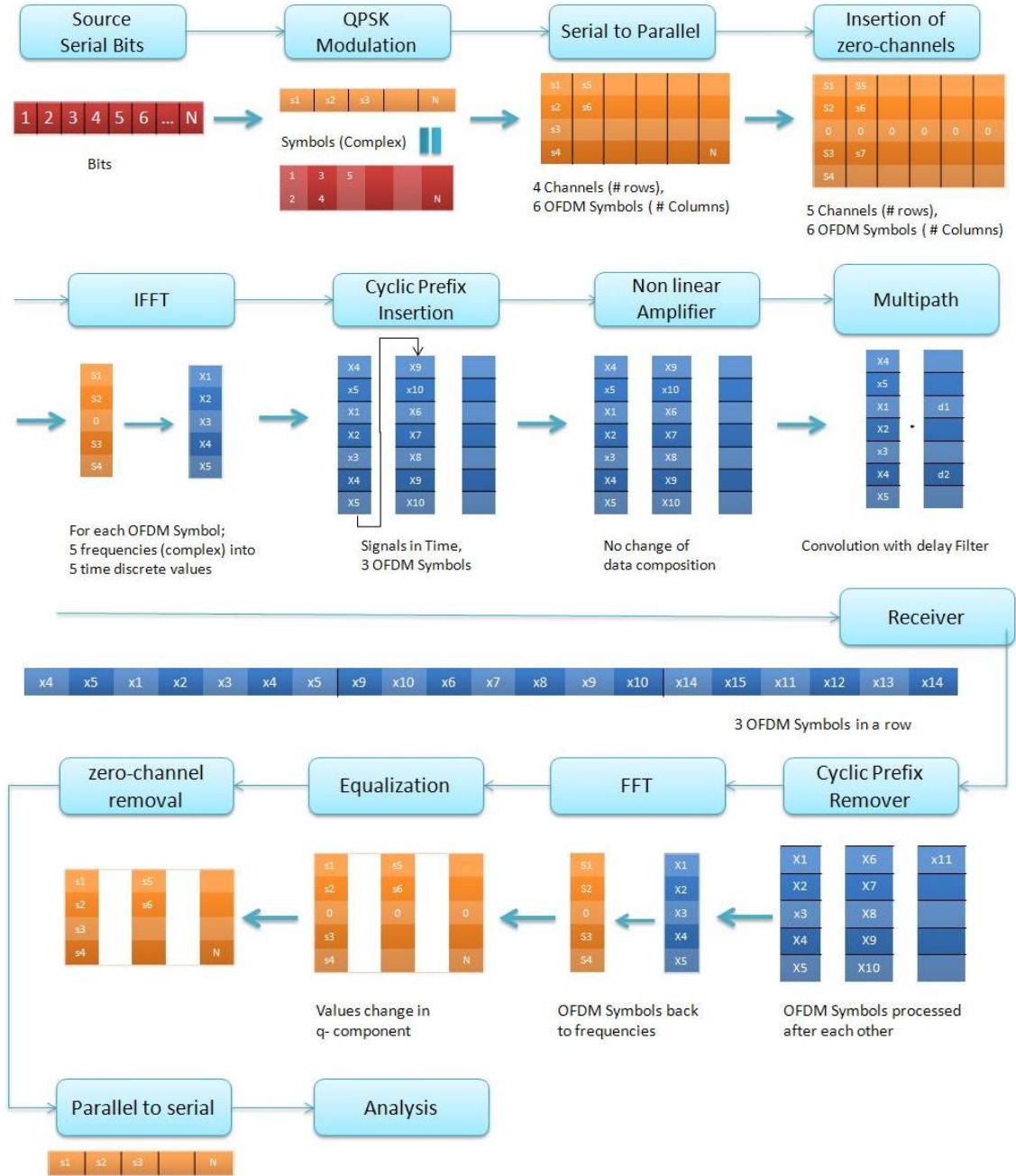


Figure 1. OFDM System Model

cyclic prefix insertion is done. In order to maintain orthogonality of the frequencies but prevent ISI, an amount of *guard values* are copied from the end of each OFDM symbol to its beginning. The number of rows in the simulation matrix grows by that by the number of *guard values*.

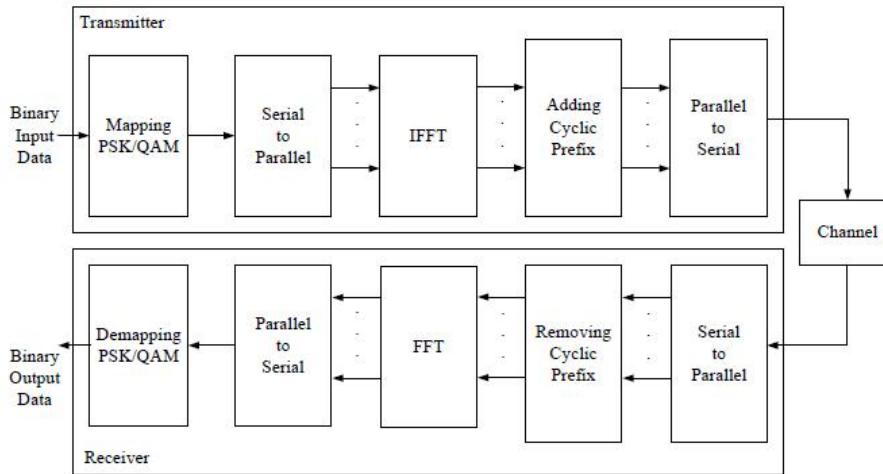
The following block is the NLA which depends on the optimization parameter β (back-off). At this point the transmitter side ends. In order to simulate the multipath a convolution is made on each OFDM symbol with the delay filter. Since the simulation is made on each OFDM symbol separated, this operation works with a memory in order simulate a serial transmission.

The receiver side is just the opposite of the transmitter. In the cyclic prefix remover the copied values are deleted and the simulation matrix size decreases. The next block performs the FFT on each OFDM symbol which reconstructs the as frequencies interpreted complex numbers.

The following equalization block tries to remove the effect of the multipath. For the simulation a multiplication with the inverted transfer function of the multipath is operated. By this, only the phase of the complex symbols changes.

Finally, the zero channels are removed and the matrix structure is reconverted to a series of symbols. The following analysis is done on the received symbols and consequently they are not demodulated into a bit-stream.

According to the above analysis, the basic architecture for a baseband OFDM system that contains the essential parts is shown in Figure



baseband OFDM system

figureBasic

In practice, to prevent sharp transactions at the sample time boundaries, a windowing block is used for filter shaping. In conclusion, spectrum utilization is enhanced dramatically. Therefore, the baseband OFDM symbol can be written as

below:

$$s_k(t) = \begin{cases} w(t - t_s) \sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1} d_{i+\frac{N}{2}} \exp[j2\pi\frac{i}{T}(t - t_s - Tg)], & t_s \leq t < t_s + (1 + \beta)T_{sym} \\ 0, & \text{otherwise} \end{cases} \quad (4)$$

where T_g is the guard interval duration, $T_{sym} = T + T_g$ is the OFDM symbol period, symbol starting time $t_s = kT_{sym}$, and $w(t - t_s)$ is the pulse shaping window, which is usually a raised cosine filter, and β is the roll-off factor.

The OFDM mechanism is used in 802.11 and Wimax standards. It has good tolerance against multipath and the receiver is easier to implement. We will see the details of implementations in practical systems.

0.6 OFDM Specifications in IEEE 802.11a Standard

0.6.1 Introduction of IEEE 802.11

The Institute of Electronic and Electrical Engineers (IEEE) has released IEEE 802.11 in June 1997. The standard defined physical and MAC layers of wireless local area networks (WLANs).

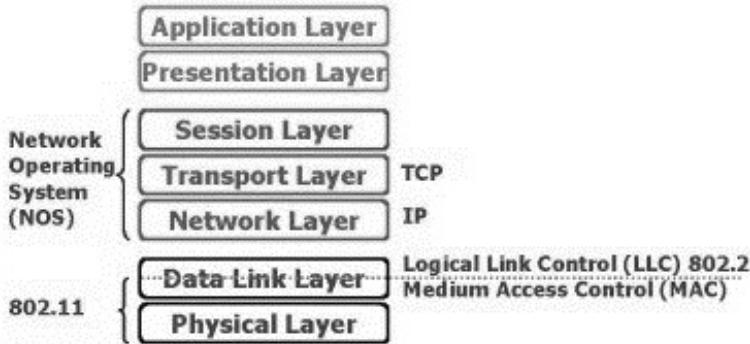
The physical layer of the original 802.11 standardized three wireless data exchange techniques:

- Infrared (IR);
- Frequency hopping spread spectrum (FHSS);
- Direct sequence spread spectrum (DSSS).

The 802.11 radio WLANs operate in the $2.4GHz$ (2.4 to $2.483GHz$) unlicensed Radio Frequency (RF) band. The maximum isotropic transmission power in this band allowed by FCC in US is $1Wt$, but 802.11 devices are usually limited to the $100mWt$ value.

The physical layer in 802.11 is split into Physical Layer Convergence Protocol (PLCP) and the Physical Medium Dependent (PMD) sub layers. The PLCP prepares/parses data units transmitted/received using various 802.11 media access techniques. The PMD performs the data transmission/reception and modulation/demodulation directly accessing air under the guidance of the PLCP. The 802.11 MAC

layer to the great extend is affected by the nature of the media. For example, it implements a relatively complex for the second layer fragmentation of PDUs.



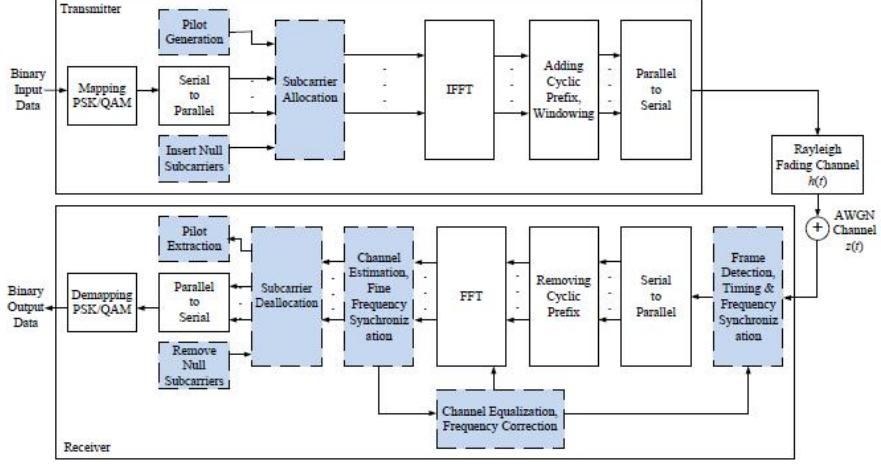
figureOSI Reference

Model.

0.6.2 System Design

In reality, having an anti-aliasing configuration, oversampling is performed before passing the digital signal to digital-to-analog converter. There are many other blocks in standards like channel coding, symbol interleaving and channel estimation.

In comparison to the fundamental architecture shown in Figure 000, some other building blocks are added in a practical IEEE 802.11 design shown in Fig 00, marked with blue and dashed on line. At the transmitter, several "null" subcarriers or tones are reserved besides of the data subcarriers in order to perform oversampling of the transmitted signal. In this context, "null" means the symbol carried on this subcarrier has a value of zero. Besides, some other subcarriers used as pilot for channel estimation are also inserted. The subcarriers are allocated at the input of the IFFT block to generate a phase shift. The windowing for pulse shaping is achieved after CP extension.



figureArchitecture of an OFDM system

At the receiver side, the frame synchronization and detection for both timing and frequency is performed in the first stage. Channel estimation is performed after the FFT block outputs the preambles in the frequency domain. The result is fed back to the FFT block for the equalization, which eliminates the effects of fading channel, while the fine synchronization for both timing and frequency is also added to further improve the system performance.

At least these basic parameters should be specified for a system design:

1. Delay spread expected for the channel (300ns)
2. Guard duration (800ns) which describes symbol duration (4.0 μ s)
3. Available bandwidth
4. Data rate

For indoor environment a delay spread less than 300 ns expected. We consider the guard duration 800 ns, which effectively protects the signal from ISI in the indoor environment and some of the outdoor wireless communication environments. Five times the guard duration for limiting the power and bandwidth loss is regarded for the symbol duration, and is set to 4.0 μ s in our case. Hence, the OFDM symbol rate is 0.25 mega symbol per second (Mbaud).

Keep in mind, the useful OFDM symbol duration without the guard interval is 3.2 μ s. So, the subcarrier spacing, which is the reciprocal of the useful symbol duration, can be determined as 312.5 kHz. Assuming that there is a bandwidth of 20 MHz available, the number of subcarriers is calculated to be 64. This is exactly the same as the specification defined in IEEE 802.11a standard.

As mentioned, some tones are reserved for pilot subcarries (channel estimation), null subcarriers (realizing oversampling to avoid aliasing) and windowing (reduce the out-of-band spectral energy).

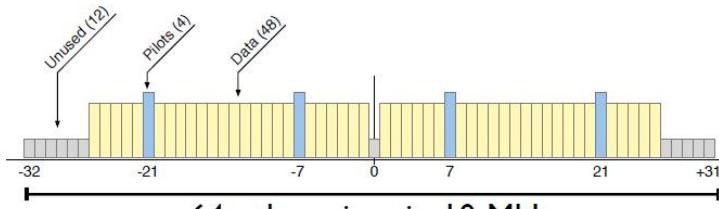
In our design we chose 48 data tones and 4 pilot subcarriers. So, 52 subcarries are occupied. Applying a raised-cosine window with roll-off factor $\beta = 0.02$ the total occupied bandwidth is

$$(1 + 0.02) \times (52 \times 312.5 \text{kHz}) \approx 16.6 \text{MHz} \quad (5)$$

To accomplish Oversampling, some zeros before and after the data vector are appended in the frequency domain as shown below.

$$\overbrace{0, 0, \dots, 0}^{1/2 \text{ appended zeros}}, \underbrace{d_{-\frac{N_d}{2}}, d_{-\frac{N_d}{2}+1}, \dots, d_{-1}}_{\text{Negative subcarriers}}, \underbrace{d_1, d_2, \dots, d_{\frac{N_d}{2}}}_{\text{Positive subcarriers}}, \overbrace{0, 0, \dots, 0}^{1/2 \text{ appended zeros}} \quad (6)$$

In the IEEE 802.11a transmitter, a 64 point IFFT multiplexes the orthogonal sub-carriers and the sub-carriers are renumbered as in Figure



figureThe frequency allocation of IEEE 802.11a sub-carriers

The nonzero data values are mapped onto the subcarriers around 0 Hz, and the zeros are mapped onto frequencies around sampling rate. Basically, in the BPSK modulation is applied on each subcarrier, each symbol for an individual subcarrier has one bits. The bit rate achieves without channel coding:

$$\frac{1}{4.0 \mu s} \times 48 \times 1 = 12 \text{Mbps} \quad (7)$$

The same calculation can be perform for QPSK to reach 24Mbps. But, channel coding will reduce this values. Variation of coding rates and modulation methods, In the 802.11a standard, the data rate ranges from 6 Mbps to 54 Mbps.

tableSystem parameters defined for the proposed OFDM system

Parameter	Description	Value
B_w	Available channel bandwidth	20MHz
σ_τ	Delay spread of the channel	< 300ns
T_g	Guard interval duration (Cyclic Prefix)	0.8μs
T_{sym}	OFDM symbol period	4.0μs
T	Effective symbol duration (FFT period)	3.2μs (= $T_g - T_{sym}$)
Δf	Subcarrier spacing	312.5kHz (= 1/T)
N_g	Number of guard samples	16
N	FFT size	64 = $B/\Delta f s$
N_d	Number of data subcarriers	48
N_p	Number of pilot subcarriers	4
N_u	Number of used subcarriers	52
B_u	Signal occupied bandwidth	16.6MHz
	Modulation type	BPSK, QPSK
R_b	Data rate without coding	12Mbps, 24Mbps

Table

tableRate dependant parameters in IEEE 802.11a Standard

Data rate	Modulation	Code Rate	Coded bits per symbol	Data bits per symbol
6 Mbps	BPSK	1/2	48	24
9 Mbps	BPSK	3/4	48	36
12 Mbps	QPSK	1/2	96	48
18 Mbps	QPSK	3/4	96	72
24 Mbps	16QAM	1/2	192	96
36 Mbps	16QAM	3/4	192	144

The theoretical equation of the Bit-Error Rate for a QPSK channel is:

$$P_b(e) = \frac{1}{2} \operatorname{erfc} \left(\sqrt{\frac{E_b}{N_0}} \right) \quad (8)$$

It is discussed that the BER can be computed by considering the non-ideality which the two parameters *guard time* and *pilots* will inject into the result. The formulation would be:

$$P_b(e) = \frac{1}{2} \operatorname{erfc} \left(\sqrt{\frac{E_b}{N_0} \frac{T}{T + T_g} \frac{N_u}{N_u + N_p}} \right) \quad (9)$$

Replacing the standard value from Table

$$P_b(e) = \frac{1}{2} \operatorname{erfc}\left(\sqrt{\frac{E_b}{N_0}} 0.65\right) \quad (10)$$

0.6.3 IEEE 802.11a Standard in Time and Frequency

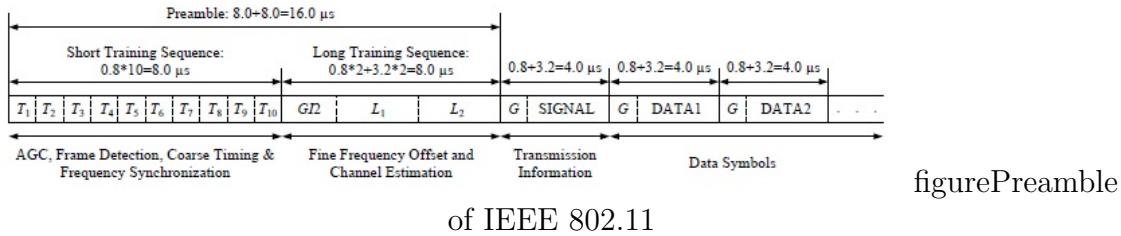
A packet of OFDM will be described here. In an OFDM frame, a preamble which carries no data is transmitted first, followed by the signal field which give some information about data and transmitted data. As indicated in Figure 00, an OFDM frame has the general form as below:

$$s_{OFDM}(t) = s_{preamble}(t) + s_{signal}(t - T_{preamble}) + s_{data}(t - T_{preamble} - T_{signal}) \quad (11)$$

where

$$s_{preamble}(t) = s_{short}(t) + s_{long}(t - T_{short}) \quad (12)$$

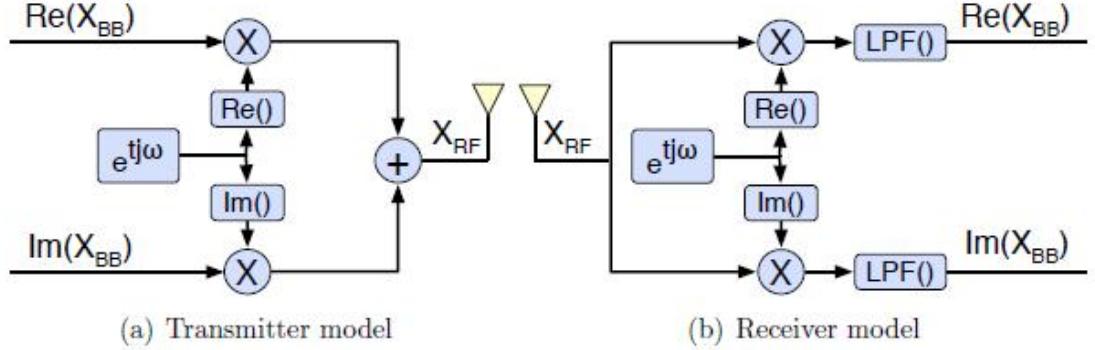
As shown in Figure



As we already analyzed, 52 subcarriers are used for an OFDM data symbol and pilot. Oversampling is achieved by adding 12 null subcarriers in order to eliminate aliasing which might occur during digital to analog conversion. Because FFT shift is performed, the null subcarriers with a value of zero are located in the middle of the input vector for the IFFT block. Note that dc carrier is not used to transmit data. The short and long training sequences can also be applied to this mapping rule, since they both have a length of 52 samples with frequency index from -26 to +26.

0.6.4 Origin of CFO

A simple model of a radio transmitter and receiver can depict the basis of the CFO source.



figureGeneral models of a direct conversion RF

In Figure

$$\begin{aligned}
 X_{RF} &= TX(X_{BB}) \\
 &= Re(X_{BB}) \cos(\omega t) - Im(X_{BB}) \sin(\omega t) \\
 &= \frac{1}{2}(X_{BB}e^{jt\omega} + X_{BB}^*e^{-jt\omega})
 \end{aligned} \tag{13}$$

$$\begin{aligned}
 X_{BB} &= RX(X_{RF}, \omega) \\
 &= LPF(X_{RF}e^{j\omega t})
 \end{aligned}$$

Assume a signal S_{BB} transmitted with carrier frequency ω_S which is received with carrier frequency ω_D . we can express the received baseband signal D_{BB} in terms of the transmitted baseband signal S_{BB} and the carrier frequencies. Then:

$$\begin{aligned}
 D_{BB} &= LPF\left(\frac{(S_{BB}e^{jt\omega_S} + S_{BB}^*e^{-jt\omega_S})e^{jt\omega_D}}{2}\right) \\
 &= S_{BB}(e^{jt(\omega_S - \omega_D)})
 \end{aligned} \tag{14}$$

The received baseband signal is equal to the original baseband signal modulated by a complex sinusoid. In the frequency domain, this gives a received spectrum equal to the transmitted one, only shifted away from DC by the difference in the carrier frequencies of the transmitter and receiver (i.e. $\omega_S - \omega_D$). This shift of the received signal is the baseband manifestation of carrier frequency offset.

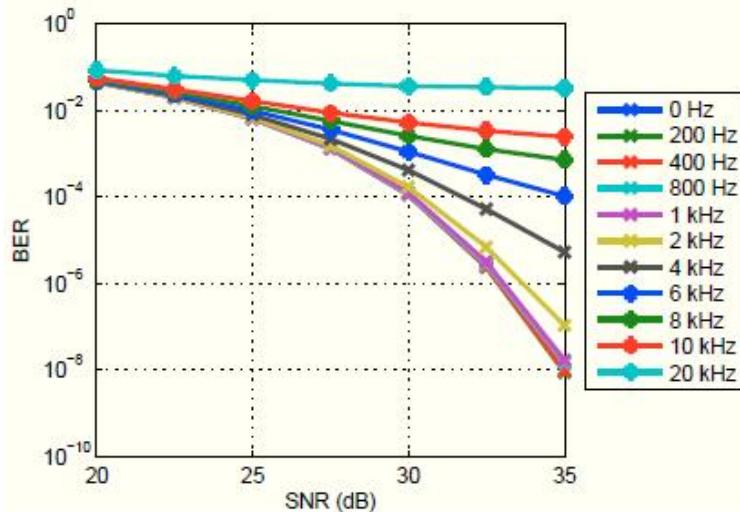
0.6.5 Impact of CFO

There are two destructive impacts on an OFDM system. Firstly, the phase offset across subcarriers in an symbol which can be estimated and corrected in frequency

domain to prevent errors in a constant rotated constellation. Some subcarriers are allocated as pilot tones which receiver can estimate phase errors.

The second effect of CFO is the degradation of orthogonality between subcarriers in receiver's FFT which causes inter-carrier interference (ICI). ICI acts an effective SNR reduction as a result of CFO increasing. [...]

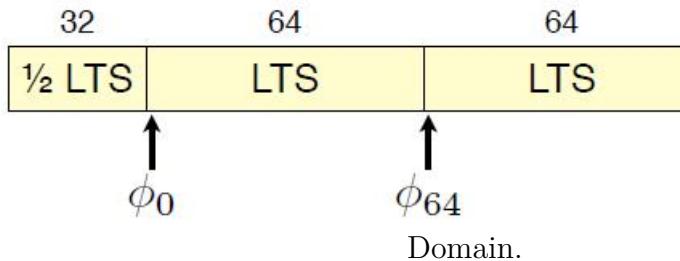
The impact is displayed in Figure



figureOFDM performance loss due to CFO-induced ICI.

The results shows that for large CFOs errors caused by ICI dominate performance, even at high SNR. It is also clear that for small CFOs performance is dominated by SNR. Specifically, for frequency offsets smaller than 1 kHz, the performance degradation due to ICI is negligible.

Let's focus on LTS part in a OFDM symbol, Figure



figureLTS in Time Domain.

We can say:

$$CFO \approx (\phi_{64} - \phi_0)$$

$$CFO_{EST} = \frac{f_s}{2\pi \cdot 64^2} \sum_{n=64}^{127} \phi_n - \phi_{(n-64)} \quad (15)$$

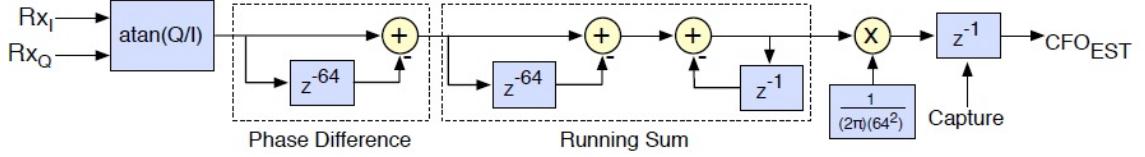


figure Time Domain CFO Estimation.

Which CFO_{EST} is the estimated CFO. To have such the structure in the Simulink we can arrange as Figure

0.6.6 Synchronization

The synchronization tasks is challenging in an OFDM-based communication system. Prior to performing channel estimation equalization and demodulation, OFDM symbol timing must be detected. The receiver has no information when a packet starts, and so the first synchronization task is packet detection. Once a packet has been detected the remaining synchronization functions include coarse and fine timing recovery and carrier recovery.

Figure

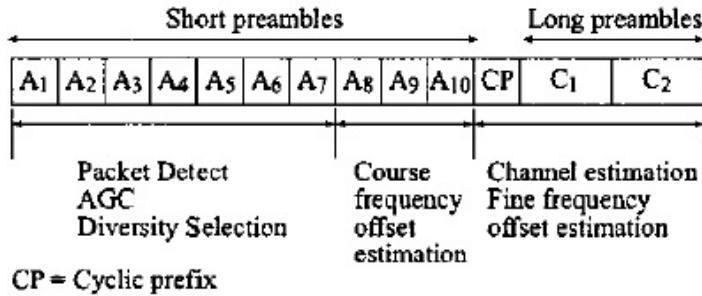


figure IEEE 802.11a

preamble.

The packet detector is based on the Schimdt and Cox delay and correlate algorithm employed for acquiring symbol timing commonly. The algorithm, as illustrated in Figure

The sliding window P computes a auto-correlation between the input signal and a D-sample delayed version on short preamble interval. We chose D=16. The second sliding window R is used to compute the received signal energy in the cross-correlation interval.

$$P(n) = \sum_{m=0}^{L-1} r_{n+m} r_{n+m+D}^* \quad (16)$$

$$R(n) = \sum_{m=0}^{L-1} r_{n+m+D} r_{n+m+D}^* \quad (17)$$

The cross-correlation $P(n)$ and auto-correlation $R(n)$ are calculated according to Equation

$$M(n) = \frac{|P(n)|^2}{R(n)^2} \quad (18)$$

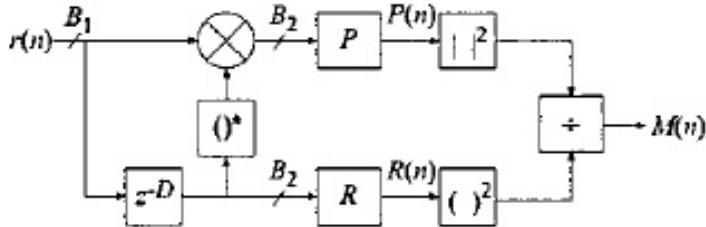


figure Schimdl and Cox
Delay and Correlate Algorithm.

0.6.7 Channel Estimation and Distortion Reject

Imagine the estimated channel is \hat{H} and the input information is A . So, we can expect to compensate the signal as below:

$$\begin{aligned} A_{\text{compensate}} &= \frac{A}{\hat{H}} \\ &= \frac{A \cdot \hat{H}^*}{|\hat{H}|} \end{aligned} \quad (19)$$

If the estimation is done correctly and the channel is perfect without any distortion, we expect \hat{H} to be a flat shape in whole frequencies. Such the estimation is done by LTS to have the same input on all the tones at the transmitter and calculate the channel in the receiver by studying LTS.

Part III

FPGA Implementation

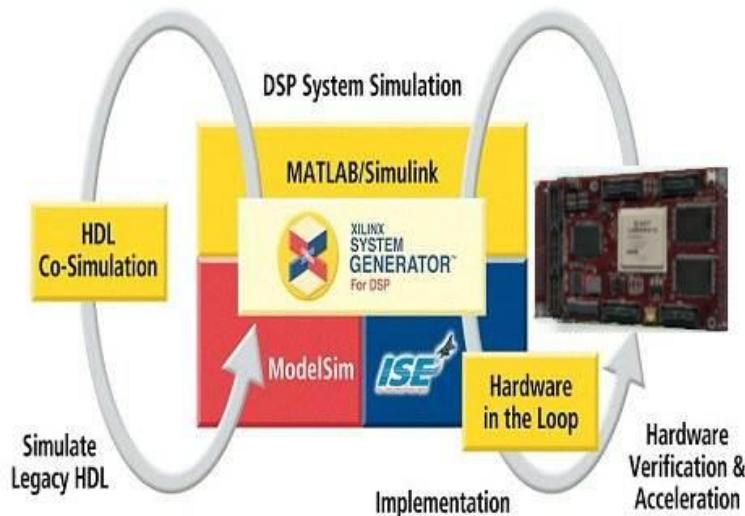
Abstract

The hardware is introduced with some details of the implementations. The main FPGA side project is done in Xilinx System Generator which is a high level alternative with standard scripting languages like VHDL and Verilog. An overview to select the radio board and the clock chain inside will be described.

Main blocks in transmitter and receiver is defined and the mechanism for packet detection is illustrated in details.

0.7 System Design in System Generator

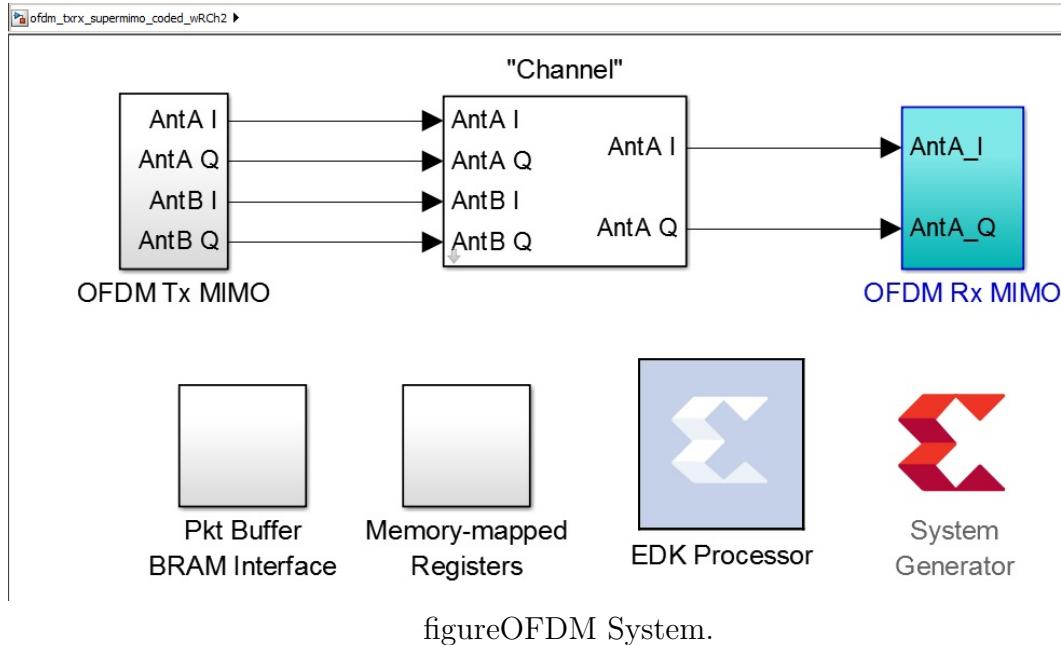
Simulink® from The MathWorks® is a powerful graphical modeling system which allows complex systems to be designed using a block diagram methodology. Xilinx System Generator for DSP is a blockset for Simulink® which allows the modeling of fixed point systems which can be transformed into VHDL and targeted at an FPGA. Automatic generation of the bitstream is supported with the synthesis and implementation tools run from within the Simulink® environment.



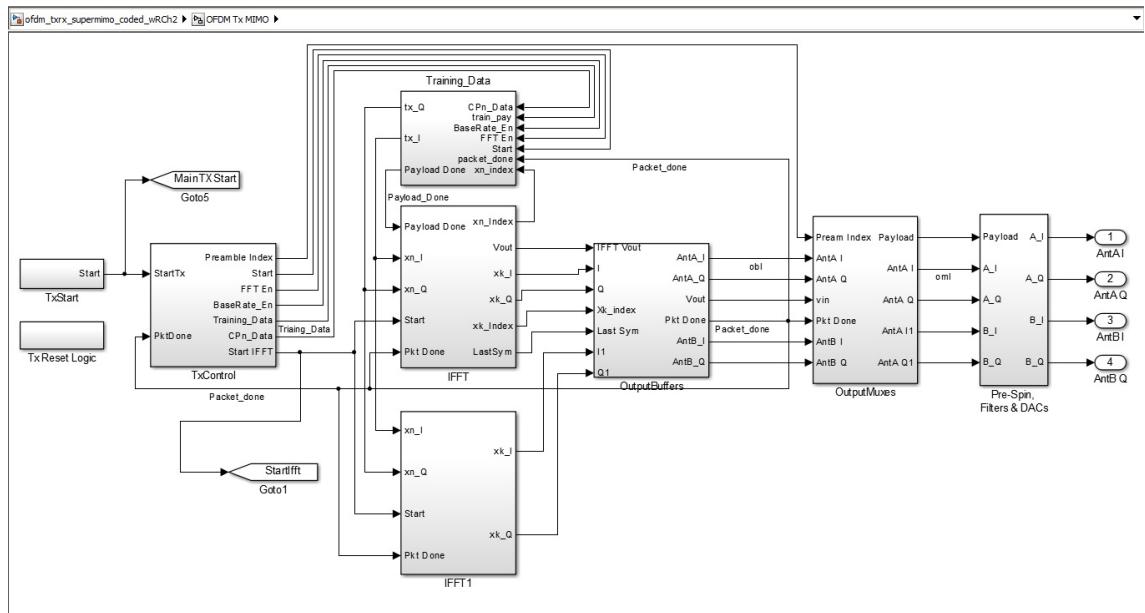
figureSystem Generator
Cycle.

Then main core of an OFDM modulator and demodulator are the inverse FFT (IFFT) and FFT respectively. In 802.11a WLAN standard a 64-point transform with 52 of the subcarriers are carrying user data in a BPSK, QPSK, 16-QAM or 64-QAM alphabet. The symbol rate in this systems is $20MSym/s$. The OFDM symbol period is $4\mu s$, with $3.2\mu s$ of this interval occupied by the 64-point FFT symbol and the additional $0.8\mu s$ used for the cyclic prefix.

Figure



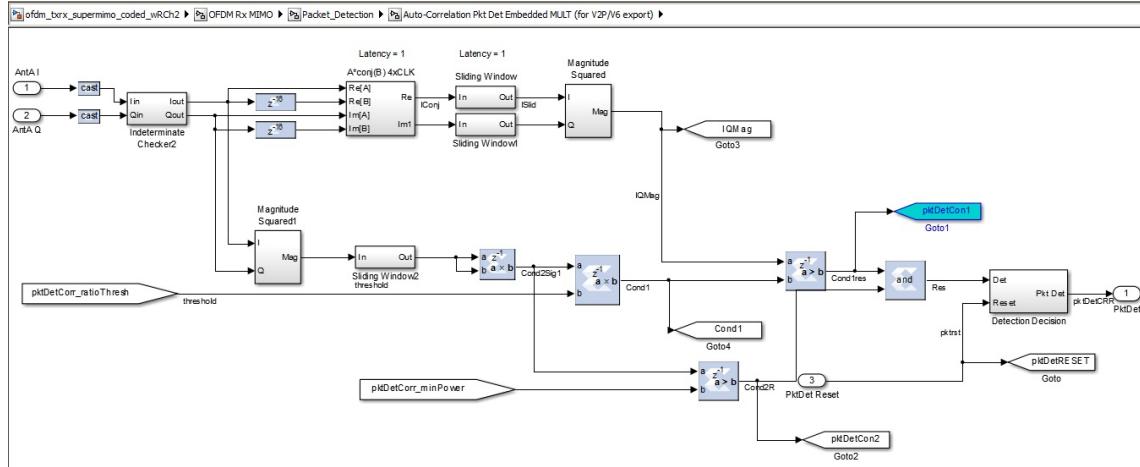
Figure



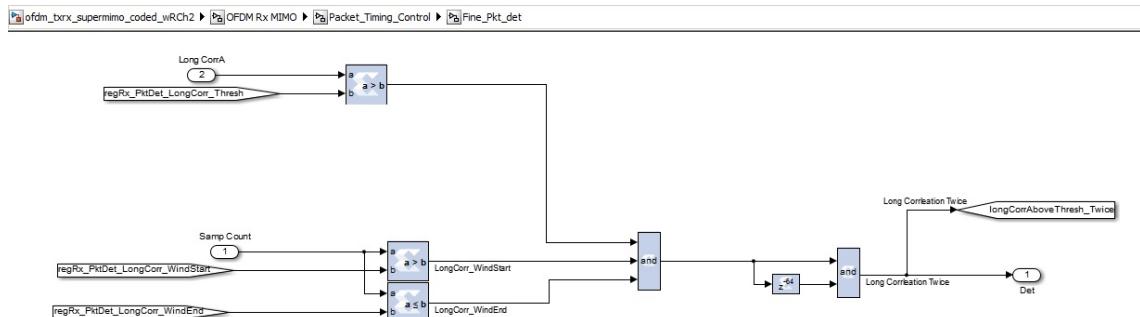
figureOFDM Transmitter Block.

Figure

In the *Packet Detection* block an auto-correlation approach is done on the signal to detect the energy of the preamble in the beginning of STS shows in Figure

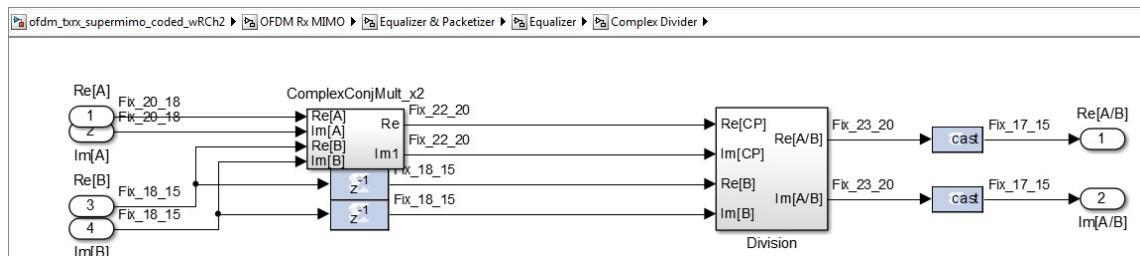


figureAuto-Correlation Block.

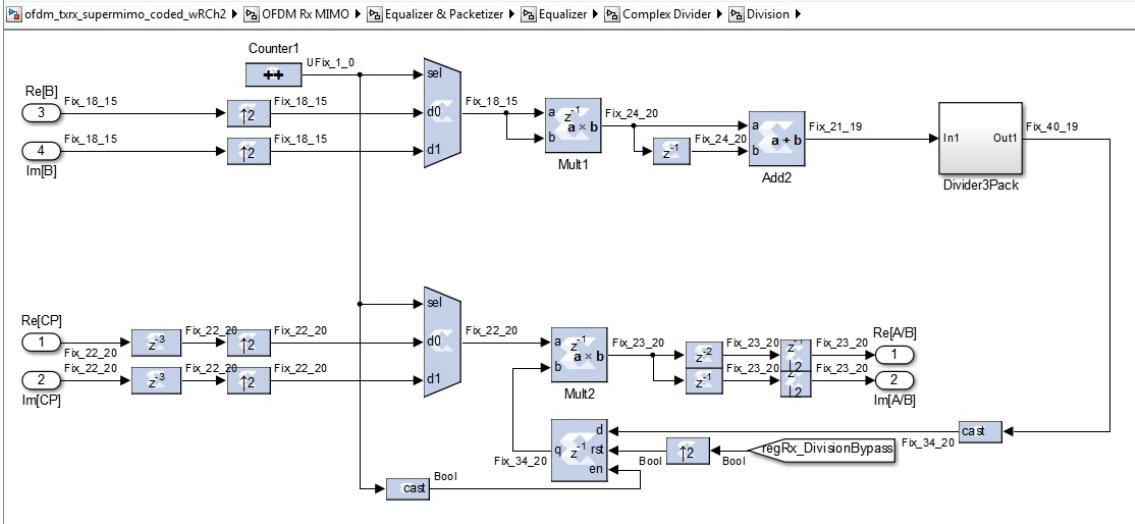


figureFine Packet Detection Block.

As described in Section



figureComplex Division Block.



figureDivision Block.

0.8 Hardware Introduction

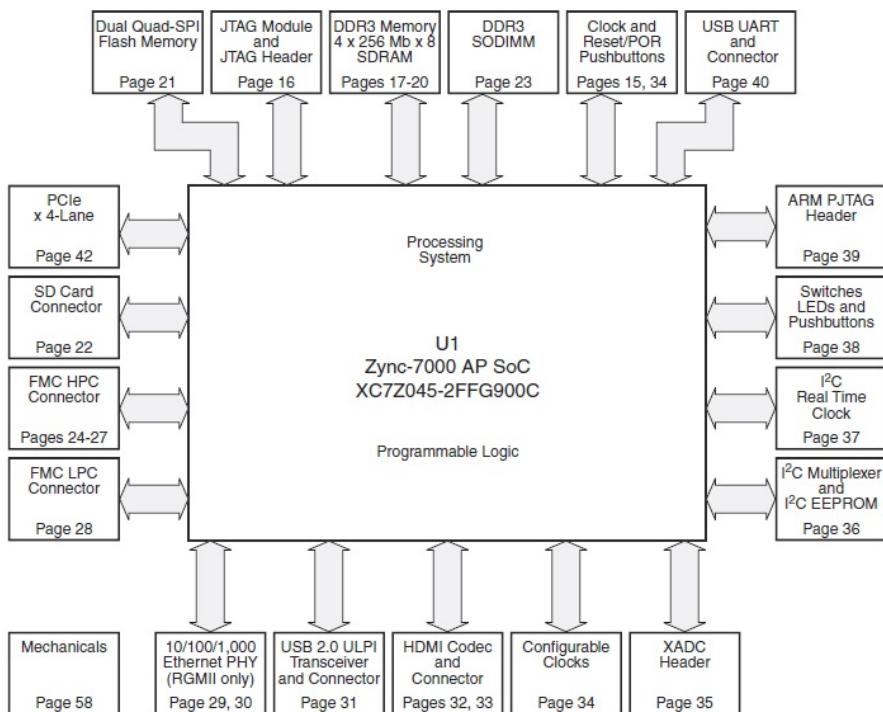
0.8.1 FPGA Board

The ZC706 evaluation board for the XC7Z045 All Programmable SoC (AP SoC) provides a hardware environment for developing and evaluating designs targeting the Zynq-7000 XC7Z045-2FFG900C AP SoC. The ZC706 evaluation board provides features common to many embedded processing systems, including DDR3 SODIMM and component memory, a four-lane PCI Express interface, an Ethernet PHY, general purpose I/O, and two UART interfaces. Other features can be supported using VITA-57 FPGA mezzanine cards (FMC) attached to the low pin count (LPC) FMC and high pin count (HPC) FMC connectors. For details of architecture see Section



figureZC706

Evaluation Board Block Diagram.



Note: Page numbers reference the page number of schematic 0381513.

UG954 c1 01 1002012

figureXilinx

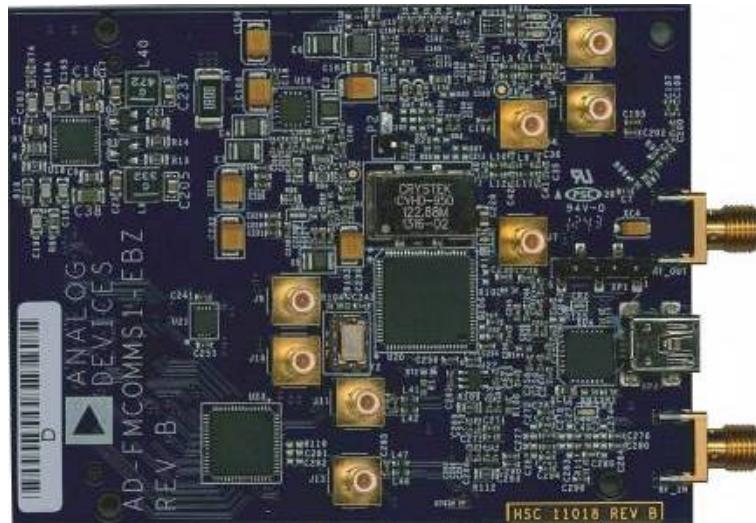
Zynq-7000 SoC ZC706 Evaluation Kit

0.8.2 Radio Board

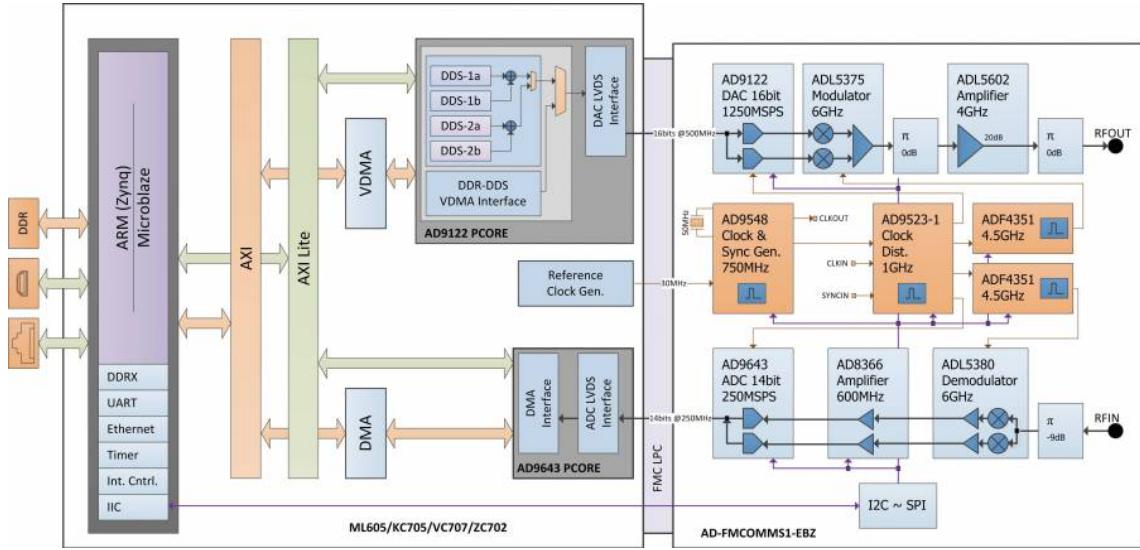
The AD-FMCOMMS1-EBZ high-speed analog module is designed to showcase one of the latest generation high-speed data converters. The AD-FMCOMMS1-EBZ

provides the analog front-end for a wide range of compute-intensive FPGA-based radio applications.

The AD-FMCOMMS1-EBZ enables RF applications from 400MHz to 4 GHz. The module is customizable to a wide range of frequencies by software without any hardware changes, providing options for GPS or IEEE 1588 Synchronization, and MIMO configurations. When combined with the Xilinx ZC706, AD-FMCOMMS1-EBZ enables a variety of wireless communications functions at the physical layer, from baseband to RF. With up to 4 GB of flash storage space, 512 MB of RAM, Gigabit Ethernet interface (depending on the base platform). The platform offers enough flexibility for many applications, and supports streaming data, and standard web interfaces to analyze transmitted RF data.



figureAD-FMCOMMS1-EBZ (Radio Board)

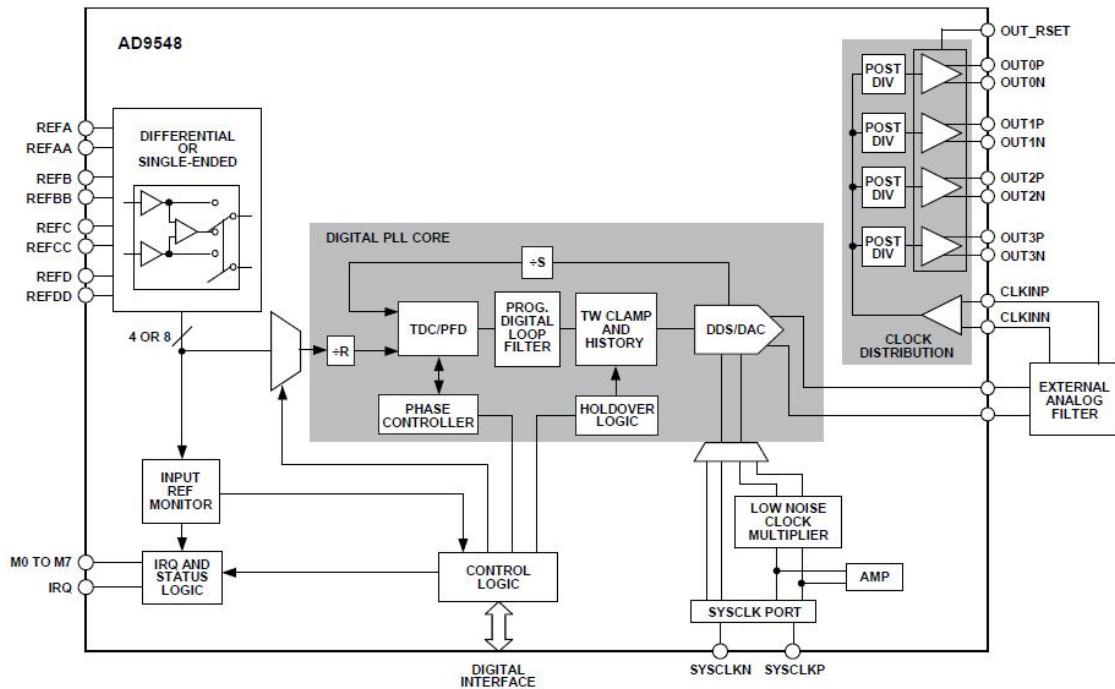


figureAD-FMCOMMS1-EBZ Block Diagram

0.8.3 Clock Chain on FMCOMMS1

Now, we discuss more about the clock chain and distribution mechanism on the board to find some meaningful number. As you can see in the figure, we configure the board and internal FPGA architecture to generate a 30MHz clock to the RF board. This 30MHz is just chosen because a relevant crystal mounted on the Zynq board and the all generated clock is supposed to be in-phased with it. This 30MHz is an input for AD9548 as a clock generator/synchronizer which has a very precise PLL inside to generate a 20MHz.

The AD9548 generates an output clock synchronized to one of up to four differential or eight single-ended external input references. The digital PLL allows for reduction of input time jitter or phase noise associated with the external references. The AD9548 continuously generates a clean (low jitter), valid output clock even when all references have failed by means of a digitally controlled loop and holdover circuitry. AD9548 is a very complicated device to generate 20MHz with maximum precision.

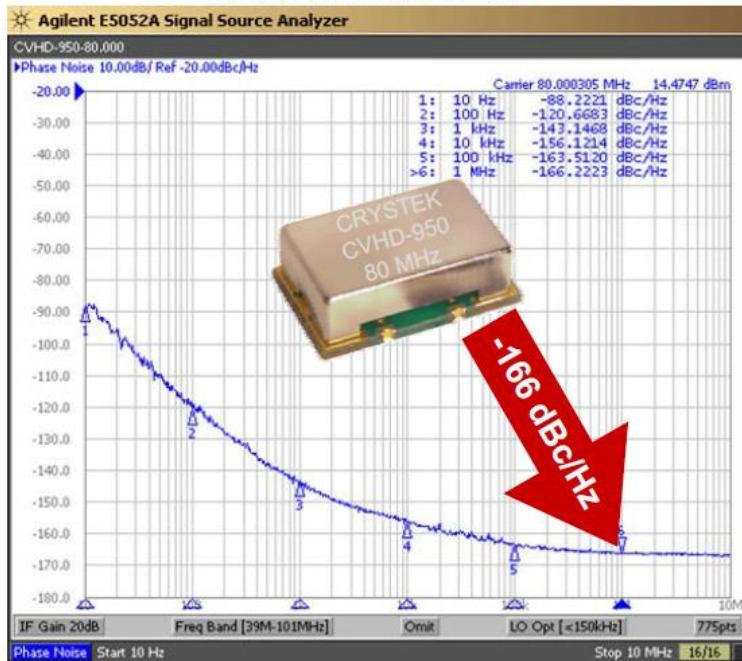


figureAD9548 Block Diagram

The next IC in the clock chain is AD9523-1 which is Low Jitter Clock Generator. The AD9523-1 provides a low power, multi-output, clock distribution function with low jitter performance, along with an on-chip PLL and VCO with two VCO dividers. The on-chip VCO tunes from 2.94 GHz to 3.1 GHz. The AD9523-1 is defined to support the clock requirements for long term evolution (LTE) and multicarrier GSM base station designs. It relies on an external VCXO to provide the reference jitter cleanup to achieve the restrictive low phase noise requirements necessary for acceptable data converter SNR performance.

The input receivers, oscillator, and zero delay receiver provide both single-ended and differential operation. When connected to a recovered system reference clock and a VCXO, the device generates 14 low noise outputs with a range of 1 MHz to 1 GHz, and one dedicated buffered output from the input PLL (PLL1). The frequency and phase of one clock output relative to another clock output can be varied by means of a divider phase select function that serves as a jitter-free, coarse timing adjustment in increments that are equal to half the period of the signal coming out of the VCO. In our chain we have a 80MHz VCXO connected to AD9523-1. It is supposed to generated 40MHz for ADC, DAC and also the main OFDM architecture FPGA program. You can see the specification of the crystal oscillator in

80 MHz HCMOS 3.3V



figureCVHD-950 Ultra

Low Phase Noise Oscillator

0.9 Expectations for CFO on FMCOMM1

In implementation of an OFDM chain, we should have good understanding the range of carrier frequency offsets which can be expected on our hardware platform. Our RF board foundation is based on FMCOMMS1. As a result, the elements in term of phase -noise and CFO should be studied. The main RF frequency reference is a Crystek CVHD-950 (VCXO). This VCXO provides a clock signal at a nominal frequency of 80 MHz. Actual output frequency varies as a function of multiple factors, and is only specified by the manufacturer with some tolerance. The CVHD-950 is specified with a frequency tolerance of ± 4 ppm. Thus, we must design for a reference frequency of 80 ± 0.000320 MHz. Imagine our target RF carrier frequency is 2452 MHz which implies 2400 MHz ± 4 ppm (or 2400 ± 0.009600 MHz).

The worst case CFO will occur when the transmit and receive nodes operate at opposite ends of this range. Thus, for operation in the 2.4 GHz band our OFDM transceiver design must be ready to handle any carrier frequency offset up to ≈ 20 kHz.

0.10 Time Domain CFO Correction

Prevention of the degradation of CFO, the receiver should estimate and correct the offset in the time domain before the FFT block. The FFT block translates the received signal into the frequency. Regarding to the variety issue of OFDM, many estimation algorithms have been proposed.

0.11 Carrier Frequency Offsets

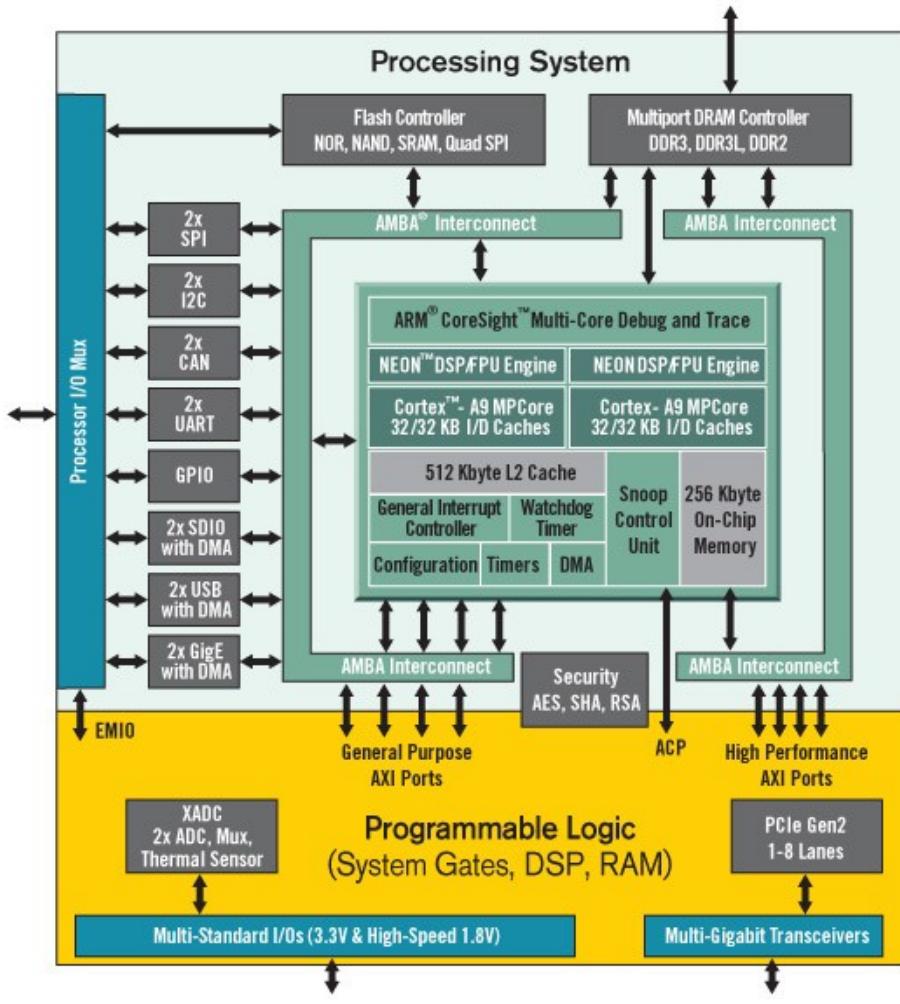
As a result of the frequency variation between local oscillators of the transmitter and the receiver nodes that generate the carrier signals, carrier frequency offsets (CFO) is happened. It causes when the baseband signal is going to be translated to RF. The issue is understood well but the impact to overcome CFO and suppression this phenomena is always depend on the specific parameters of the given transceiver and the hardware.

The origin of the CFO effect is studied in this section. We explore in a specific scenario of OFDM and the impact on the hardware design. Both simulation and experiments will be demonstrated and the CFO estimation and compensation is described.

0.12 FPGA Architecture

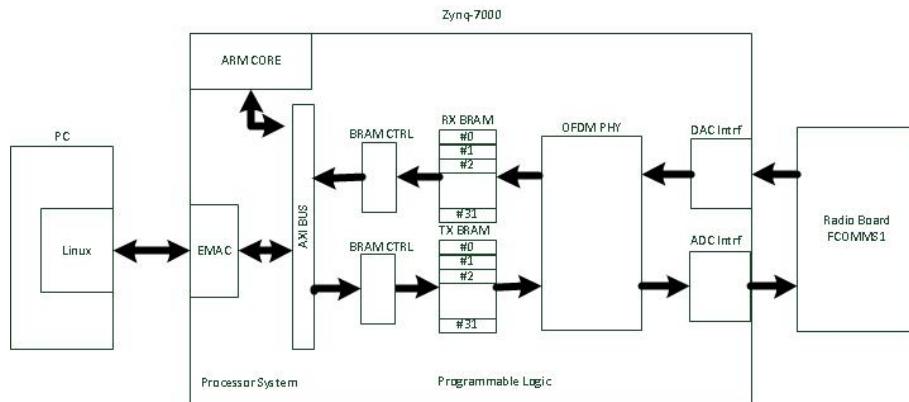
Based on the Xilinx All programmable SoC architecture, the Zynq-7000 All Programmable SoCs enable extensive system level differentiation, integration, and flexibility through hardware, software, and I/O programmability. Using the Zynq-7000 platform, you can design smarter systems with tightly coupled software based control and analytic with real time hardware-based processing and optimized system interfaces.

As you can see in Figure



figureZynq-7000 Diagram

The block diagram of the design is illustrated in Figure



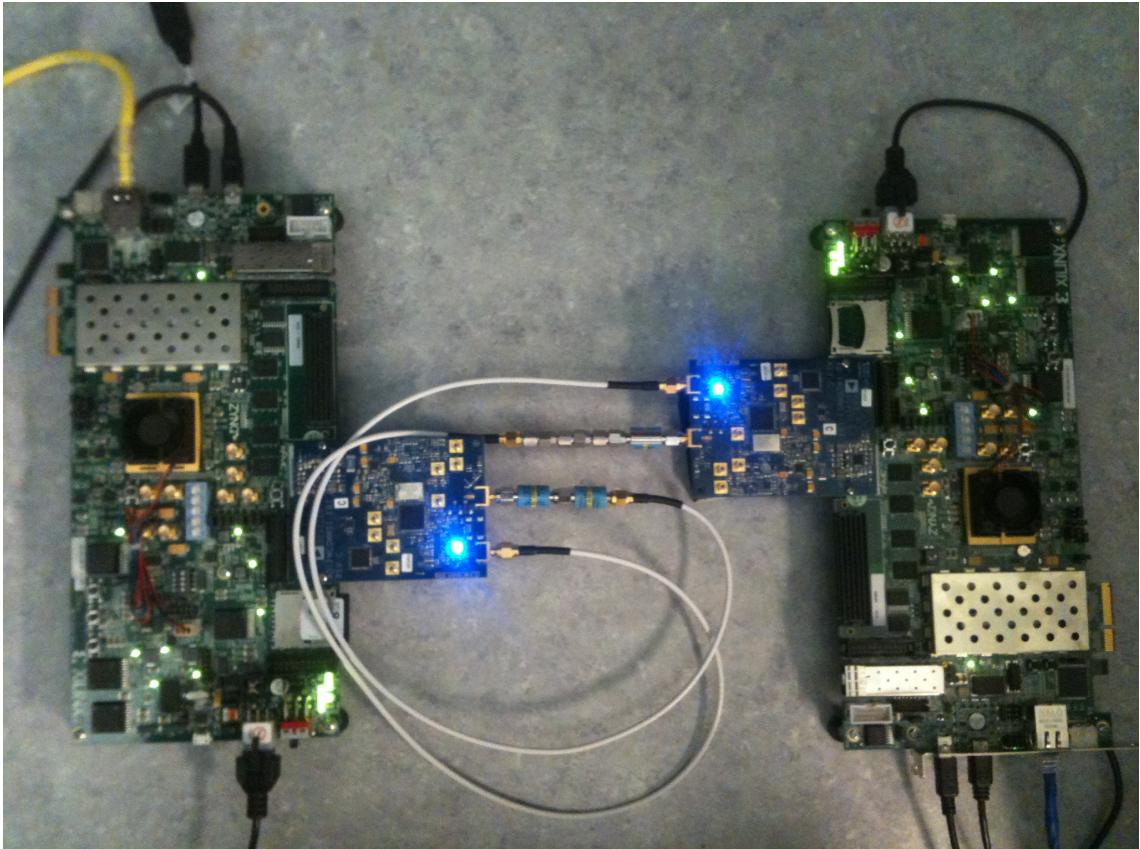
figureDesign

Block Diagram

As you can see in the block diagram the connection bridge between the Processor System and the Programmable Logic in the Zynq architecture can be AXI protocol. You can find the detail of AXI at ref..... There are some other communication protocols but in the Zynq design AXI works optimum. For easier programming issues in PC side, we used Linux Virtual Machine inside a Windows OS. It is very helpful because this configuration prevents unnecessary data exchange of the system and helps us to have a real estimation of the bit rate.

0.13 Test Methodology

The configuration set-up is consisted of two Zynq board each carrying a FMCOMMS1 radio board. They are connected to two individual PC via Ethernet cables as shown in Figure



figureHardware set-up

This configuration should be tested partially and have realistic estimation of the maximum possible bit-rate and then calculate SNR of channel. Having engineering

steps to examine each hardware block, we check the loops illustrated in

Part IV

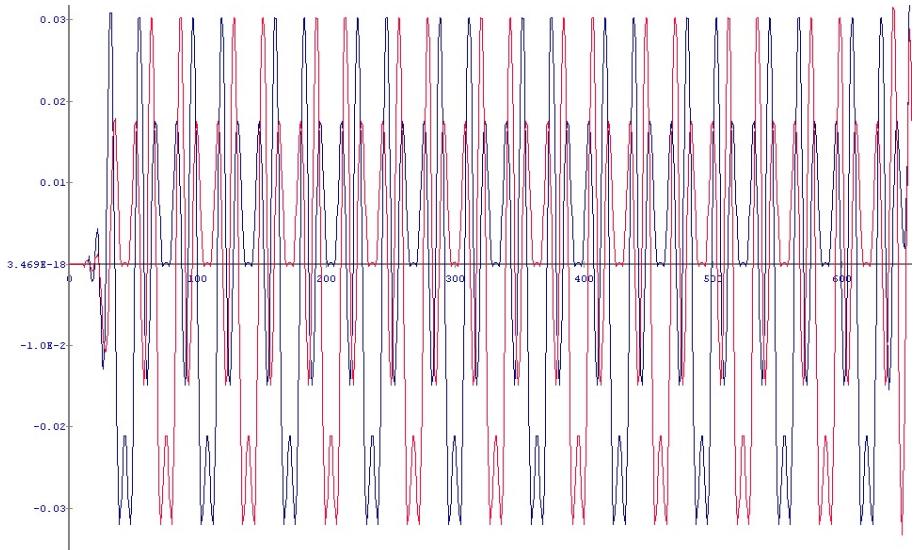
Sample Analysis and Conclusion

Abstract

After explanation of the system architecture and hardware design, the test methodology and the analysis of the results from the hardware is defined. The results are captured thanks to ChipScope software which help for internal acquisitions in various points of the Programmable Logic of FPGA. There are other tests we did to have an estimation of the system in total. For instance, we send a random data stream from a PC and send it via Ethernet in different packet size to a board and compare it in another PC where we generate the same random set.

0.14 Hardware Samples and Analysis

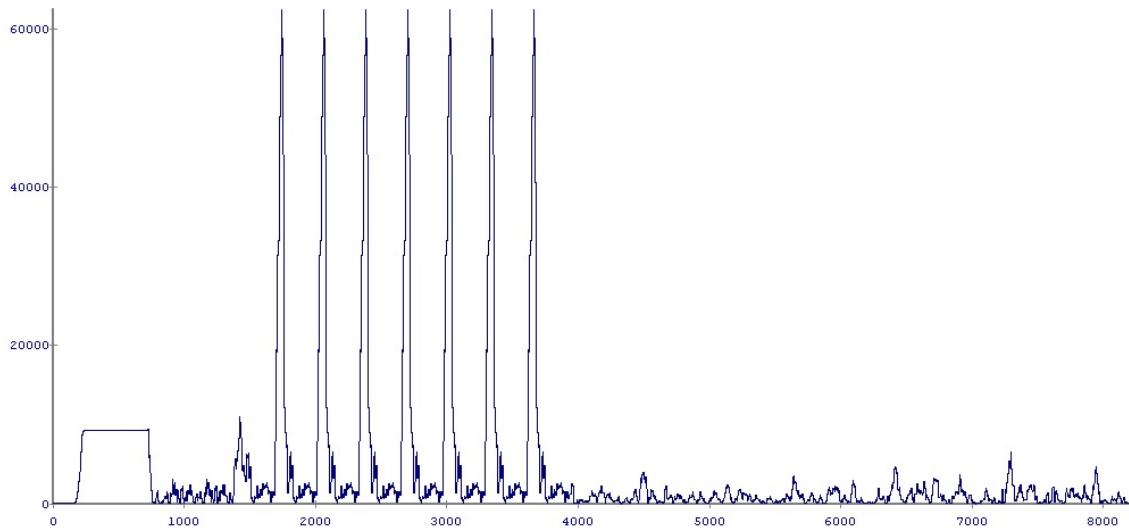
A complete OFDM frame is illustrated in Figure



figureSTS

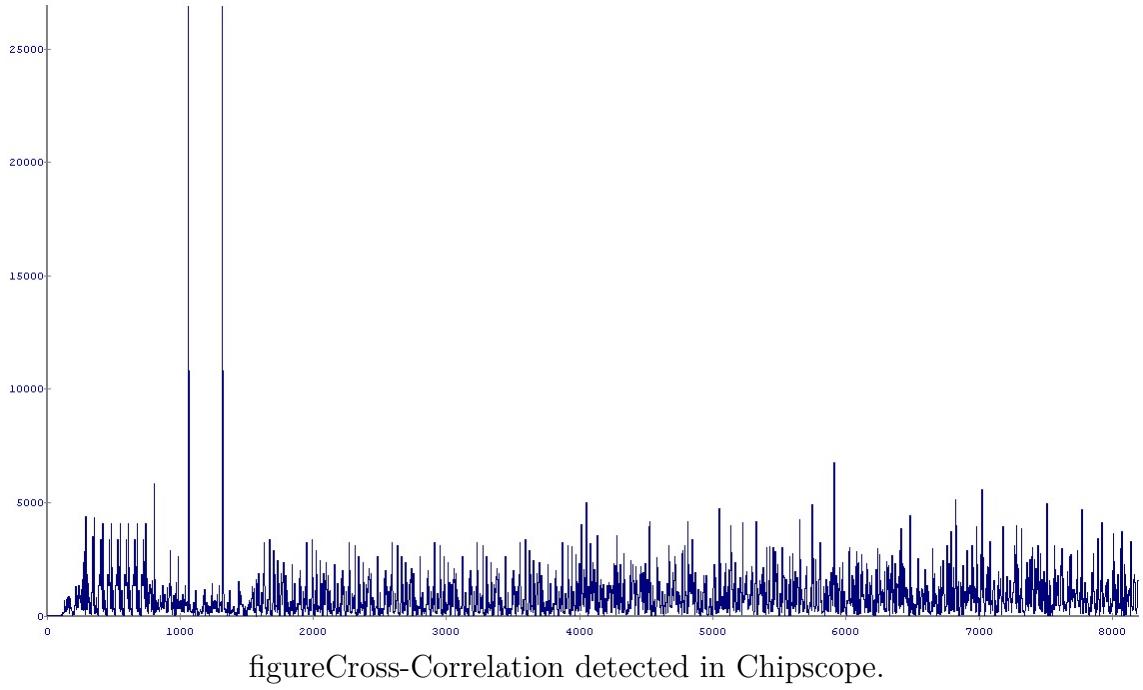
(I/Q) detected in Chipscope.

The auto-correlation is perform to catch the begining of the preamble with is STS. The output of the block is shown in Figure

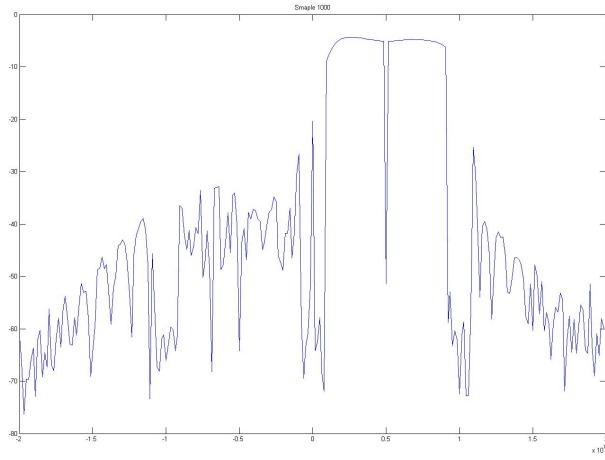


figureAuto-Correlation detected in Chipscope.

The cross-correlation on the LTS with a pre-defined expected LTS is shown in Figure

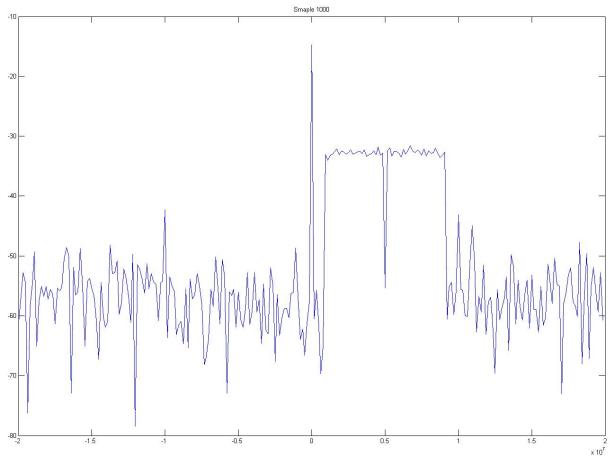


The LTS section is supposed to carry a flat shape in frequency that is used for the channel response estimation. In the Figure



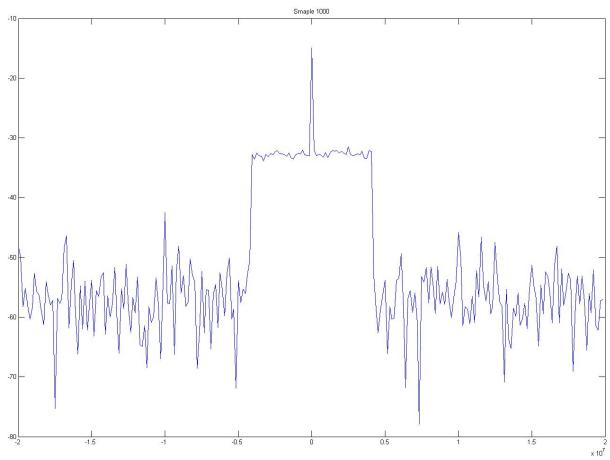
figureLTS Spectrum in
Baseband chain (IF filter on 5MHz is enable)

Passing the signal through the RF side which modulate around $2.4GHz$ and demodulate it again we have a shape as shown in Figure



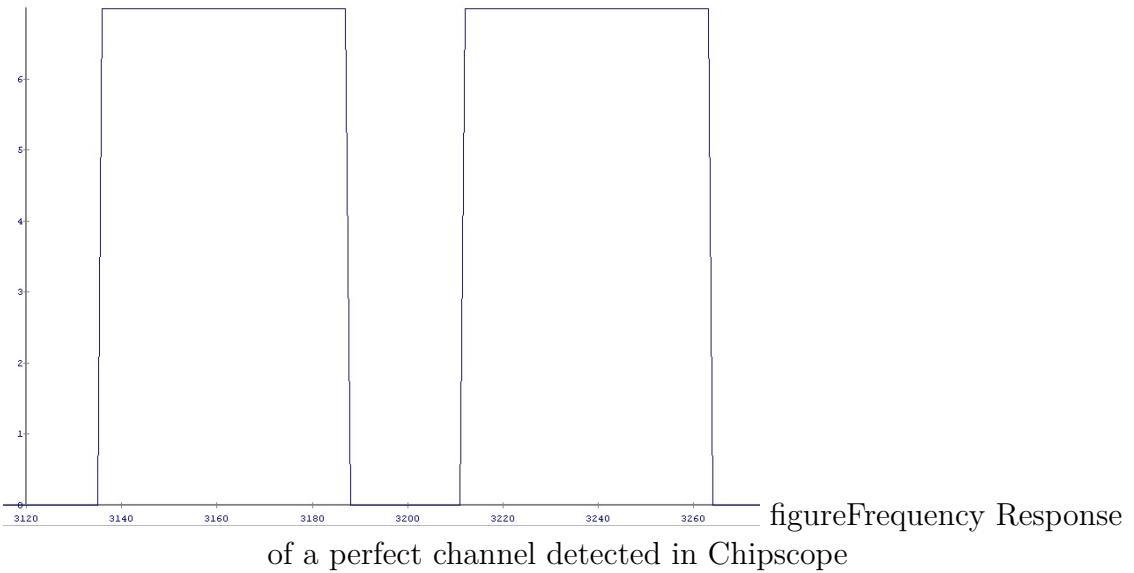
figureLTS Spectrum-passed RF chain (IF filter on 5MHz is enable)

We have a shape of LTS frequency response like Figure

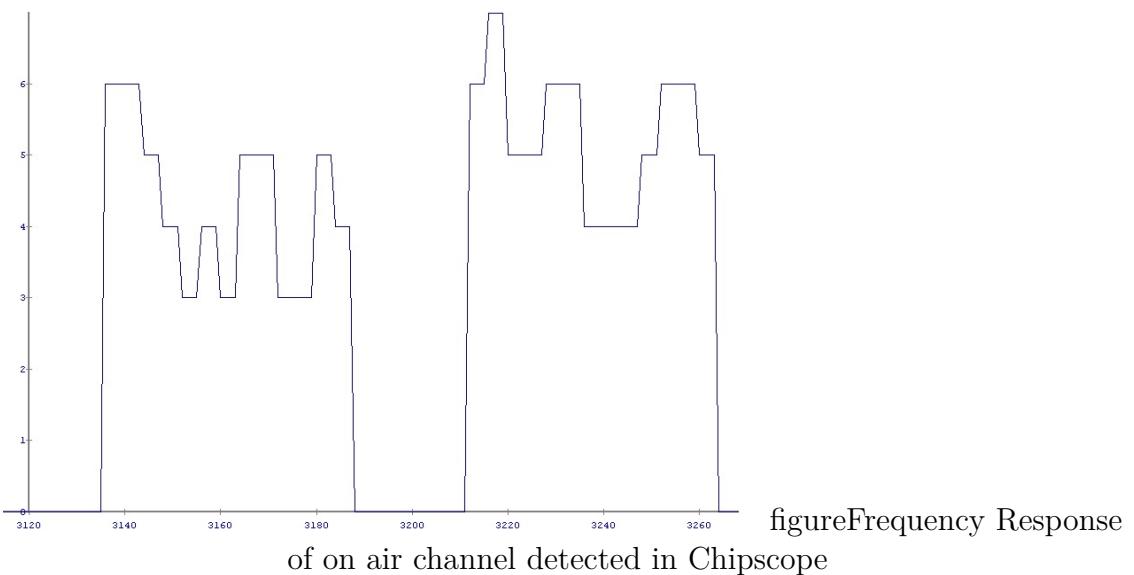


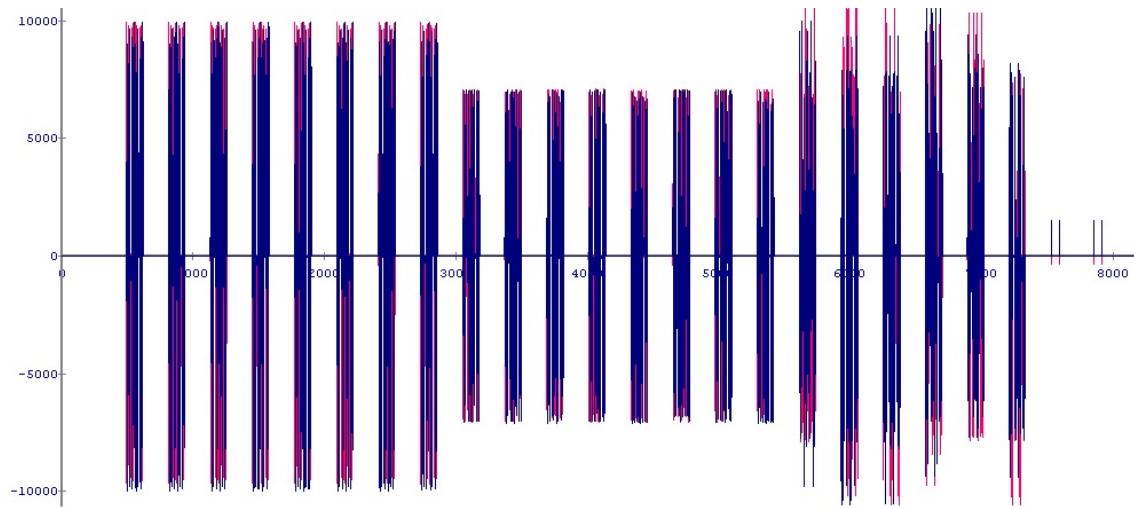
figureLTS Spectrum-passed RF chain (IF filter is disable)

Figure



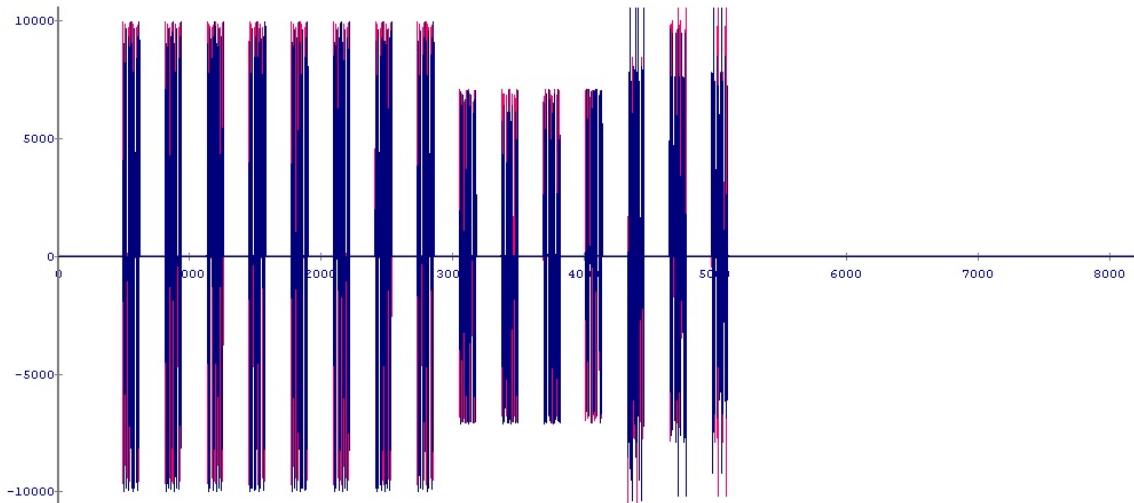
Figure





figureOFDM Symbols of a 16QAM 64-byte message Coded 1/2 rate

Figures



figureOFDM Symbols of a 16QAM 64-byte message no-Coded

0.15 Bit-Error Rate Calculation

Will be add later!!!

0.16 FPGA Resource Consumption

The device used in our implementation is XC7Z045-22FFG900C and in Table

tableDevice Utilization Summary (actual values)

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	42,703	437,200	9%
Number of Slice LUTs	59,787	218,600	27%
Number used as Memory	5,384	70,400	7%
Number of occupied Slices	21,749	54,650	39%
Number of DSP48E1s	149	900	16%

Keep in mind this table shows all the utilization of the ADC/DAC interface, BRAM, clock generator and OFDM PHY module. For OFDM PHY module we could reach Net Skew 0.51 ns and maximum Delay 1.91ns. About the ARM processor, we used one of the ARM cores although we have a dual core architecture. It works with 666.6MHz clock. It is almost 20% of the processor.

0.17 Conclusion

This thesis has presented the theoretical analysis and simulation and FPGA implementation details of a baseband OFDM system with channel estimation and timing synchronization. A radio board also is explained for the practical usage and proof of the feasibility. The OFDM system is prototyped based on IEEE 802.11a standard and transmits/receives signals on a 20 MHz bandwidth. The conceptual design is done in System Generator and ported on a FPGA. With QPSK modulation scheme, the system achieves a throughput of 24 Mbps.

Another critical part of the project is to reach an acceptable communication bit-rate in the processor side to the peripherals, more specifically Ethernet, for conveying data between two PC which is done perfectly.

0.17.1 Future Work

No doubt, System Generator is a very powerful tool for conceptual proof but is not still an industrial support. There are still difference in the Simulation in Matlab and what we have in the hardware. To overcome this issue we needed to make some changes to have a logical margin of the hardware difficulties. The resource consumption is not very optimized which expected to have better performance using VHDL programming. There are many low-level techniques to manage the power, speed and area which is not applicable in the system.

Some other problems like model-based system maintenance, extend for the future

and the bug detection difficulties make us to hesitate to industrialized a System Generator model at the moment. However, the accuracy of the theory is done perfectly in the current mechanism.

There are some projects in the department to extend the model for MIMO system design which is a good starting point. Besides, they try to upgrade the FFT point to higher levels for better bandwidth usage. A customized radio board is in the future program activities.