

Ehsan Yousefzadeh-Asl-Miandoab

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EDUCATION	◇ Sharif University of Technology , Tehran, Iran	2016 - 2018
	— M.Sc. in Computer Engineering - Computer Architecture	GPA: 17.20/20
	Coursework:	
	Advanced Computer Architecture	17.5/20
	Green Computing	20/20
	Fault Tolerant Systems	17.3/20
	Embedded System Design	17.4/20
	M.Sc. Dissertation	19.7/20 (Excellent)
	◇ University of Tabriz , Tabriz, Iran	2012 - 2016
	— B.Sc. in Computer Engineering - Hardware	GPA: 18.42/20
RESEARCH INTERESTS	Coursework:	
	Digital Design	18.5/20
	Computer Architecture	19/20
	Microprocessor	20/20
	Electrical Circuits	19/20
	Data Structures	20/20
	Operating Systems	18.5/20
	VLSI Design	20/20
	B.Sc. Project	20/20
	◇ Shahid Furoughi High School , Miandoab, Iran	2008 - 2012
HONORS AND AWARDS	— High School Diploma in Mathematics and Physics	GPA: 19.05/20
	◇ Computer Architecture	
	◇ Parallel Computing Systems	
	◇ Energy Efficient Designs	
	◇ GPUs and Heterogeneous Systems	
	◇ Hardware Accelerators for ML and NN applications	
	◇ Using Machine Learning in Computer Architecture	
	◇ Embedded Systems Design	
	◇ Ranked 1st in terms of cumulative GPA among Computer Hardware Engineering Students, University of Tabriz (2016)	
	◇ Admitted to the M.Sc. program at Sharif University of Technology as an Exceptional Talented Student (2016)	
TECHNICAL SKILLS	◇ Programming Languages : Python, C++, C, Java, MATLAB, VB	
	◇ Hardware Description Language (HDL) : Verilog	
	◇ Simulation Tools : Altera Quartus II, Mentor Modelsim, Proteus Design Suite, Synopsys Hspice and Pspice, GPGPU-Sim.	
	◇ Document Preparation : MS Office, L ^A T _E X.	
	◇ Having Experience with : Linux Terminal, Git, MVC, MySQL, VB programming for Microsoft Excel	
PUBLICATIONS	◇ OSM : Off-chip Shared Memory for GPUs	
	Ehsan Yousefzadeh-Asl-Miandoab , Mohammad Sadrosadati, Hajar Falahati, Sina Daraby, Parsoa Khursand, Negar Akbarzadeh, Pejamn Lotfi-Kamran, Hamid Sarbazi-Azad.	
	- Submitted to the IEEE TPDS 2021 .	
	- Proposing a unified on-chip memory for serving global accesses alongside shared accesses based on the extensive study of the shared memory access patterns and its nature and impact on the GPUs' total performance to mitigate underutilization and other downsides of the shared memories.	

TEACHING EXPERIENCE

◇ Teaching Assistant

- Department of Computer Engineering, Sharif university of Technology

- Computer Architecture Lab. Head TA Prof. Sarbazi-Azad Summer 2017
- Microprocessor Lab. Head TA Prof. Sarbazi-Azad Fall 2017
- Computer Architecture Head TA Prof. Jahangir Spring 2018
- Computer Architecture Lab. Head TA Prof. Jahangir Spring, Summer 2018
- Microprocessor Lab. Head TA Prof. Jahangir Spring, Summer 2018

- Department of Electrical and Computer Engineering, University of Tabriz

- Logic Circuit Design - Prof. Mina Zolfy Spring 2016

- Fundamentals of Programming Tutor

- Teaching first-year undergraduates how to program with C language, Summer, 2018

RESEARCH EXPERIENCE

◇ Sharif University of Technology Sep. 16 - Aug. 19 Sep. 20 - Now

- High Performance Computing Architectures and Networks (HPCAN)

- Supervisor: Prof. Hamid Sarbazi-Azad

Focus of my research has been to introduce an energy and area efficient on-chip memory design with negligible performance overhead for GPU Streaming Multiprocessors (SMs). I implemented and analyzed proposed designs using simulators such as GPGPU-Sim, and self-written C codes.

Over the past years I have accomplished two submission, one was submitted to *IEEE CAL* 2020, which based on the rejection we got, then the journal version is submitted to the *IEEE TPDS* 2021.

These days, my study focus is on memory consistency, and cache coherence protocols, especially for GPUs, and heterogeneous systems.

PROJECTS

◇ A Unified On-chip Memory for Shared and L1 Cache Accesses for GPUs in C++

- For my master's thesis, I implemented a unified on-chip memory to service both the shared memory and level one data cache accesses. I logged the addresses generated by the GPGPUSim simulator, and then I fed them to my designed and implemented on-chip memory in C++ to handle them simultaneously and efficiently.

◇ Mano's Basic Computer

- During the Computer Architecture course in my bachelor's, I designed and implemented a basic computer in the Quartus II Schematics. Then in my M. Sc. when I was computer architecture course's TA, I implemented this basic computer in Verilog HDL with more details again.

◇ Cache with different Configs

- I implemented direct-mapped and set-associative cache for my advanced computer architecture course. Then, I did experiments on it to observe the effects of different policies on hit/ miss rate. It is accessible here on Github.

◇ Python Basics and Data Structures, Algorithms, etc. Tutorial with Examples on Github

- In my leisure time during my master's years, I worked on preparing easy and quick tutorials for those who like to learn Python and Data Structures and some other things easily. You can check them out on my GitHub page.

◇ Web Development Projects

- I worked as a back-end developer in several web development teams. I was preparing queries to the databases to get out the wanted data for the designed forms by the front-end team. Additionally, I was responsible for providing APIs to send the needed data to the mobile programmers. Also, I contributed to a URL Shortener on GitHub. Recently, I tried to develop an API in golang to ease the job of people who want to write API endpoints in golang, and they don't know how and where to start.

◇ Design and Implementation of An Efficient Archiving System in Excel and some other automation systems in MS

- During my conscription, I designed, implemented, and organized an efficient archiving system in Excel with VBA with regard to the documents type and their transactions.

Additionally, most of the work was done manually, so I automatized the processes, which in result we had much more free time.

**LANGUAGE
SKILLS**

- **English:** fluent; The TOEFL exam is scheduled to be taken on April 30th, 2021.
- **Azerbaijani:** mother tongue.
- **Persian:** native.
- **Turkish:** fluent.