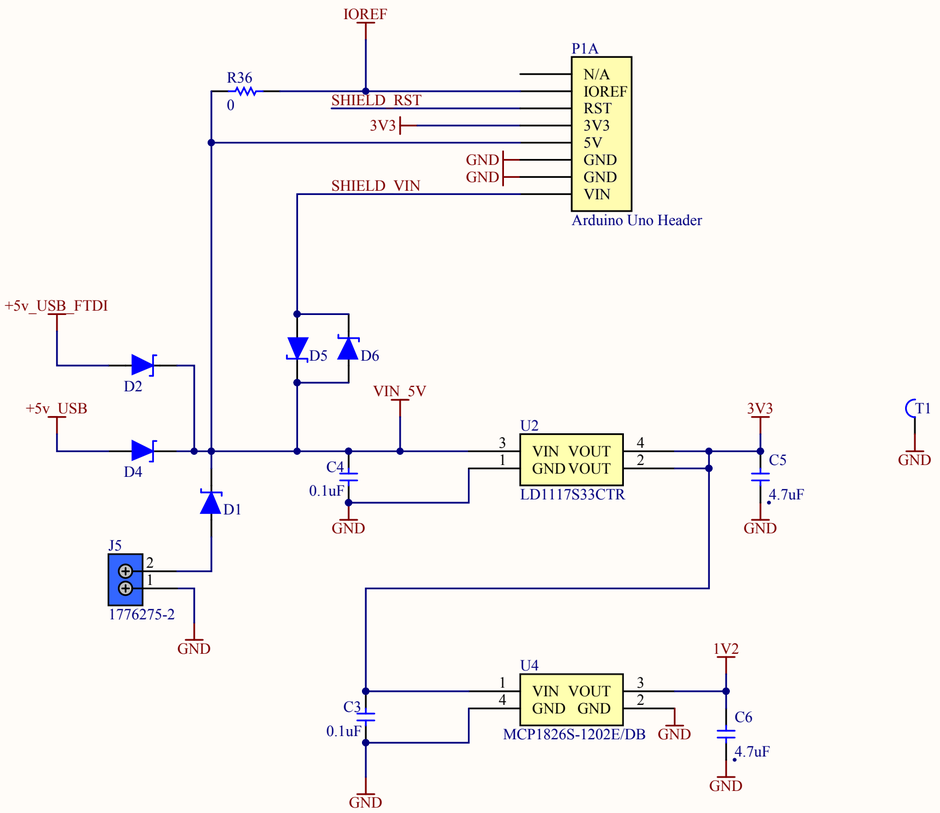
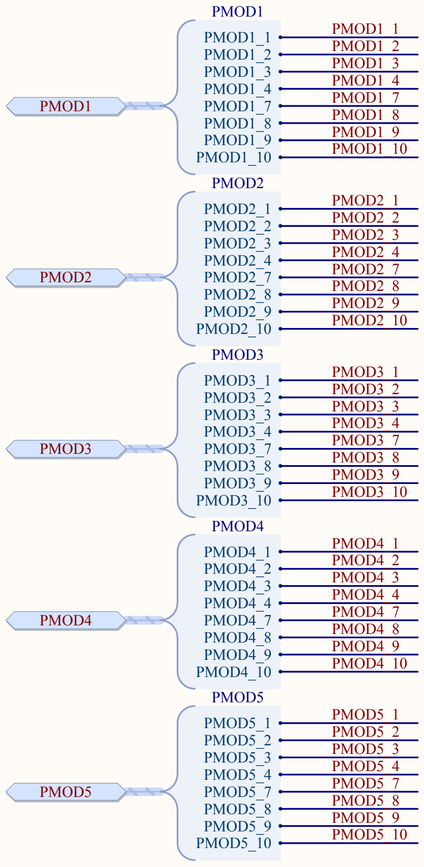
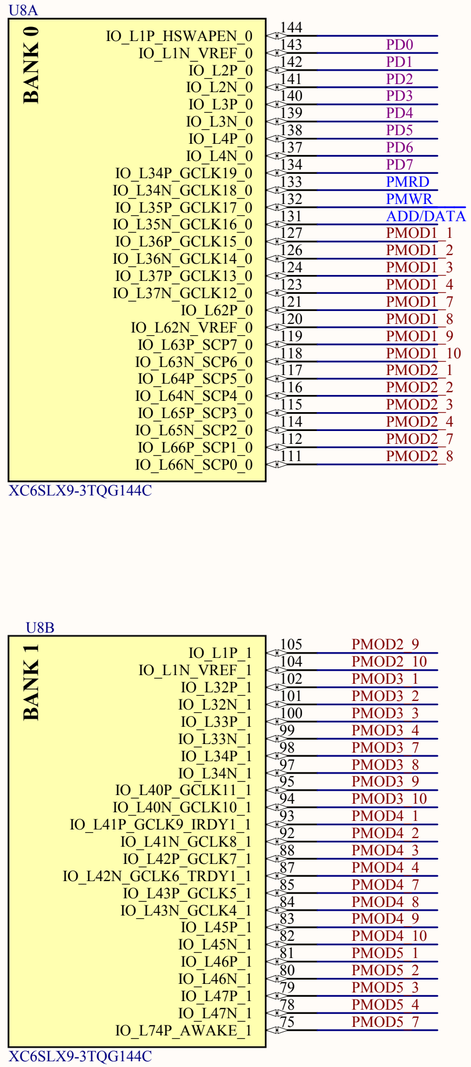
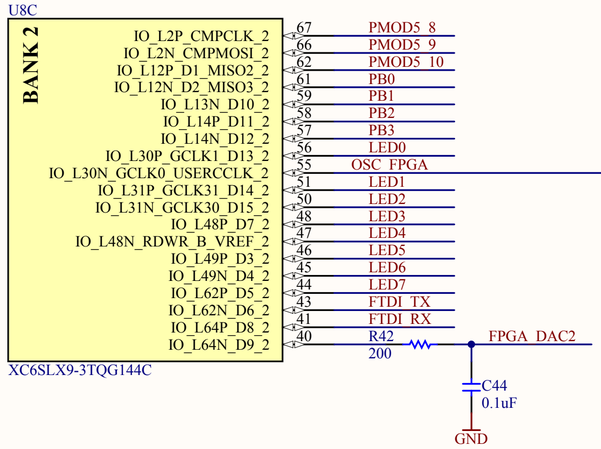
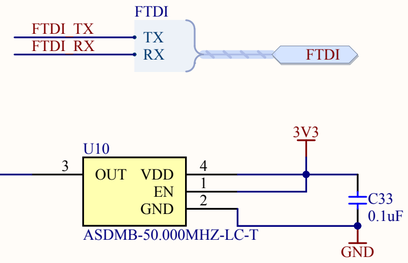


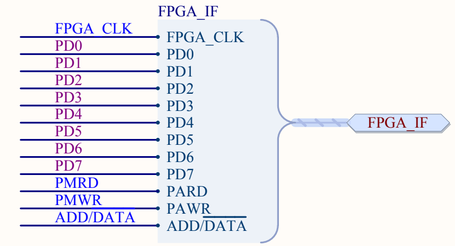
Wavenumber Technologies	**Power Supply**
Rev: α	**FPGA MARK-1**
Sheet 1 of 7	**E.Hughes**

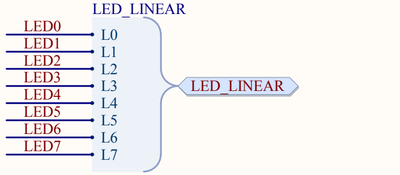


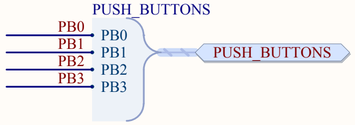


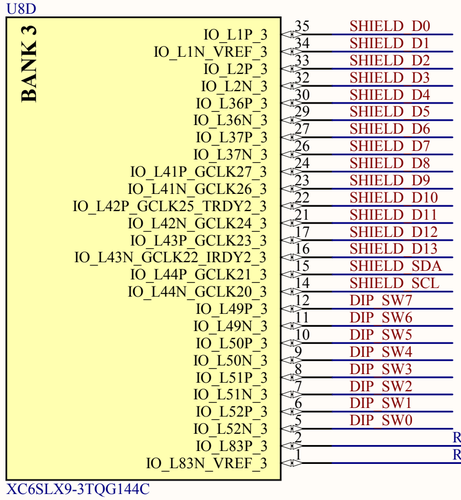


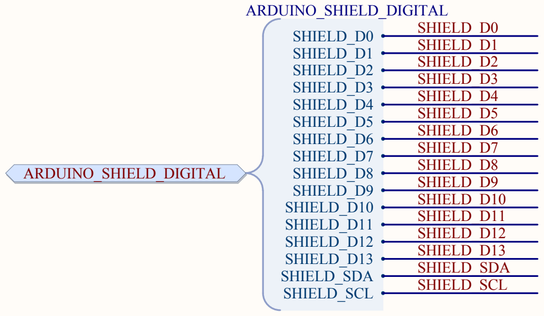


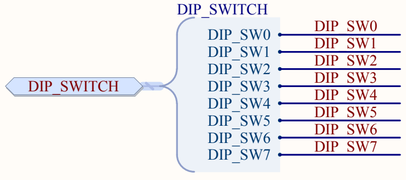




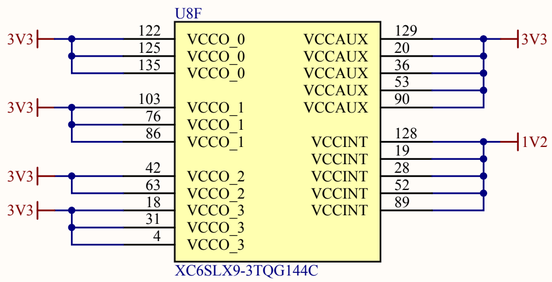


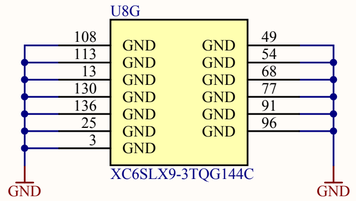


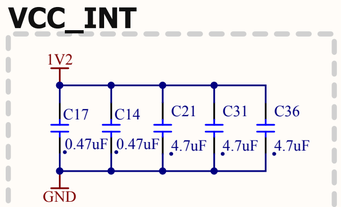


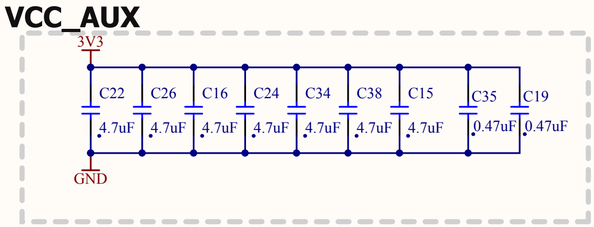


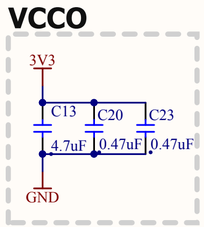
2πλ⁻¹ Wavenumber Technologies	FPGA-LOGIC	
	Rev: α	FPGA MARK-1
	Sheet 2 of 7	E.Hughes

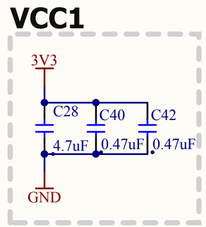


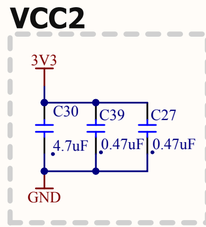


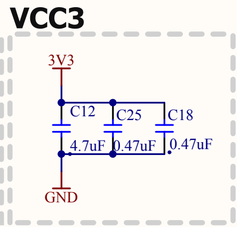




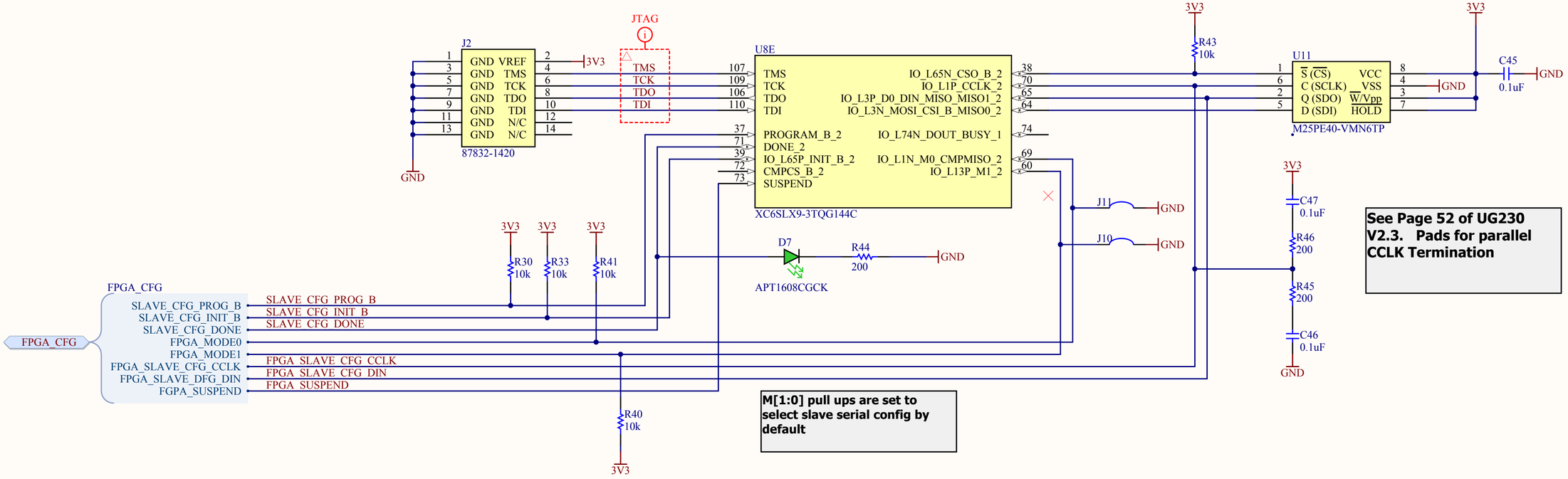








Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution



Wavenumber Technologies	FPGA-CONFIG	
	Rev: α	FPGA MARK-1
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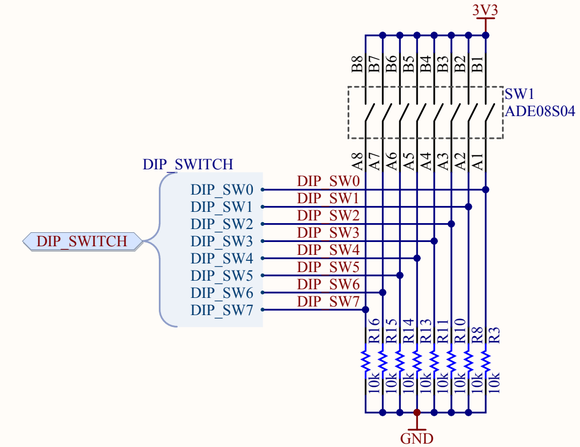
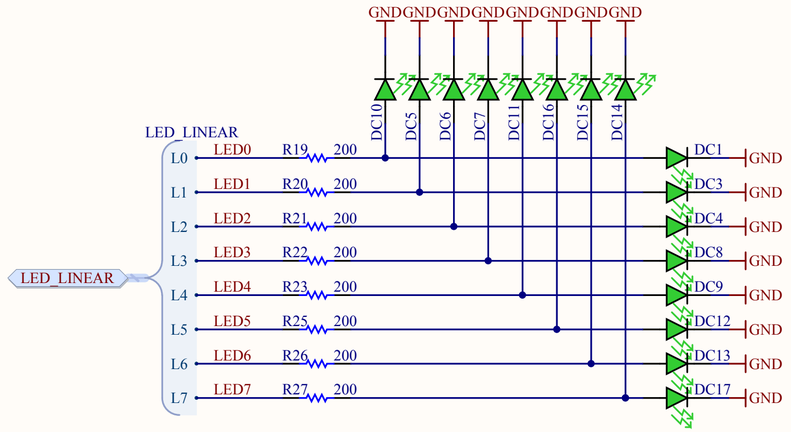
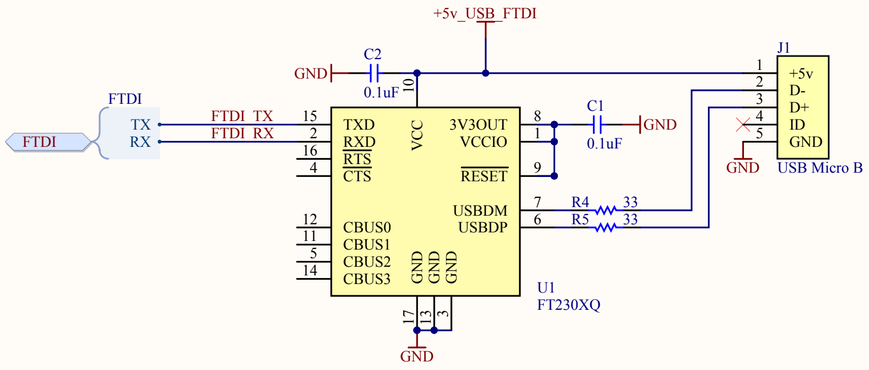
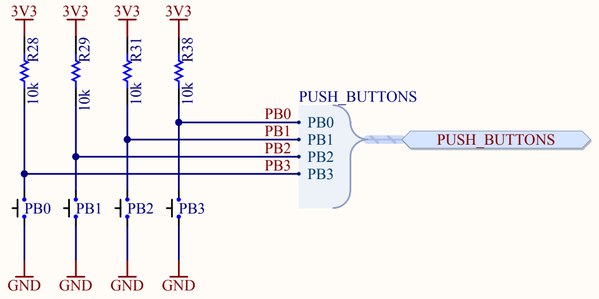
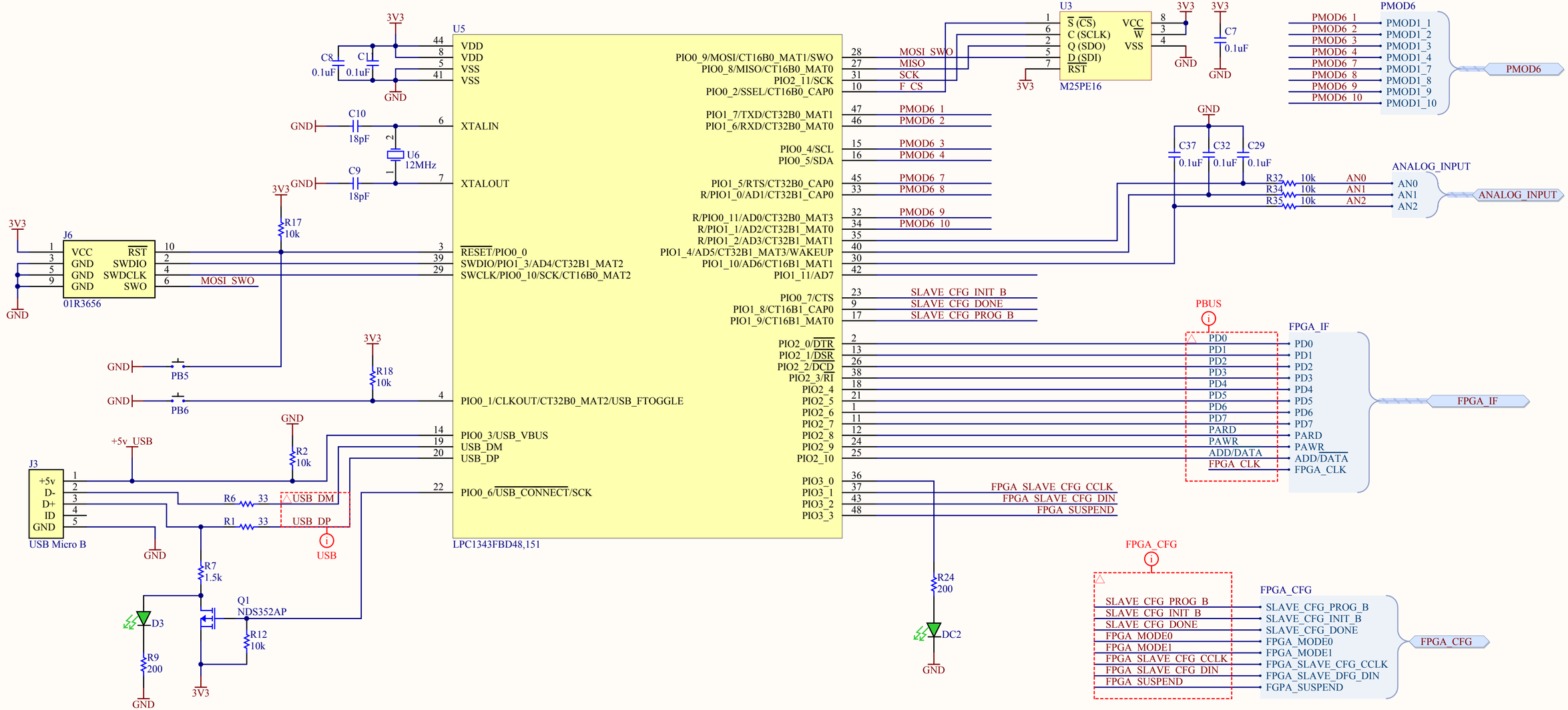




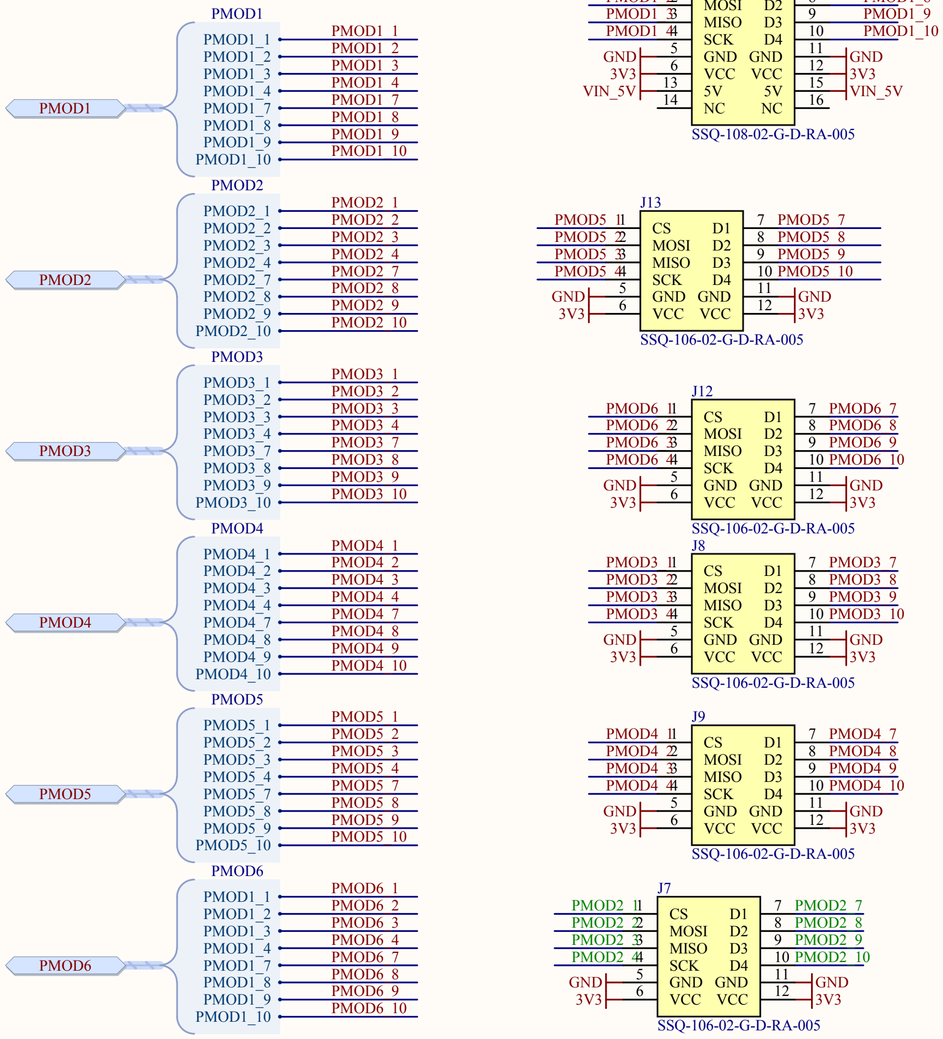




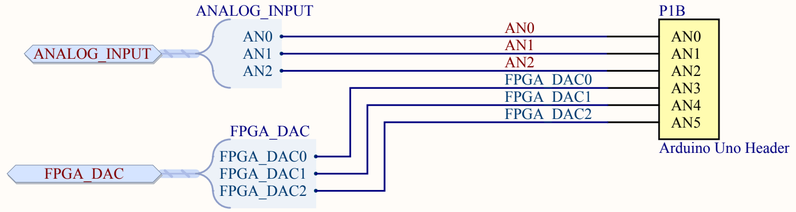
Wavenumber Technologies	Digital IO	
	Rev: α	FPGA MARK-1
	Sheet 4 of 7	E.Hughes

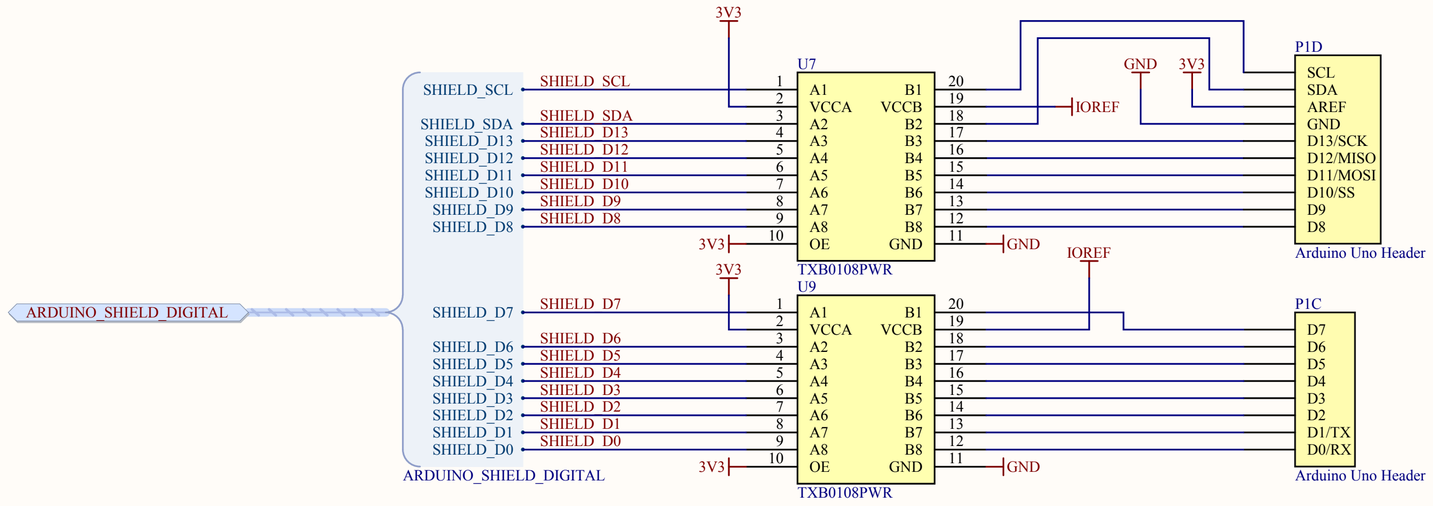


Wavenumber Technologies	MCU-LOGIC
Rev: α	FPGA MARK-1
Sheet 5 of 7	E.Hughes

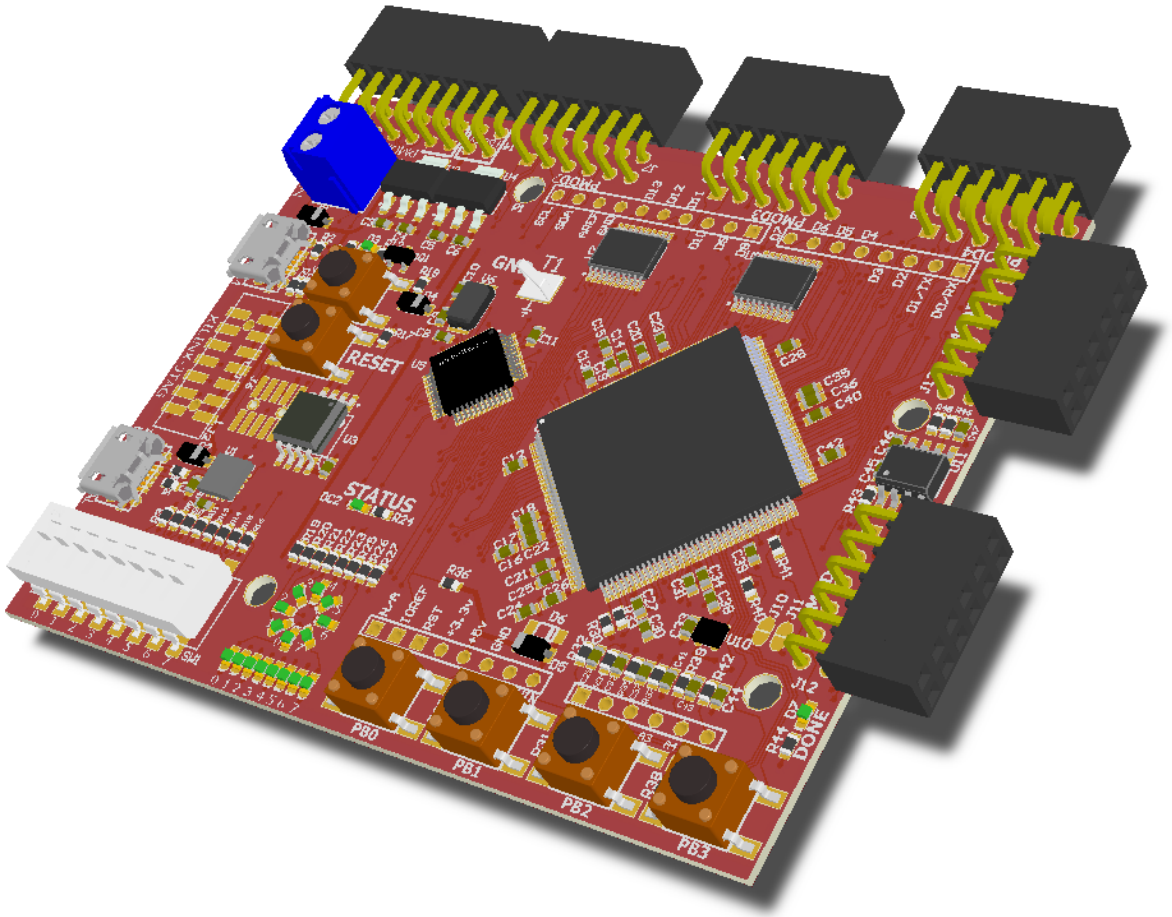


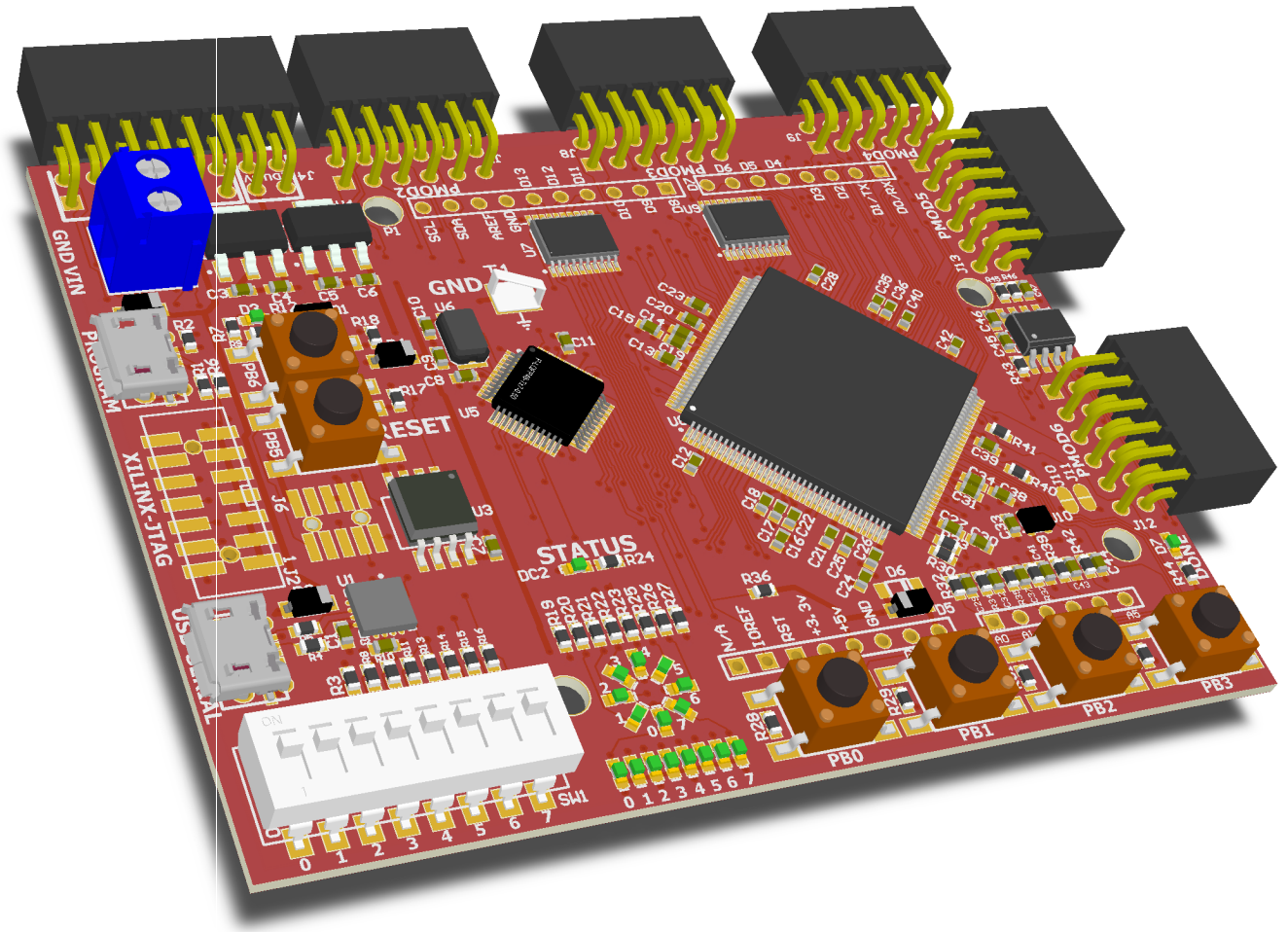
Wavenumber Technologies	**PMOD IO**
Rev: α	**FPGA MARK-1**
Sheet 6 of 7	**E.Hughes**





2πλ⁻¹ Wavenumber Technologies	Arduino IO	
	Rev: α	FPGA MARK-1
	Sheet 7 of 7	E.Hughes


RESET
STATUS
PB0
PB1
PB2
PB3
DONE


GND VIN
PMOD2
PMOD3
PMOD4
PMOD5
PMOD6
PMOD7
GND
RESET
STATUS
XILINX-JTAG
PB0
PB1
PB2
PB3
SW1
0 1 2 3 4 5 6 7