NXP Semiconductors
User's Guide

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Hardware Development Guide for the RT600 Processor

Contents

Chapter 1
Introduction

This document’s purpose is to help hardware engineers design and test their RT600 processor-based designs. It provides information about board layout recommendations and design checklists to ensure first-pass success and avoidance of board bring-up problems.

This guide is released along with the relevant device-specific hardware documentation such as data sheets, reference manuals, and application notes available on nxp.com.

Chapter 2
Background

The RT600 is a family of dual-core microcontrollers for embedded applications featuring an Arm® Cortex®-M33 CPU combined with a Cadence Xtensa HiFi4 advanced Audio Digital Signal Processor CPU. The Cortex-M33 includes two hardware coprocessors providing enhanced performance for an array of complex algorithms. The family offers a rich set of peripherals and very low power consumption. The RT600 processors are specifically useful for applications such as:

- High-end audio device
- Motor control
- Home appliances
- IoT

Chapter 3
Power supply

See Table 1 to Table 3 for the power domains and power supply decoupling recommendations.

Table 1. Power domains

Power rail	MIN (V)	TYP (V)	MAX (V)	Description
LDO_ENABLE	—	—	—	When 1, enables the on-chip regulator to power core logic through the VDDCORE pins. Tie low if an off-chip PMIC is used to supply power to core logic. This pin can not be left floating. 100 K external pull-up or 10 K external pull-down is recommended.
VDD_AO1V8	1.71	1.80	1.89	Supply 1.8 V supply for **always on** features. This includes the RTC, RESETN, LDO_ENABLE, PMIC_IRQ_N, PMIC_MODE0, and PMIC_MODE1.
VDDIO_0	1.71 3.00	1.8 3.30	1.89 3.60	Single 1.8 V to 3.3 V power supply for GPIOs defined as belonging to the VDDIO_0 group. VDDIO_0, VDDIO_1, and VDDIO_0 may be supplied at different voltage levels as needed by the application. VDDIO_0 supplies the following port pins: • PIO0_0 to PIO0_13 • PIO1_11 to PIO1_29 • PIO2_12 to PIO2_23 • PIO3_25 to PIO3_31 • PIO4_0 to PIO4_10 • PIO7_24 to PIO7_31 • PIO5_19 to PIO5_31 • PIO6_0 to PIO6_27
VDDIO_1	1.71 3.00	1.80 3.30	1.89 3.60	Single 1.8 V to 3.3 V power supply for GPIOs defined as belonging to the VDDIO_1 group. VDDIO_0, VDDIO_1, and VDDIO_1 may be supplied at different voltage levels as needed by the application. VDDIO_1 supplies the following port pins: • PIO0_14 to PIO0_31 • PIO1_0 to PIO1_10 • PIO2_24 to PIO2_31 • PIO3_0 to PIO3_24 • PIO4_11 to PIO4_31 • PIO5_0 to PIO5_18

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Table 1. Power domains (continued)

Power rail	MIN (V)	TYP (V)	MAX (V)	Description
VDDIO_2	1.71 3.00	1.80 3.30	1.89 3.60	Single 1.8 V to 3.3 V power supply for GPIOs defined as belonging to the VDDIO_2 group. VDDIO_0, VDDIO_1, and VDDIO_2 may be supplied at different voltage levels as needed by the application. VDDIO_2 supplies the following port pins: • PIO1_30 to PIO1_31 • PIO2_0 to PIO2_11
VDD1V8	1.71	1.80	1.89	1.8 V supply voltage for on-chip analog functions other than the ADC and comparator.
VDDA_ADC1V8	1.72	1.80	1.89	1.8 V analog supply voltage for ADC and comparator.
VDDA_BIAS	1.71	1.80	1.89	Must equal to max analog input voltage. For ADC and comparator input range from 0 – 1.8 V, connect VDDA_BIAS to 1.8 V.
	3.0	3.30	3.6	Must equal to max analog input voltage. For ADC and comparator input range from 0 - 3.3 V, connect VDDA_BIAS to 3.3 V.
VDDCORE/VDDCORE_CAP	0.7	1.0	1.155	The minimum voltage is 0.7 in retention mode, and 0.85 in active mode. Power supply for core logic may be supplied from the on-chip regulator or by an off-chip PMIC. An external filter capacitor is always required on these pins. For detais. see the power connection information for values and other recommendations.
	0.85	1.0	1.155	
VREFP	1.71	1.80	1.89	ADC positive reference voltage.
VREFN	—	0	—	ADC negative reference voltage. Tie to the Ground.
USB_VBUS	4.4	5	5.5	VBUS pin (power on USB cable).
USB1_VDD3V3	3.00	3.30	3.60	USB1 analog 3.3 V supply.

Table 2. Power supply decoupling recommendations

Power Pin	Decoupling and bulk capacitors (min qty)	Description
VDD_AO1V8	2 × 0.1 µF[1] + 1 × 10 µF[2]	Place at least one 10 µF capacitor to VDD_AO1V8 and place each 0.1 µF capacitor next to each ball.
VDDIO0	7 × 0.1 µF[1] + 1 × 10 µF[2]	Place at least one 10 µF capacitor to VDDIO0 and place each 0.1 µF capacitor next to each ball.

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Table 2. Power supply decoupling recommendations (continued)

Power Pin	Decoupling and bulk capacitors (min qty)	Description
VDDIO1	7 × 0.1 µF[1] + 1 × 10 µF[2]	Place at least one 10 µF capacitor to VDDIO1 and place each 0.1 µF capacitor next to each ball.
VDDIO2	3 × 0.1 µF[1] + 1 × 10 µF[2]	Place at least one 10 µF capacitor to VDDIO2 and place each 0.1 µF capacitor next to each ball.
VDD1V8	9 × 0.1 µF[1] + 1 × 10 µF[2]	Place at least one 10 µF capacitor to VDD1V8 and place each 0.1 µF capacitor next to each ball.
VDDCORE	8 ×0.1 µF[1] + 1 × 10 µF[2]	Place at least one 10 µF capacitor to VDDCORE and place each 0.1 µF capacitor next to each ball. The 0.1 µF capacitor must place within 50 mil from VDDCORE_CAP pads.

1. For the 0.1 µF capacitors, use the 0201 package.
2. For the 10 µF capacitors, the 0603 package is preferred; the 0805 and 1206 packages are acceptable.

Table 3. Power sequence and recommendations

Item	Recommendation	Description
1. Power sequence	Comply with the power-up/power-down sequence guidelines (as described in the data sheet) to guarantee a reliable operation of the device.	PMIC is not a must for RT600 power sequence. If not using PMIC, users should power RT600 in the following sequence: 1. VDD_AO1V8, VDD1V8, and VDD1V8_1 pins should be powered first. There is no power sequence requirement between powering the VDD_AO1V8 and VDD1V8 pins. 2. VDDA_ADC1V8 and VREFP can be powered concurrently with VDD_AO1V8 and VDD1V8 or later. 3. VDDIO_x and VDDA_BIAS pins can be powered concurrently with VDD_AO1V8 and VDD1V8 if these pins are 1.8 V range or later if these pins are 3.3 V range.

When the external PMIC is not used, the VDDCORE pin will be supplied from the internal LDO and the LDO is powered from the VDD1V8. An external capacitor (4.7 µF) must be connected on the VDDCORE pin.

When using external PMIC, RESETN should be held low until vddcore is valid in the timing diagram. VDDCORE should not be ramped up until after all the other supplies have completed ramp up. Figure 1 shows the timing diagram.

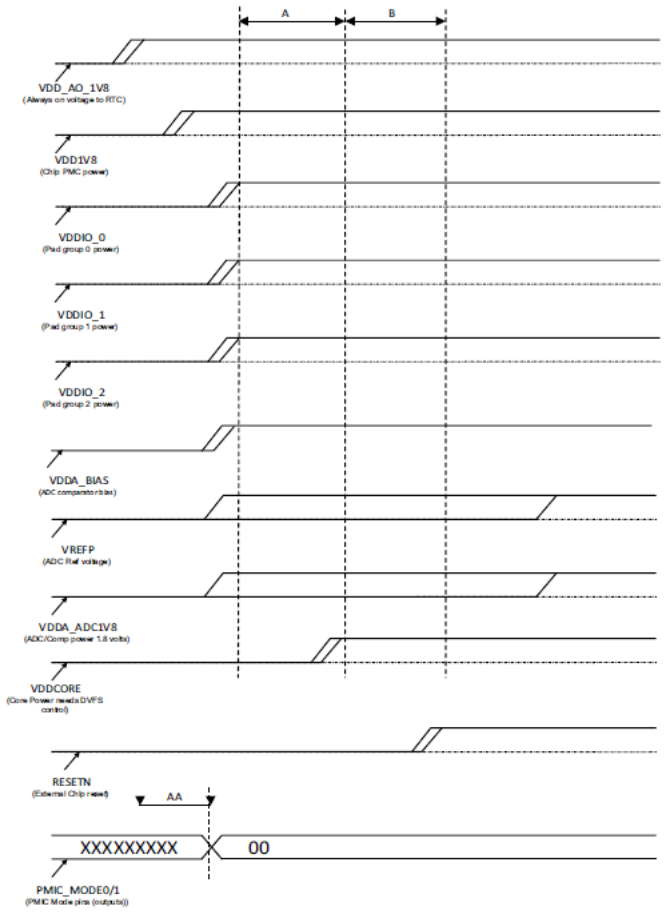


Figure 1. Power-up timing diagram

3.1 Power supply for pins

Table 4 describes the GPIOs belonging to the specific VDDIO groups and VDD_AO1V8 domain. Each VDDIO supply pin may be supplied at different voltage levels as needed by the application and can be powered between 1.71 V to 3.6 V.

Table 4. Power supply for pins

Power pins domain	GPIO pins
VDDIO_0	PIO0_0 to PIO0_13 PIO1_11 to PIO1_29 PIO2_12 to PIO2_23
VDDIO_1	PIO0_14 to PIO0_31 PIO1_0 to PIO1_10 PIO2_24 to PIO2_31 PMIC_I2C_SCL PMIC_I2C_SDA

Table continues on the next page...

Table 4. Power supply for pins (continued)

Power pins domain	GPIO pins
VDDIO_2	PIO1_30 to PIO1_31 PIO2_0 to PIO2_11
VDD_AO1V8	RESETN LDO_ENABLE PMIC_IRQ_N PMIC_MODE0 and PMIC_MODE1

3.2 Recommendation for RT600 when using PMIC (PCA9420)

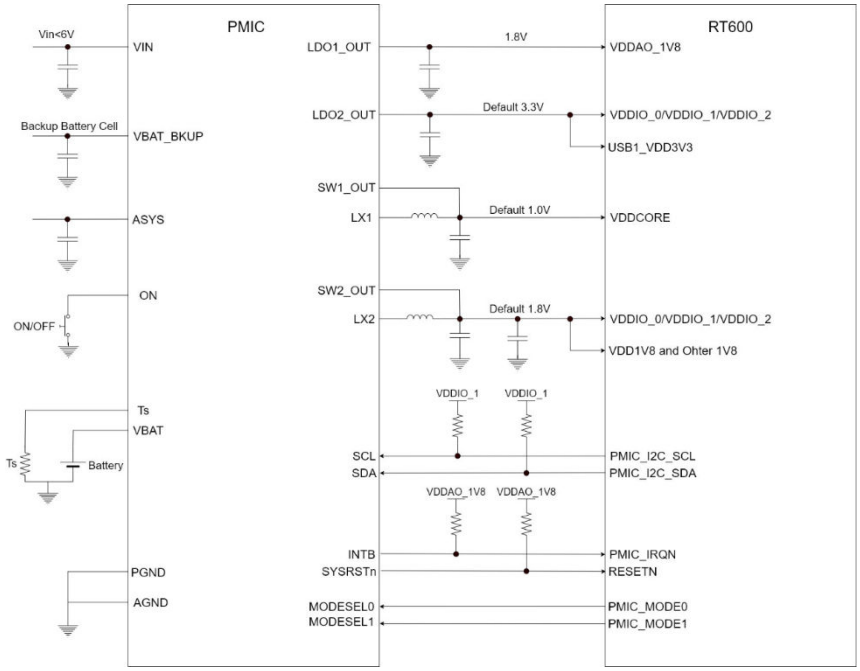


Figure 2. Power diagram with PMIC

When using PCA9420 SW2_OUT as the power supply for VDD1V8, it supplies analog circuits, such as Crystal, FRO and PLL. In low load conditions, Load current < 50 mA, the PCA9420 SW2_OUT has more than 20 mV of low frequency ripple ranging from 4 KHz to 30 KHz depending on the load. The reason is that the PMIC uses PFM mode at lower loads and 1 MHz PWM mode at higher loads. Due to the multiple options available for configuring and connecting the PMIC to RT device, if the switching output SW2 is used to power an analog input of the RT device, the low frequency ripple can propagate through the crystal circuit and unwanted jitter is observed on the clock using CLKOUT pin.

Table 5 displays the jitter observed when using SW2_OUT vs using LDO.

Table 5. Clock configurations

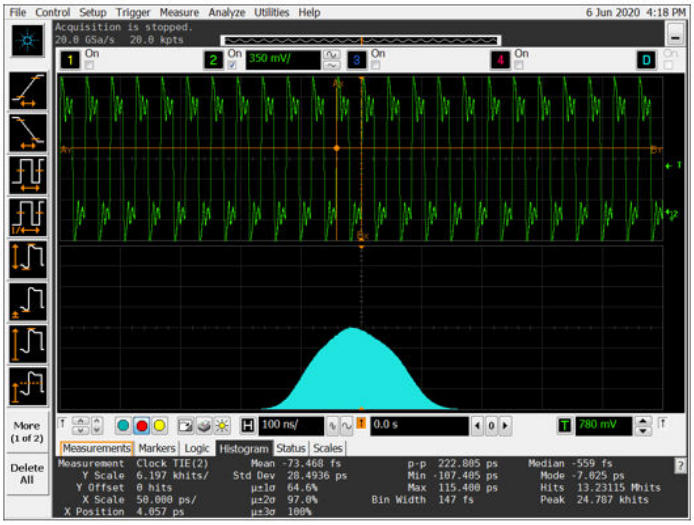
	Using SW2_OUT (PMIC)		Using LDO	
Test case	TIE - StdDev	TIE - Pk-2-Pk	TIE - StdDev	TIE - Pk-2-Pk
	ps	ps	ps	ps
Oscillator to Clkout	28.5	222.8	20.45	268.7
Oscillator to PLL to Clkout	28.1	220.1	21.79	205.4

The following figures show the jitter being measured by oscilloscope:

- 24 MHz OSC CLKOUT PMIC

Project	RT685
Board	EVK TR20100647
Measurement	TIE

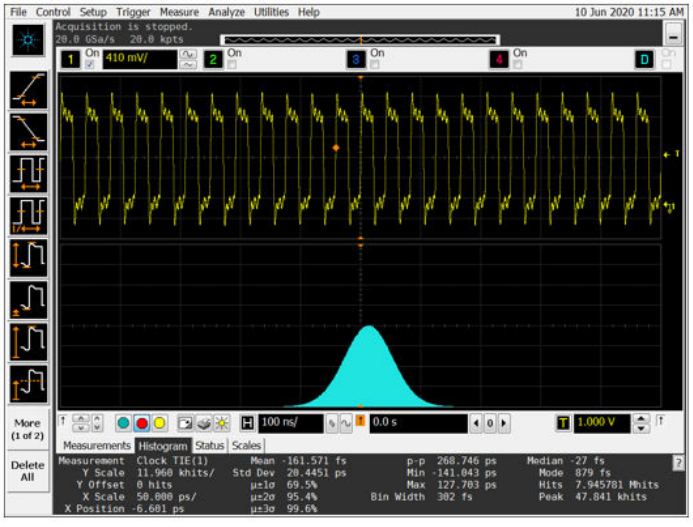
Conditions	24 OSC to ClkOut, No Chip Activity
STD Dev	28.5 ps
Peak-2-Peak	222.8 ps



- 24 MHz OSC CLKOUT LDO

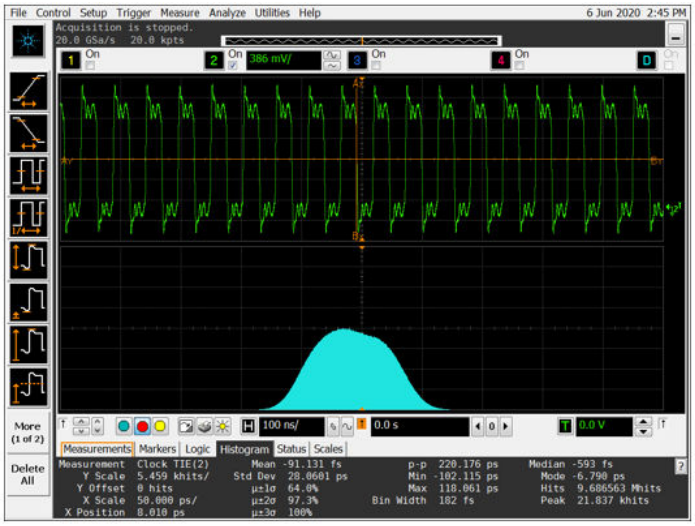
Project	RT685
Board	EVK TR20100647
Measurement	TIE

Conditions	24 OSC to ClkOut
STD Dev	20.45 ps
Peak-2-Peak	268.7 ps



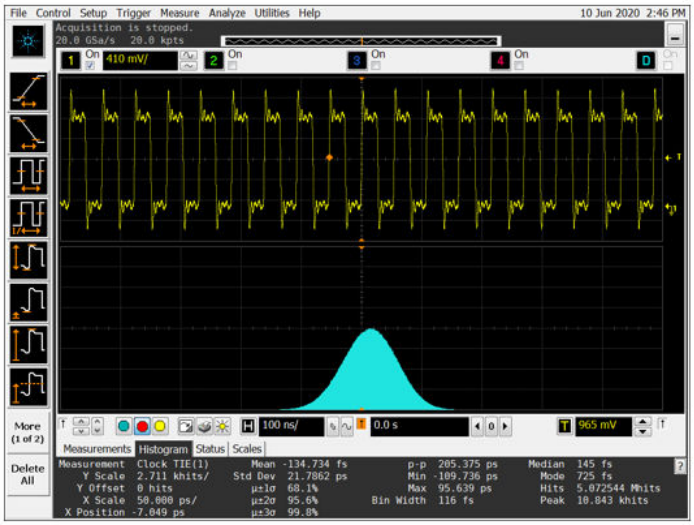
- PLL to CLKOUT PMIC

Project	RT685
Board	EVK TR20100647
Measurement	TIE
Conditions	PLL to CLKOUT /16, No Activity
STD Dev	28.1 ps
Peak-2-Peak	220.1 ps



- **PLL to CLKOUT LDO**

Project	RT685
Board	EVK TR20100647
Measurement	TIE
Conditions	PLL to CLKOUT /16, Run Hammer
STD Dev	21.79 ps
Peak-2-Peak	205.4 ps



There are two ways to solve this issue:

1. Use PCA9420 `SW2_OUT` as the power supply for VDD1V8. In this way, an additional bulk capacitance with value of 30-uF on `SW2_OUT` will be needed to reduce ripple. It was tested that an additional 30-uF could reduce the ripple by approximately one half. Low ESR ceramic capacitors are strongly recommended.
2. Use an LDO as the power supply of VDD1V8 pin.

3.3 Recommendation for RT600 with external discrete regulator

When using the external discrete regulator as the power supply domain for RT600, there are some recommendations shown as below:

- Keep the power pin voltage in recommended range shown in Table 1. Assign the right voltage for GPIOs with setting corresponding power supply pins shown in Table 4.
- Pay attention to the power sequence without PMIC shown in Table 3.
- The `VDDCORE` could be powered by on-chip regulator by setting the LDO enable pin to logic **1**.

Chapter 4
Clocks

Table 6 describes the clock configurations. The 32.768-kHz and a high-frequency oscillator (4-32 MHz) are used for the RT600 design.

Table 6. Clock configurations

Signal name	Recommended connections	Description
RTCXIN/RTCXOUT	Connect a 32.768 kHz crystal between RTCXIN and RTCXOUT. Choose a crystal with Load Capacitance (LC) of 9 to 12.5 pF, maximum Equivalent Series Resistance (ESR) of 80 kΩ, and typical drive level of 0.1 uW. For guidance on selecting external load capacitor values, see the RTC Oscillator section in *RT600 Product data sheet* (document RT600).	Use short traces between the crystal and the processor, with a ground plane under the crystal, load capacitors, and associated traces.
XTALIN/XTALOUT	Connect a high-frequency, fundamental-mode crystal between XTALIN and XTALOUT. Choose a crystal with CL of 8 to 18 pF, maximum ESR of 60 ohms for 32 MHz (80 Ω for 24 MHz and 100 Ω for 16 MHz), and typical drive level of 10 uW. For guidance on selecting external load capacitor values, see the XTAL Oscillator section in *RT600 Product data sheet* (document RT600).	If this clock is used as a reference for USB, there should be strict frequency tolerance and jitter requirements.

When using an external clock as the clock source input, there are two ways to do the circuit design.

1. Use the XTALIN pin as the active oscillator input source in bypass mode. Set bit 1 to **1** in the system oscillator control 0, `CLKCTL0_SYSOSCCTL0`, float the XTALOUT pin, and drive XTALIN with the voltage range from 0.7 to 1.8 V.
2. Use the CLKIN pin as the active oscillator input source. Set CLKIN PIN as clock function by setting the IOCON. Then set `SYSOSCBYPASS[2:0]` to **1**, which is used to set the CLKIN function as the external source for the internal `clk_in` signal.

Table 7. Dynamic characteristics of external clock and CLKIN pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_i	Input frequency	—	—	—	50	MHz
Voltage	IO voltage	—	1.71	—	3.6	V

Table 8. SYSCON PIN description

Function	Type	Available pins	Description
CLKIN	I	`PIO0_25`, `PIO2_15`, `PIO2_30`	External clock input
CLKOUT	O	`PIO0_24`, `PIO1_10`, `PIO2_29`	CLKOUT clock output

Chapter 5
Debugging and programming

The LPCLink2 on the EVK board is implemented as a debugger, which eliminates the cost for the users. It provides the debug connection via SWD interface.

See Table 9 for the SWD signals design recommendation. The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.

Table 9. SWD signals design recommendation

Signals	Recommendation	Description
SWDIO[1]	An external 10 kΩ pull-up resistor is recommended.	Bi-directional debug data signal for SWD.
SWCLK[2]	An external 10 kΩ pull-up resistor is recommended.	Clock signal to target for SWD
SWO	—	The SWO pin optionally provides data from the ITM for an external debug tool to evaluate.

1. At reset release, there is a weak pull-up internally on this pin. But it is disabled by default.
2. At reset release, there is a weak pull-down internally on this pin. But it is disabled by default.

Table 10. Flash loader peripheral I/Os

Signals	Recommendation	Description
UART0	The Serial Downloader provides a means to download a program image to the chip over the USB and UART/I2C/SPI serial connections. In this mode, ROM continuously polls for the USB or flexcomm connection. If no activity is found on USB1 or flexcomm and the watchdog timer expires, the Arm core is reset.	The ROM code firstly polls the communication interface According to ISP [0:2] settings. The ROM enables the internal pull-up resistor on the UART pins to avoid an invalid trigger of the UART port in the serial download mode. Before jumping to the user application, the boot ROM resets the UART for user configurations.
I2C2		
SPI14(HS_SPI)		
USB1		

Chapter 6
Boot, reset, and miscellaneous

See Table 11 for the boot, reset, and miscellaneous configurations, such as ON/OFF, TEST_MODE, NC pins, and other.

Table 11. Boot configurations

Item	Recommendation	Description
ISP [2:0] ISP2: PIO1_17 ISP1: PIO1_16 ISP0: PIO1_15	1. Use **ISP[2:0] = 110**(Serial ISP) for debug. 2. Following layout is proposed for ease of use on boards using push buttons. ROM enables internal pull-ups on these pins and reads the state during boot time to determine the mode. Single button press is needed for most commonly used boot modes.	111-(ISP[2:0]) - Serial-master boot (SPI-slave, I2C-slave, UART or USB-HID) is used to download a boot image over the serial interface. 110 - Serial ISP (UART, SPI-slave, I2C-slave or USB-HID) is used to program OTP, external Flash, SD or eMMC device. 101 - Reserved 100 - SDIO0 (eMMC) 011 - FlexSPI port A 010 - FlexSPI port B 001 - SDIO0 (SD card) 000 - Reserved (for test mode)

Table 12. Reset and miscellaneous recommendations

Item	Recommendation	Description
1. RESETN	If the external RESETN signal is used to control the processor RESETN, then RESETN must be immediately asserted at the power-up and remain asserted until the VDDCORE and VDD1V8 supplies are stable.	—

Table 13. ROM bootloader peripheral PinMux

Boot device	IO function/comments	Pins
FlexSPI0 Port A	CLK	P1 (18)
	SSEL0	P1 (19)
	D0	P1 (20)
	D1	P1 (21)
	D2	P1 (22)
	D3	P1 (23)
	D4	P1 (24)
	D5	P1 (25)

Table continues on the next page...

Table 13. ROM bootloader peripheral PinMux (continued)

Boot device	IO function/comments	Pins
	D6	P1 (26)
	D7	P1 (27)
	DQS	P1 (28)
	SSEL1	P1 (29)
FlexSPI0 Port B	CLK	P1 (29)
	SSEL0	P2 (19)
	D0	P1 (11)
	D1	P1 (12)
	D2	P1 (13)
	D3	P1 (14)
	D4	P2 (17)
	D5	P2 (18)
	D6	P2 (22)
	D7	P2 (23)
	SSEL1	P2 (21)
USB	USB1_VBUS	
	USB1_VDD1V8	
	USB1_VDD3V3	
	USB1_DM	
	USB1_DP	
	USB1_ID	
SPI (FC14)	HS_SPI_SCK	P1 (11)
	HS_SPI_MISO	P1 (12)
	HS_SPI_MOSI	P1 (13)
	HS_SPI_SSELN0	P1 (14)
I2C (FC2)	SCL	P0 (15)

Table continues on the next page...

Table 13. ROM bootloader peripheral PinMux (continued)

Boot device	IO function/comments	Pins
	SDA	P0 (16)
UART (FC0)	TXD	P0 (1)
	RXD	P0 (2)
SDIO0	SD0_CLK	P1 (30)
	SD0_CMD	P1 (31)
	SD0_D0	P2 (0)
	SD0_D1	P2 (1)
	SD0_D2	P2 (2)
	SD0_D3	P2 (3)
	SD0_WR_PRT	P2 (4)
	SD0_D4	P2 (5)
	SD0_D5	P2 (6)
	SD0_D6	P2 (7)
	SD0_D7	P2 (8)
	SD0_CARD_DET	P2 (9)
	SD0_RESET_N	P2 (10)
	SD0_VOLT	P2 (11)
SDIO1	SD1_CLK	P3 (8)
	SD1_CMD	P3 (9)
	SD1_D0	P3 (10)
	SD1_D1	P3 (11)
	SD1_D2	P3 (12)
	SD1_D3	P3 (13)
	SD1_WR_PRT	P3 (14)
	SD1_D4	P3 (15)
	SD1_D5	P3 (16)

Table continues on the next page...

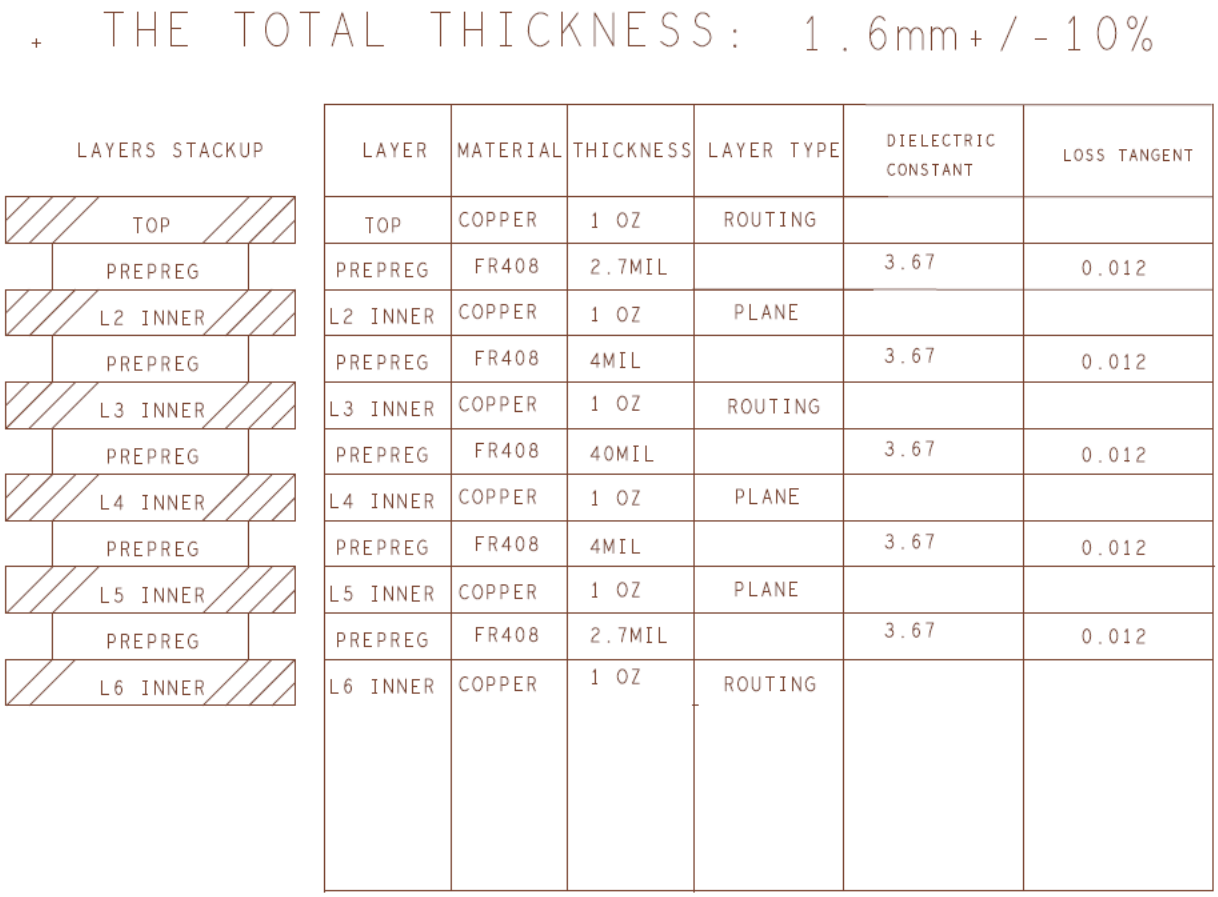
Table 13. ROM bootloader peripheral PinMux (continued)

Boot device	IO function/comments	Pins
	SD1_D6	P3 (17)
	SD1_D7	P3 (18)
	SD1_CARD_DET	P3 (19)
	SD1_RESET_N	P3 (20)
	SD1_VOLT	P3 (21)

Chapter 7
Layout recommendations

7.1 Stack-up

A high-speed design requires a good stack-up to have the right impedance for the critical traces.



LAYER	MATERIAL	THICKNESS	LAYER TYPE	DIELECTRIC CONSTANT	LOSS TANGENT
TOP	COPPER	1 OZ	ROUTING		
PREPREG	FR408	2.7MIL		3.67	0.012
L2 INNER	COPPER	1 OZ	PLANE		
PREPREG	FR408	4MIL		3.67	0.012
L3 INNER	COPPER	1 OZ	ROUTING		
PREPREG	FR408	40MIL		3.67	0.012
L4 INNER	COPPER	1 OZ	PLANE		
PREPREG	FR408	4MIL		3.67	0.012
L5 INNER	COPPER	1 OZ	PLANE		
PREPREG	FR408	2.7MIL		3.67	0.012
L6 INNER	COPPER	1 OZ	ROUTING		

Figure 3. Example stack-up

The constraints for the trace width depend on many factors, such as the board stack-up and the associated dielectric and copper thickness, required impedance, and required current (for power traces). The stack-up also determines the constraints for routing and spacing. Consider the following when designing the stack-up and selecting the material for your board:

- The board stack-up is critical for the high-speed signal quality.
- Preplan the impedance of the critical traces.
- The high-speed signals must have reference planes on adjacent layers to minimize crosstalk.
- The NXP reference design equals Isola FR4.
- The NXP validation boards equal Isola FR4.
- At least six-layer stack-up is recommended, with the layer stack shown in Figure 3.

Figure 4 shows the trace width and impedance requirements provided by NXP inside the fabrication detail as a part of the Gerber files.

DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE TOLERANCE IS 10%

Layers	Single Ended		Single Ended		Differential			Differential			Differential		
	Trace Width (Mils)	Impedance (Ohms)	Trace Width (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Airgap" (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Airgap" (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing "Airgap" (Mils)	Impedance (Ohms)
L1_TOP	4.5	50						4.5	5	90	4	7	100
L3 & L4	4.5	50						4.5	5	90	4	7	100
L6_BOTTOM	4.5	50						4.5	5	90	4	7	100

Figure 4. Example trace width and impedance implementation

7.2 Placement of bulk and decoupling capacitors

Place the small decoupling capacitors and the larger bulk capacitors on the bottom side of the CPU. The 0402 decoupling capacitors and the 0603 bulk capacitors must be placed as close as possible to the power balls. Placing the decoupling capacitors close to the power pins is critical to minimize inductance and ensure the high-speed transient current demand of the processor. The correct via size, trace width, and trace space are critical to preserve the adequate routing space. The recommended geometry is as follows:

- The via type is 18/8 mils, the trace width is 5 mils, and the trace space is 7 mils.
- Use the NXP design strategy for power and decoupling.

7.3 USB

Use these recommendations for the USB:

- Route the high-speed clocks and the DP and DM differential pair firstly.
- Route the DP and DM signals on the top (or bottom) layer of the board.
- The trace width and spacing of the DP and DM signals must meet the differential impedance requirement of 90 Ω.
- Route the traces over the continuous planes (power and ground):
  - They must not pass over any power/GND plane slots or anti-etch.
  - When placing the connectors, make sure that the ground plane clearouts around each pin have ground continuity between all pins.
- Maintain the parallelism (skew-matched) between DP and DM, and match the overall differential length difference to less than 5 mils.
- Maintain the symmetric routing for each differential pair.
- Do not route the DP and DM traces under the oscillators or parallel to the clock traces (and/or data buses).
- Minimize the lengths of the high-speed signals that run parallel to the DP and DM pair.
- Keep the DP and DM traces as short as possible.
- Route the DP and DM signals with a minimum amount of corners. Use 45-degree turns instead of 90-degree turns.
- Avoid layer changes (vias) on the DP and DM signals. Do not create stubs or branches.
- Provide the ground return vias within a 50-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.

7.4 High-speed signal routing recommendations

The following provides recommendations for routing the traces for high-speed signals.

NOTE

The propagation delay and the impedance control must match to have a correct communication with the devices.

- The high-speed signals (USB , SD card) must not cross gaps in the reference plane.
- Avoid creating slots, voids, and splits in the reference planes. Review the via voids to ensure that they do not create splits (space out vias).
- Provide the ground return vias within a 100-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- A solid GND plane must be directly under the crystal-associated components, and traces.
- The clocks or strobes that are on the same layer need at least 2.5× spacing from the adjacent traces (2.5× height from the reference plane) to reduce crosstalk.
- Provide the ground return vias within a 100-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- All synchronous modules must have the bus length matching and relative clock length control.
- For the SD module interfaces, Match the data, clock, and CMD trace lengths (length delta depends on the bus rates).

Chapter 8
Six-layer board design

8.1 MCU pinout

From design phase, RT600 pinout was adjusted properly to meet six-layer board design especially for some high speed signals. For example, signals like QSPI, SDHC, USB need to route at same length and don't across with each other, as shown in Figure 5.

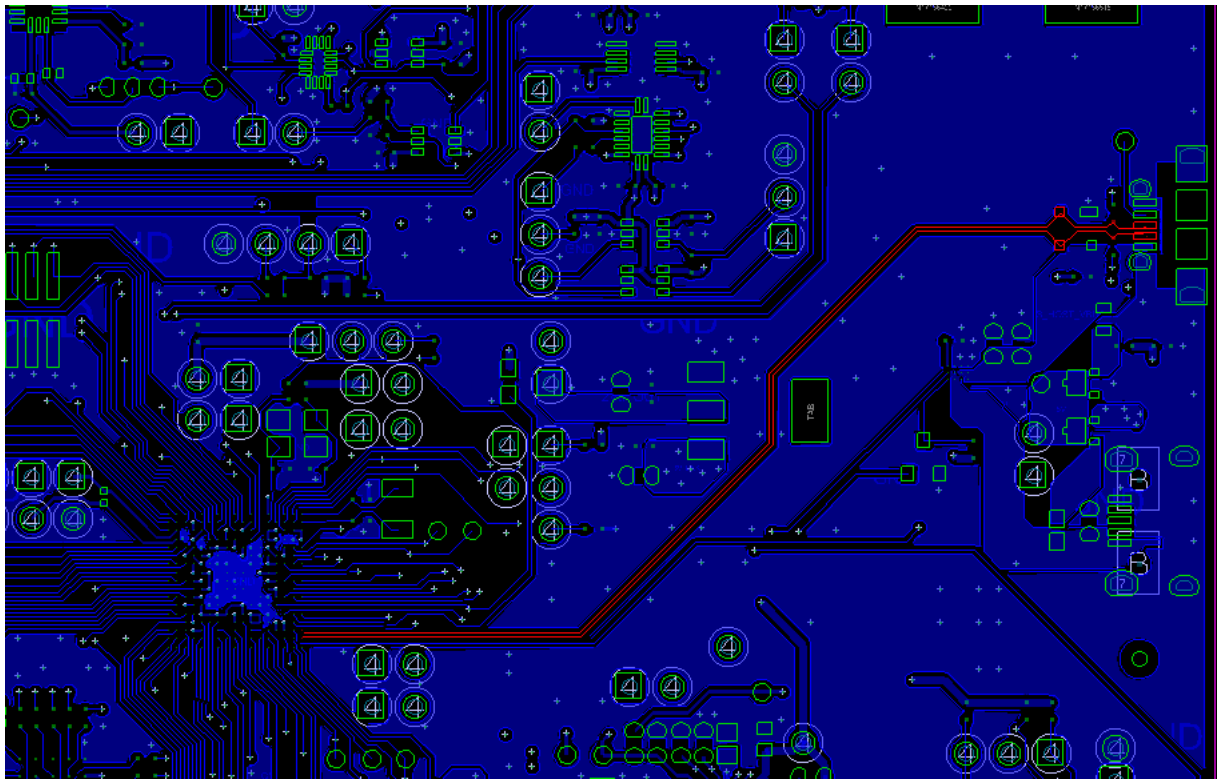


Figure 5. USB differential traces on RT600 EVK

8.2 Power supply

RT600 power supply is designed with six-layer board and almost each power domain will have GND pad in parallel, as shown in Figure 6. With such power pin design, it's easier for placing decoupling capacitor to the board.

At the same time, it needs to keep the bottom layer of MCU to have a somehow overall GND plane and make sure the board has a good current loop to the external power supply to improve the EMC performance, as shown in Figure 7.

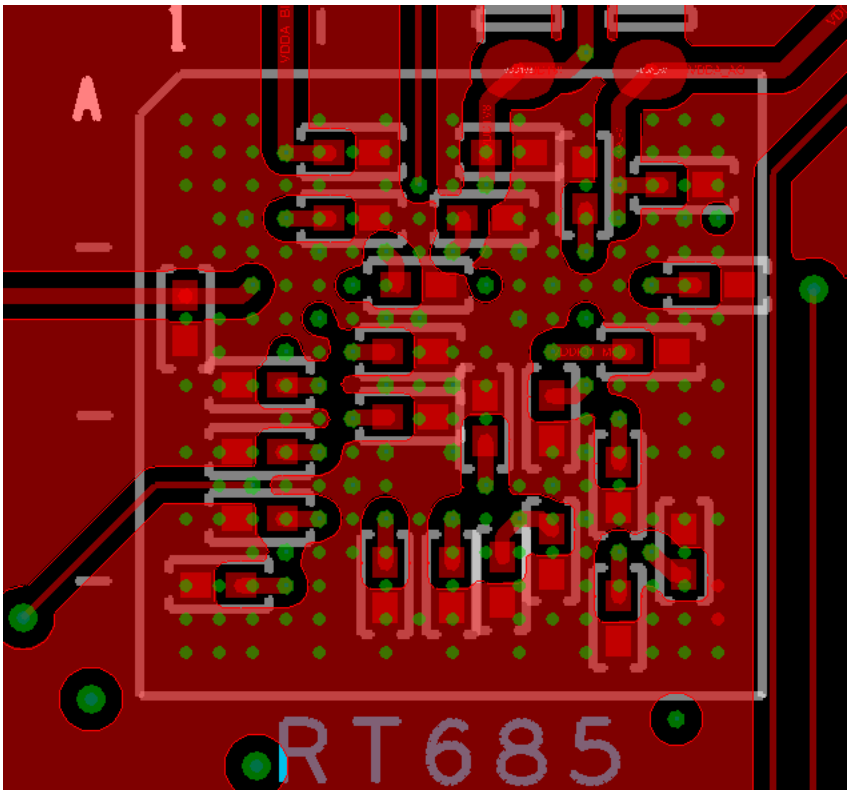


Figure 6. RT600-EVK MCU power

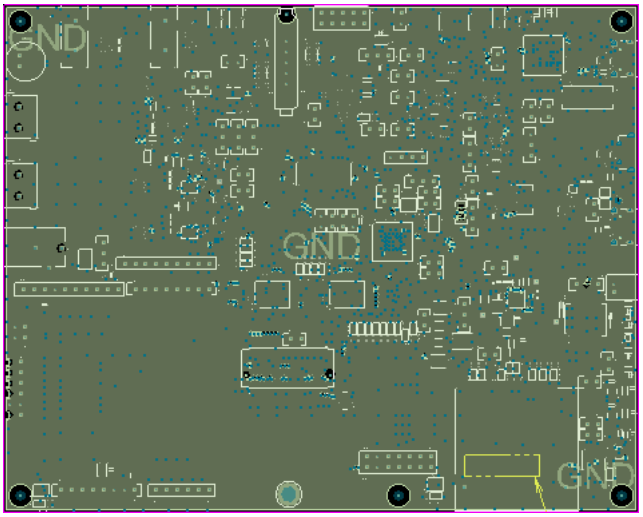


Figure 7. RT600-EVK GND plane

8.3 Routing rule

There are some general high speed layout guideline which mentioned above. For six-layer board design, it’s better to have each high speed signals with GND in parallel which will help impedance matching and improve the signal quality.

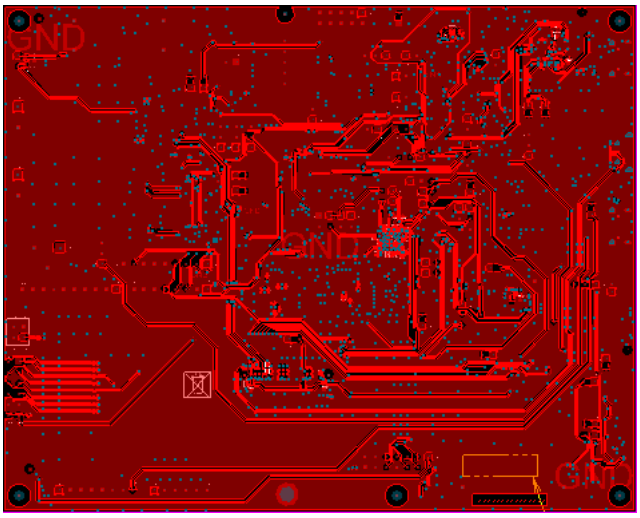


Figure 8. RT600-EVK bottom layer

Chapter 9
Revision history

Table 14. Revision history

Rev	Date	Description
0	03/2020	Initial release
1	08/2020	Updated Recommendation for RT600 when using PMIC (PCA9420) and Clocks

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