Farhana Sultana Chowdhury

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PROFESSIONAL SUMMARY

Electrical & Electronic Engineer specializing in semiconductor test methodologies and ASIC design principles. Demonstrated proficiency in end-to-end DFT implementation, including scan architecture development, automated test pattern generation, and fault coverage optimization exceeding industry benchmarks. My background combines academic knowledge and hands-on experience in VLSI, digital circuits, and microelectronics. Passionate about applying these skills in semiconductors, telecommunications, and tech industries to drive innovation and improve product quality.

WORK EXPERIENCE

Ulkasemi Private Limited **Dhaka**
Trainee Engineer, DFT, Silicon Engineering Department *December, 2024 – May, 2025*

- Deployed scan chains (Muxed-D), lockup latches, and clock domain management using Synopsys Design Compiler; resolved scanability DRCs and optimized chain balancing.
- Implemented On-Chip Clocking (OCC) for at-speed testing and IEEE 1500 Wrapper Cells for core isolation, managing OCC signals, wrapper operations (Intest/Extest), and grey-box modeling.
- Generated test patterns via Synopsys TetraMAX for stuck-at/transition faults; performed coverage analysis (95%+ targets), debugged AU/UD faults.
- Reduced test data volume through decompressor/compressor design, X-blocking.
- Owned synthesis, DFT planning, scan/compression/OCC/wrapper insertion, and ATPG for CM3_FPB & SSE050_Integration.
- Developed test plans and bench architectures in System Verilog & UVM for AMBA APB and 4-bit counter IPs using industry-standard methodologies.

EDUCATION

Ahsanullah University of Science and Technology **Dhaka**
B.Sc. in Electrical & Electronic Engineering | CGPA: 3.28 *2024*

Adamjee Cantonment College **Dhaka**
Higher Secondary Certificate | GPA: 5.00 *2018*

Matripith Govt. Girls' High School **Chandpur**
Secondary School Certificate | GPA 5.00 *2016*

LEADERSHIP EXPERIENCE

Information & Research Secretary *Fall 2022*
AUST Debating Club

- Organizer Of 5th AUSTDC National Debating Competition - 2023
- Conducted Classes on Basics of Debating.

Communication Secretary *Fall 2021*
AUST Debating Club

- Organizer of 4th AUSTDC national debating competition 2022
- Acted as convenor for multiple debating program
- Arranged online seminar & workshops and maintained communication with chief guest and speakers

Communication Secretary *Fall 2021*
AUST Debating Club

- Took part in multiple debating program

ACADDEMIC TRAINING

Neural Semiconductor Limited **Dhaka**
July 2024

- Overview of functions of a semiconductor company & its operation.
- Overview of RTL analog sector.
- Sessions on IC design.

CORE COMPETENCIES

- Physical Design Knowledge
- Design For Testability
- Problem Solving Skill
- Leadership
- Teamwork & Communication
- Adaptability

SKILLS & INTERESTS

- C++, Linux, Bash, TCL
- Verilog & System Verilog
- Modelsim
- Cadence IUS Tool
- Synopsys Design Compiler
- Synopsys Tetramax ATPG

ACADEMIC PROJECTS

Robotic Arm Motion Control via Computer Vision
(Hardware Implementation | Sensor Fusion | Embedded Systems)

CMOS Ring Oscillator: Design & Frequency Stability Analysis
(VLSI Design | Cadence Virtuoso | Performance Optimization)

PROFESSIONAL PROJECTS

CM3_FPB DFT Implementation
Scan Insertion | ATPG Pattern Generation | Synopsys DC/TetraMAX

SSE050 DFT Flow Automation
Scan Compression (CODEC) | OCC Integration | Fault Coverage Optimization

APB-SPI Protocol Verification Framework
Test Plan Development | Coverage-Driven Validation | UVM Compliance

FIELD OF INTEREST

- VLSI
- Physical Design & Verification
- Digital Electronics

REFERENCES

Md Mohfizul Islam
Managing Director
Motaleb Monowara Composite (Pvt) Ltd
Narayanganj
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Syed Shouvik Islam
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DFT (DV), Silicon Engineering Division
Ulkasemi Pvt. Limited, Bangladesh
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