Instruction	Clock 1	2	3	4	5	6	7	8	9	10	11	12
LW R1,0(R2)	IF	ID	EX	MEM	WB							
ADDI R1,R1,#1D		IF	stall(R1 unknown)	ID(R1)	EX	MEM	WB					
SW 0(R2),R1				IF	ID(R1)	EX	MEM	WB				
ADDI R2,R2,#4					IF	ID	EX	MEM	WB			
SUB R4,R3,R2						IF	ID (R2)	EX	MEM	WB		
BNEZ R4, Loop							stall(bus busy)	IF	ID(R4)	EX	MEM	WB
			Hazard								(calcul du PC)	IF

With new processor (dataram and coderam), the bus will not be busy