Description

EC-01M is an EtherCAT Master controller developed by NEXTW Technology Company. Host chips or devices can communicate with EC-01M by SPI or USB interface. EC-01M provides an easy way to migrate the EtherCAT master functions to the precise motion control applications.

Feature

EtherCAT

- Supports maximum 40 EtherCAT Slaves*
- Supports minimum 0.25ms DC cycle time
- Supports DCM Master Shift mode

Ethernet MAC Controller

- 100 Mbps data transmission
- Supports RMII interface

SPI Interface

- Supports full duplex slave mode
- MSB first transfer fashion
- Clock frequency up to 24 MHz

USB Interface

- USB 2.0 with on-chip transceiver
- Implements USB HID class

GPIO

- 6 general purpose TTL inputs
- 6 general purpose push-pull outputs

Application

PLC

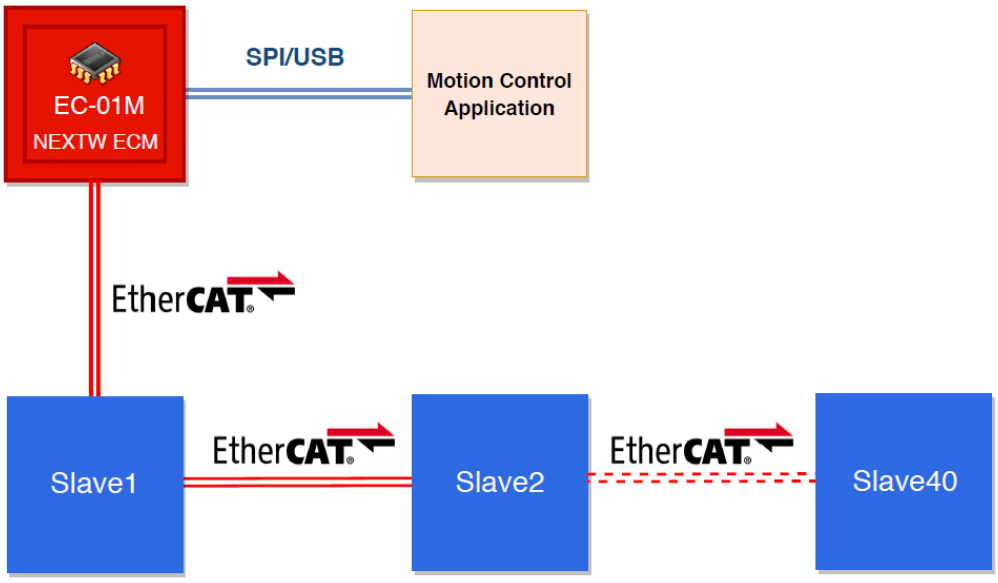
CNC

Robot

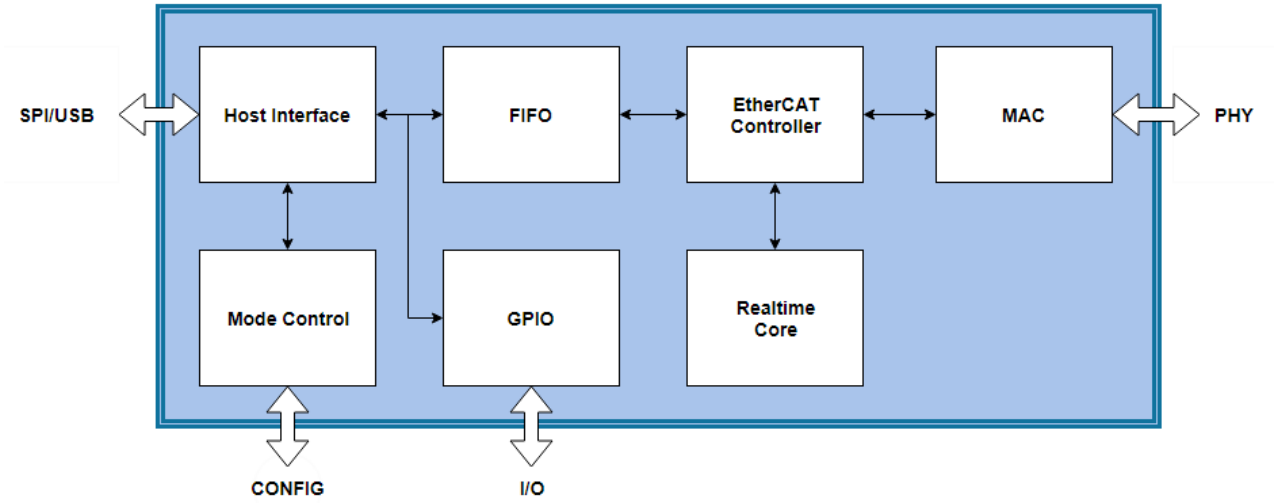
Automation

*Standard CANopen over EtherCAT(CoE) servo drives, NEXTW EtherCAT slaves. (Refer the support list)

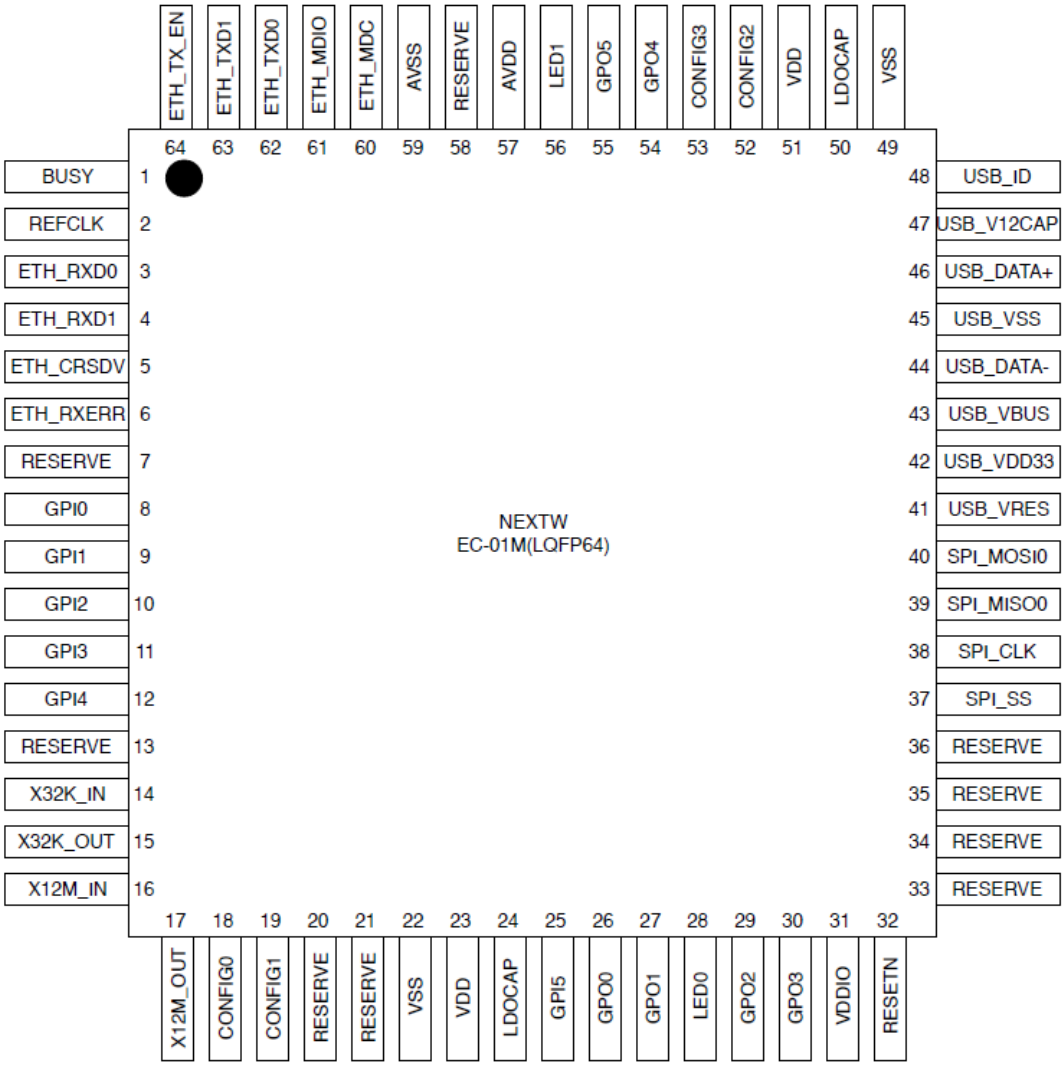
Typical Applications Diagram



Block Diagram



Pinout Diagram



Signal Description

Pin	Name	Type	Description
1	BUSY	O	System busy indicator pin.
2	REFCLK	I	EMAC RMII reference clock input pin.
3	ETH_RXD0	I	EMAC RMII receive data bus bit 0.
4	ETH_RXD1	I	EMAC RMII receive data bus bit 1.
5	ETH_CRSDV	I	EMAC RMII carrier sense/receive data input pin.
6	ETH_RXERR	I	EMAC RMII receive data error input pin.
7	RESERVE		
8	GPI0	I	General purpose digital input pin0.
9	GPI1	I	General purpose digital input pin1.
10	GPI2	I	General purpose digital input pin2.
11	GPI3	I	General purpose digital input pin3.
12	GPI4	I	General purpose digital input pin4.
13	RESERVE		
14	X32K_IN	I	External 32.768 kHz crystal input pin.
15	X32K_OUT	O	External 32.768 kHz crystal output pin.
16	X12M_IN	I	External 12 MHz crystal input pin.
17	X12M_OUT	O	External 12 MHz crystal output pin.
18	CONFIG0	I	Configuration pin 0.
19	CONFIG1	I	Configuration pin 1.
20	RESERVE		
21	RESERVE		
22	VSS	P	Ground pin for digital circuit.
23	VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
24	LDOCAP0	P	LDO output pin.
25	GPI5	I	General purpose digital input pin5.
26	GPO0	O	General purpose digital output pin0.
27	GPO1	O	General purpose digital output pin1.
28	LED0	O	LED output pin0.
29	GPO2	O	General purpose digital output pin2.
30	GPO3	O	General purpose digital output pin3.
31	VDDIO	P	Power supply for I/O ports

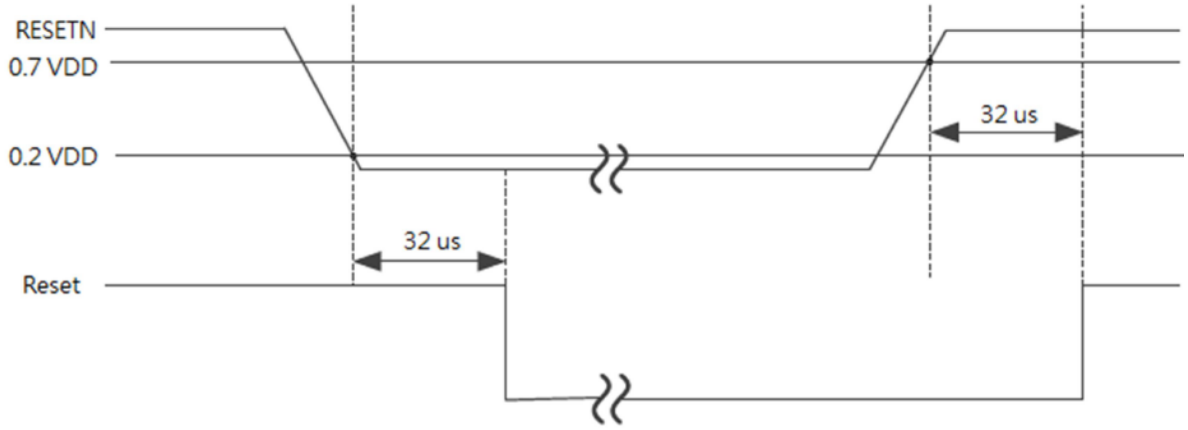
Pin	Name	Type	Description
32	RESETN	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
33	RESERVE		
34	RESERVE		
35	RESERVE		
36	RESERVE		
37	SPI_SS	I	SPI slave select pin.
38	SPI_CLK	I	SPI serial clock pin.
39	SPI_MISO	O	SPI MISO (Master In, Slave Out) pin.
40	SPI_MOSI	I	SPI MOSI (Master Out, Slave In) pin.
41	USB_VRES	A	USB module reference resister
42	USB_VDD33	P	Power supply for USB
43	USB_VBUS	P	USB power supply from USB host or HUB.
44	USB_D-	A	USB differential signal D-.
45	USB_VSS	P	Ground pin for USB.
46	USB_D+	A	USB differential signal D+.
47	HSUSB_VDD12_CAP	P	USB Internal power regulator output 1.2V decoupling pin. Note: This pin needs to be connected with a 1uF capacitor.
48	USB_ID	I	USB identification.
49	VSS	P	Ground pin for digital circuit.
50	LDO_CAP	P	LDO output pin.
51	VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
52	CONFIG2	I	Configuration pin 2.
53	CONFIG3	I	Configuration pin 3.
54	GPO4	O	General purpose digital output pin4.
55	GPO5	O	General purpose digital output pin5.
56	LED1	O	LED output pin1.
57	AVDD	P	Power supply for internal analog circuit.
58	RESERVE		
59	AVSS	P	Ground pin for analog circuit.

Pin	Name	Type	Description
60	ETH_MDC	O	EMAC RMII PHY Management Clock output pin.
61	ETH_MDIO	I/O	EMAC RMII PHY Management Data pin.
62	ETH_TXD0	O	EMAC RMII Transmit Data bus bit 0.
63	ETH_TXD1	O	EMAC RMII Transmit Data bus bit 1.
64	ETH_TX_EN	O	EMAC RMII Transmit Enable output pin.

FUNCTIONAL DESCRIPTION

Reset

A reset signal by pulling low RESETN pin can be used to reset system at any time. When the RESETN voltage is lower than 0.2VDD and the state keeps longer than 32 us, the EC-01M will be reset. It will be in reset state until the RESETN voltage rises above 0.7VDD and the state keeps longer than 32 us.



BUSY

While EC-01M is initializing or handling the data over the SPI interface, the level of BUSY pin will be HIGH. Host should not do SPI data exchanging while the BUSY pin outputs HIGH.

CONFIG[0:3]

EC-01M has four configuration pins as follows.

Name	Function
CONFIG0	Host interface selection
CONFIG1	Test mode enable
CONFIG2	PDO size selection
CONFIG3	FIFO abandon enable

When the CONFIG0 is set to LOW, the USB will be available for host interface. When the CONFIG0 is set to HIGH, the SPI will be the host interface.

CONFIG0	L	Host interface is set as USB
	X	Host interface is set as SPI (Default)
	H	

X: Floating, L: Low, H: High

When the CONFIG1 is set to HIGH, EC-01M enter test mode. If NEXTW 16-ch digital inputs and 16-ch digital outputs slaves are connected with EC-01M, the slaves will enter operational state automatically. All output LEDs will light for 2 seconds, and then the output LEDs will be blinking sequentially. If the users set the values for the outputs by the host interface, the digital output LEDs will stop blinking and will be set to the values which users assign.

CONFIG1	X	Normal mode (Default)
	L	
	H	Test mode

X: Floating, L: Low, H: High

When the CONFIG2 is set to LOW, the data size of each slave will be 12 Bytes. When the CONFIG2 is set to HIGH, the data size of each slave will be 16 Bytes.

CONFIG2	X	Data size of each slave is 12 Bytes (Default)
	L	
	H	Data size of each slave is 16 Bytes

X: Floating, L: Low, H: High

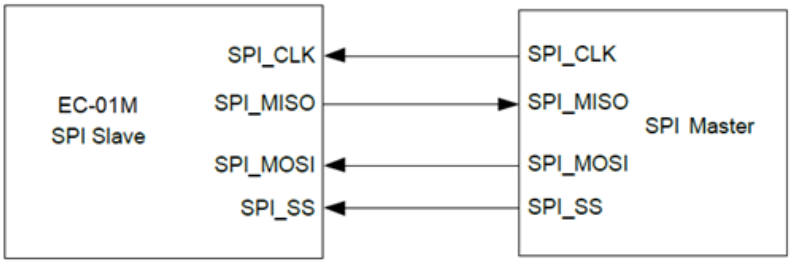
When the CONFIG3 is set to LOW, the BUSY pin will be HIGH to wait the complete data exchanging finished. When the CONFIG3 is set to HIGH, the commands in the FIFO will be abandoned if the data do not received completely by EC-01M in the 100 EtherCAT communication cycle time.

CONFIG3	L	FIFO abandon disable
	X	FIFO abandon enable (Default)
	H	

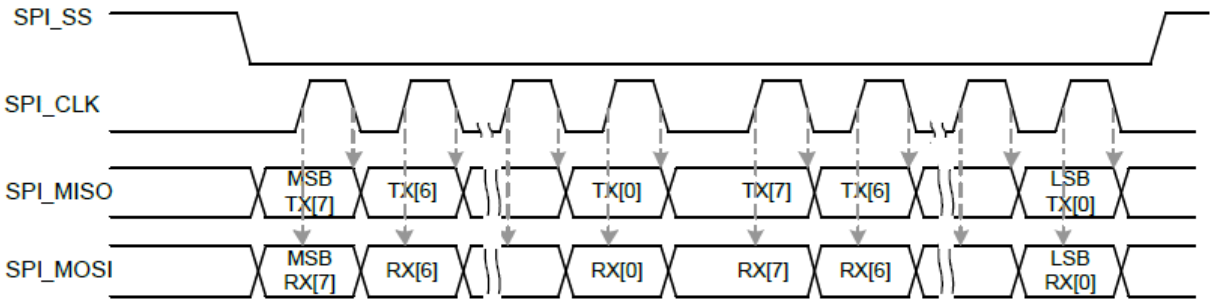
X: Floating, L: Low, H: High

SPI

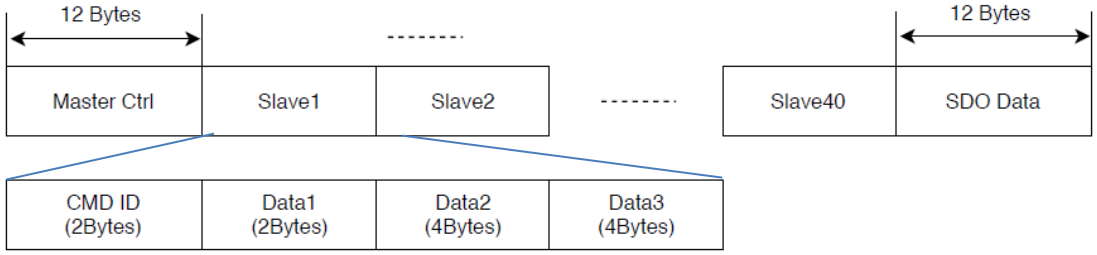
EC-01M supports full duplex transfer in the slave mode with the 4-wire bi-direction interface.



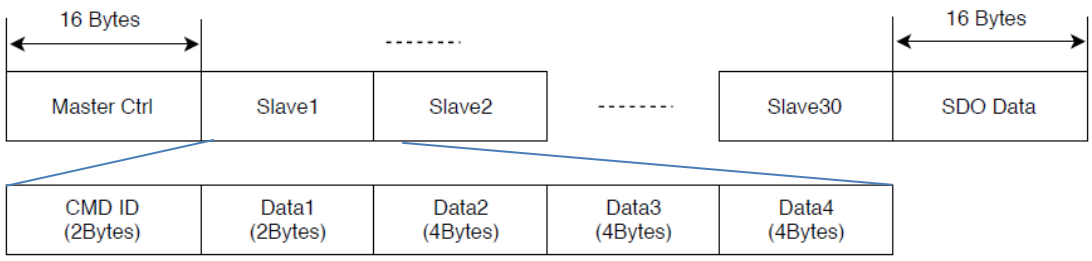
EC-01M transmits/receives data with the most-significant bit (MSB) first. The edge of SPI clock to transmit/receive is shown below.



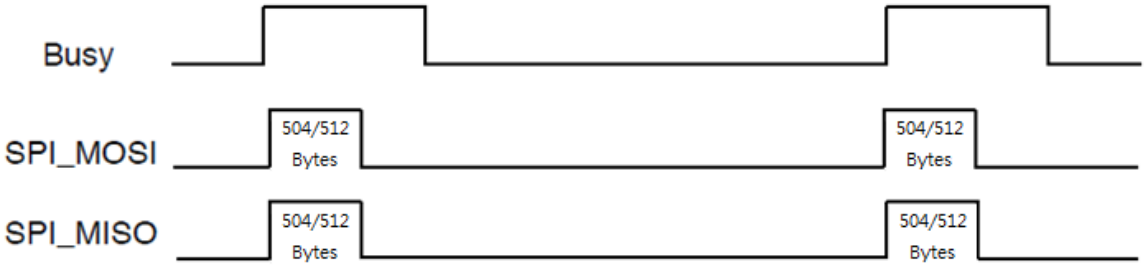
Complete SPI transmit/receive data should be 504 or 512 bytes depend on CONFIG2 pin. The data size of SPI transmit/receive for each slave will be 12 bytes if the CONFIG2 pin has pull-low, and the maximum 40 slaves will be control.



The data size of SPI transmit/receive for each slave will be 16 bytes if the CONFIG2 pin has pull-high, and the maximum 30 slaves will be control. For the detail definition of the data, please refer to the “ECM-SK Quick Start Guide”



The busy pin is HIGH while SPI data is exchanging. The next data exchange will be accepted while the busy pin is LOW. While the CONFIG3 pin has pull-high, the commands in the FIFO will be abandoned if the complete data do not be exchanged in the 100 EtherCAT communication cycle time. After abandoning the incompletely data, the following data transfer can work normally.

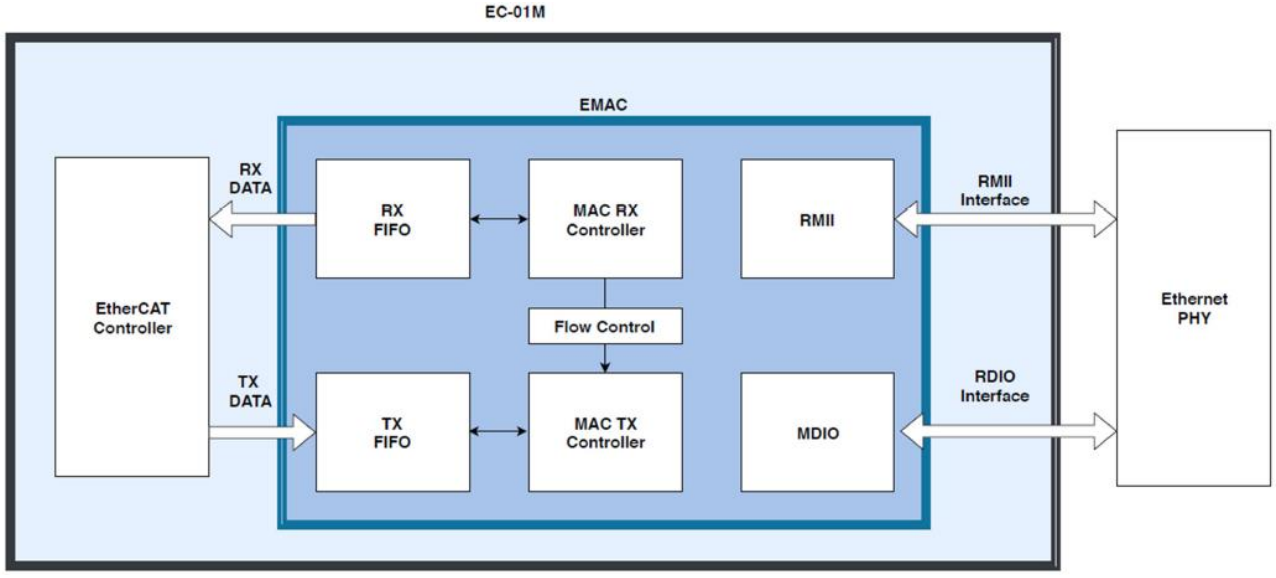


USB

The Interrupt IN and the Interrupt OUT with the fixed 512 bytes packet size are supported for the USB communication. If the CONFIG2 pin has pull-low, only the front 504 bytes are useful. The data structure is same as the SPI communication. For the detailed operation of the USB Human Interface Device (HID) of NEXTW EC-01M, please refer to the "ECM-SK Quick Start Guide"

Ethernet MAC Controller

The EMAC controller of EC-01M supports Reduced MII (RMII) interface to connect with external Ethernet PHY and provides TX/RX data transfer to the EtherCAT controller internally.



EtherCAT

EC-01M provides fixed PDO mappings for the EtherCAT CoE servo drives, the EtherCAT 16-ch digital input and 16-ch digital output slaves, and the NEXTW HSP slaves. Users can access PDO data through the host interface.

The RxPDO and the TxPDO for the EtherCAT 16-ch digital inputs and 16-ch digital outputs slave are defined as follows

RxPDO	Digital Outputs

TxPDO	Digital Inputs

The RxPDOs and the TxPDO in CSP, CSV, and CST mode for the EtherCAT CoE servo drives show as follows.

CSP(Cyclic Sync Position)

RxPDO	Controlword (6040h)	Target Position (607Ah)	

CSV(Cyclic Sync Velocity)

RxPDO	Controlword (6040h)	Target Velocity (60FFh)	

CST(Cyclic Sync Torque)

RxPDO	Controlword (6040h)	Target Torque (6071h)	

CSP&CSV&CST

TxPDO	Statusword (6041h)	Position Actual Value (6064h)	Torque Actual Value (6077h)	Error Code (603Fh)

The RxPDOs and the TxPDO in CSP and CSV mode for the NEXTW HSP slaves are as follows.

CSP(Cyclic Sync Position)

RxPDO	Controlword (6040h)	Target Position (607Ah)	Digital Outputs (60FEh)	Controlword (6840h)	Target Position (687Ah)	Digital Outputs (68FEh)

CSV(Cyclic Sync Velocity)

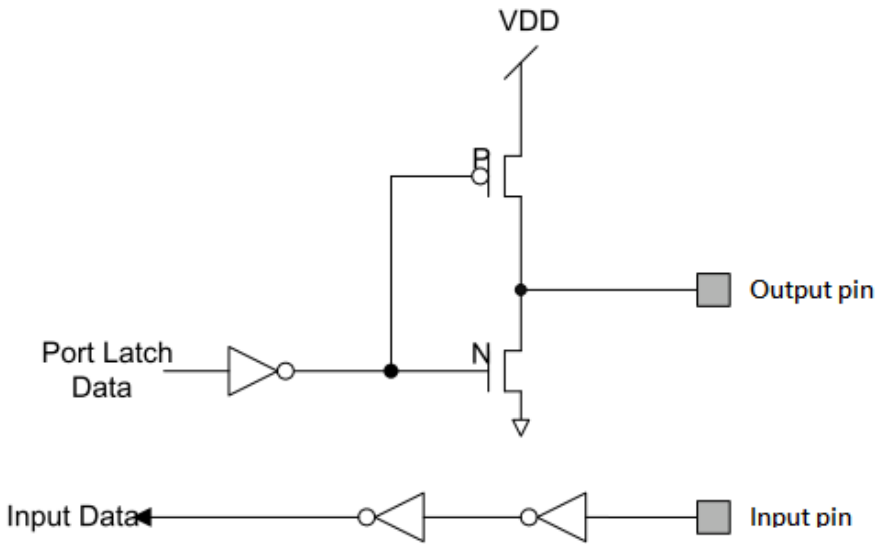
RxPDO	Controlword (6040h)	Target Velocity (60FFh)	Digital Outputs (60FEh)	Controlword (6840h)	Target Velocity (68FFh)	Digital Outputs (68FEh)

CSP&CSV

TxPDO	Statusword (6041h)	Position Actual Value (6064h)	Digital Inputs (60FDh)	Statusword (6841h)	Position Actual Value (6864h)	Digital Inputs (68FDh)

GPIO

EC-01M has 6 general purpose push-pull output pins. Users can control the LOW or HIGH level outputs by the host interface. EC-01M also has 6 general purpose TTL input pins with high impendence. When input signals are LOW or HIGH level, users can get the values through the host interface



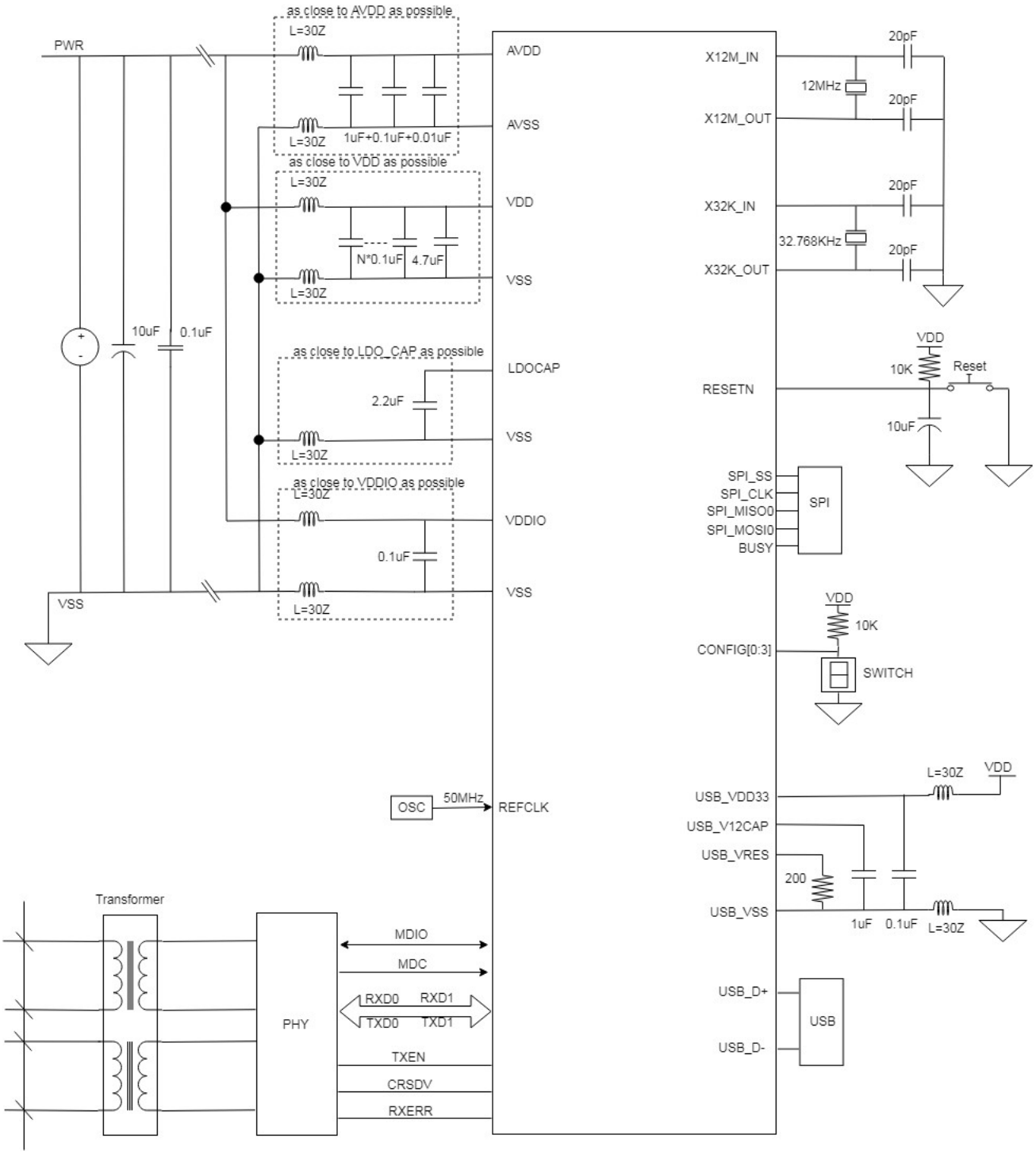
LED Indicator

The LED Indicators can show the state of EtherCAT slaves.

LED0	L	Slaves are not in Safe-Operational state
	H	Slaves are in Safe-Operational state
LED1	L	Slaves are not in Operational state
	H	Slaves are in Operational state

L: Low, H: High

APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS

Voltage Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VDD	Operation voltage	1.8	3.3	3.6	V
AVDD	Analog operation voltage	VDD			
VDDIO	Power supply for GPIO	1.8	3.3	3.6	
LDO_CAP	LDO output voltage	1.08	1.2	1.32	

Current Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
IDD	Maximum current into VDD		200	mA
IDDIO	Maximum current into VDDIO		100	
ISS	Maximum current out of VSS		100	

PIN DC Characteristics

GPIO

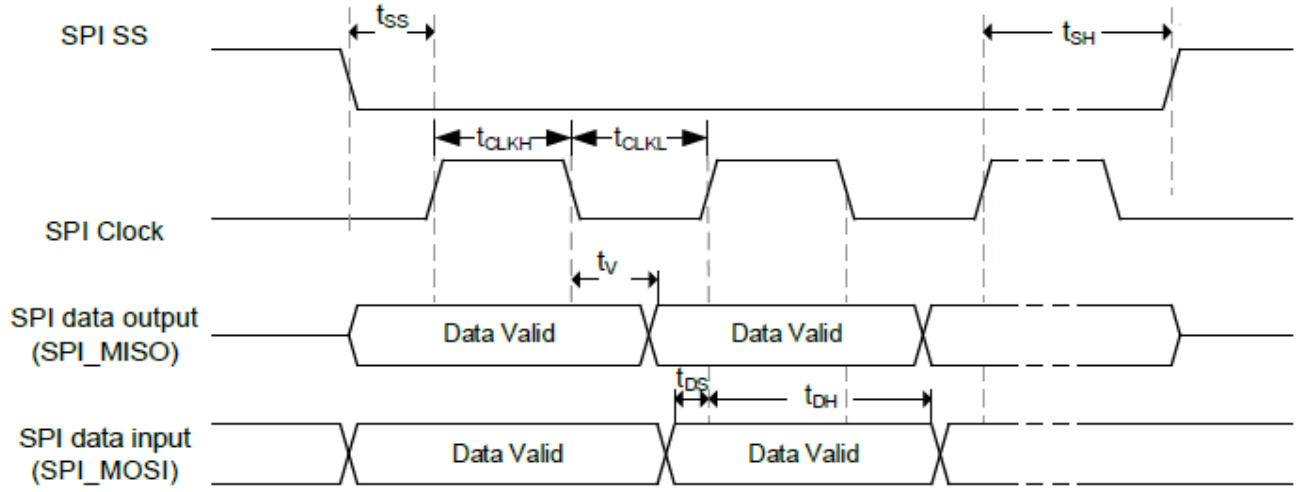
PARAMETER	MIN	TYP	MAX	UNIT	Test Conditions
Input Low voltage			0.8	V	VDD = VDDIO = 3.6 V
Input High voltage	2			V	VDD = VDDIO = 3.6 V
Output source current		-18		mA	VDD = VDDIO = 3.3 V
Output sink current		17		mA	VDD = VDDIO = 3.3 V

RESETN

PARAMETER	MIN	TYP	MAX	UNIT	Test Conditions
Negative going threshold (Schmitt input),			0.3 VDD	V	VDD = 3.3V
Positive going threshold (Schmitt Input)	0.7 VDD				VDD = 3.3V
Internal RESETN input filtered time pin pull up resistor		50		KΩ	
RESETN input filtered time		32		us	

SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{CLkH}	Clock output High time			$T_{SPICLK}/2$	ns
t_{CLkL}	Clock output Low time			$T_{SPICLK}/2$	
T_{SS}	Slave select setup time	$T_{SPICLK}+2$			
T_{SH}	Slave select hold time	T_{SPICLK}			
T_{DS}	Data input setup time	0			
T_{DH}	Data input hold time	2			
T_V	Data output valid time			8	



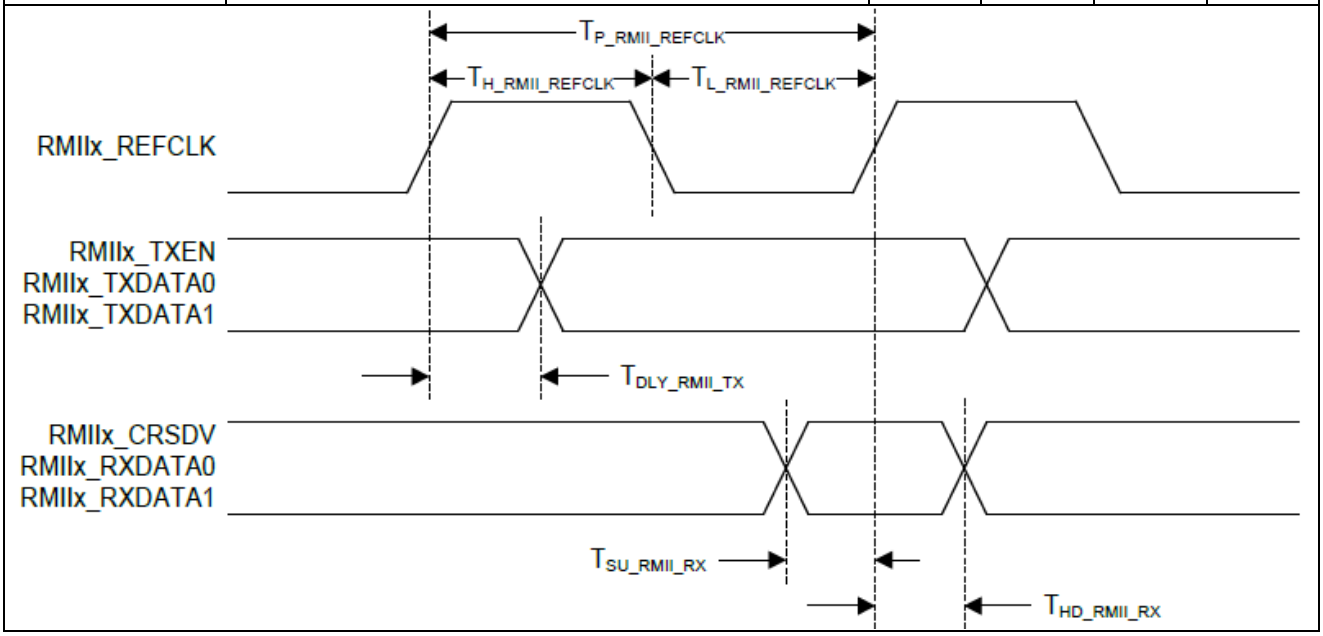
USB Characteristics

PARAMETER	MIN	TYP	MAX	UNIT	Test Conditions
Input Low voltage			0.8	V	VDD = VDDIO = 3.6 V
Input High voltage	2			V	VDD = VDDIO = 3.6 V
Output source current		-18		mA	VDD = VDDIO = 3.3 V

RMII Interface Timing

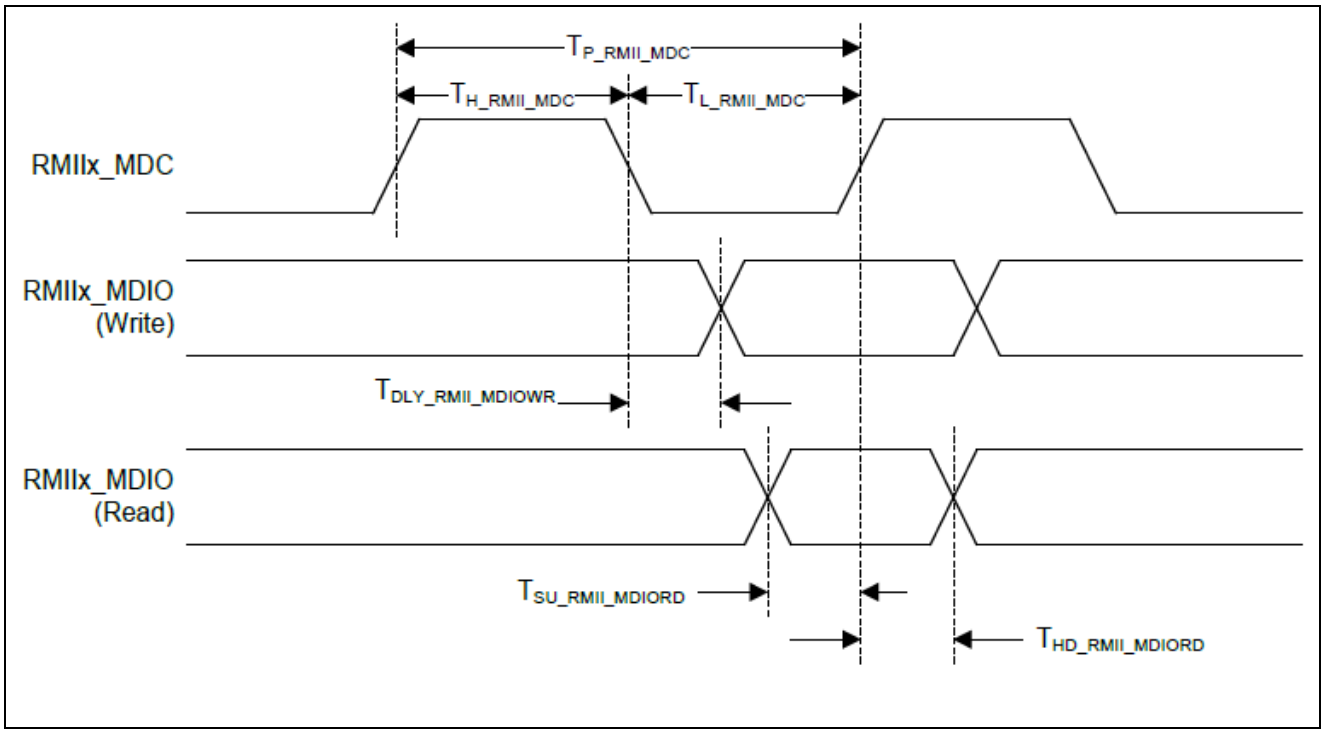
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
$T_{P\_RMII\_REFCLK}$	RMII_REFCLK Period		20.0 +/- 50 ppm		ns
$T_{H\_RMII\_REFCLK}$	RMII_REFCLK High Time	8.0	10.0	12.0	
$T_{L\_RMII\_REFCLK}$	RMII_REFCLK Low Time	8.0	10.0	12.0	

T DLY_RMII_TX	RMII_REFCLK Rising to Valid RMII_TXEN, RMII_TXDATA0 and RMII_TXDATA1 Delay			10	
T SU_RMII_RX	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Setup Time to RMII_REFCLK Rising	5			
T HD_RMII_RX	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Hold Time from RMII_REFCLK Rising	2			

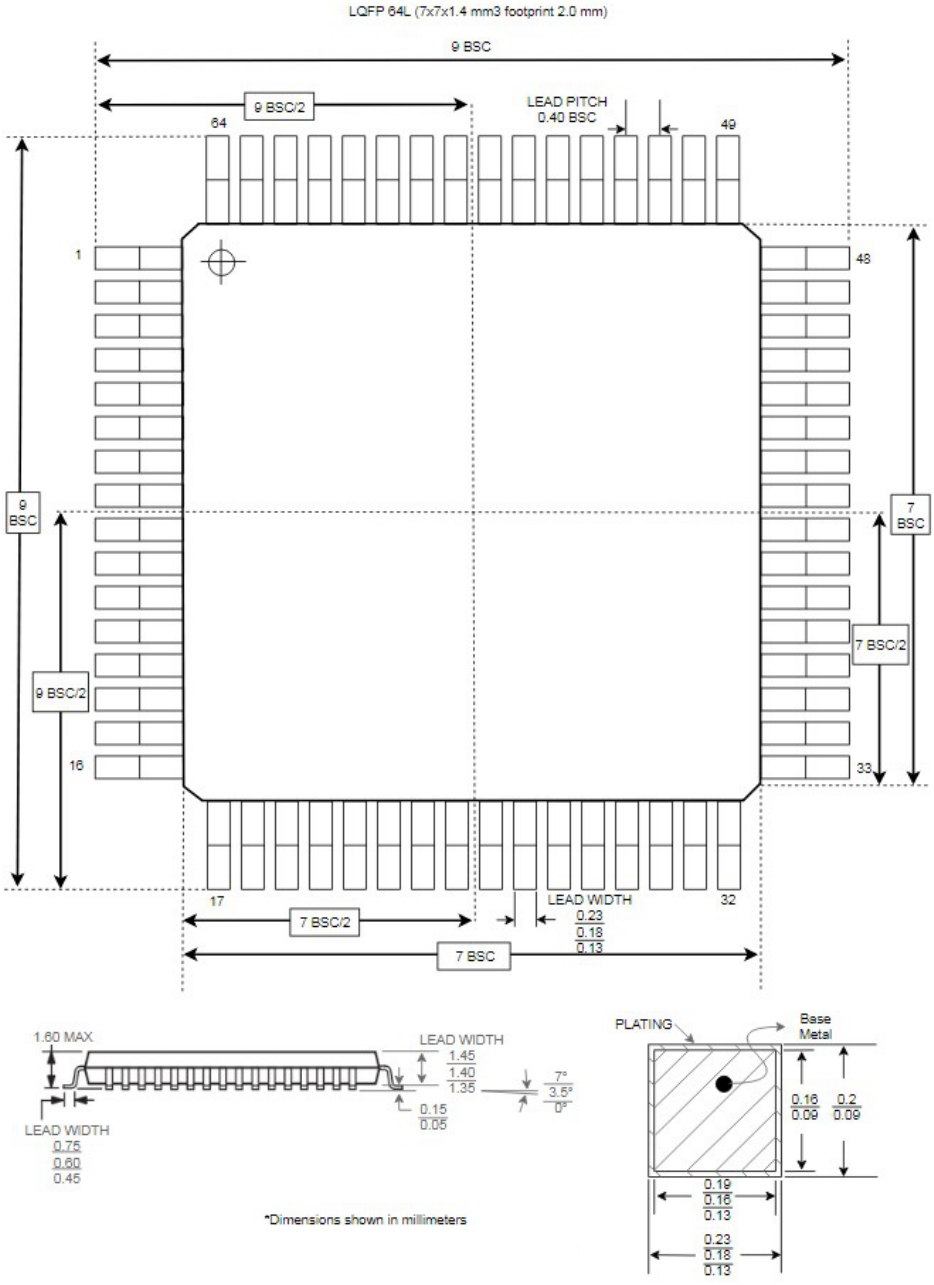


Ethernet PHY Management Interface Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
TP_RMII_MDC	RMII_MDC Period	400			ns
TH_RMII_ MDC	RMII_MDC High Time	200			
TL_RMII_ MDC	RMII_MDC Low Time	200			
T DLY_RMII_MDIOWR	RMII_MDC Falling to Valid RMII_MDIO Delay			10	
T SU_RMII _ MDIORD	RMII_MDIO Setup Time to RMII_MDC Rising	10			
T HD_RMII _ MDIORD	RMII_MDIO Hold Time from RMII_MDC Rising	10			


TP_RMII_MDC
TH_RMII_MDC
TL_RMII_MDC
RMIIx_MDC
RMIIx_MDIO
(Write)
TDLY_RMII_MDIOWR
RMIIx_MDIO
(Read)
TSU_RMII_MDIORD
THD_RMII_MDIORD

Package Dimensions



REVISION HISTORY

Data	Revision	Description
2019.04.23	1.00	First release