

Recommendations:

Hotspots: Start with Hotspots analysis to understand the efficiency of your algorithm.

Use Hotspots analysis to identify the most time consuming functions. Drill down to see the time spent on every line of code.

Microarchitecture Exploration: There is low microarchitecture usage (19.0%) of available hardware resources. of Pipeline Slots

Run Microarchitecture Exploration analysis to analyze CPU microarchitecture bottlenecks that can affect application performance.

Memory Access: The Memory Bound metric is high (23.0%). A significant fraction of execution pipeline slots could be stalled due to demand memory load and stores. of Pipeline Slots

Use Memory Access analysis to measure metrics that can identify memory access issues.

Threading: There is poor utilization of logical CPU cores (19.4%) in your application.

Use Threading to explore more opportunities to increase parallelism in your application.

Elapsed Time:	0.139s
CPU:	
IPC:	2.232
SP GFLOPS:	0.000
DP GFLOPS:	0.000
x87 GFLOPS:	0.001
Average CPU Frequency:	2.414 GHz

GPU:	
Time:	0.0% (0s) of Elapsed time

GPU utilization is low. Consider offloading more work to the GPU to increase overall application performance.

IPC Rate:	1.000
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Effective Logical Core Utilization: 19.4% (1.552 out of 8)

The metric value is low, which may signal a poor logical CPU cores utilization. Consider improving physical core utilization as the first step and then look at opportunities to utilize logical cores, which in some cases can improve processor throughput and overall performance of multi-threaded applications.

Effective Physical Core Utilization: 37.5% (1.500 out of 4)

The metric value is low, which may signal a poor physical CPU cores utilization caused by:

- load imbalance
- threading runtime overhead
- contended synchronization
- thread/process underutilization
- incorrect affinity that utilizes logical cores

instead of physical cores

Explore sub-metrics to estimate the efficiency of MPI and OpenMP parallelism or run the Locks and Waits analysis to identify parallel bottlenecks for other parallel runtimes.

Microarchitecture Usage: 19.0% of Pipeline Slots

You code efficiency on this platform is too low.

Possible cause: memory stalls, instruction starvation, branch misprediction or long latency instructions.

Next steps: Run Microarchitecture Exploration analysis to identify the cause of the low microarchitecture usage efficiency.

Retiring: 19.0% of Pipeline Slots
Front-End Bound: 29.5% of Pipeline Slots

Issue: A significant portion of Pipeline Slots is remaining empty due to issues in the Front-End.

Tips: Make sure the code working size is not too large, the code layout does not require too many memory accesses per cycle to get enough instructions for filling four pipeline slots, or check for microcode assists.

Back-End Bound: 44.1% of Pipeline Slots

A significant portion of pipeline slots are remaining empty. When operations take too long in the back-end, they introduce bubbles in the pipeline that ultimately cause fewer pipeline slots containing useful work to be retired per cycle than the machine is capable to support. This opportunity cost results in slower execution. Long-latency operations like divides and memory operations can cause this, as can too many operations being directed to a single execution port (for example, more multiply operations arriving in the back-end per cycle than the execution unit can support).

Memory Bound: 23.0% of Pipeline Slots

The metric value is high. This can indicate that the significant fraction of execution pipeline slots could be stalled due to demand memory load and stores. Use Memory Access analysis to have the metric breakdown by memory hierarchy, memory bandwidth information, correlation by memory objects.

Core Bound: 21.1% of Pipeline Slots

This metric represents how much Core non-memory issues were of a bottleneck. Shortage in hardware compute resources, or dependencies software's instructions are both categorized under Core Bound. Hence it may indicate the machine ran out of an OOO resources, certain execution units are overloaded or dependencies in program's data- or instruction- flow are limiting the performance (e.g. FP-chained long-latency arithmetic operations).

Bad Speculation: 7.3% of Pipeline Slots

Memory Bound: 23.0% of Pipeline Slots

The metric value is high. This can indicate that the significant fraction of execution pipeline slots could be stalled due to demand memory load and stores. Use Memory Access analysis to have the metric breakdown by memory hierarchy, memory bandwidth information, correlation by memory objects.

L1 Bound: 10.6% of Clockticks

This metric shows how often machine was stalled without missing the L1 data cache. The L1 cache typically has the shortest latency. However, in certain cases like loads blocked on older stores, a load might suffer a high latency even though it is being satisfied by the L1.

L2 Bound: 0.6% of Clockticks
L3 Bound: 1.3% of Clockticks
DRAM Bound: 6.5% of Clockticks
DRAM Bandwidth Bound: 0.0% of Elapsed Time
Store Bound: 3.7% of Clockticks

Vectorization: 0.0% of Packed FP Operations

A significant fraction of floating point arithmetic instructions are scalar. Use Intel Advisor to see possible reasons why the code was not vectorized.

Instruction Mix:
SP FLOPs: 0.0% of uOps
Packed: 0.0% from SP FP
128-bit: 0.0% from SP FP
256-bit: 0.0% from SP FP
Scalar: 100.0% from SP FP

This code has floating point operations and is not vectorized. Consider using Intel Advisor to vectorize the loops.

DP FLOPs: 0.0% of uOps
Packed: 0.0% from DP FP
128-bit: 0.0% from DP FP
256-bit: 0.0% from DP FP
Scalar: 100.0% from DP FP

This code has floating point operations and is not vectorized. Consider using Intel Advisor to vectorize the loops.

x87 FLOPs: 0.0% of uOps
Non-FP: 100.0% of uOps

FP Arith/Mem Rd Instr. Ratio: 0.000

The metric value is low. This can be a result of unaligned access to data for vector operations. Use Intel Advisor to find possible data access inefficiencies for vector operations.

FP Arith/Mem Wr Instr. Ratio: 0.001

The metric value is low. This can be a result of unaligned access to data for vector operations. Use Intel Advisor to find possible data access inefficiencies for vector operations.

GPU Active Time: 0.0%

GPU utilization is low. Consider offloading more work to the GPU to increase overall application performance.

Collection and Platform Info:

Application Command Line: ./codecs/hm/decoder/TAppDecoderStatic "-b" "./bin/hm/encoder_randomaccess_main.cfg/CLASS_A/Kimono_1920x1080_24_QP_27_hm.bin"

Operating System: 5.4.0-65-generic DISTRIB_ID=Ubuntu
DISTRIB_RELEASE=18.04 DISTRIB_CODENAME=bionic
DISTRIB_DESCRIPTION="Ubuntu 18.04.5 LTS"

Computer Name: eimon

Result Size: 3.7 MB

Collection start time: 09:57:25 10/02/2021 UTC

Collection stop time: 09:57:25 10/02/2021 UTC

Collector Type: Event-based sampling driver,Event-based counting driver

CPU:

Name: Intel(R) Processor code named Kabylake
ULX

Frequency: 1.992 GHz

Logical CPU Count: 8

Max DRAM Single-Package Bandwidth: 10.000 GB/s

Cache Allocation Technology:**Level 2 capability:** not detected**Level 3 capability:** not detected**GPU:****Name:**

Display controller: Intel Corporation Device 22807

Vendor: Intel Corporation**EU Count:** 24**Max EU Thread Count:** 7**Max Core Frequency:** 1.150 GHz