Intel® oneAPI VTune™ Profiler 2021.1.1 Gold

Elapsed Time: 1.256s

> Application execution time is too short. Metrics data may be
> unreliable. Consider reducing the sampling interval or
> increasing your application execution time.

Clockticks:	4,311,000,000
Instructions Retired:	10,402,200,000
CPI Rate:	0.414
MUX Reliability:	0.998
Retiring:	62.6% of Pipeline Slots
Light Operations:	57.5% of Pipeline Slots
FP Arithmetic:	1.0% of uOps
FP x87:	0.0% of uOps
FP Scalar:	1.0% of uOps
FP Vector:	0.0% of uOps
Other:	99.0% of uOps
Heavy Operations:	5.1% of Pipeline Slots
Microcode Sequencer:	1.2% of Pipeline Slots
Assists:	0.0% of Pipeline Slots
Front-End Bound:	17.5% of Pipeline Slots
Front-End Latency:	7.5% of Pipeline Slots
ICache Misses:	2.5% of Clockticks
ITLB Overhead:	0.4% of Clockticks
Branch Resteers:	3.6% of Clockticks
Mispredicts Resteers:	2.5% of Clockticks
Clears Resteers:	0.0% of Clockticks
Unknown Branches:	1.1% of Clockticks
DSB Switches:	1.3% of Clockticks
Length Changing Prefixes:	0.0% of Clockticks
MS Switches:	0.0% of Clockticks
Front-End Bandwidth:	10.0% of Pipeline Slots
Front-End Bandwidth MITE:	27.6% of Clockticks
Front-End Bandwidth DSB:	7.5% of Clockticks
(Info) DSB Coverage:	37.5%
Bad Speculation:	7.8% of Pipeline Slots
Branch Mispredict:	7.8% of Pipeline Slots
Machine Clears:	0.0% of Pipeline Slots

Back-End Bound:	12.0% of Pipeline Slots	
Memory Bound:	2.8% of Pipeline Slots	
L1 Bound:	3.8% of Clockticks	
DTLB Overhead:	0.2% of Clockticks	
Load STLB Hit:	0.0% of Clockticks	
Load STLB Miss:	0.2% of Clockticks	
Loads Blocked by Store Forwarding:	6.5% of Clockticks	
Lock Latency:	0.0% of Clockticks	
Split Loads:	0.0% of Clockticks	
4K Aliasing:	1.4% of Clockticks	
FB Full:	0.0% of Clockticks	
L2 Bound:	0.0% of Clockticks	
L3 Bound:	1.3% of Clockticks	
Contested Accesses:	0.0% of Clockticks	
Data Sharing:	0.0% of Clockticks	
L3 Latency:	2.8% of Clockticks	
SQ Full:	0.0% of Clockticks	
DRAM Bound:	0.0% of Clockticks	
Memory Bandwidth:	0.0% of Clockticks	
Memory Latency:	5.0% of Clockticks	
Store Bound:	1.3% of Clockticks	
Store Latency:	9.3% of Clockticks	
False Sharing:	0.0% of Clockticks	
Split Stores:	0.2% of Clockticks	
DTLB Store Overhead:	5.2% of Clockticks	
Store STLB Hit:	5.1% of Clockticks	
Store STLB Hit:	0.1% of Clockticks	
Core Bound:	9.2% of Pipeline Slots	
Divider:	0.0% of Clockticks	
Port Utilization:	20.2% of Clockticks	
Cycles of 0 Ports Utilized:	6.9% of Clockticks	
Serializing Operations:	0.0% of Clockticks	
Mixing Vectors:	0.0% of uOps	
Cycles of 1 Port Utilized:	5.0% of Clockticks	
Cycles of 2 Ports Utilized:	8.1% of Clockticks	
Cycles of 3+ Ports Utilized:	30.1% of Clockticks	
ALU Operation Utilization:	37.9% of Clockticks	
Port 0:	33.8% of Clockticks	
Port 1:	38.8% of Clockticks	
Port 5:	37.6% of Clockticks	
Port 6:	41.3% of Clockticks	
Load Operation Utilization:	35.1% of Clockticks	
Port 2:	43.8% of Clockticks	
Port 3:	45.1% of Clockticks	
Store Operation Utilization:	35.1% of Clockticks	
Port 4:	35.1% of Clockticks	
Port 7:	16.3% of Clockticks	
Vector Capacity Usage (FPU):	25.0%	
Average CPU Frequency:	3.487 GHz	
Total Thread Count:	1	

Paused Time: 0s

Effective Physical Core Utilization: 24.6% (0.984 out of 4)

> The metric value is low, which may signal a poor physical
> CPU cores utilization caused by:
>   - load imbalance
>   - threading runtime overhead
>   - contended synchronization
>   - thread/process underutilization
>   - incorrect affinity that utilizes logical cores instead
> of physical cores
> Explore sub-metrics to estimate the efficiency of MPI and
> OpenMP parallelism or run the Locks and Waits analysis to
> identify parallel bottlenecks for other parallel runtimes.

Effective Logical Core Utilization: 12.3% (0.984 out of 8)

> The metric value is low, which may signal a poor logical
> CPU cores utilization. Consider improving physical core
> utilization as the first step and then look at
> opportunities to utilize logical cores, which in some
> cases can improve processor throughput and overall
> performance of multi-threaded applications.

Collection and Platform Info:

Application Command Line: ./codecs/HM/encoder/TAppEncoderStatic "-c" "./configs/HM/encoder_lowdelay_main.cfg" "-i" "./sequences/CLASS_C/RaceHorses_416x240_30.yuv" "-wdt" "416" "-hgt" "240" "-b" "./bin/HM/encoder_lowdelay_main.cfg/CLASS_C/RaceHorses_416x240_30_QP_37_HM.bin" "-o" "./rec_yuv/HM/encoder_lowdelay_main.cfg/CLASS_C/RaceHorses_416x240_30_QP_37_HM.yuv" "-fr" "30" "-fs" "0" "-f" "2" "-q" "37"

User Name: root

Operating System: 5.4.0-72-generic DISTRIB_ID=Ubuntu DISTRIB_RELEASE=18.04 DISTRIB_CODENAME=bionic DISTRIB_DESCRIPTION="Ubuntu 18.04.5 LTS"

Computer Name: eimon

Result Size: 17.0 MB

Collection start time: 22:03:09 18/04/2021 UTC

Collection stop time: 22:03:10 18/04/2021 UTC

Collector Type: Event-based sampling driver

CPU:
    Name: Intel(R) Processor code named Kabylake ULX

    Frequency: 1.992 GHz

    Logical CPU Count: 8

    Cache Allocation Technology:
        Level 2 capability: not detected

        Level 3 capability: not detected