

**Recommendations:**

**Hotspots: Start with Hotspots analysis to understand the efficiency of your algorithm.**

Use Hotspots analysis to identify the most time consuming functions. Drill down to see the time spent on every line of code.

**Microarchitecture Exploration: There is low microarchitecture usage (52.1%) of available hardware resources. of Pipeline Slots**

Run Microarchitecture Exploration analysis to analyze CPU microarchitecture bottlenecks that can affect application performance.

**Threading: There is poor utilization of logical CPU cores (14.5%) in your application.**

Use Threading to explore more opportunities to increase parallelism in your application.

<b>Elapsed Time:</b>	0.589s
<b>CPU:</b>	
<b>IPC:</b>	2.100
<b>SP GFLOPS:</b>	0.000
<b>DP GFLOPS:</b>	0.043
<b>x87 GFLOPS:</b>	0.003
<b>Average CPU Frequency:</b>	3.043 GHz

**GPU:**

**Time:** 0.0% (0s) of Elapsed time

GPU utilization is low. Consider offloading more work to the GPU to increase overall application performance.

<b>IPC Rate:</b>	1.000
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**Effective Logical Core Utilization:** 14.5% (1.163 out of 8)

The metric value is low, which may signal a poor logical CPU cores utilization. Consider improving physical core utilization as the first step and then look at opportunities to utilize logical cores, which in some cases can improve

processor throughput and overall performance of multi-threaded applications.

**Effective Physical Core Utilization:** 28.4% (1.137 out of 4)

The metric value is low, which may signal a poor physical CPU cores utilization caused by:

- load imbalance
- threading runtime overhead
- contended synchronization
- thread/process underutilization
- incorrect affinity that utilizes logical cores instead of physical cores

Explore sub-metrics to estimate the efficiency of MPI and OpenMP parallelism or run the Locks and Waits analysis to identify parallel bottlenecks for other parallel runtimes.

**Microarchitecture Usage:** 52.1% of Pipeline Slots

**Retiring:** 52.1% of Pipeline Slots

**Front-End Bound:** 25.5% of Pipeline Slots

Issue: A significant portion of Pipeline Slots is remaining empty due to issues in the Front-End.

Tips: Make sure the code working size is not too large, the code layout does not require too many memory accesses per cycle to get enough instructions for filling four pipeline slots, or check for microcode assists.

**Back-End Bound:** 13.8% of Pipeline Slots

**Memory Bound:** 4.8% of Pipeline Slots

**Core Bound:** 9.1% of Pipeline Slots

**Bad Speculation:** 8.6% of Pipeline Slots

**Memory Bound:** 4.8% of Pipeline Slots

**L1 Bound:** 8.7% of Clockticks

**L2 Bound:** 0.5% of Clockticks

**L3 Bound:** 0.6% of Clockticks

**DRAM Bound:** 2.1% of Clockticks

**DRAM Bandwidth Bound:** 0.0% of Elapsed Time

**Store Bound:** 1.9% of Clockticks

**Vectorization:** 52.1% of Packed FP Operations

A significant fraction of floating point arithmetic instructions are scalar. Use Intel Advisor to see possible reasons why the code was not vectorized.

**Instruction Mix:**

<b>SP FLOPs:</b>	0.0% of uOps
<b>Packed:</b>	50.0% from SP FP
<b>128-bit:</b>	0.0% from SP FP
<b>256-bit:</b>	50.0% from SP FP
<b>Scalar:</b>	50.0% from SP FP

A significant fraction of floating point arithmetic instructions are scalar. Use Intel Advisor to see possible reasons why the code was not vectorized.

<b>DP FLOPs:</b>	0.4% of uOps
<b>Packed:</b>	57.8% from DP FP
<b>128-bit:</b>	57.8% from DP FP

A significant fraction of floating point arithmetic vector instructions is executed with a partial vector load. Make sure you compile the code with the latest instruction set or use Intel Advisor for vectorization help.

<b>256-bit:</b>	0.0% from DP FP
<b>Scalar:</b>	42.2% from DP FP

A significant fraction of floating point arithmetic instructions are scalar. Use Intel Advisor to see possible reasons why the code was not vectorized.

<b>x87 FLOPs:</b>	0.0% of uOps
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<b>Non-FP:</b>	99.6% of uOps
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**FP Arith/Mem Rd Instr. Ratio:** 0.017

The metric value is low. This can be a result of unaligned access to data for vector operations. Use Intel Advisor to find possible data access inefficiencies for vector operations.

**FP Arith/Mem Wr Instr. Ratio:** 0.040

The metric value is low. This can be a result of unaligned access to data for vector operations. Use Intel Advisor to

find possible data access inefficiencies for vector operations.

**GPU Active Time:** 0.0%

GPU utilization is low. Consider offloading more work to the GPU to increase overall application performance.

### Collection and Platform Info:

**Application Command Line:** ./codecs/hhi-vvc-codec/encoder/vvencFFapp "-c" "./configs/hhi-vvc-codec/randomaccess\_faster.cfg" "-i" "./sequences/CLASS\_C/RaceHorses\_416x240\_30.yuv" "-wdt" "416" "-hgt" "240" "-b" "./bin/hhi-vvc-codec/randomaccess\_faster.cfg/CLASS\_C/RaceHorses\_416x240\_30\_QP\_37\_hhi-vvc-codec.bin" "-o" "./rec\_yuv/hhi-vvc-codec/randomaccess\_faster.cfg/CLASS\_C/RaceHorses\_416x240\_30\_QP\_37\_hhi-vvc-codec.yuv" "-fr" "30" "-fs" "0" "-f" "2" "-q" "37"

**Operating System:** 5.4.0-62-generic DISTRIB\_ID=Ubuntu  
DISTRIB\_RELEASE=18.04 DISTRIB\_CODENAME=bionic  
DISTRIB\_DESCRIPTION="Ubuntu 18.04.5 LTS"

**Computer Name:** eimon

**Result Size:** 3.7 MB

**Collection start time:** 04:53:53 02/02/2021 UTC

**Collection stop time:** 04:53:54 02/02/2021 UTC

**Collector Type:** Event-based sampling driver,Event-based counting driver

### CPU:

**Name:** Intel(R) Processor code named Kabylake  
ULX

**Frequency:** 1.992 GHz

**Logical CPU Count:** 8

**Max DRAM Single-Package Bandwidth:** 10.000 GB/s

### Cache Allocation Technology:

**Level 2 capability:** not detected

**Level 3 capability:** not detected

**GPU:**

**Name:**

Display controller: Intel Corporation Device 22807

**Vendor:**

Intel Corporation

**EU Count:**

24

**Max EU Thread Count:**

7

**Max Core Frequency:**

1.150 GHz