



<b>Elapsed Time:</b>	1.570s
<b>Clockticks:</b>	5,275,800,000
<b>Instructions Retired:</b>	12,362,400,000
<b>CPI Rate:</b>	0.427
<b>MUX Reliability:</b>	0.997
<b>Retiring:</b>	58.4% of Pipeline Slots
<b>Light Operations:</b>	57.8% of Pipeline Slots
<b>FP Arithmetic:</b>	0.9% of uOps
<b>FP x87:</b>	0.0% of uOps
<b>FP Scalar:</b>	0.9% of uOps
<b>FP Vector:</b>	0.0% of uOps
<b>Other:</b>	99.1% of uOps
<b>Heavy Operations:</b>	0.5% of Pipeline Slots
<b>Microcode Sequencer:</b>	0.9% of Pipeline Slots
<b>Assists:</b>	0.0% of Pipeline Slots
<b>Front-End Bound:</b>	18.8% of Pipeline Slots
<b>Front-End Latency:</b>	7.4% of Pipeline Slots
<b>ICache Misses:</b>	2.0% of Clockticks
<b>ITLB Overhead:</b>	0.2% of Clockticks
<b>Branch Resteers:</b>	3.5% of Clockticks
<b>Mispredicts Resteers:</b>	3.1% of Clockticks
<b>Clears Resteers:</b>	0.0% of Clockticks
<b>Unknown Branches:</b>	0.5% of Clockticks
<b>DSB Switches:</b>	2.0% of Clockticks
<b>Length Changing Prefixes:</b>	0.0% of Clockticks
<b>MS Switches:</b>	0.0% of Clockticks
<b>Front-End Bandwidth:</b>	11.4% of Pipeline Slots
<b>Front-End Bandwidth MITE:</b>	24.4% of Clockticks
<b>Front-End Bandwidth DSB:</b>	6.4% of Clockticks
<b>(Info) DSB Coverage:</b>	44.6%
<b>Bad Speculation:</b>	10.3% of Pipeline Slots
<b>Branch Mispredict:</b>	10.3% of Pipeline Slots
<b>Machine Clears:</b>	0.0% of Pipeline Slots

<b>Back-End Bound:</b>	12.4% of Pipeline Slots
<b>Memory Bound:</b>	3.2% of Pipeline Slots
<b>L1 Bound:</b>	5.1% of Clockticks
<b>DTLB Overhead:</b>	0.1% of Clockticks
<b>Load STLB Hit:</b>	0.0% of Clockticks
<b>Load STLB Miss:</b>	0.1% of Clockticks
<b>Loads Blocked by Store Forwarding:</b>	6.0% of Clockticks
<b>Lock Latency:</b>	0.0% of Clockticks
<b>Split Loads:</b>	0.0% of Clockticks
<b>4K Aliasing:</b>	1.5% of Clockticks
<b>FB Full:</b>	0.0% of Clockticks
<b>L2 Bound:</b>	1.0% of Clockticks
<b>L3 Bound:</b>	0.0% of Clockticks
<b>Contested Accesses:</b>	0.0% of Clockticks
<b>Data Sharing:</b>	0.0% of Clockticks
<b>L3 Latency:</b>	2.4% of Clockticks
<b>SQ Full:</b>	0.0% of Clockticks
<b>DRAM Bound:</b>	0.0% of Clockticks
<b>Memory Bandwidth:</b>	1.0% of Clockticks
<b>Memory Latency:</b>	3.1% of Clockticks
<b>Store Bound:</b>	1.0% of Clockticks
<b>Store Latency:</b>	9.5% of Clockticks
<b>False Sharing:</b>	0.0% of Clockticks
<b>Split Stores:</b>	0.3% of Clockticks
<b>DTLB Store Overhead:</b>	4.4% of Clockticks
<b>Store STLB Hit:</b>	4.3% of Clockticks
<b>Store STLB Hit:</b>	0.1% of Clockticks
<b>Core Bound:</b>	9.2% of Pipeline Slots
<b>Divider:</b>	0.0% of Clockticks
<b>Port Utilization:</b>	20.8% of Clockticks
<b>Cycles of 0 Ports Utilized:</b>	7.4% of Clockticks
<b>Serializing Operations:</b>	0.0% of Clockticks
<b>Mixing Vectors:</b>	0.0% of uOps
<b>Cycles of 1 Port Utilized:</b>	5.3% of Clockticks
<b>Cycles of 2 Ports Utilized:</b>	9.0% of Clockticks
<b>Cycles of 3+ Ports Utilized:</b>	30.8% of Clockticks
<b>ALU Operation Utilization:</b>	40.3% of Clockticks
<b>Port 0:</b>	36.1% of Clockticks
<b>Port 1:</b>	40.3% of Clockticks
<b>Port 5:</b>	41.4% of Clockticks
<b>Port 6:</b>	43.5% of Clockticks
<b>Load Operation Utilization:</b>	38.7% of Clockticks
<b>Port 2:</b>	46.7% of Clockticks
<b>Port 3:</b>	47.8% of Clockticks
<b>Store Operation Utilization:</b>	35.0% of Clockticks
<b>Port 4:</b>	35.0% of Clockticks
<b>Port 7:</b>	18.0% of Clockticks
<b>Vector Capacity Usage (FPU):</b>	25.0%
<b>Average CPU Frequency:</b>	3.410 GHz
<b>Total Thread Count:</b>	1

**Paused Time:** 0s

**Effective Physical Core Utilization:** 23.8% (0.950 out of 4)

The metric value is low, which may signal a poor physical CPU cores utilization caused by:

- load imbalance
- threading runtime overhead
- contended synchronization
- thread/process underutilization
- incorrect affinity that utilizes logical cores instead

of physical cores

Explore sub-metrics to estimate the efficiency of MPI and OpenMP parallelism or run the Locks and Waits analysis to identify parallel bottlenecks for other parallel runtimes.

**Effective Logical Core Utilization:** 12.3% (0.985 out of 8)

The metric value is low, which may signal a poor logical CPU cores utilization. Consider improving physical core utilization as the first step and then look at opportunities to utilize logical cores, which in some cases can improve processor throughput and overall performance of multi-threaded applications.

### Collection and Platform Info:

**Application Command Line:** ./codecs/HM/encoder/TAppEncoderStatic "-c" "./configs/HM/encoder\_lowdelay\_main.cfg" "-i" "./sequences/CLASS\_C/RaceHorses\_416x240\_30.yuv" "-wdt" "416" "-hgt" "240" "-b" "./bin/HM/encoder\_lowdelay\_main.cfg/CLASS\_C/RaceHorses\_416x240\_30\_QP\_32\_HM.bin" "-o" "./rec\_yuv/HM/encoder\_lowdelay\_main.cfg/CLASS\_C/RaceHorses\_416x240\_30\_QP\_32\_HM.yuv" "-fr" "30" "-fs" "0" "-f" "2" "-q" "32"

**User Name:** root

**Operating System:** 5.4.0-72-generic DISTRIB\_ID=Ubuntu  
DISTRIB\_RELEASE=18.04 DISTRIB\_CODENAME=bionic  
DISTRIB\_DESCRIPTION="Ubuntu 18.04.5 LTS"

**Computer Name:** eimon

**Result Size:** 17.9 MB

**Collection start time:** 22:01:58 18/04/2021 UTC

**Collection stop time:** 22:02:00 18/04/2021 UTC

**Collector Type:** Event-based sampling driver

**CPU:**

**Name:** Intel(R) Processor code named Kabylake  
ULX

**Frequency:** 1.992 GHz

**Logical CPU Count:** 8

**Cache Allocation Technology:**

**Level 2 capability:** not detected

**Level 3 capability:** not detected