TFE4152 Design of Integrated Circuits Semester Project Presentation

Digital camera

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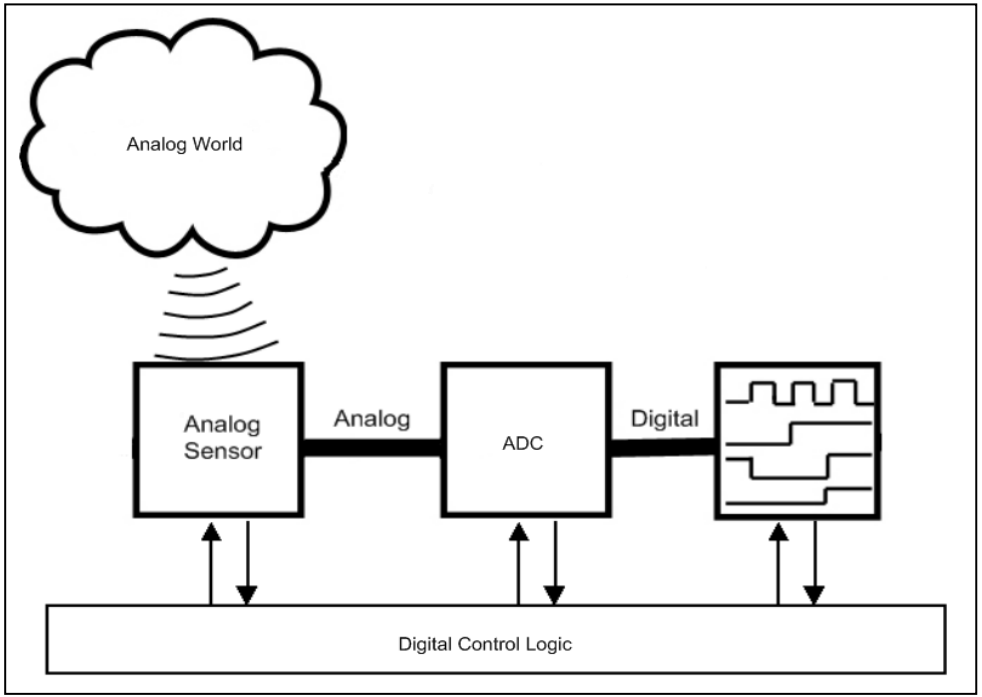
Overview of project

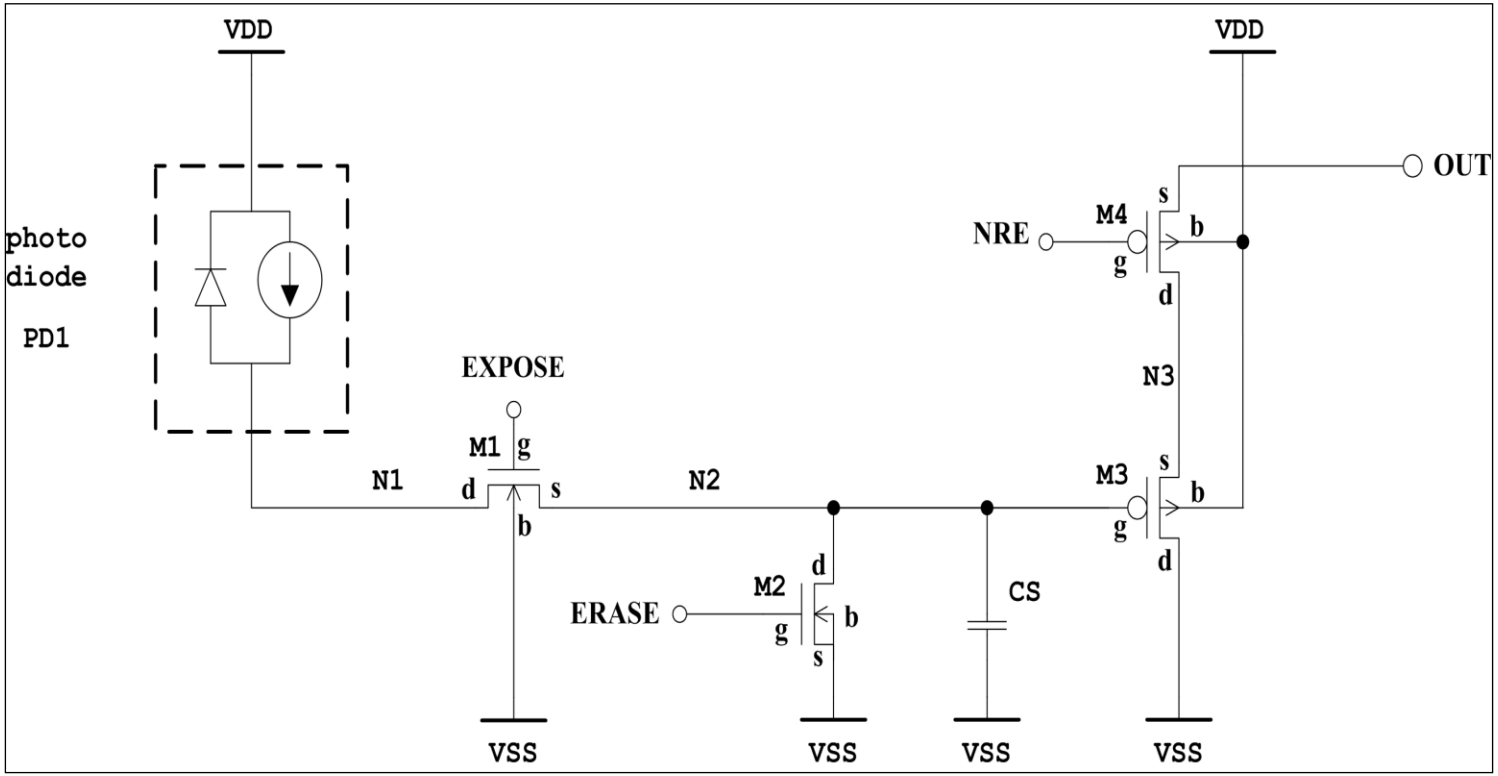


- Application: digital camera.
- # pixels = 4
- This is a mixed-signal design
- Light to voltage conversion
- A/D conversion
- Digital signal processing
- Focus: Analog readout + control signals.

Analog Circuitry

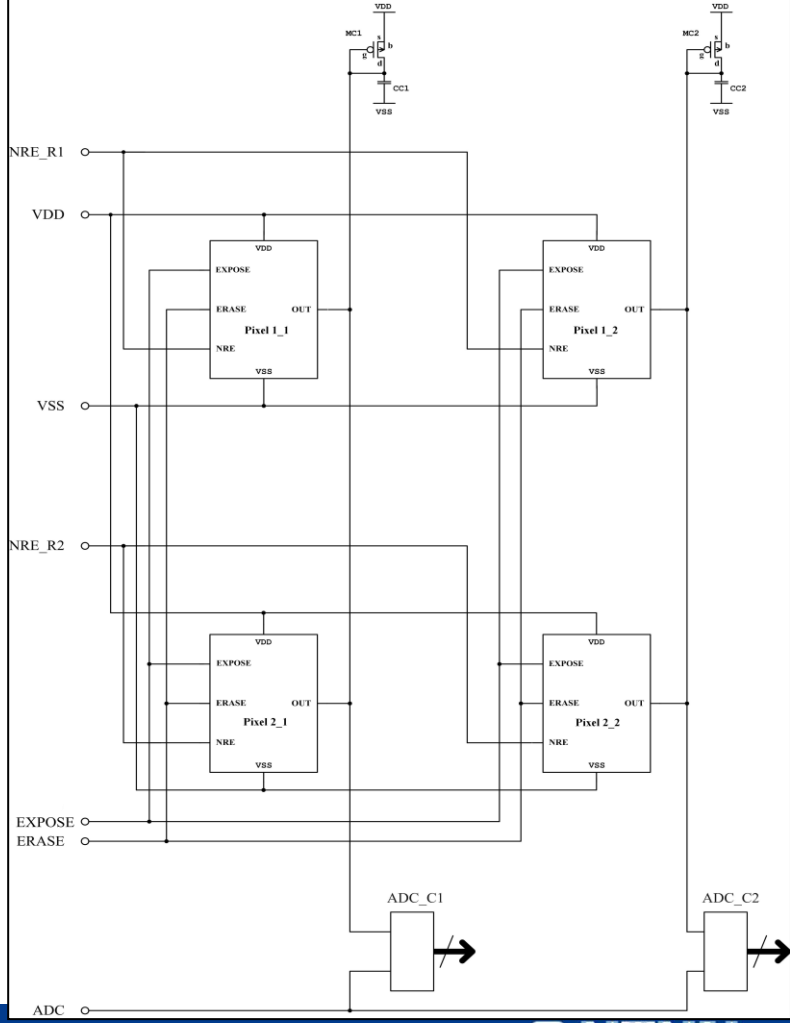
- The pixel topology is given. The task is to dimension the transistors.
- You will use AIM-Spice to simulate your circuit
- You will use the same transistor technology as you have done already in the exercises (180 nm, tt corner)
- We will give you some specifications for your design.

Pixel Circuit



Camera overview

- You will design a 2x2 pixel camera
- Only one row can be connected to the ADCs at a time to ensure correct readout value.
- Each column is connected to an ADC and an active load
- You will not simulate the circuit with the ADC.
- You don’t need to think about what happens after the ADC. That’s beyond the scope of this project



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Design start

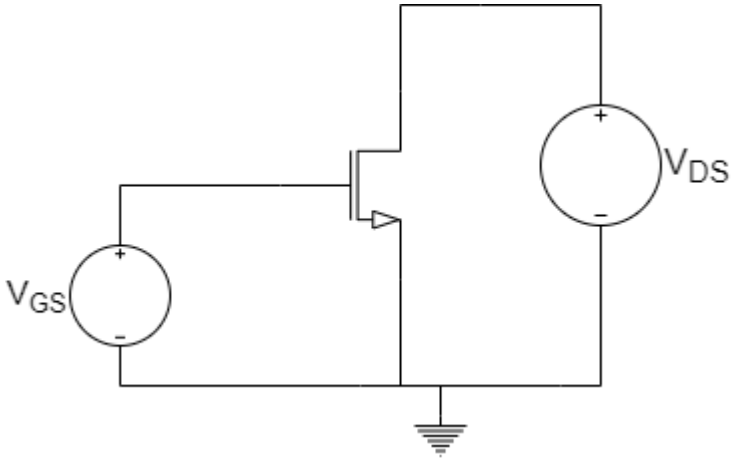
- Before you write any netlist, make sure you know what all components are supposed to do.
- Which transistors are used as switches, as amplifiers, as active loads, etc..
- How is light converted into a voltage?

Analog design strategy

- Do not start with simulating the entire circuit, break it down into smaller parts that can be tested individually.
- For the switches, make sure that you understand how W/L influences speed, voltage drop and leakage.
- For the amplifiers, find the expressions for the gain, and use this as a starting point.
- What size is reasonable for the sampling capacitor?
- Putting different parts of the design into subcircuits is useful.
- Have a look at the diode model, so that you know how it works.

Process variations

- Corners, FF, FS,SF and SS
  - Fast (F): lower threshold voltage, higher mobility
  - Slow (S): higher threshold voltage, lower mobility
  - NMOS, PMOS
- Resistance in an NMOS switch
  - V_{GS} is either 0 or V_{DD}
  - V_{DS} is swept from 0 to V_{DD}



Spice code

*Model files:

.include p18_cmos_models_tt.inc

.include p18_cmos_models_ss.inc

.include p18_cmos_models_ff.inc

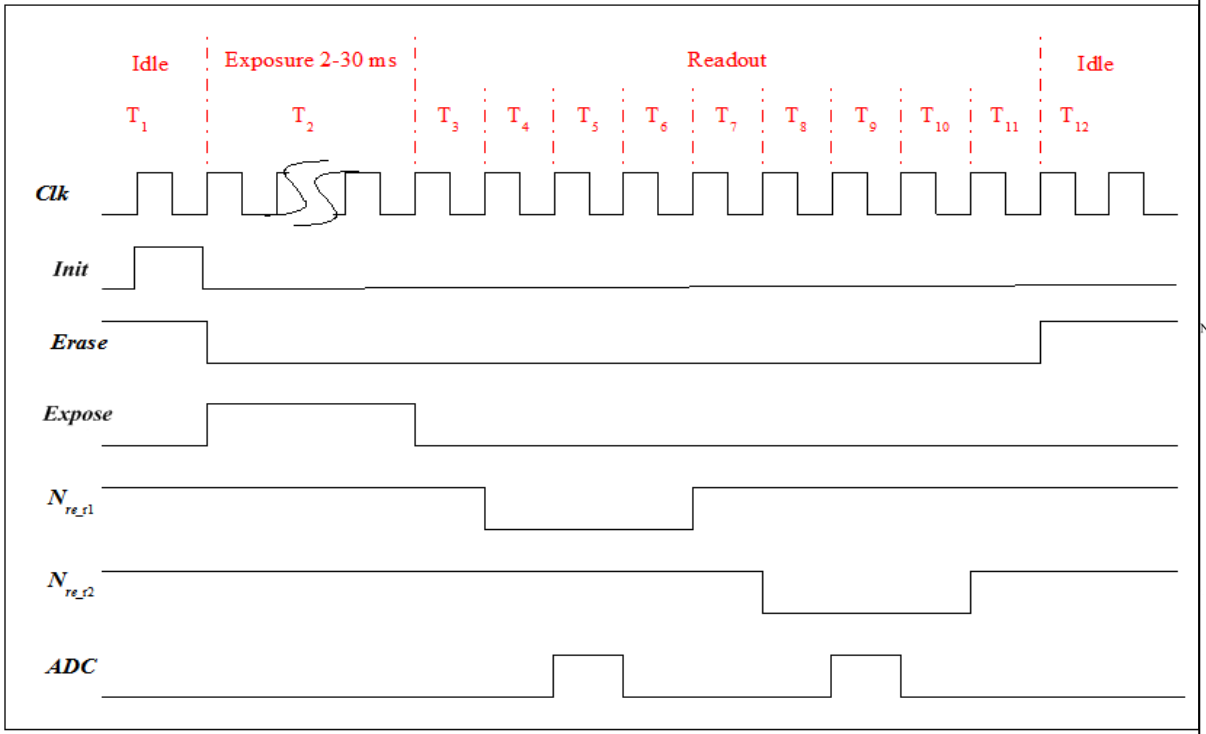
*Photo diode:

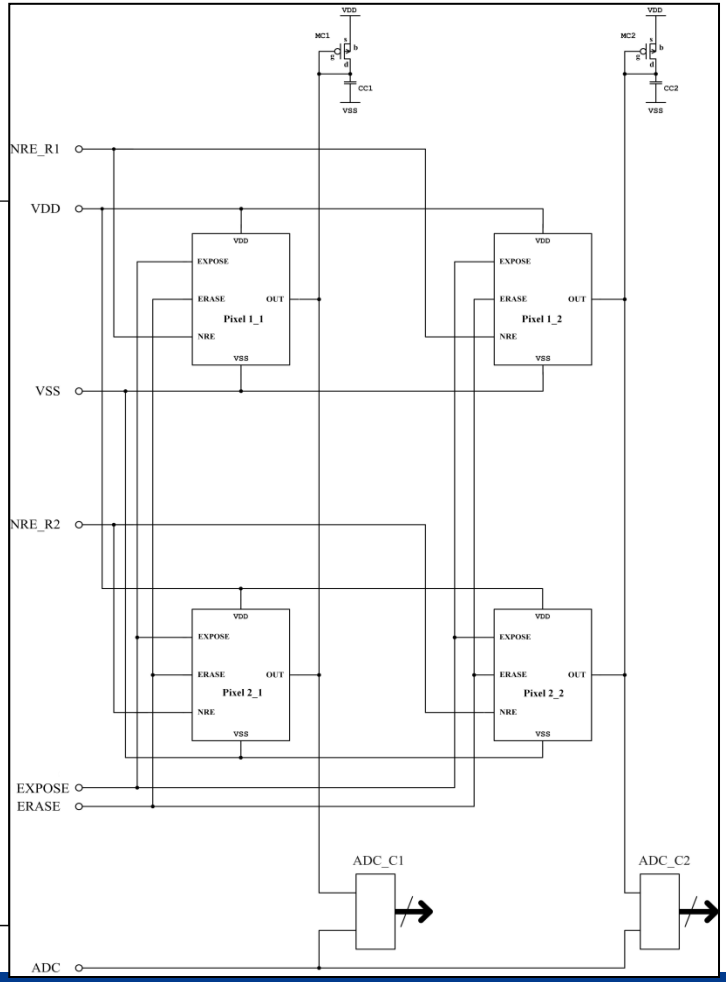
```
.subckt PhotoDiode  VDD N1_R1C1
I1_R1C1  VDD   N1_R1C1   DC  Ipd_1
d1 N1_R1C1 VDD dwell 1
.model dwell d cj0=1e-14 is=1e-12 m=0.5 bv=40
Cd1 N1_R1C1 VDD 30f
.ends
```

Digital Circuitry

- You do not have to design this with transistors.
- The digital part will be written as HDL (hardware description language)
- You will use Active HDL and write verilog NOT vhdl
- The clock frequency is 1 kHz

Digital Circuitry





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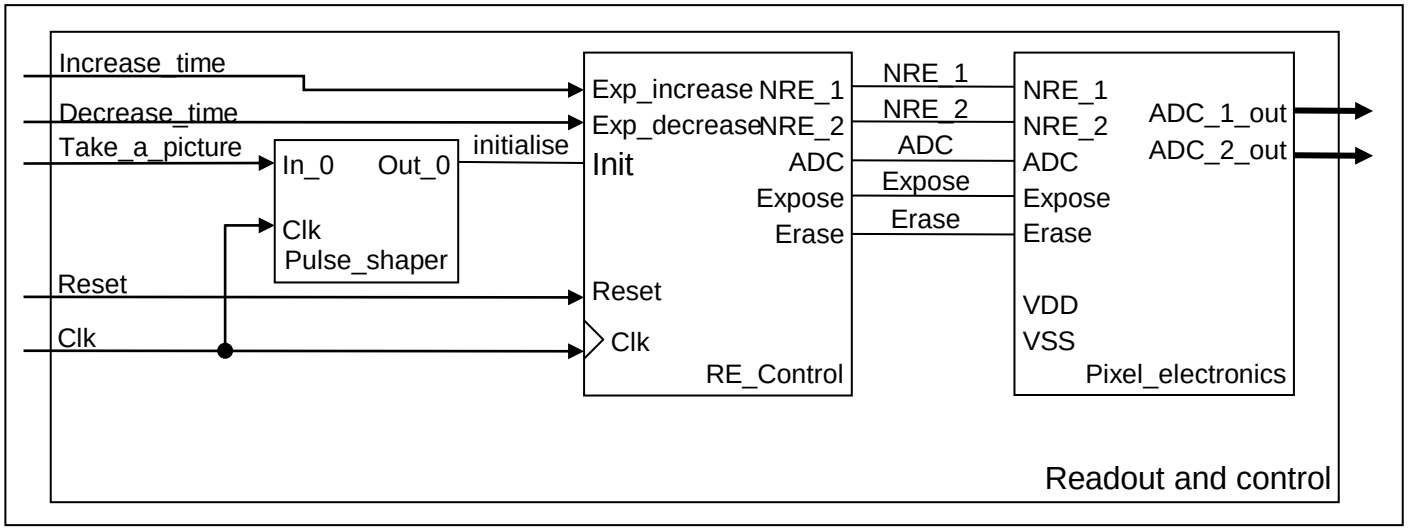
Digital Circuitry

- The digital circuitry will generate the needed control signals to the analog circuitry
- The control signals needed for analog circuitry:
  - Enable signal for pixel readout
  - Expose signal. This signals enables the conversion between light and voltage. The exposure time can be varied between 2 ms and 30 ms
  - Readout signals
  - Erase signal to clear pixel circuit of charge

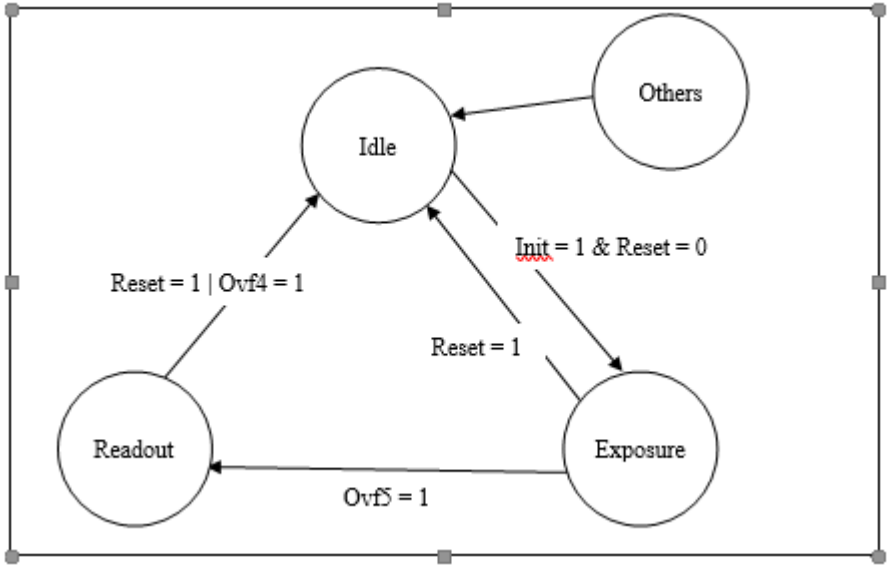
External signals

- Init – initialises the capture of an image
- Exp_increase, Exp_decrease – increase/decrease the exposure time
- Clk – the system clock
- Reset - put the system back into idle



Digital Circuitry

- You probably want to implement part of your digital circuit as a finite state machine (FSM)
- A FSM implementation is beneficial, as the the different steps involved in taking a photo needs to be in a specific order
- A very simplified example is shown on the right



Digital Circuitry

- As before, do not implement everything in one piece of code
- You probably want seperate your code into smaller functions
- Remember to test everything before starting something else. Debugging is so much easier this way.

Additional tips

- Start already next week. Starting late will make things stressful towards the end
- Designing might take longer than you think
- Write the theory part of your report early
- Use the exercise hours

Organization

- The project is to be done in groups of two.
  - If you already have a group: sign up on BB.
  - If you haven’t found a group: either start an empty group or join a group that has only one member.
  - If you have a good reason not to work in a pair, contact me or prof. Snorre Aunet.
- The report counts 30% of the total grade
- Deadline: 19th November, 14:00
- A detailed description of the project will be uploaded to BB.

Questions?