NTNU

Kunnskap for en bedre verden

Department of Electronic Systems

TFE4187 - Analog CMOS 1

Term project - design review

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1 MOSDESIGNER & Hand calculations

Choose two-stage Miller OTA as OTA topology.
Specification:
$V_{DD} = 1V$
Large-signal low-frequency open-loop gain $A_0 > 54dB$
Unity-gain frequency $f_{ug} > 200MHz$
SNDR @ $f_{in} = 10MHz$ & $V_{OUT,P-P} = 0.5V > 40dB$
Phase margin at unity-gain feedback $> 60°$

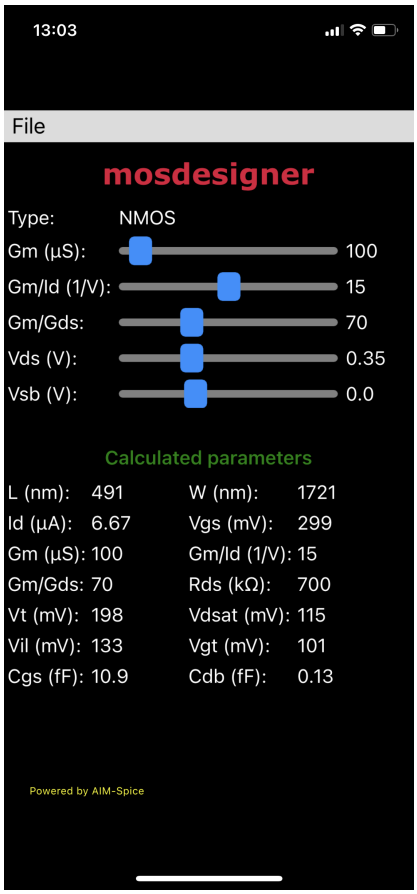
Initial guess: $C_L = 50fF$
$g_m > 2\pi f_{ug} C_L = 2\pi \cdot 300MHz \cdot 50fF$
$\Rightarrow g_m = 94.25\mu S \approx 100\mu S$

$A_O > 54dB$
$\Rightarrow \frac{g_m}{g_{ds}} = 2 \cdot \sqrt{10^{\frac{60dB}{20}}} = 63.25 \approx 70$

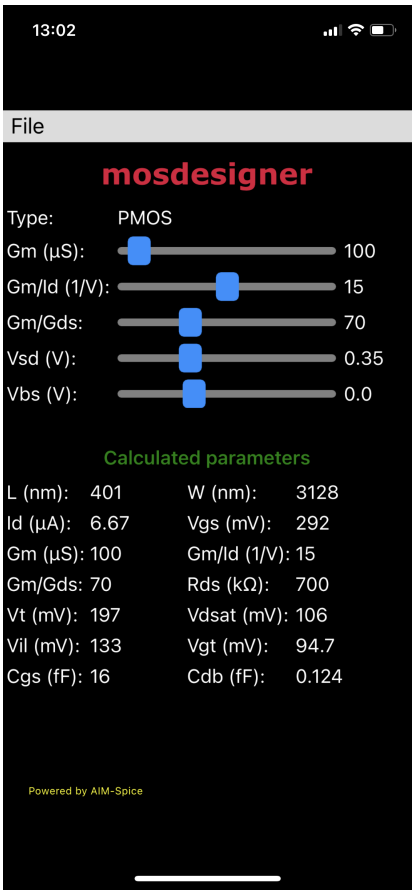
$\frac{g_m}{I_D} = 15$

$V_{ds} = V_{sd} = 0.33V \overset{\text{mosdesigner}}{=} 0.35V$

$V_{bs} = V_{sb} = 0V$, shorted bulk.



(a) NMOS parameters



(b) PMOS parameters

Figure 1: Transistor parameters from mosdesigner using the values from the hand calculation

Since the PMOS bias input feeds the differential input of the current mirror, the current needs to be doubled as follows:

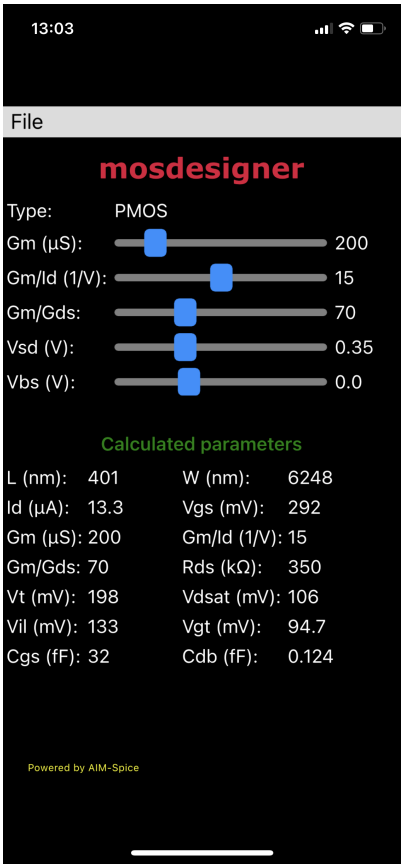


Figure 2: Bias PMOS parameters

The circuit was setup in Cadence Virtuoso as shown in figure 3

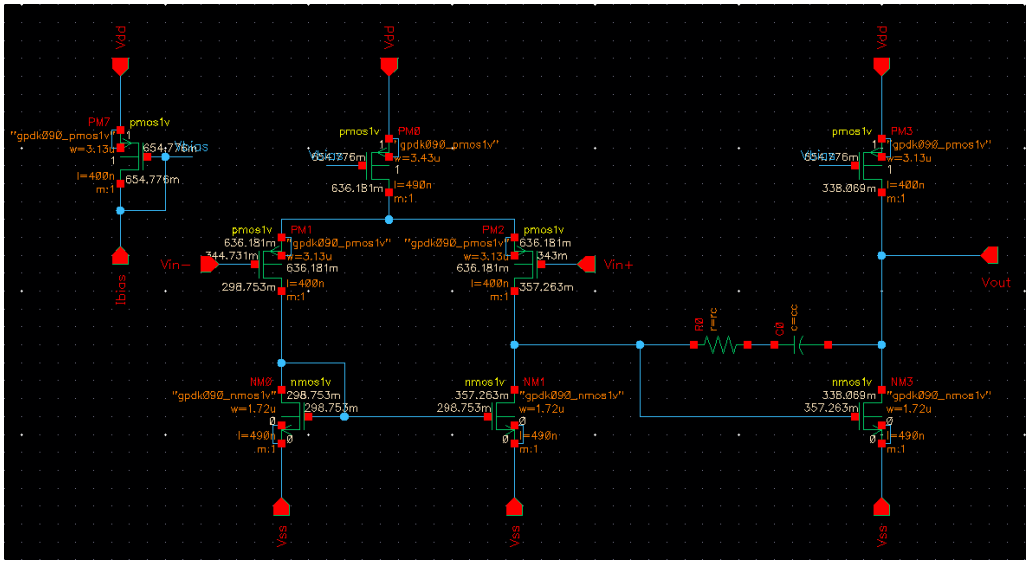


Figure 3: Circuit setup

2 AC-analysis

AC-analysis and simulations where done with the following simulation setup.

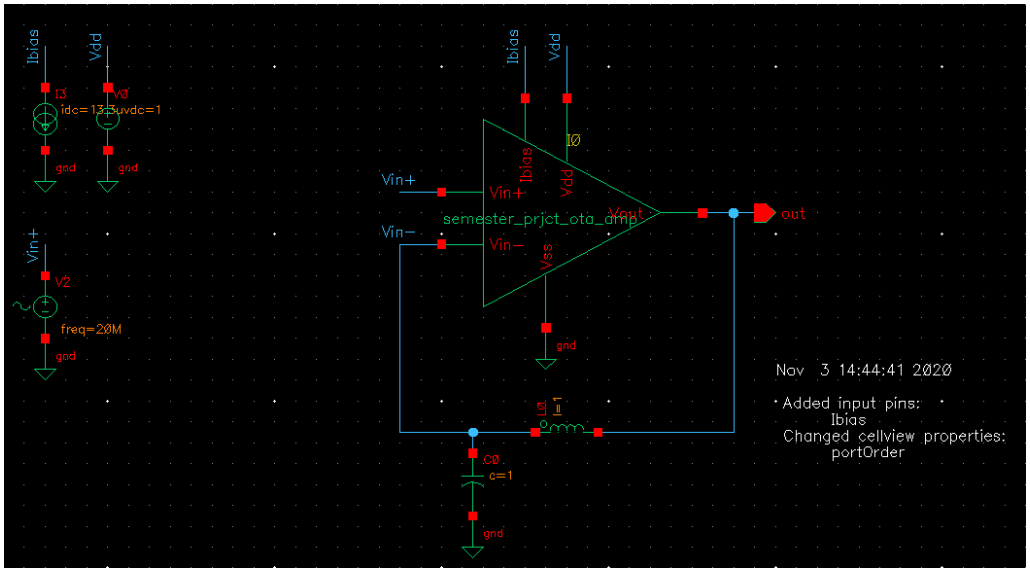


Figure 4: AC testbench

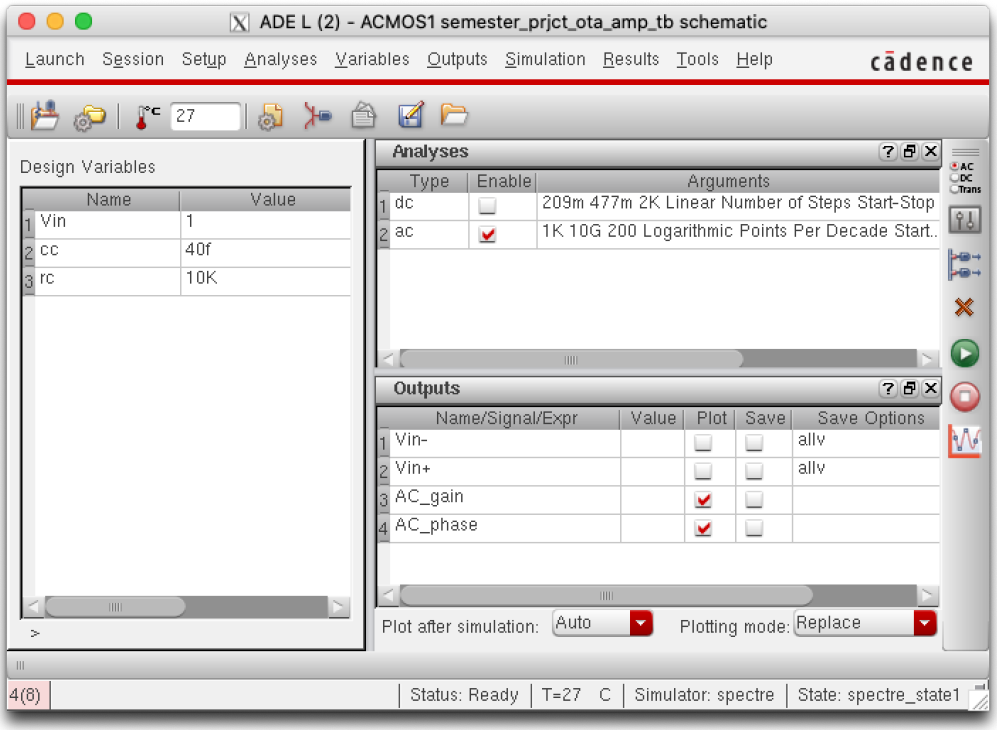


Figure 5: ADE L setup for AC analysis

Had to add compensation components, started with $C_c = 50fF$ & $R_C = 1k\Omega$. After some tweaking the values where changed to $C_c = 40fF$ and R_C, as this creates a decent phasemargin while still maintaining a decent gain, as seen in figure 6 and figure 7.

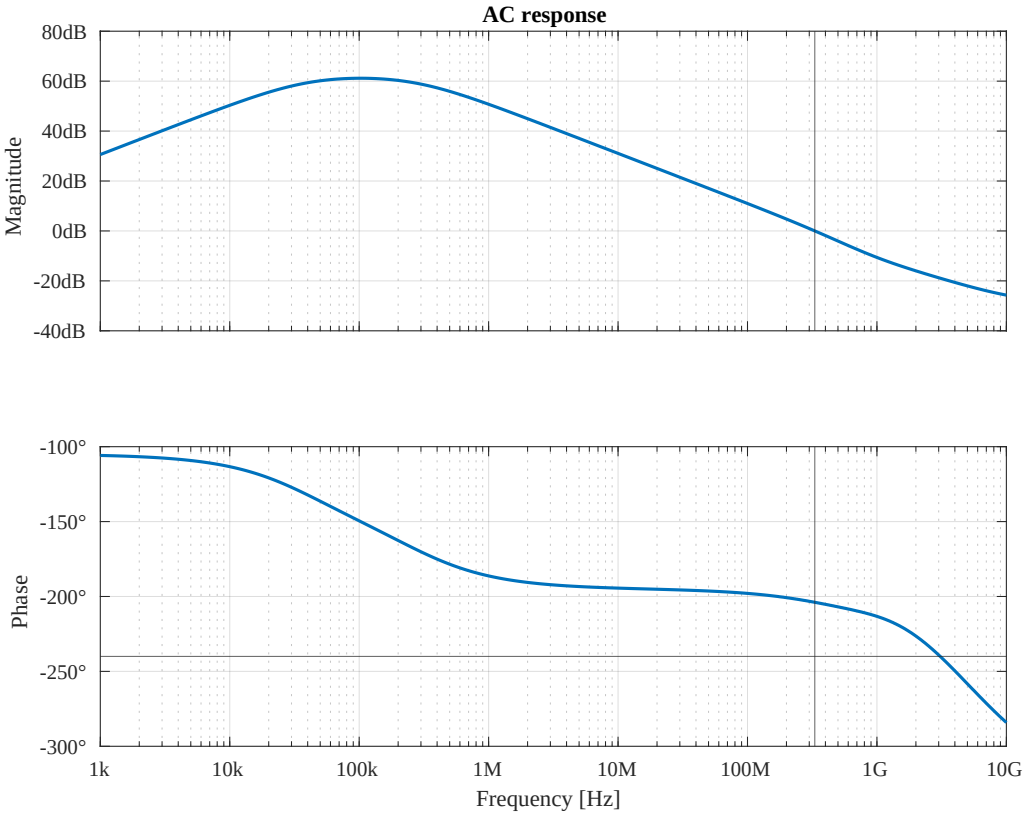


Figure 6: AC response with $C_C = 40fF$ and $R_C = 10k\Omega$

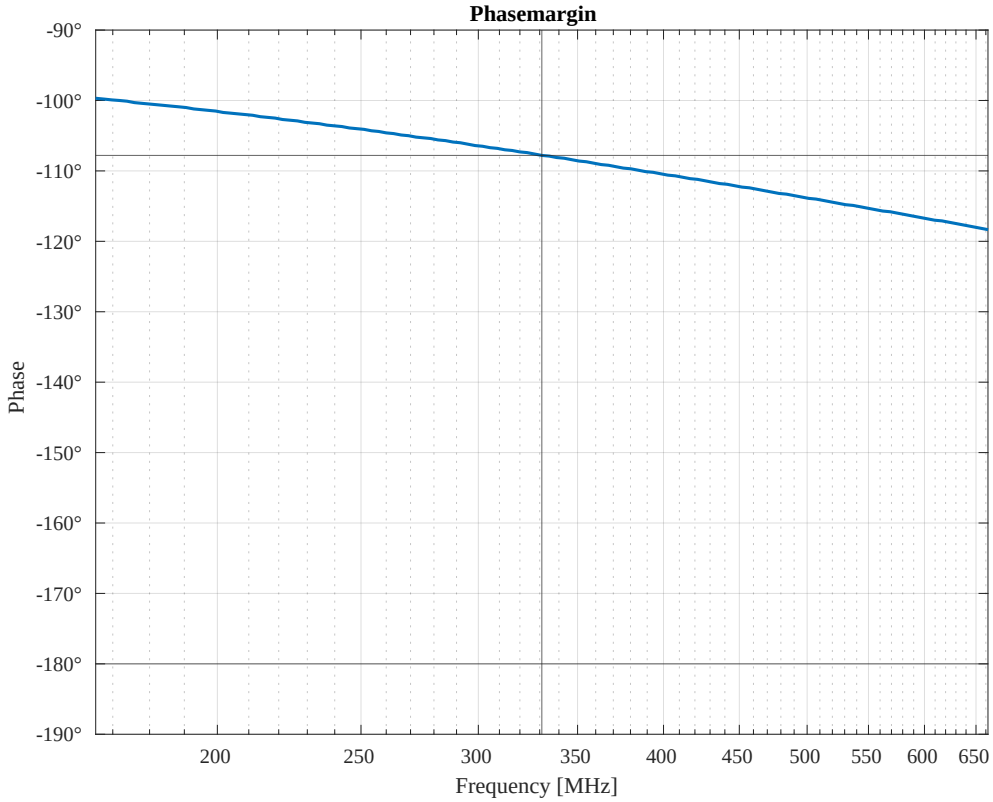


Figure 7: Phase margin with $C_C = 40fF$ and $R_C = 10k\Omega$

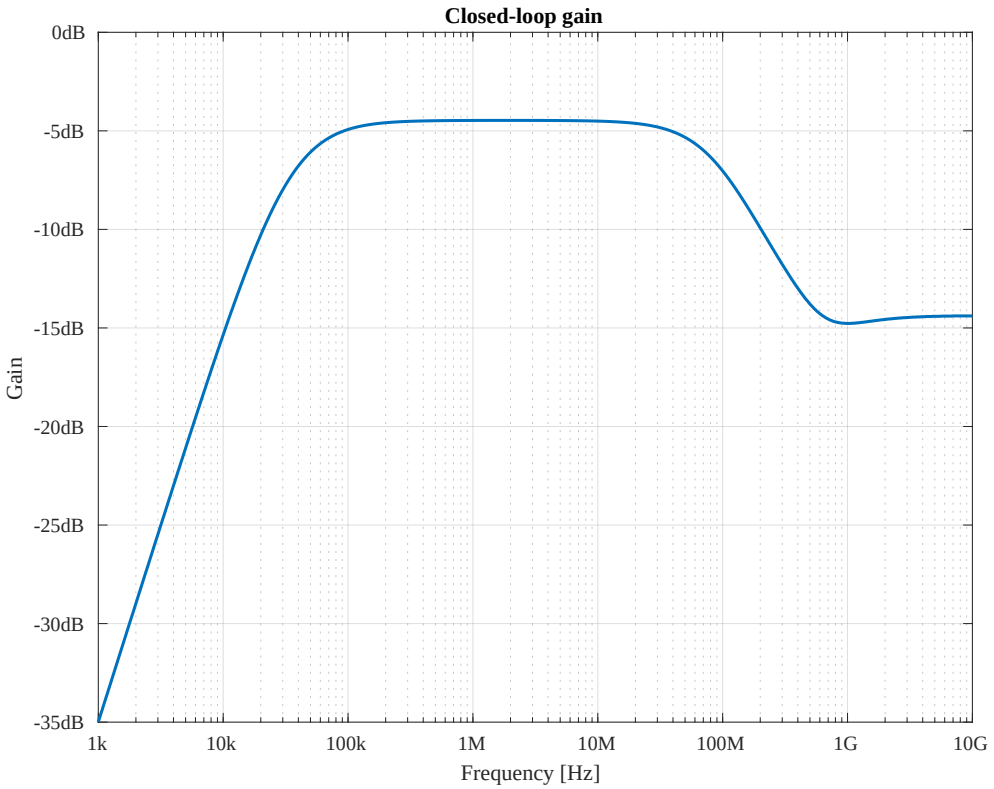


Figure 8: Closed-loop gain

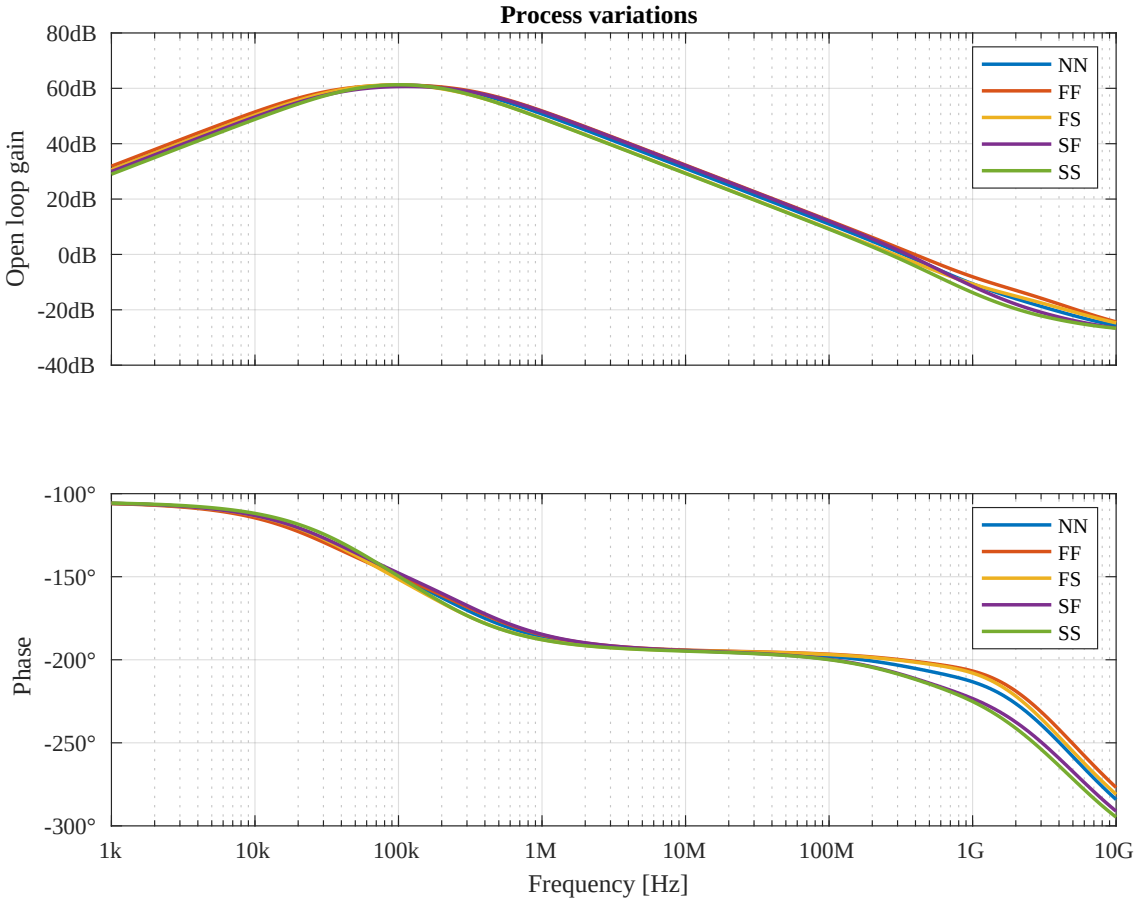


Figure 9: Process variations

3 Transient analysis

Transient analysis and simulations where done with the following simulation setup.

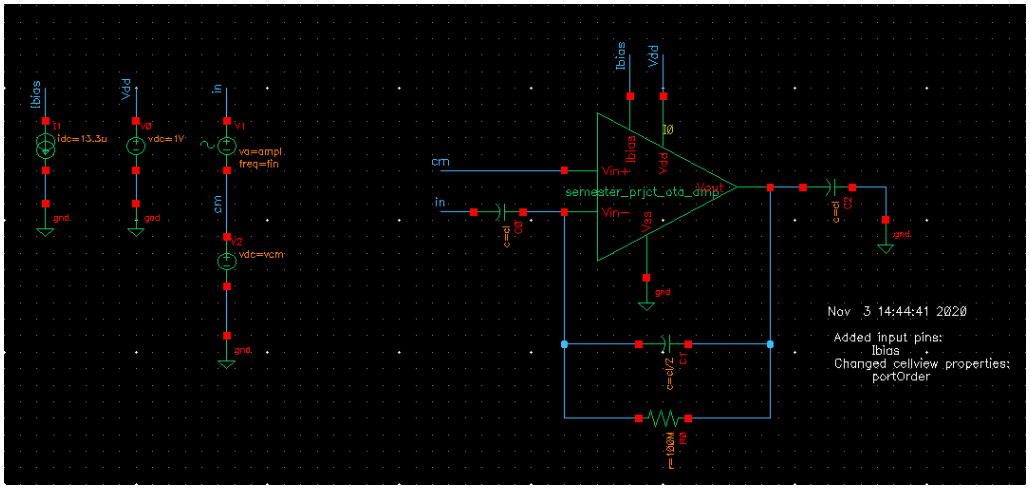


Figure 10: Transient testbench

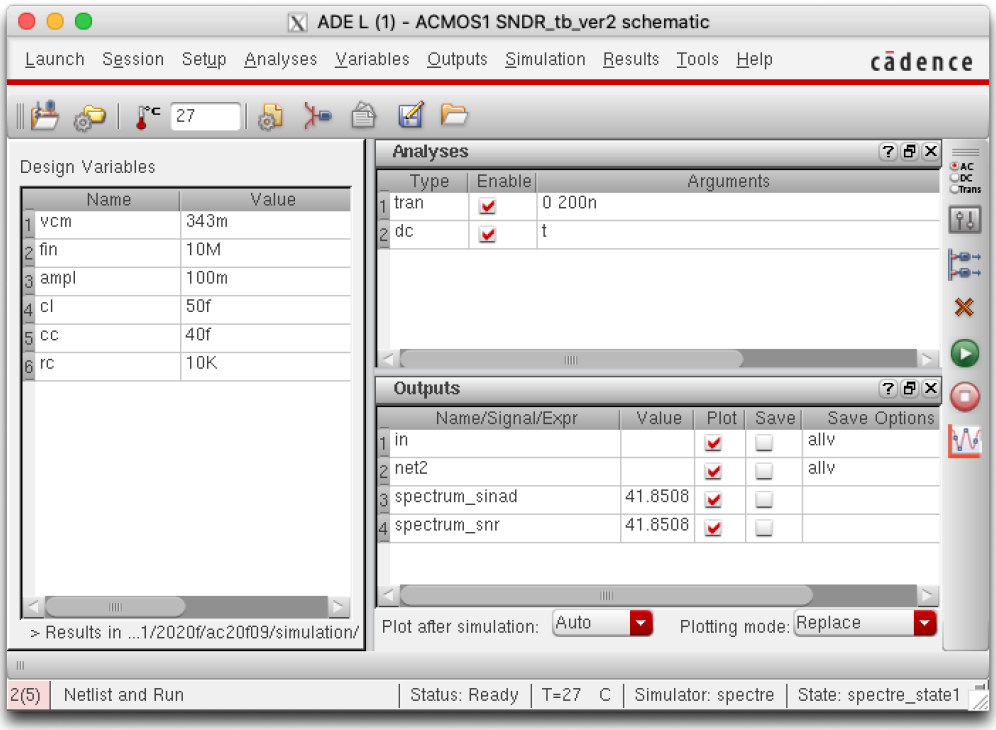


Figure 11: ADE L setup for transient analysis

As seen in figure 11, $SNDR(SINAD) = 41.85dB$.

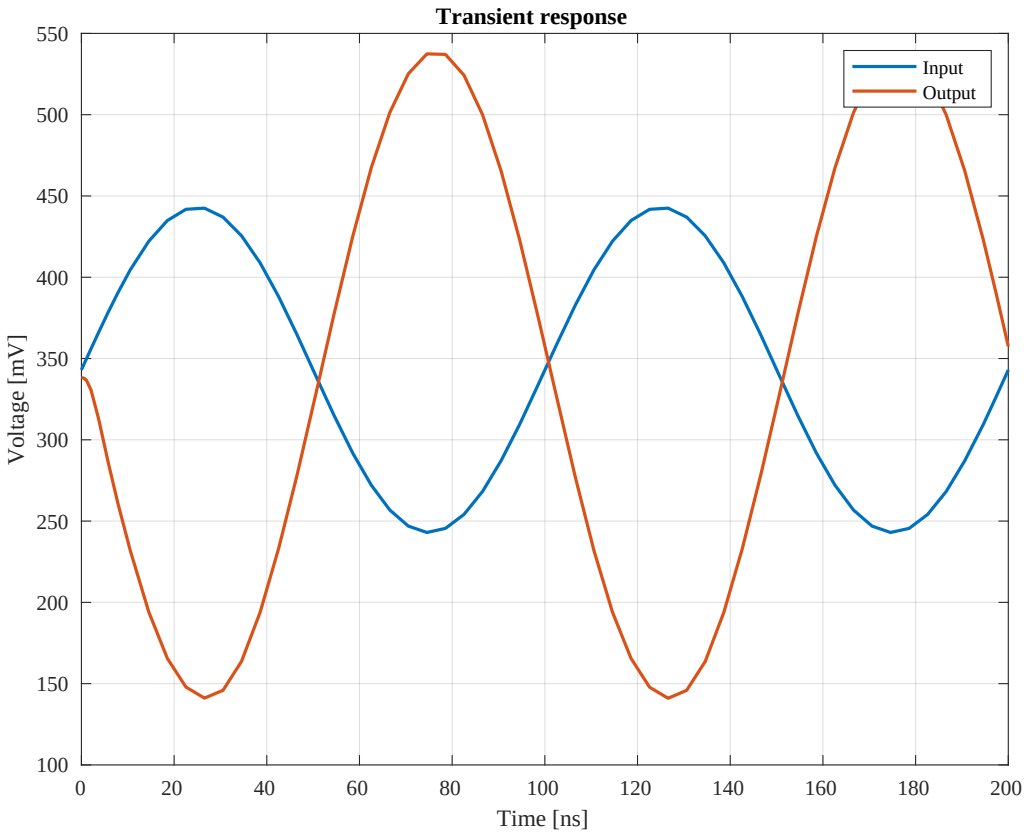


Figure 12: Transient response

Figure 12 shows 0.5V voltage swing at output.