NTNU
Faculty of Information Technology
and Electrical Engineering
Department of Electronic Systems

TFE4187 - Analog CMOS 1

Term project - Design of an Operational Transconductance Amplifier (OTA)

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1 Topology & Hand calculations

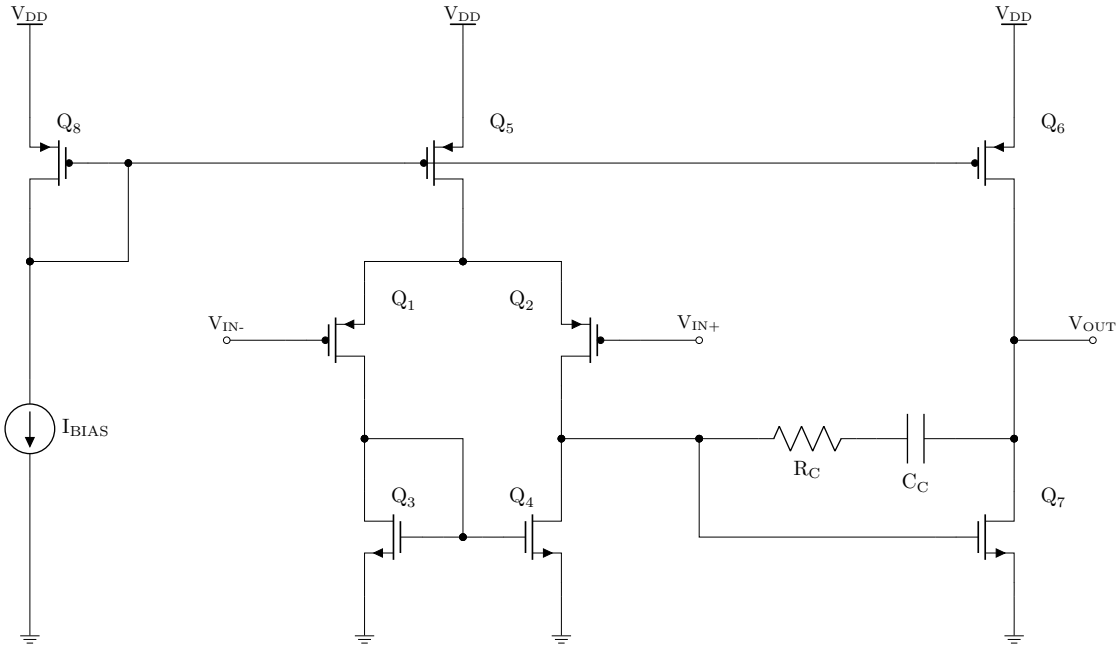


Figure 1: Two-stage Miller OTA

For the OTA design, the two-stage Miller OTA topology was chosen. Topology presented in figure 1

Specification:

V_{DD}	=	1 V
Large-signal low-frequency open-loop gain A_0	>	54 dB
SNDR at $f_{in} = 10\,\text{MHz}$ & $V_{OUT,P-P} = 0.5V$	>	40 dB
Phase margin at unity-gain feedback	=	60°

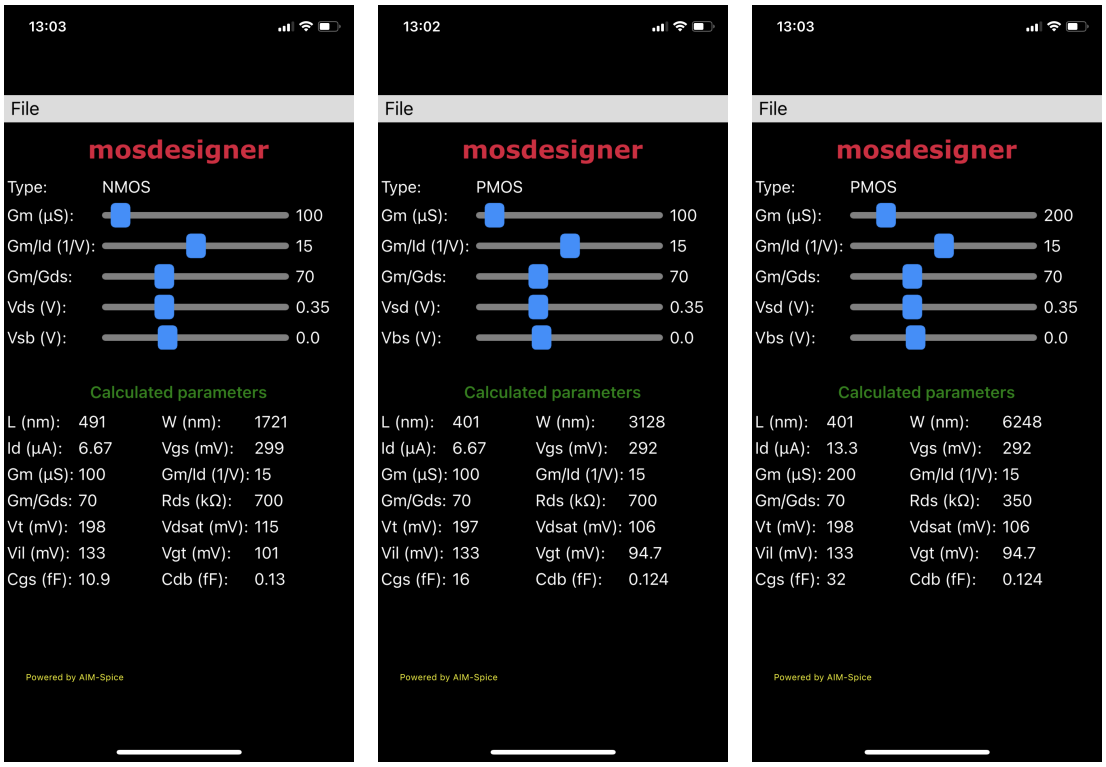
Initial guess, $C_L = 50\,\text{fF}$:

$$\Rightarrow g_m > 2\pi f_{ug} C_L = 2\pi \cdot 300\,\text{MHz} \cdot 50\,\text{fF}$$
$$g_m = 94.25\,\mu\text{S} \approx \underline{100\,\mu\text{S}}$$

$$A_O > 54dB$$
$$\Rightarrow \frac{g_m}{g_{ds}} = 2 \cdot \sqrt{10^{\frac{60dB}{20}}} = 63.25 \approx \underline{70}$$

$$\frac{g_m}{I_D} = \underline{15\,\text{V}^{-1}}$$

$$V_{ds} = V_{sd} = 0.33\,\text{V} \approx \underline{0.35\,\text{V}}$$
$$V_{bs} = V_{sb} = \underline{0\,\text{V}}, \text{ shorted bulk.}$$



(a) NMOS parameters **(b)** PMOS parameters **(c)** Bias PMOS parameters

Figure 2: Transistor parameters from *mosdesigner* using the values from the hand calculations

As the PMOS input from the current mirror *Q5* has to be able to bias the differential input gain stage *Q1, Q2, Q3* and *Q4*. The current through *Q5* needs to be twice the branch current of the differential stage to be able to bias both branches with the required current. Hence the bias PMOS transistor needs to be twice the width of the ones in the differential stage, as shown in figure 2.

The circuit was setup in *Cadence Virtuoso* as shown in figure 3

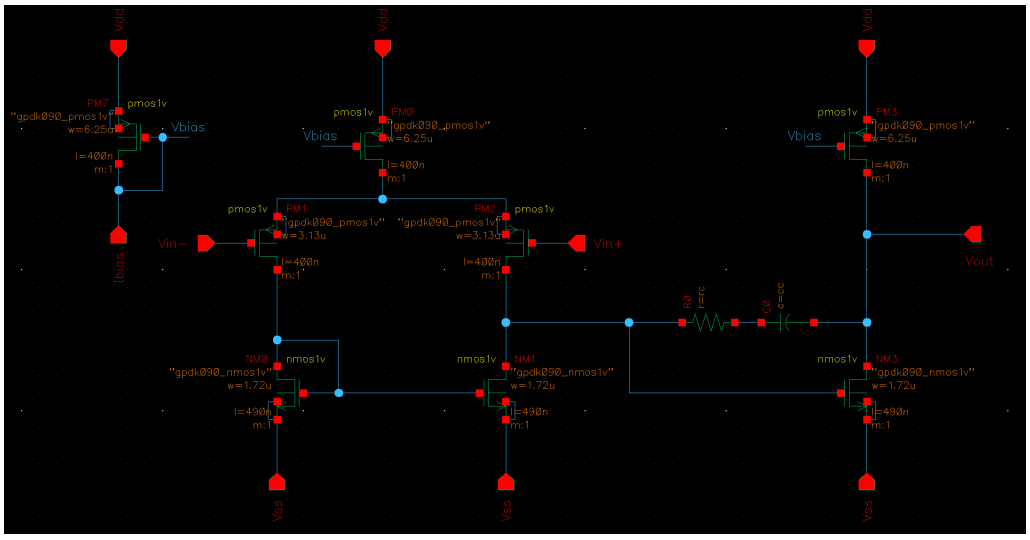


Figure 3: OTA setup in *Virtuoso*

2 AC-analysis

AC-analysis and simulations where done with the following simulation setup.

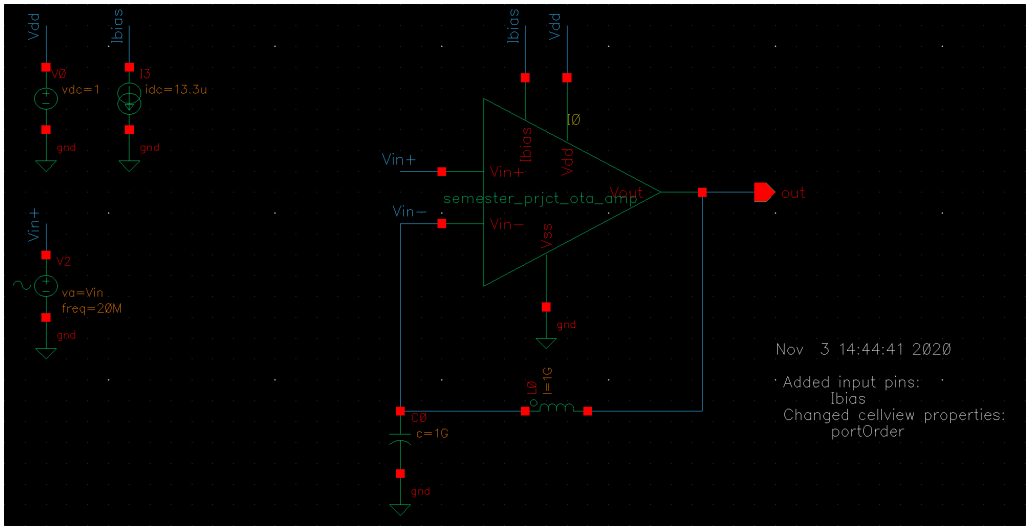


Figure 4: AC testbench

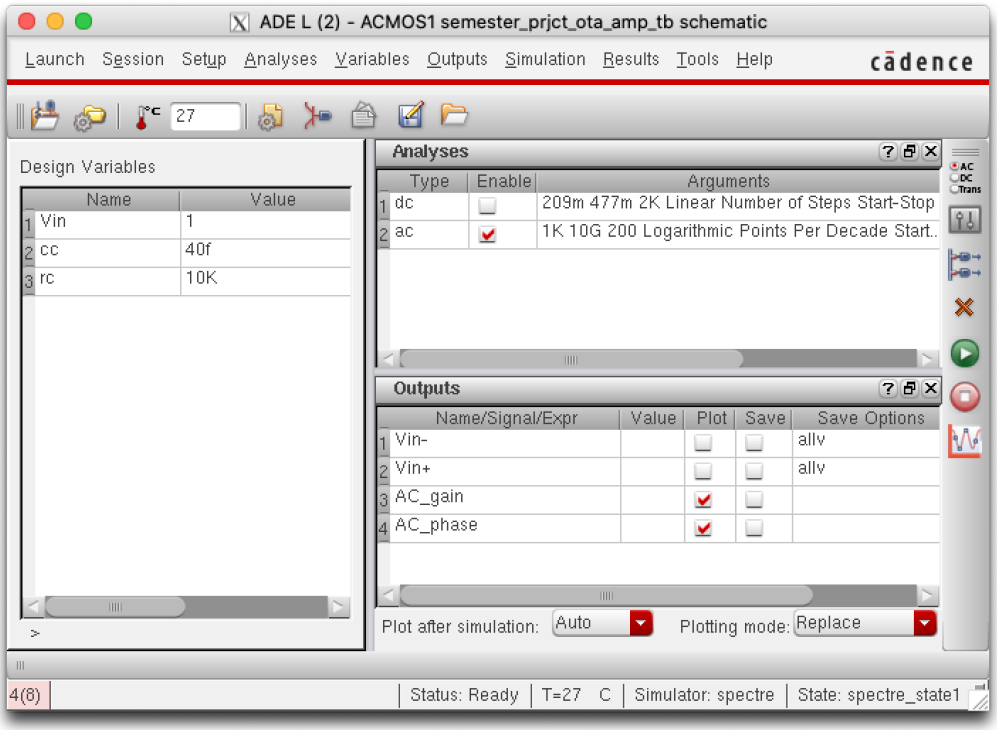


Figure 5: ADE L setup for AC analysis

Had to add compensation components, started with $C_c = 50\,\text{fF}$ & $R_C = 10\,\text{k}\Omega$. After some tweaking the values where changed to $C_c = 40\,\text{fF}$ and R_C, as this creates a decent phasemargin while still maintaining a decent gain, as seen in figure 6 and figure 7.

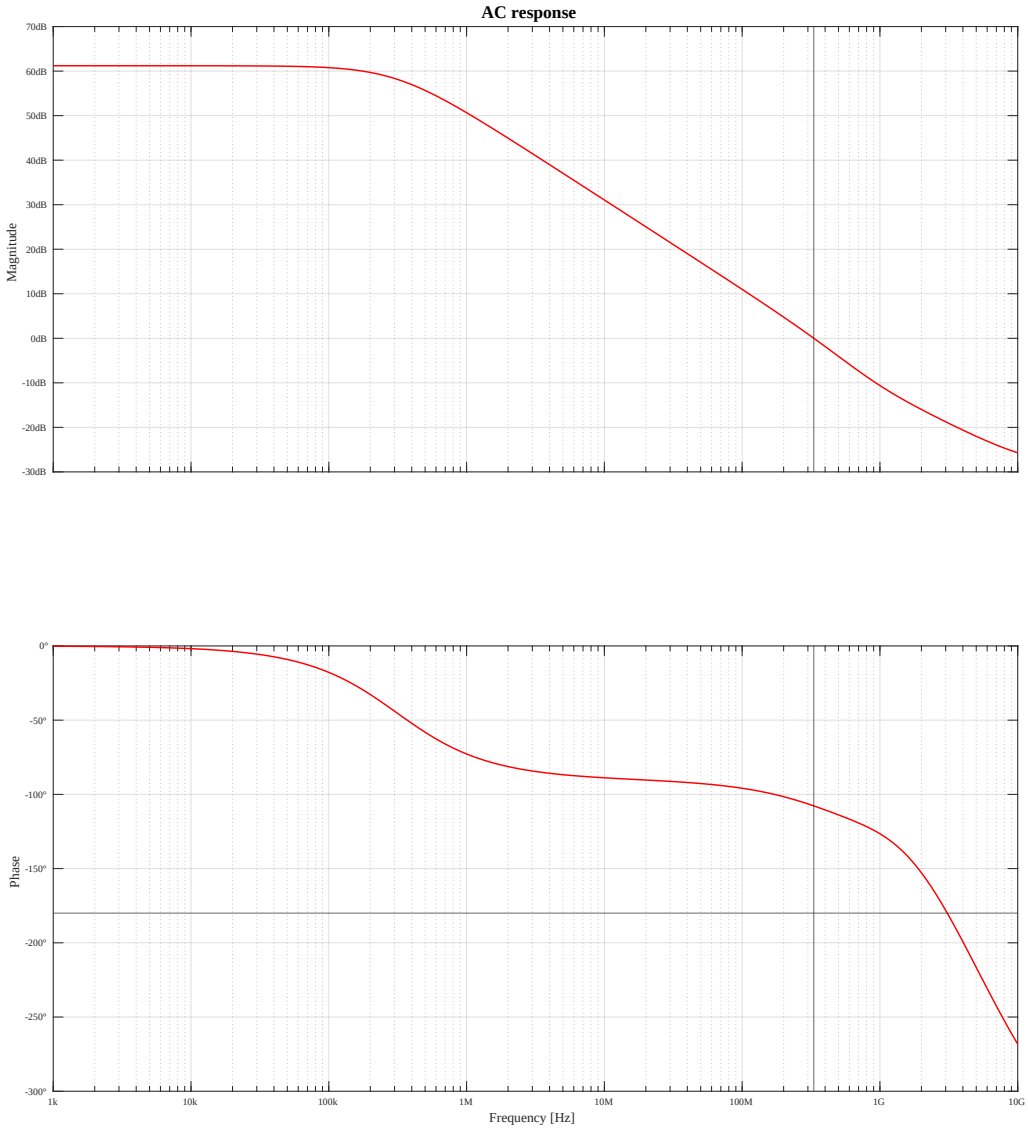


Figure 6: AC (open-loop) response with $C_C = 40\,\mathrm{fF}$ and $R_C = 10\,\mathrm{k\Omega}$

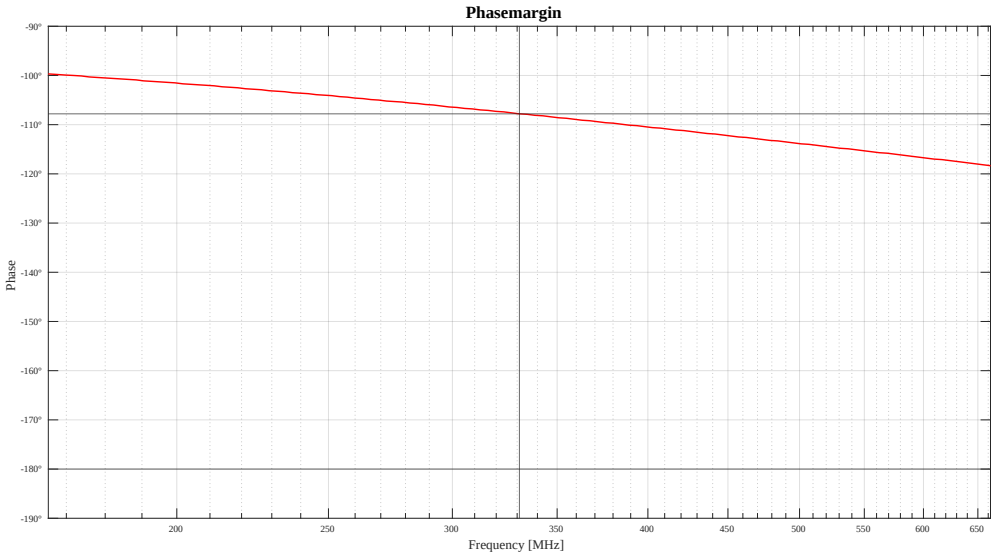


Figure 7: Phase margin with $C_C = 40\,\mathrm{fF}$ and $R_C = 10\,\mathrm{k\Omega}$

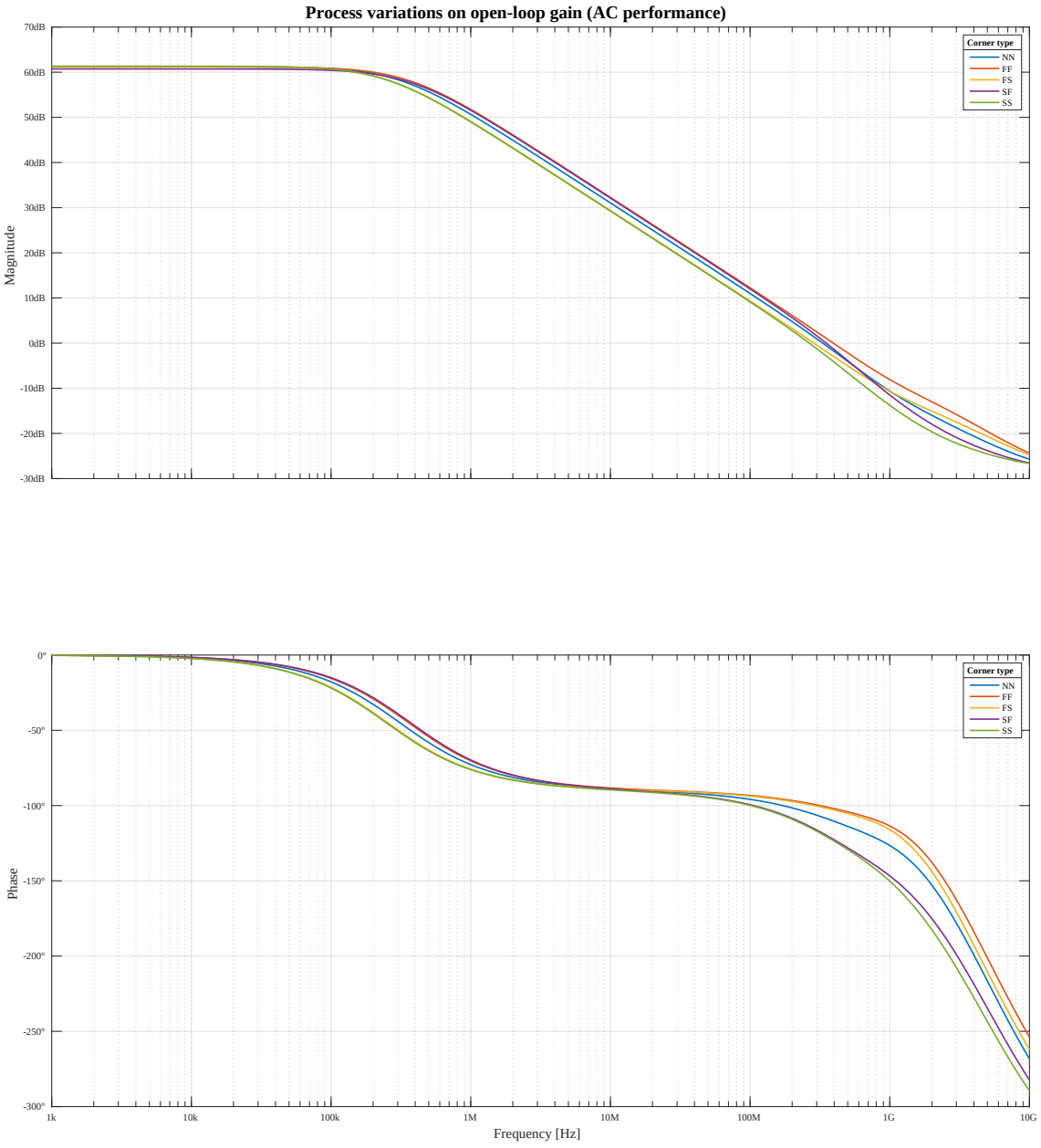


Figure 8: Process variations

3 Closed-loop analysis

Closed-loop analysis was done using the following setup:

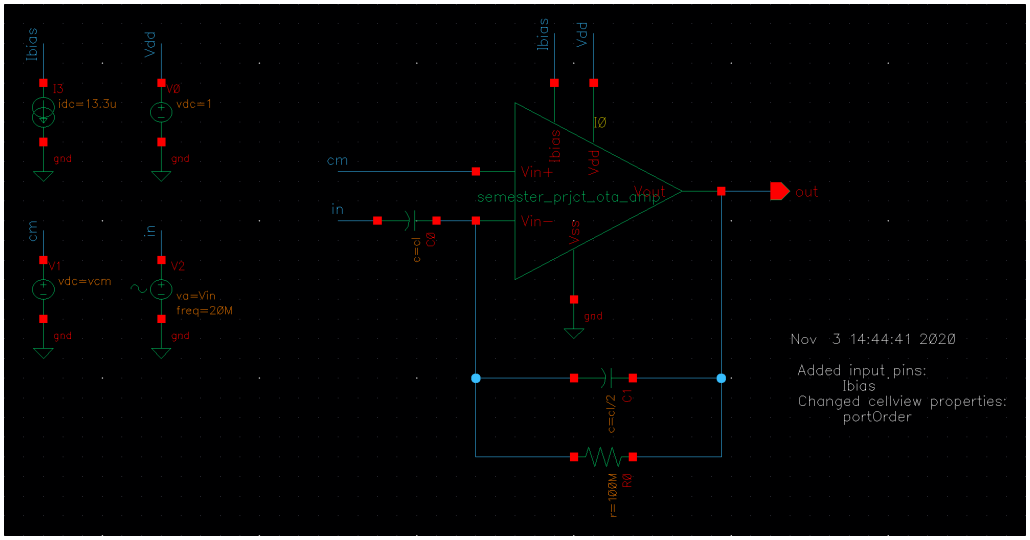


Figure 9: Closed-loop testbench

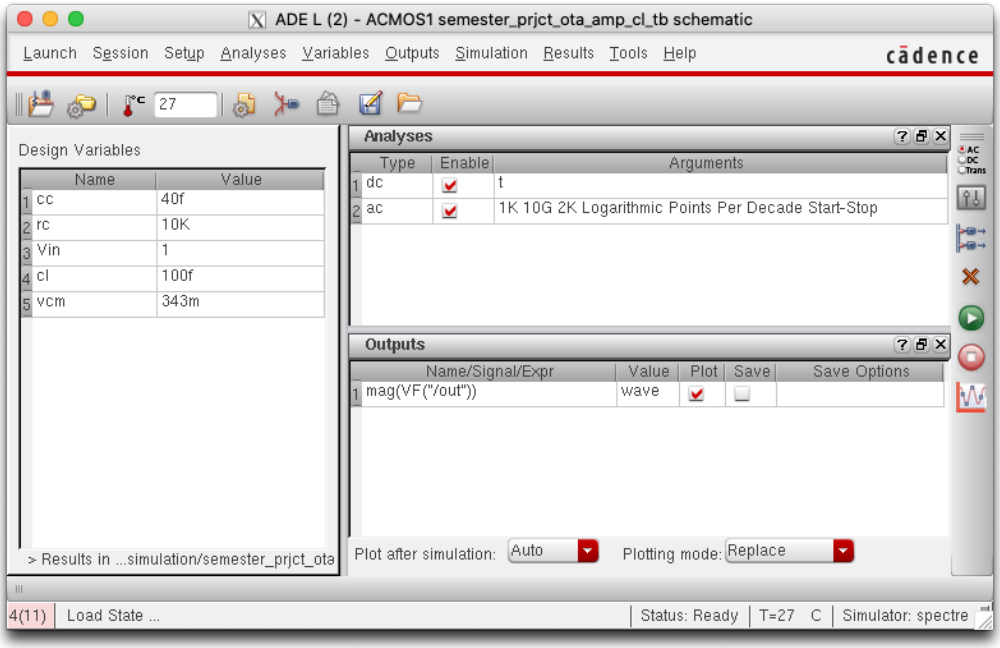


Figure 10: ADE L setup for closed-loop simulation

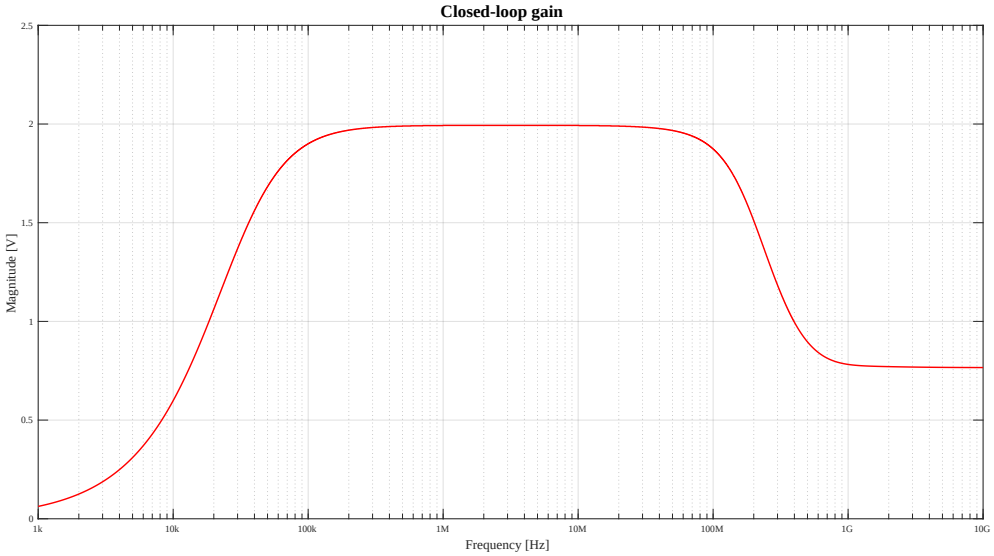


Figure 11: Closed-loop gain

4 Transient analysis

Transient analysis and simulations where done with the following simulation setup.

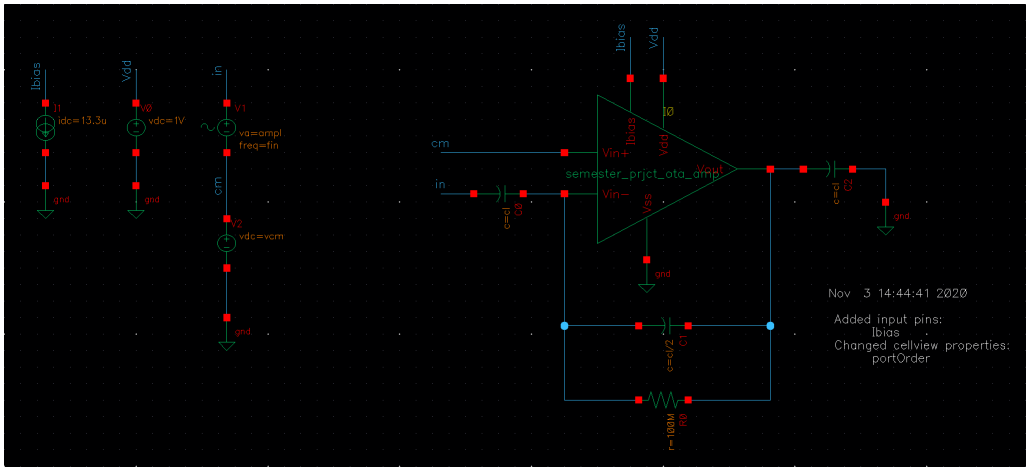


Figure 12: Transient testbench

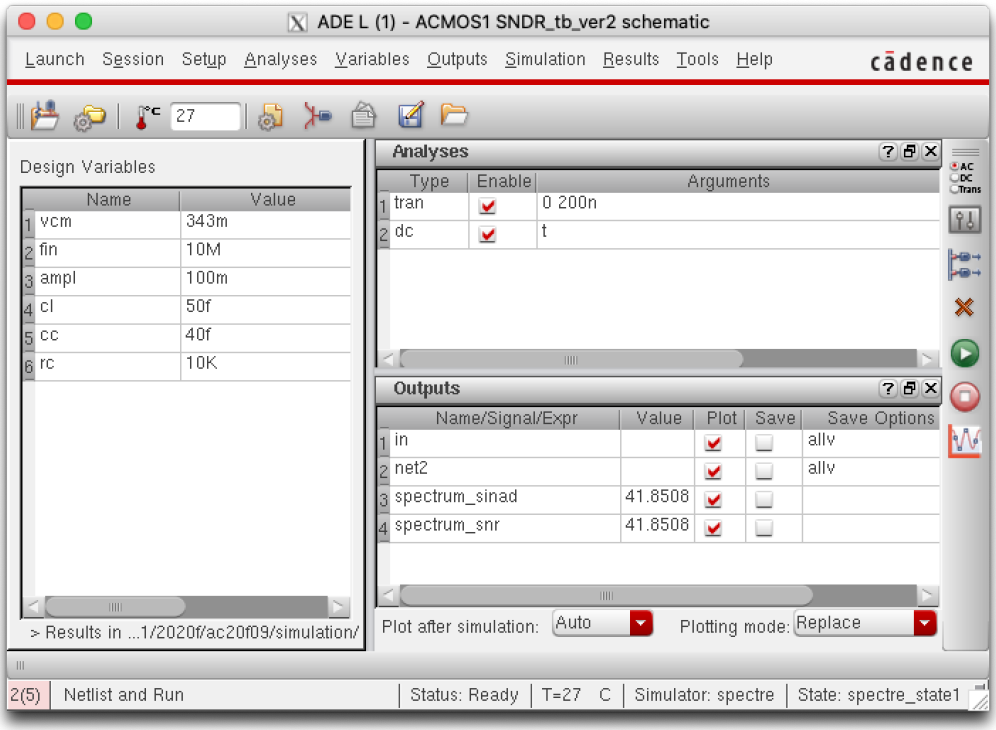


Figure 13: ADE L setup for transient analysis

As seen in figure 13, SNDR(SINAD) = 41.85 dB

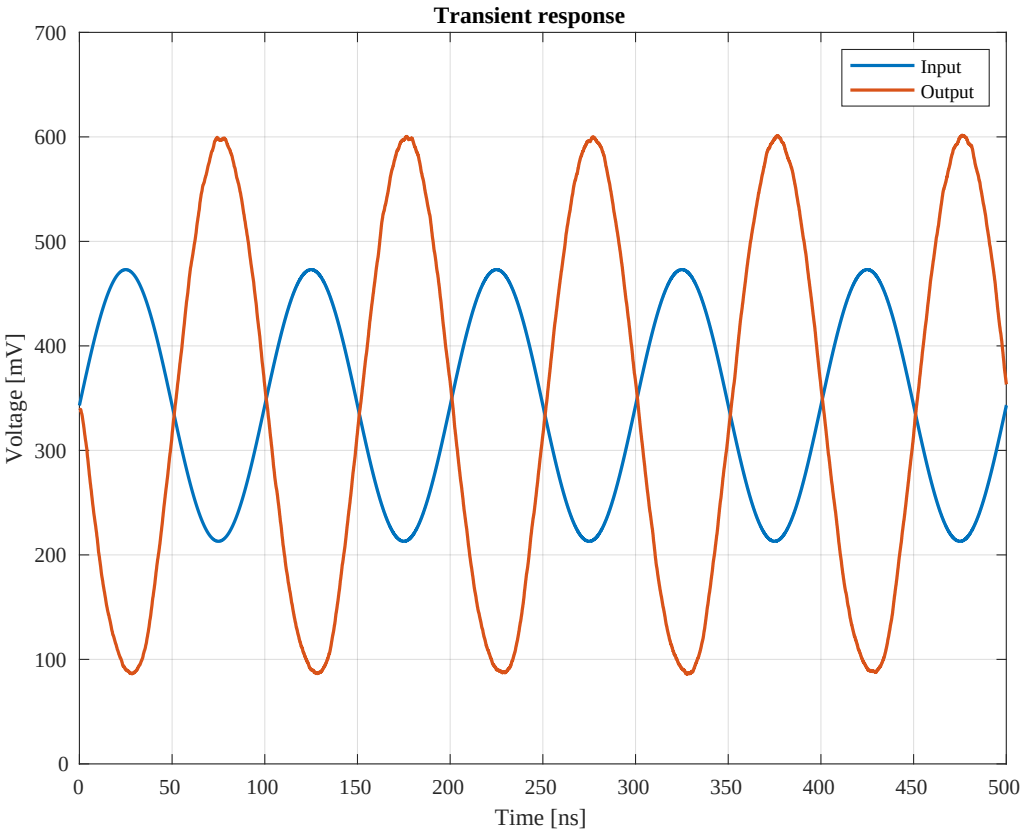


Figure 14: Transient response

Figure 14 shows approximately 0.5 V voltage swing at output.