ECEN 405

Lab 2: Power converters (Part 1 - Synchronous buck converter) Submission

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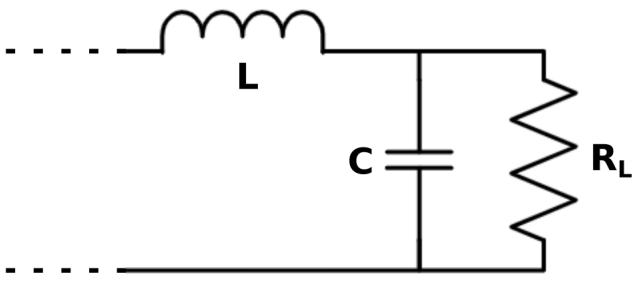
1 Output Filter

$V_{in} = 30V,\ V_{out} = 20,\ f_{sw} = 22kHz,\ R_L = 100\Omega$



$$D = \frac{V_{out}}{V_{in}} = 0.66\bar{6},\ V_{os} = 0.05V_{out} = 1V$$

$$I_L = \frac{V_{out}}{R_L}0.2A,\ I_{ripple} = 0.4I_L = 0.08A,\ I_{max} = I_L + \frac{I_{ripple}}{2} = 0.24$$

$$L = \frac{V_{out} \cdot (1-D)}{f_{sw} \cdot I_{ripple}} = 0.00378 = 3.78mH$$

$$C = \frac{I_{max}^2 \cdot L}{(V_o + V_{os})^2 - V_o^2} = 0.0000053215 = 5.32\mu F$$

1.1 Discontinuous Conduction Frequency

$$f_d = \frac{R_L\,(1-D)}{2L} = 4400Hz$$

2 Deadtime Resistance

From datasheet:
$R_{DT} = 0 \rightarrow DT = 0.4\mu S$
$R_{DT} = 200k \rightarrow DT = 5\mu S$

$$\frac{\mu S}{k\Omega} = \frac{5 - 0.4}{200} = 0.023$$

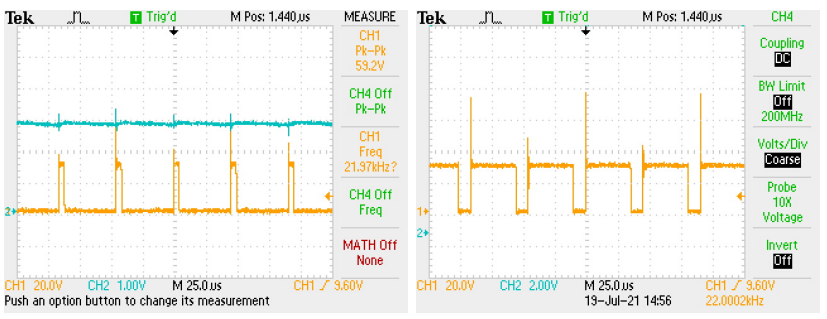
$$R_{DT} = \frac{0.5 - 0.4}{0.023} = 4.3478k\Omega$$

Deadtime, in the context on MOSFET gate driving, is the time between 1 FET's gate is switched off and the other is turned on. This prevents the circumstance when (the FETs being in series between V+ and GND without resistance) both FETS are on due to switching delays and causes a short.

3 Constant Output

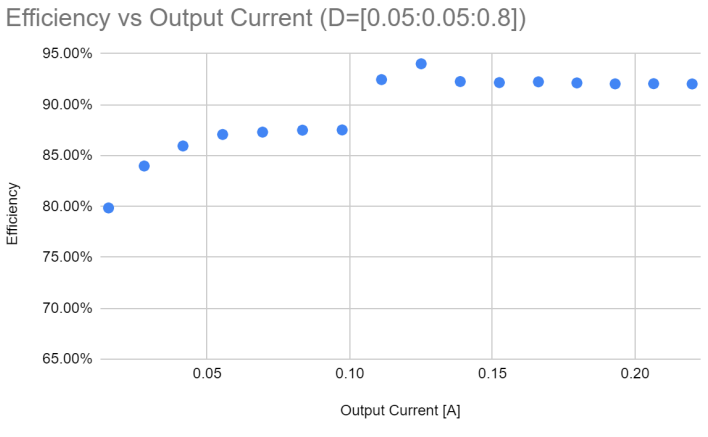
The filtering capacitance smooths the high frequency PWM output and the VL varies dependant on Vin to meet constant output voltage.

4 Waveforms



The waveforms above are captured from the S-D junction of the FETs, Ie the output, and shows the pulse width modulated signal of the Vo = 20V at both 10 and 80 percent.

5 Efficiency vs Output Current



6 Bootstrap Circuit

The bootstrap circuit provides a positive bias for the high-side gate driver. This provides the correct reference to enable the gate to be switched on when the high-side driver is active.