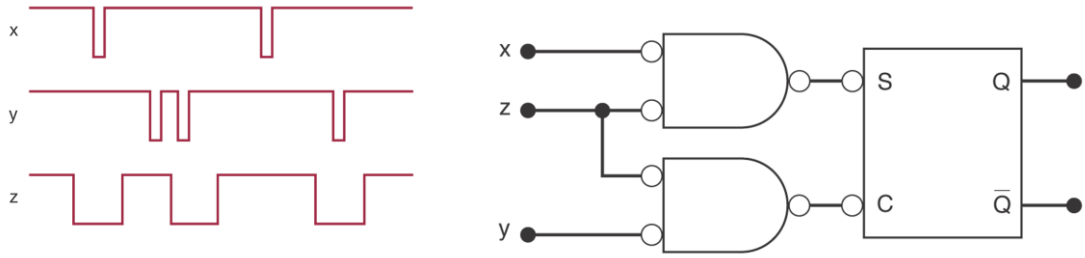
ECEN202 **Assignment 2** **2019**

Sequential Logic: Flip Flops and counters

Due Date: Monday 1 April.

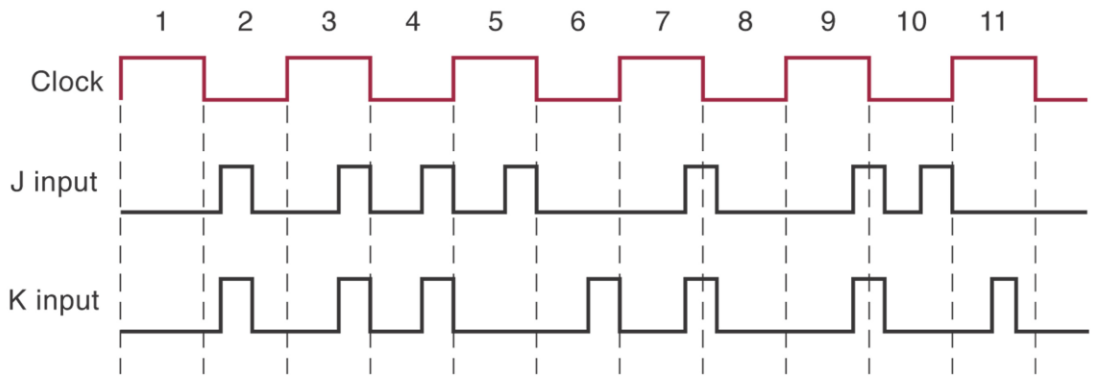
1. The waveform shown below is connected to the circuit shown. Assume that initially Q = 1 and sketch the resultant Q waveform.



2. The waveforms shown below are applied to two different FF's:
   (a) a positive edge triggered J-K
   (b) a negative edge triggered J-K.

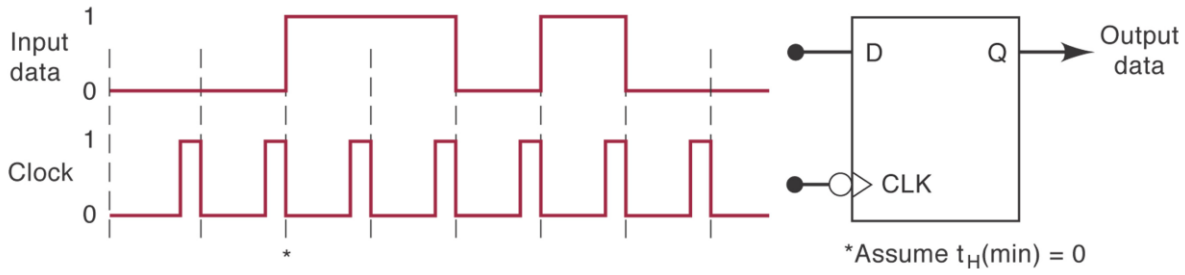
If the CLK and J and/or K appear to change simultaneously you can assume that the CLK transition always takes place before any transition in J or K.

Draw the Q waveform for each of these the two cases (a) and (b). Assume that Q = 1 initially.

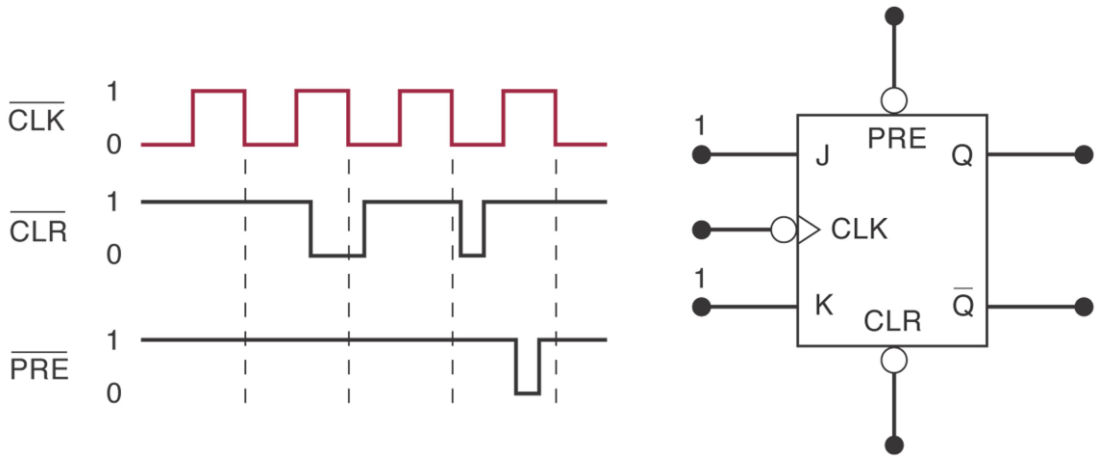


3. A D FF is sometimes used to delay a binary waveform so that the binary information appears at the O/P a certain amount of time after it appears at the D input.

(a) Determine the Q waveform for the circuit below and compare it to the I/P waveform. Note that it should be delayed from the I/P by one clock period.
(b) How can a delay of two clock periods be implemented ?



4. Determine the Q waveform in the figure below.



5. Show how you will construct a 3-bit binary down counter from J-K flip flops that trigger on the negative going transition.

6. Use J-K FF's and any other necessary logic to design an asynchronous MOD 24 counter.

7. Show how a 74LS293 counter can be used to generate a 1.2 kHz signal from a 18 kHz input signal (assume square wave).

8. Design a frequency divider that will divide the 50 Hz frequency from the mains electricity to generate a 1 Hz clock signal.

9. Sketch the design of a synchronous up/down 4-bit BCD counter. Use J-K flip flops as the counter elements and any further logic gates needed.

10. Draw a design for a MOD 60 synchronous (parallel) counter. Determine the maximum frequency the counter can operate at if each FF has t_{pd} = 20 ns and each gate had t_{pd} = 10 ns.