Quiz Night Timer

Digital Circuit Design and Implementation Report

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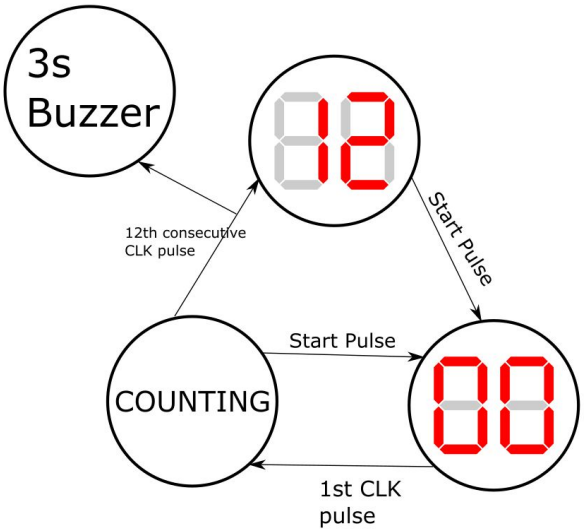
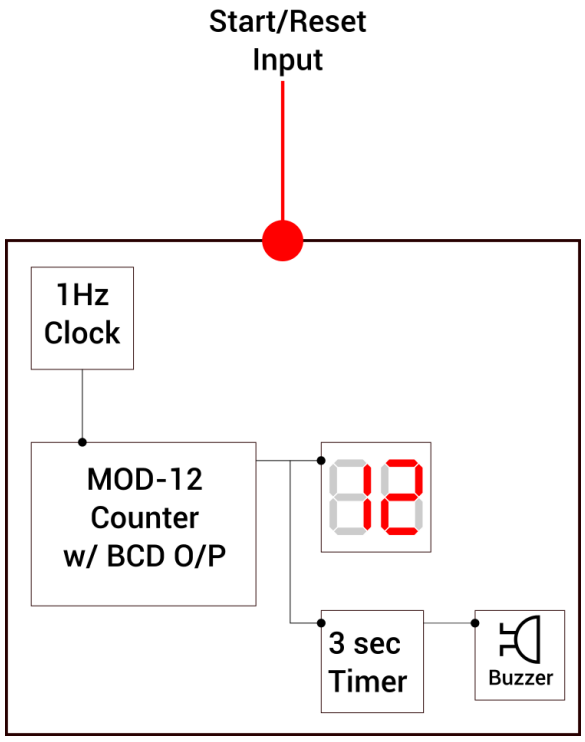
Introduction.

We designed and constructed a circuit to function as a pub quiz timer that when triggered counts for 12 seconds, sound a buzzers for 3s and stops until next triggered.
It is designed as a fully functional block of circuitry with one control input (start button) and two main outputs, the display and end buzzer, with all operations handled with internal blocks.
It needed to ensure that participants answer within a specified time, having the following specifications:

1. Includes a master start button, also resets.
2. Count in 1 second increments to a specified time, in this case 12
3. Output compatible to be displayed on 2 7-segment LED displays
4. At the timers end, timer/display stops (not resetting)
5. Triggers a 3 second buzzer



Design Methodology.



Functional Design Blocks

We had two options when designing the mod-12 counter block.

1. Use a dual decade counter chip, wired to mod-100 and modded down to 12 and each counters 4 output driving each LED 7-seg display

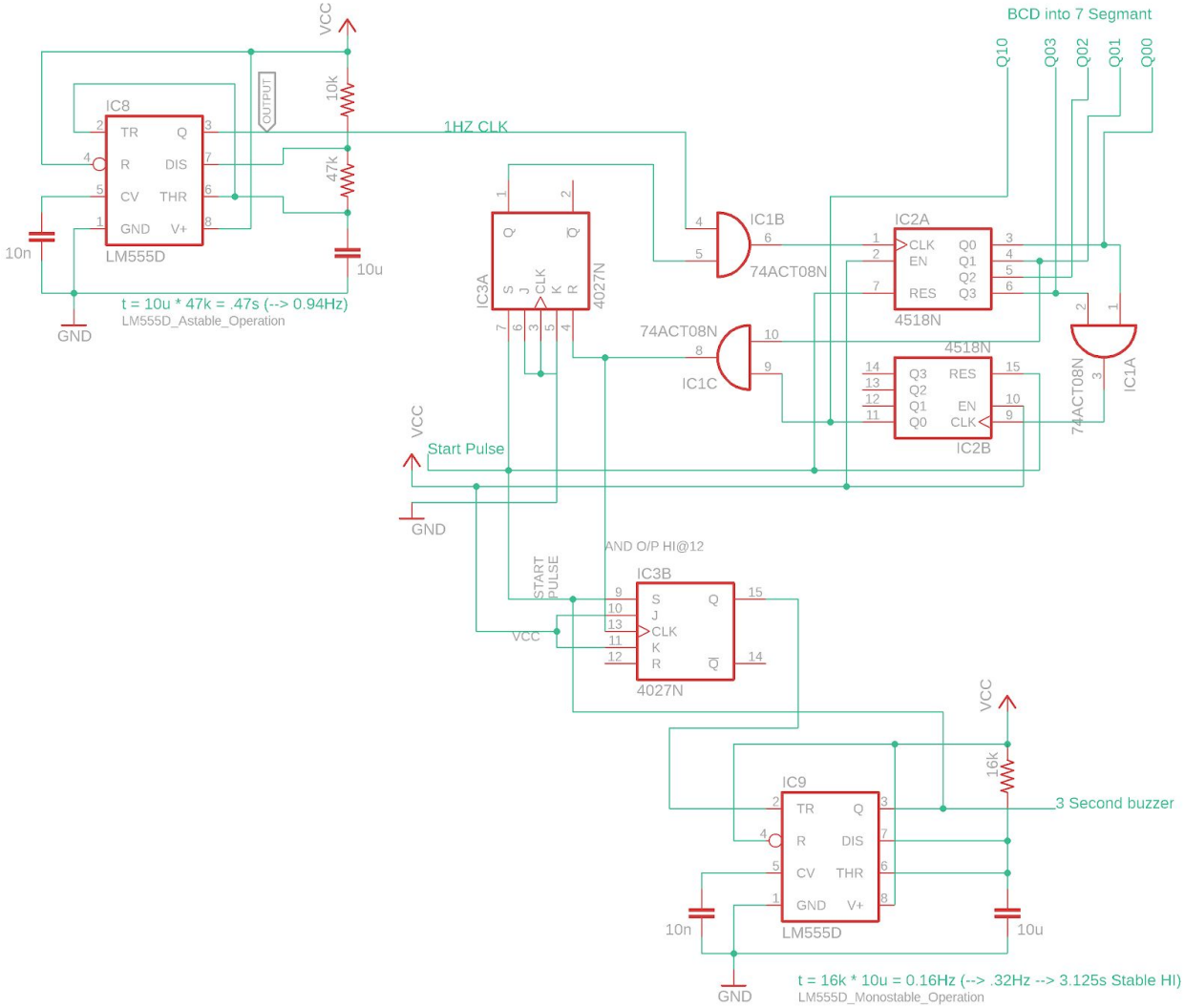
2. Or use 4 bit JK ripple counter, modded down to 12 and the the 4 bit output converted through a binary to BCD circuit or IC

The 4 bit down-modded JK design would have required 4 JKs in a ripple counter configuration or dedicated 4 bit ripple chip and additional circuitry or at least another chip to convert the outputted 4 bit binary signal to a Binary Coded Decimal signal w/ at least 5 bits, compatible with the 7-seg LED displays.

We chose to use the duel decade chip designed to minimise IC use, and complexity of the entire system. This, we thought would the more intuitive solution not only for implantation but also testing, both unit and full integration.

Design Description.

Fully Implemented Circuit Diagram

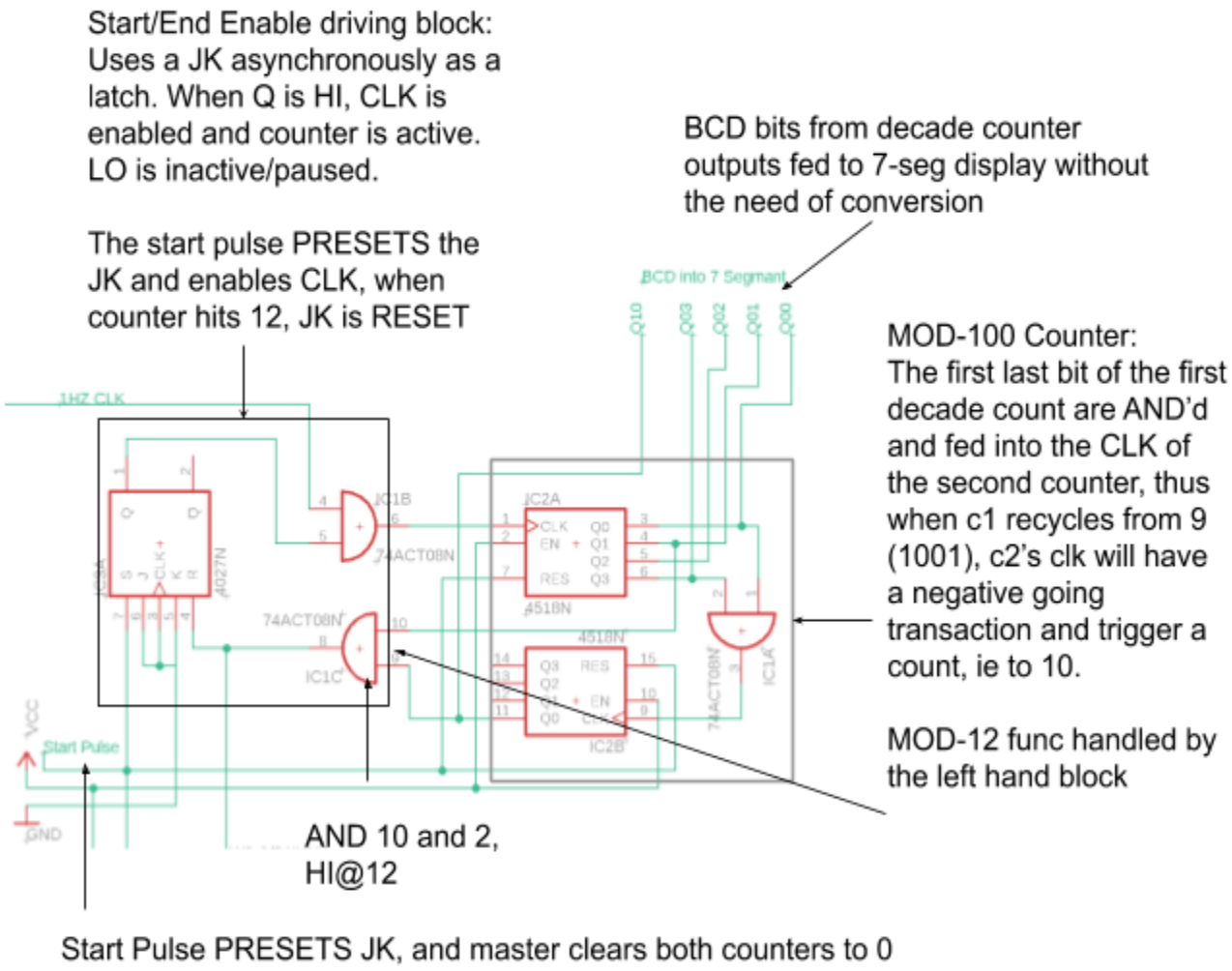


Fully implemented counter circuit design of the 3 main functional logic blocks; MOD-12 BCD counter, start pulse driving block, 1Hz clock, and 3 second timer/buzzer.
This implementation requires the following [or functionally equivalent] IC chips and components:

- 1×74HCT390 Dual decade ripple counter
- 1×74HCT112 Dual JK flip-flop with set and reset; negative-edge trigger
- 1×74HCT08 Quad 2-input AND gate
- 2×555 Timer, Monostable or Astable
- 2×10uF and 2×10nF capacitor
- 1×150k, 1×47k, and 10k ohm resistors

Our construction process involved building and unit testing each separate functional block before integrating into full circuit. In addition, we used external tools such a signal generator to emulate the 1Hz CLK functionality before we implemented it.

MOD-12 Counter w/ BDC O/P



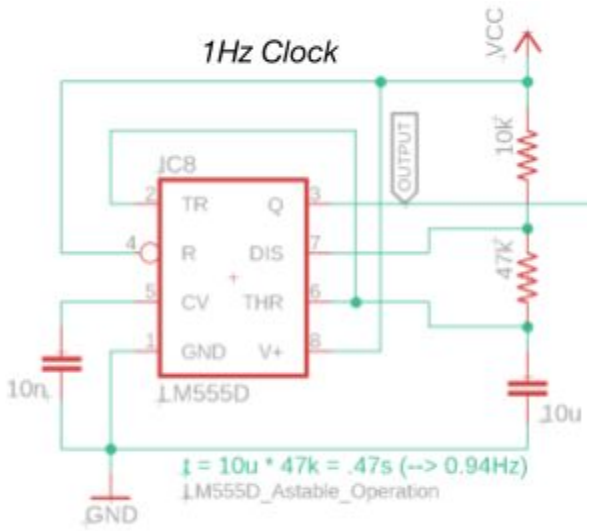
Requires: 74HCT390 Dual decade ripple counter, 74HCT112 Dual JK flip-flop, 74HCT08 Quad 2-input AND gate

This circuit is the implementation of the MOD-12 counter and start button controls blocks. It uses a duel decade counter chip (MOD-100), a JK to enable/disable counting and start pulse input to initiate counting and recycling counter from 12.

JK is setup as a Latch using the asynchronous overrides. So that when SET, the CLK is enabled and vise versa. The start pulser SETS the JK and is RESET when the counter reaches 12 [AND O/P of Q01, Q10).

The correct operation of the block is as follows:

1. Static O/P to display of 12
2. Start pulse → display clears to 00
3. Counts from 00, 01, 02,...,11, 12
4. Freezes at 12 until next start pulse

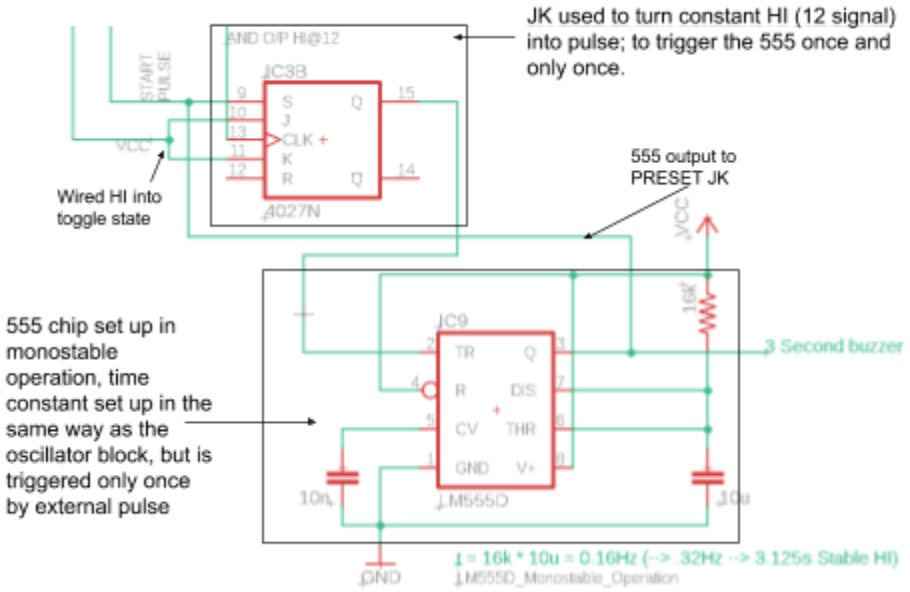


Requires: 555 Timer; Monostable/Astable, 2 resistors (one more the 3x smaller), up to 2 caps (10nF may not be needed)

To supply a 1Hz CLK signal to the main counter block, we chose to construct a standard 555 timer in a Astable operation configuration. With a VCC supply voltage, and when grounded this circuit will continuously oscillate between HI and LOW output (at Q); thus supplying a squared clock signal to the rest of the circuit.
In short this operates by utilising the charge discharge cycle of the larger capacitor to periodically grounding the reset (active LO).

To determine the frequency of this oscillation use the formulae: f = 2(Large R * Large C), in our case 2 (10u * 47k) = 0.94Hz, this gave a T = 1/.94 → so our timer kept a 1.06 second resolution

3 Second buzzer



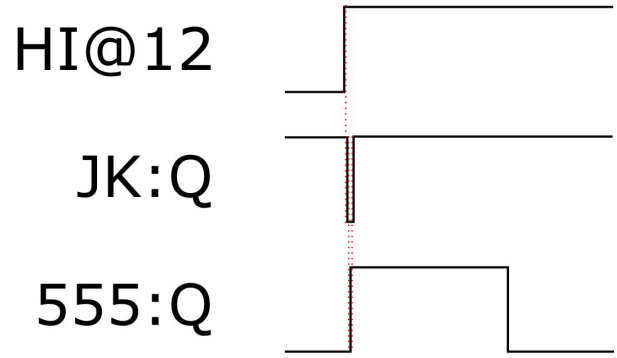
Requires: 74HCT112 Dual JK flip-flop, 555 Timer; Monostable/Astable, 1 resistor, up to 2 caps (10nF may not be needed)

This block is set up with 555 monostable operation, with a HI output stable for 3 seconds; determined by:

*2(RC); 2(16k*10u) = 0.32Hz, T = 1/0.32 → a stable HI O/P for 3.125s.*

The correct operation is when the counter hits 12 and stops, timer outputs HI for 3 seconds, to a buzzer or other indicator [to test we used and LED], then that stops and entire system becomes static (until next start pulse)

JK setup: The JK is used to turn 12 HI signal to a HI>LO>HI pulse to trigger 555. J/K inputs are HI to set into toggle state, Q is fed into TR of 555 and the PRESET is wired to the system start pulse and the 555 output, and the counter q01 AND q10 O/P is the CLK input.
Due to the PRESET wiring, its initial state is Q:HI, when counter hits 12, CLK pulses once, toggles Q:LO, this triggers the 555 and the HI 555 output PRESETS Q:HI again.



Construction note: depending on the JK chip, an inverter may be needed on the CLK I/P

Testing.

Our approach to testing our design and construction against the stated specification was a series of small unit tests being gradually integrated up towards the final function block.
For example with the main counter block, we would start with *dual decade counter* chip, set it up (say as mod-100) confirm its functionality by connecting the outputs the LED display; then adding the AND gate to mod it down 12 with the external AND + JK, test that and continuing to add chips and connections continuously confirming individual and integral functionality.

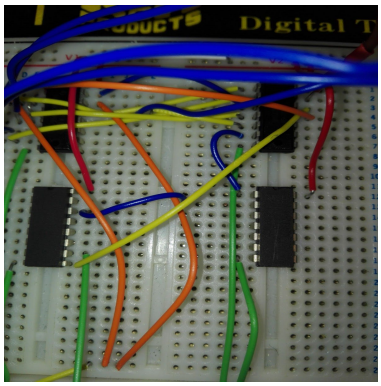
This approach allowed us the avoid having an ambiguous reason for failure, because if the block fails, we knew it was last implemented addition that caused the issue.

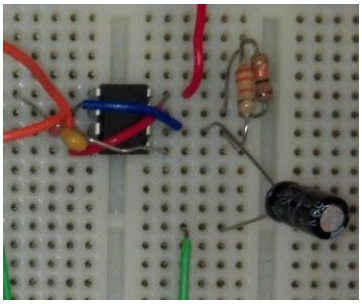
Specific issues we found in testing were; duel ripple decades usually require a manual connection between that first FF and the rest of counter so Q01 must be externally connected to CLK1. Other issues possible to encounter are the edge trigger type of the clock inputs, these may necessitate inverters depending on your systems specific block outputs.

One major issue that we were not able to physically implement the fix for was using the JK the transfer the constant HI of the counter 12 signal into a single pulse. Our problems were purely wiring the incorrect inputs and being sloppy with the asynchronous inputs. We included the correct implementation in the final design (above), it isn't a straight forward module and relies on feedback so continuous testing it highly advised.

Summary and conclusions.

In review we took a problem/scenario, in this case a Pub Quizzer timer application and firstly went about a top down functionality determination initial design, then with the use of CMOS digital IC chips and standard circuit design principles planned out a discrete circuit system to fulfil our specification.
In this we were successful (to a point), fully designing a system that allows user starting, counts for 12 seconds, stops and sends a 3 second output signal for external notification, say to a buzzer/blinker.
We also succeeded in physically implementing the circuit using IC's, breadboard and a design station.





We did not however implement or include a design the added functionality

- *If a contestant is ready to answer a question before the 12 seconds are up they should press a button and the clock should stop and indicate this time. It should then also sound a 1 second buzzer*

We could have simply did this with ORing a second pulse signal with 12 signal to the first JKs RESET and a second monostable 555 chip setup.

Personally I found this entire exercise incredibly fulfilling, undertaking a problem and using learned knowledge to design and implement a solution is exactly what I hope to be doing with my degree. Doing it as a small team was incredibly beneficial, as we were both actively inputting into this task, both to solve complex problems and to see things from differing perspectives.
I learned how to manage and test a larger project, manage and prioritise my time and built on my communication and cooperation.
The only thing I did not find enjoyable was the time restrictions and set working time though I understand their necessity, it does restrict spontaneous ideas.

All in all it was a gratifying experience and my success in it is very encouraging.