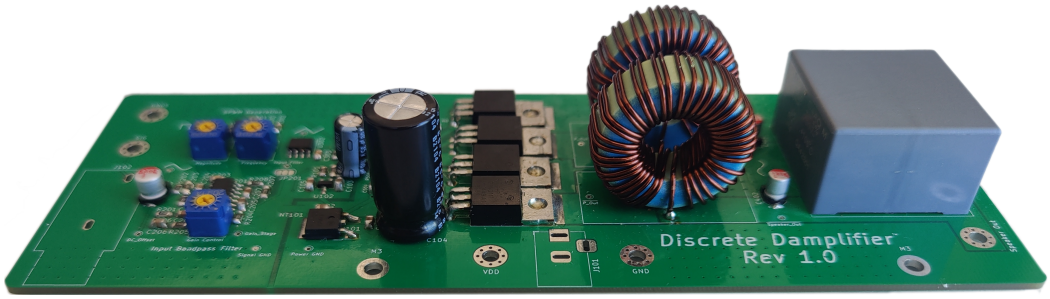
ECEN 405 - D Class Amplifier

"What a buck convertor would say if it could talk"

Daniel Eisen : 300447549
Team members: Niels CLayton & Nickolai Wolfe



1 Introduction

In the relm of auido ampliifers the D Class offers a method of supplying a high power loads with very high efficiency (esspecailly when compared to other classes). Classes A, AB offer high power output with very low signal distortion but suffer greatly in the efficency department. The D class of ampliifers can achieved up to 90-95% power efficiency by taking advantage of

Specifications

- $P_{out} = 80W$ for $R_L = 4\Omega$
- 10Hz to 200Hz Bandwidth
- Input sensitivity of 1V for maximum output (interperated as 1V amplitude, 2V pk-pk)
- Maximum costs: $50 per person

2 Design

Here you should describe how your class D amplifier works, giving details of each subsection. In detail, you should describe the section you designed and the design choices you made. If your team broke up the design of the amplifier in a way that doesn't suit individual parts being discussed, you will need to talk about the whole design in a bit more detail but you should also describe how the work was delegated and why.

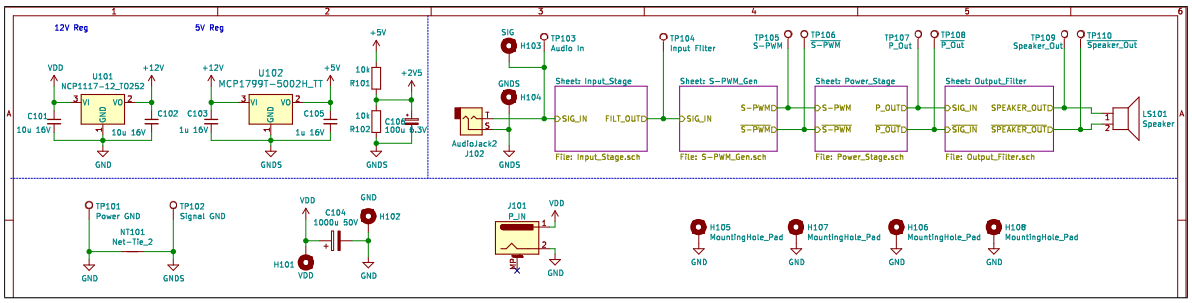


Figure 1: Top Level Design Schematic

2.1 Input Bandpass Filter

Active Bandpass filter with adjustable gain stage to pass 10Hz to 200Hz.

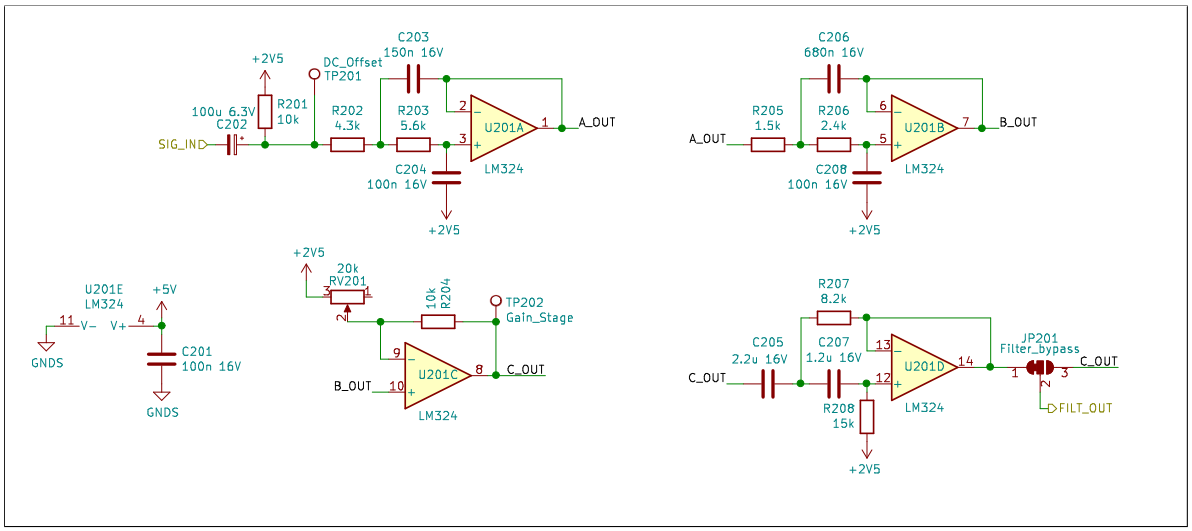


Figure 2: Input filtering schematic

2.2 Audio Sampling and SPWM

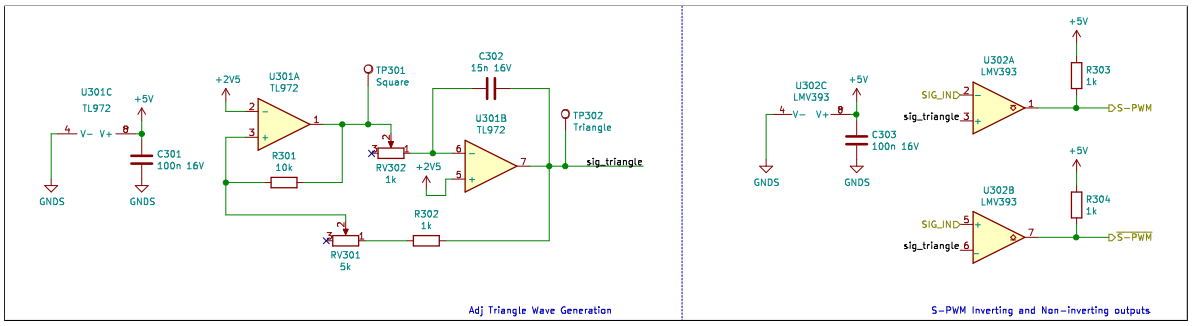


Figure 3: Sampling triangle wave & SPWM generation schematic

2.3 Power Stage and Output Filter

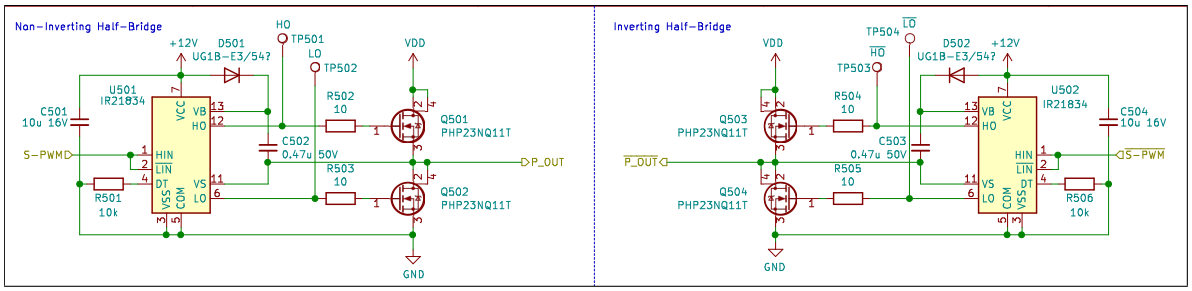


Figure 4: Gate driver schematic

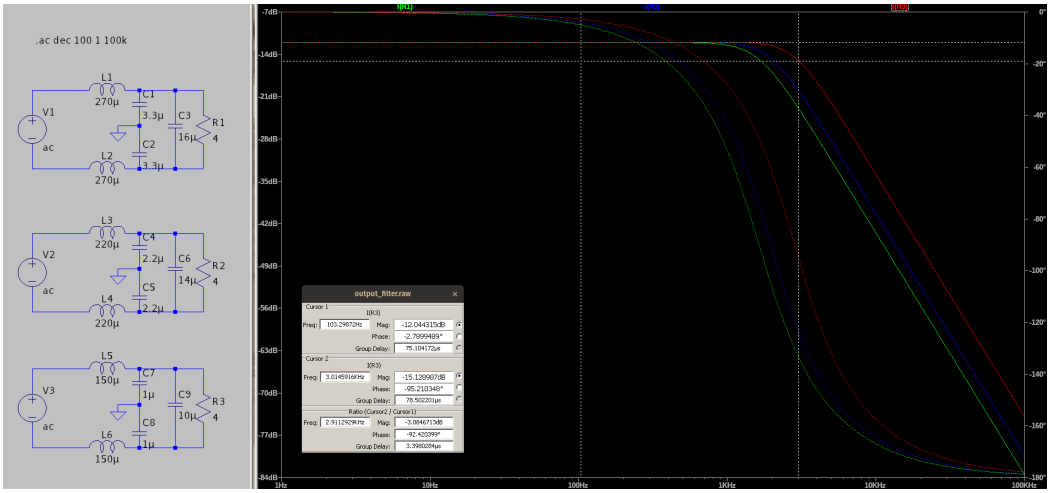


Figure 5: Output filter option simulations

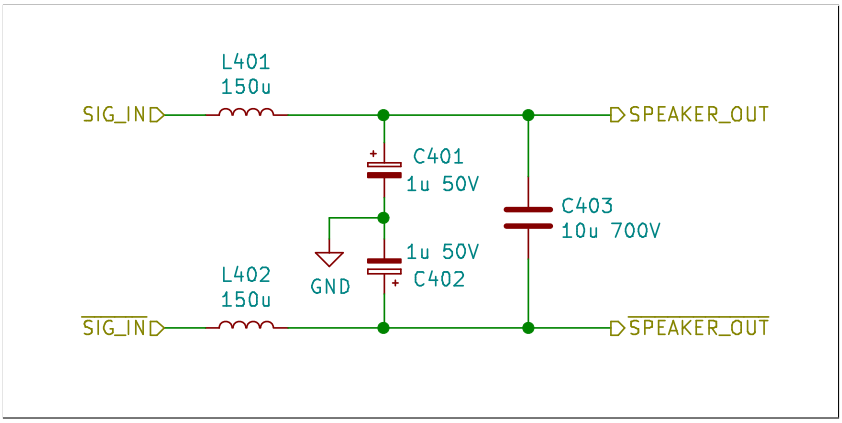


Figure 6: Final output filter schematic

3 Implementation

Here you should discuss the assembly of the amplifier and any problems you faced as a team building the amplifier. Here, the individual components should also be characterised. For example: if you have a filter, what is the response and how does it compare to the calculated? If you have a triangle wave, how does it look? Is it doing what I should? Why? Why not? How do the inputs/outputs of your comparator look? How does the square wave on the gate of the MOSFETs look?

3.1 PCB Layout

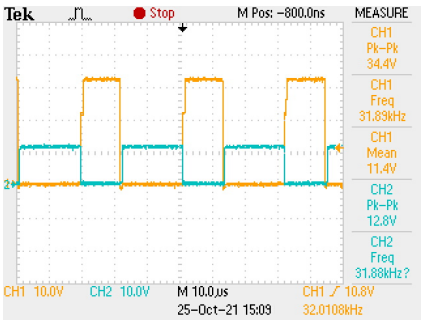
3.2 Gate Driving and Bridge Output

4 Results

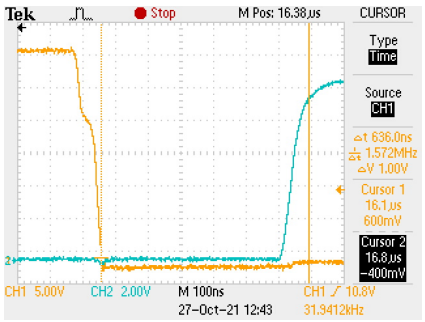
Here I would expect to see the results of the whole amp, for example: an output wave, analysis of the efficiency, discuss maximum power output (which may be frequency dependent), and THD.

5 Conclusions

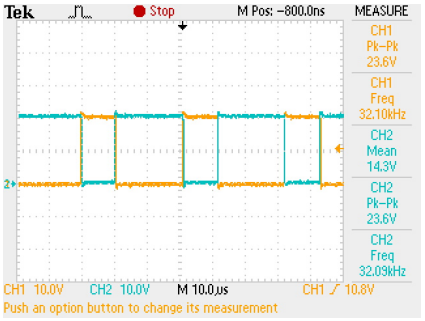
What worked, didn't work? How would you change your approach? Any interesting insights?



(a) High and Low side gate signals

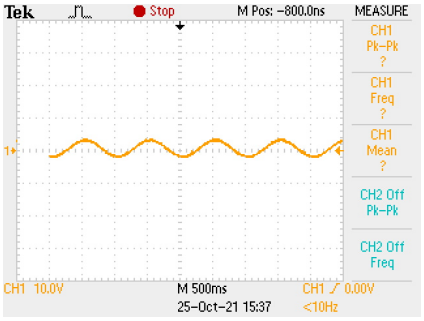


(b) Deadtime

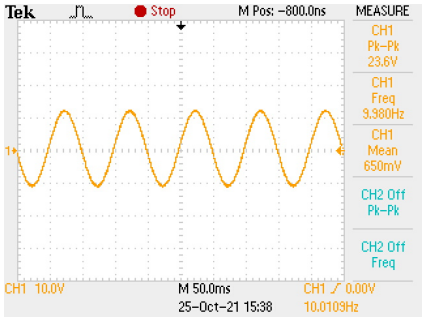


(c) Both bridges amplified SPWM (FET outputs)

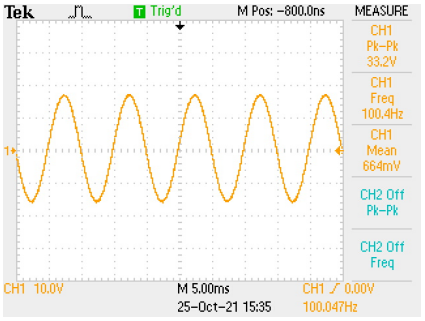
Figure 7



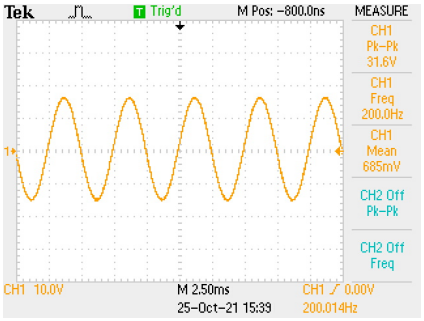
(a)



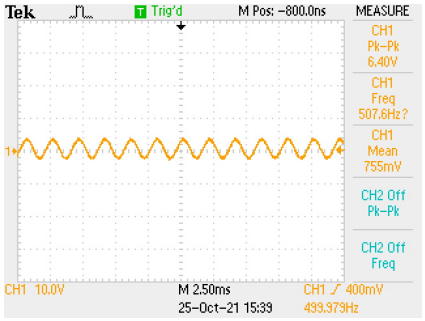
(b)



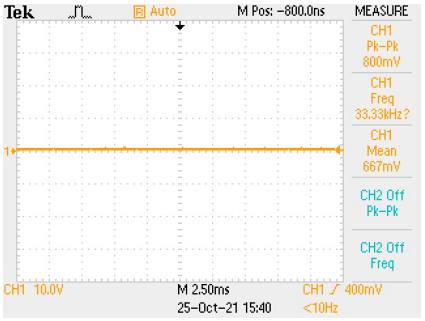
(c)



(d)



(e)



(f)

Figure 8

Frequency (Hz)	THD (%)
30	1.8
50	2.2
100	3.2
200	3.3
300	3.5
500	3.2

Table 1: Output total harmonic distortion across frequency

Appendix

Input Filter

Sampling/SPWM

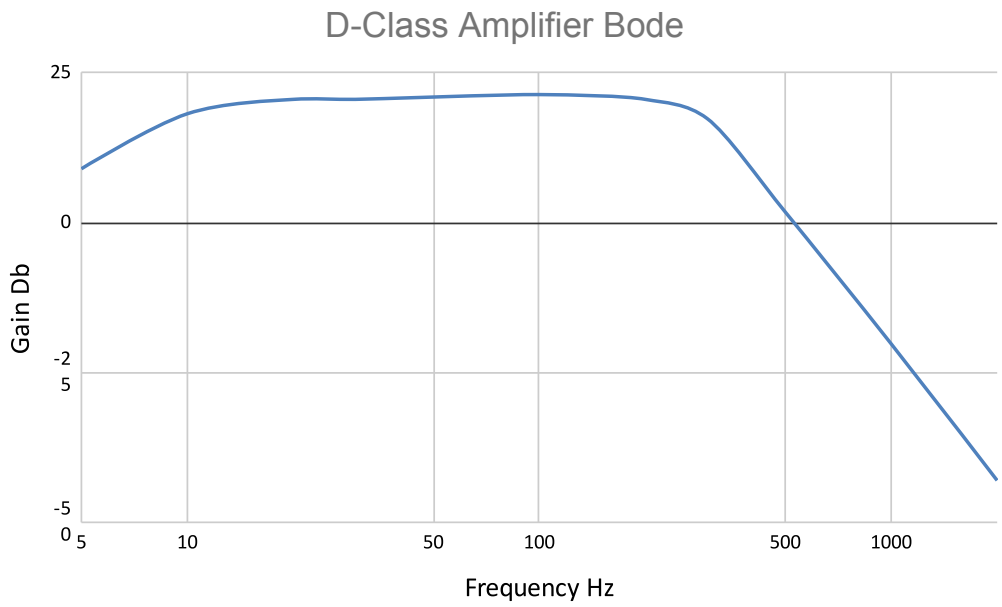


Figure 9

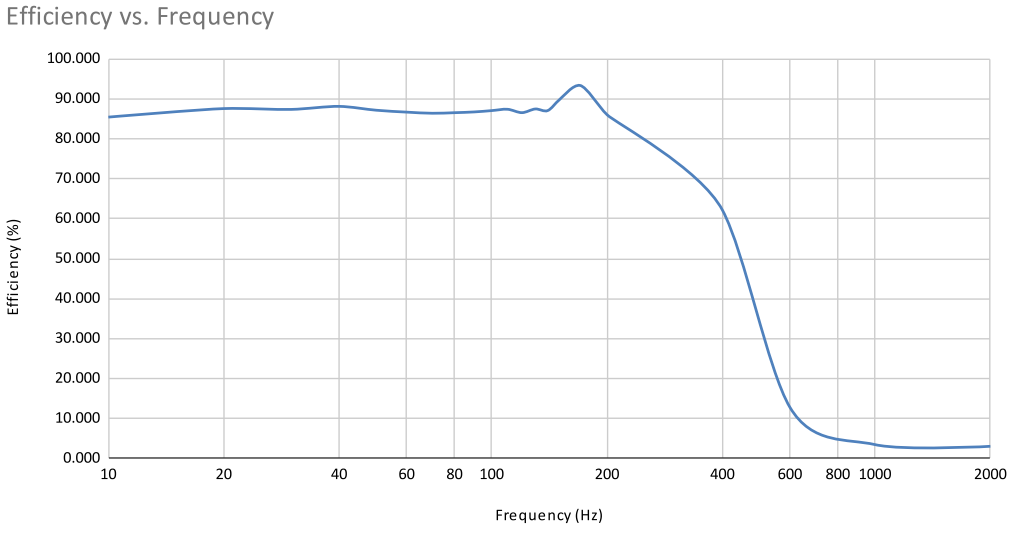
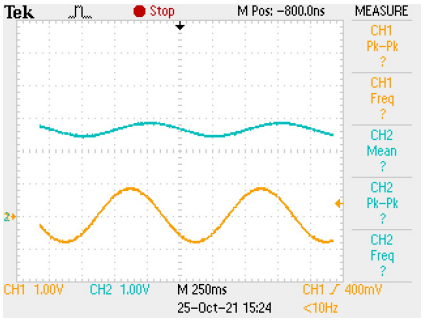
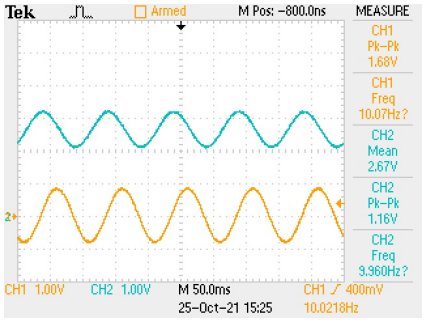


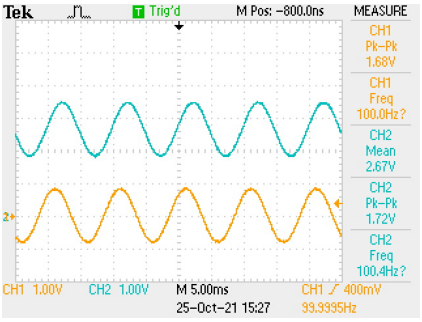
Figure 10



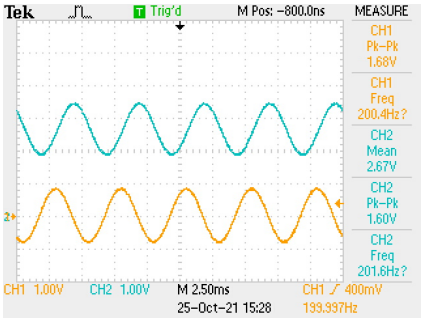
(a) 1Hz



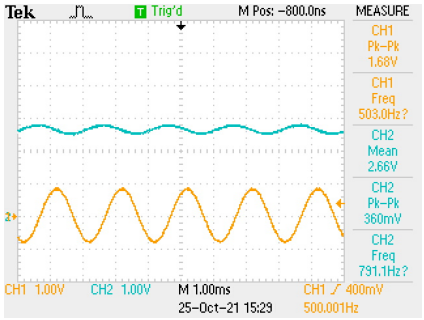
(b) 10Hz



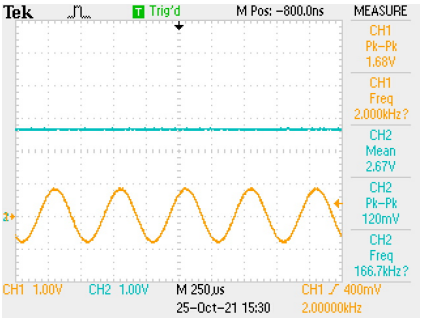
(c) 100Hz



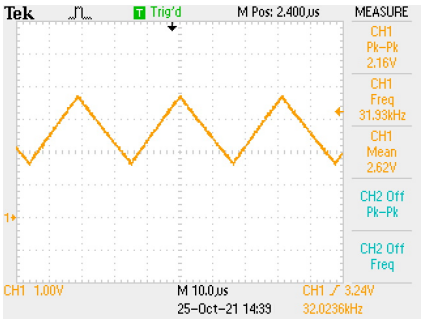
(d) 200Hz



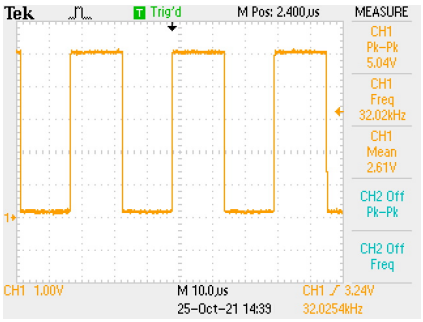
(e) 500Hz



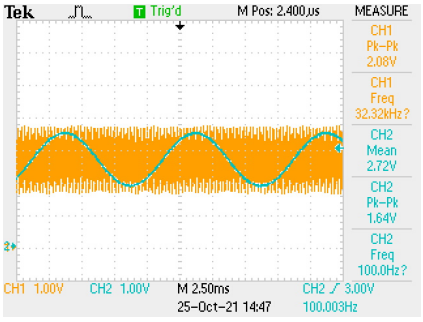
(f) 2kHz



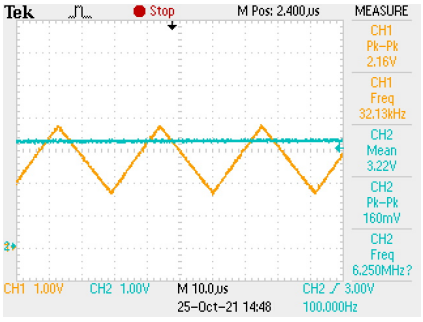
(a) Triangle Qave



(b) SPWM w/ 0V Input



(c) Input Signal Sampling Far



(d) Input Signal Sampling Near