ECEN 202 **Lab 3**

Design 1: A Quiz Night Timer

The design task

You are a keen participant at Quiz nights at your local pub. However, they need a timer to ensure that participants answer within a specified time and they approach you to design such a timer as they have heard that you are currently doing ECEN202. The timer should conform to the following design specifications:

1. It should keep time with 1 second resolution

2. Immediately after asking a question the quiz master should start the clock by pushing the "Start" button.

3. The clock should now count up (or down !) in 1 second increments while displaying this count on two 7-segment LED displays.

4. The contestants are allowed 12 seconds to answer a question – at the end of the 12 seconds the clock should stop and sound a 3 second buzzer.

Added functionality if time allows:

5. If a contestant is ready to answer a question before the 12 seconds are up they should press a button and the clock should stop and indicate this time. It should then also sound a 1 second buzzer.

Design approach

1. Design with a top down approach – i.e. what are the big block modules that are needed to make this design work. First identify each of these modules and only then decide how each of the modules will be constructed.

2. Nearly all the modules will have different options for construction. Have a good think about each of the possible options and then decide what will be easiest/most accurate/most efficient etc.

3. Construct your circuit bottom up, i.e. construct each of the modules independently and also try to test them independently. Ensure that each module is working by itself.

4. Now integrate all the modules to complete the timer.

5. You will soon have a lot of wires on your board. Use sensible, consistent colour codes for your wires to make it easier to construct.

6. Try to minimise the number of ICs used – easier to construct and debug !

7. Make detailed notes in your lab book to show your logic and your circuit diagrams.

Some hints and questions

1. One of the modules you will need to construct is a 1 Hz master clock pulse. However, do not start with this first. It is easier to cheat initially - just use the waveform generator on the design station. This will help you to get the actual counter going. You can then later come up with your own clock design.

2. An error of ±10% in the precision of the 1 Hz clock is acceptable. Do not spend too long trying to get this exactly right.

3. It looks like you will need at least a MOD 16 counter for your design. This is can be achieved with four JK flip-flop stages, but it may be much easier to use a dedicated counter IC (you have two different counters on your tray – see the list at the end of this document). You would also want the output of the timer to be in binary coded decimal rather than convention binary.

4. You will need to stop your counter before it reached the full MOD number as it only counts 0 – 12. How will you do this ?

5. Ideally you would want to display your count on the two 7-segment displays on the design station. Normal you will need a BCD to 7-segment decoder for this task. However, the 7-segment displays on the design station has this as a built-in function, so you can direct connect your decimal output of the counter to these displays. (You can also display your counter output on logic LED indicators - this might be useful in the early testing stages).

6. At the lack of a buzzer on the design station you should light up a selected logic indicator when the clock time runs out.

7. Think of any other timing and scheduling issues (such as resetting the clock between questions) that may possibly come up and how you might solve them !

Before the lab

Get together with your lab partner and decide on a basic design as based on the available ICs. Sketch a circuit diagram for the circuit you plan to construct. Bring this along to the lab and show to lab demonstrator.

Integrated circuits available for project

Device	Description	Number
74HCT00	Quad 2-input NAND gate	2
74HCT02	Quad 2-input NOR gate	2
74HCT03	Quad 2-input NAND gate; open-drain output	2
74HCT04	Hex inverter	2
74HCT08	Quad 2-input AND gate	2
74HCT14	Quad 2-input OR gate	2
74HCT32	Quad 2-input OR gate	2
74HCT73	Dual Negative-Edge-Triggered J-K Flip-Flops with Reset	2
74HCT74	Dual D-type flip-flop with set and reset; positive edge-trigger	2
74HCT86	Quad 2-input EXCLUSIVE-OR gate	2
74HCT112	Dual JK flip-flop with set and reset; negative-edge trigger	2
74HCT125	Quad buffer/line driver; 3-state	2
74HCT138	3-to-8 line decoder/demultiplexer; inverting	2
74HCT151	8-input multiplexer	2
74HCT153	Dual 4-input multiplexer	2
74HCT157	Quad 2-input multiplexer	2
74HCT374	Octal D-type flip-flop; positive edge-trigger; 3-state	2
74HCT390	Dual decade ripple counter	2
74HCT393	Dual 4-bit binary ripple counter	2
74HCT574	Octal D-type flip-flop; positive edge-trigger; 3-state	2
74HCT4511	BCD to 7-segment decoder	2
74HCT4538	Dual retriggerable precision monostable multivibrator	2
555	Timer, Monostable or Astable	2