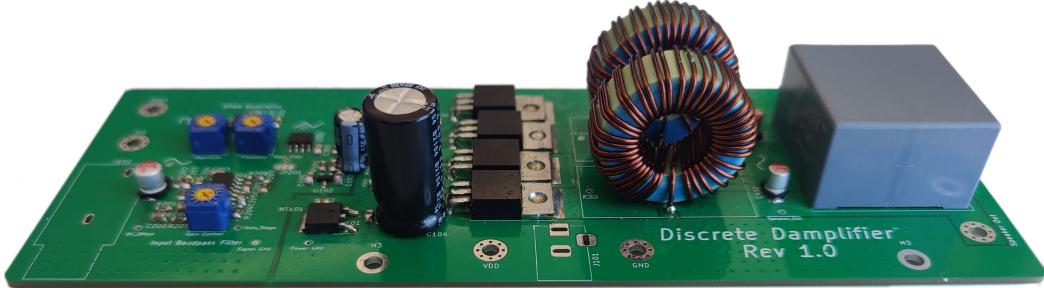


ECEN 405 - D Class Amplifier

"What a buck convertor would say if it could talk"

Daniel Eisen : 300447549
Team members: Niels Clayton & Nickolai Wolfe



1 Introduction

In the realm of audio amplifiers the D Class offers a method of supplying a high power loads with very high efficiency (especially when compared to other classes). Classes A, AB offer high power output with very low signal distortion but suffer greatly in the efficiency department due to continuous linear conduction times and resulting losses in their amplifying elements/transistors. D class amplifiers can achieve up to 90-95% power efficiency by taking advantage of a switching approach but require a more complex design process and circuit.

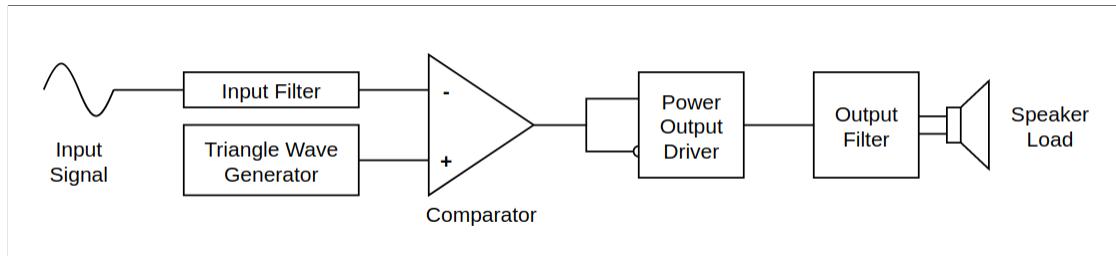


Figure 1: General Block Diagram of a D Class Amplifier

A D class design can be broken up into and explained with a series of blocks illustrated above in ???. An input signal is sampled with a triangular wave into a high frequency SPWM carrier signal that is then amplified to high power by switching a MOSFET bridge and the carrier frequency is removed with a low pass filter. As the switching elements are either ON or OFF the continuous conduction losses near eliminated*.

This report outlines and discusses the specifics in design, implementation and results of constructing a D-class amplifier project to the specifications outlined below in ???

Specifications

- $P_{out} = 80W$ for $R_L = 4\Omega$
- 10Hz to 200Hz Bandwidth
- Input sensitivity of 1V for maximum output (interpreted as 1V amplitude, 2V pk-pk)
- Maximum costs: \$50 per person

2 Design

A D-class amplifier operates on the signal sampling, switching amplification, and signal reconstruction as briefly described above. This can be practically realised . . .

Nick designed input stage that handles signal preconditioning and bandpass filtering

Niels designed Sampler and SPWM generation

I designed Power Driving Stage (Bridges) and Low Pass Output/Reconstruction filter

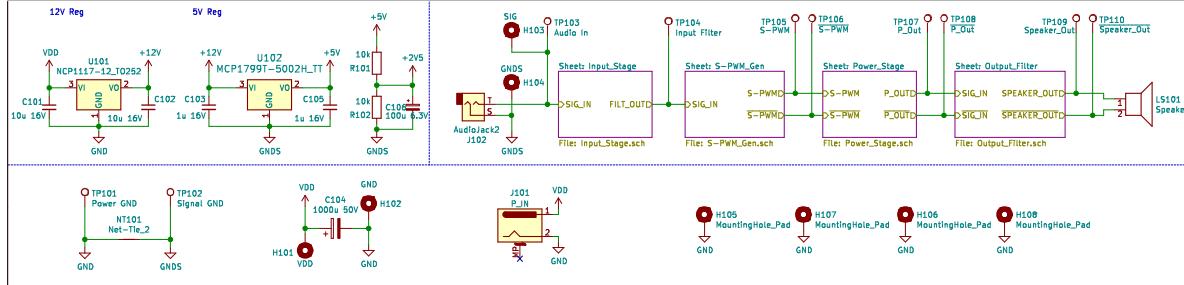


Figure 2: Top Level Design Schematic

2.1 Top Level Design Decisions

- Single main supply voltage regulated down to driver and logic supplied to produce a more cohesive final product

$$\begin{aligned}
 V_{DD} &= \sqrt{2 \cdot R_L \cdot P_{out}} \\
 &= 25.298V \\
 V_{DD} &= 26V(\min)
 \end{aligned}$$

2.2 Input Bandpass Filter

Active Bandpass filter with adjustable gain stage to pass 10Hz to 200Hz.

this is what was designed to do to meet these spec with this method, with these nice additions

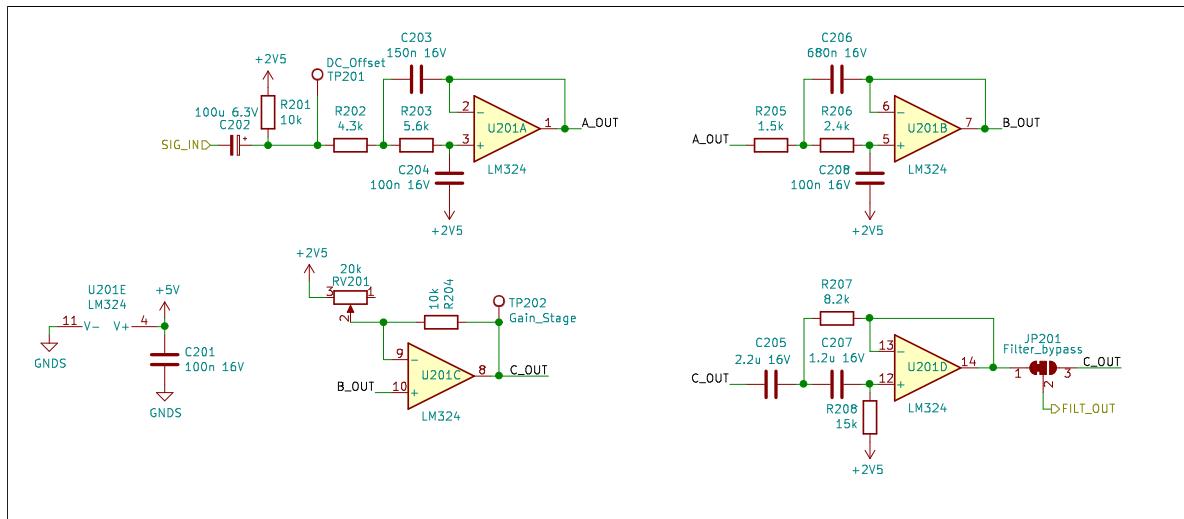


Figure 3: Input filtering schematic

2.3 Audio Sampling and SPWM

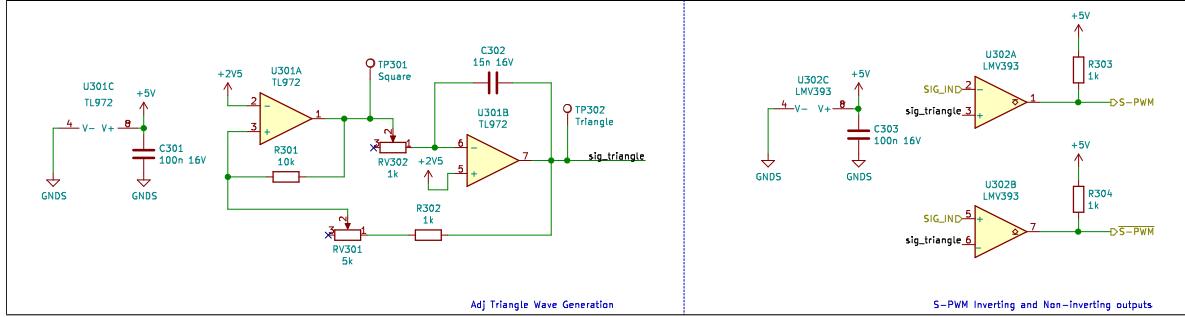


Figure 4: Sampling triangle wave & SPWM generation schematic

2.4 Power Stage and Output Filter

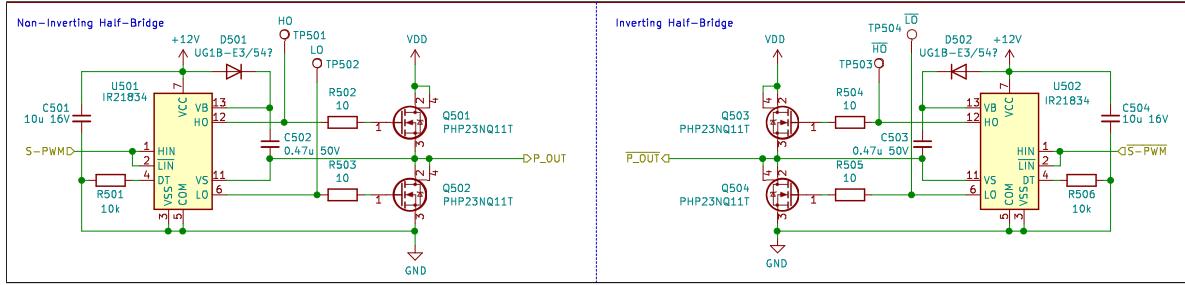


Figure 5: Gate driver schematic

Signal freq max of 200Hz, Switching frequency of 30kHz Place corner frequency of filter at 3kHz (decade centred) mes

<https://datasheets.maximintegrated.com/en/ds/MAX4295.pdf>

Figure 4c. Alternate Balanced 2-Pole Filter

Balanced 2-Pole (Figure 4b): A balanced 2-pole filter does not have the common-mode swing problem of the single-ended filter. $C = 2 / (2 \cdot RL \cdot \omega)$, $L = (2 \cdot RL) / (2 \cdot \omega)$; choosing $\omega_0 = 3\text{kHz}$ and $RL = 4\Omega$, $C_{1a} = C_{1b} = 1.87\text{F}$, $L_{1a} = L_{1b} = 150\text{H}$. A single capacitor connected across RL , with a value of $CL = 1 / (2 \cdot RL \cdot \omega)$, can be used in place of C_{1a} and C_{1b} . However, the configuration as shown gives an improved rejection to common-mode signal components of $OUT+$ and $OUT-$. If the single capacitor scheme is used, additional capacitors (C_a and C_b) can be added from frequency short to ground (Figure 4c). These capacitors should be approximately $0.2CL$.

3 Implementation

Here you should discuss the assembly of the amplifier and any problems you faced as a team building the amplifier. Here, the individual components should also be characterised. For example: if you have a filter, what is the response and how does it compare to the calculated? If you have a triangle wave, how does it look? Is it doing what I should? Why? Why not? How do the inputs/outputs of your comparator look? How does the square wave on the gate of the MOSFETs look?

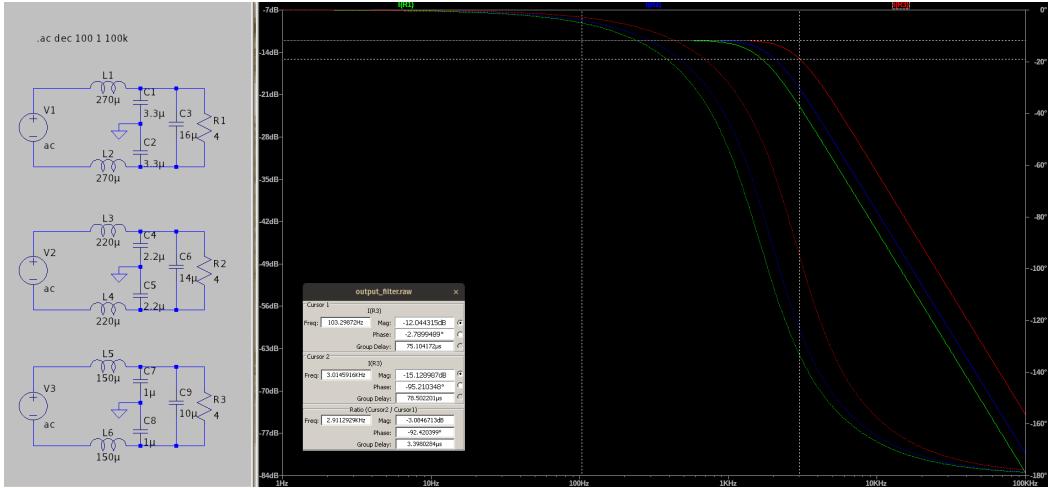


Figure 6: Output filter option simulations

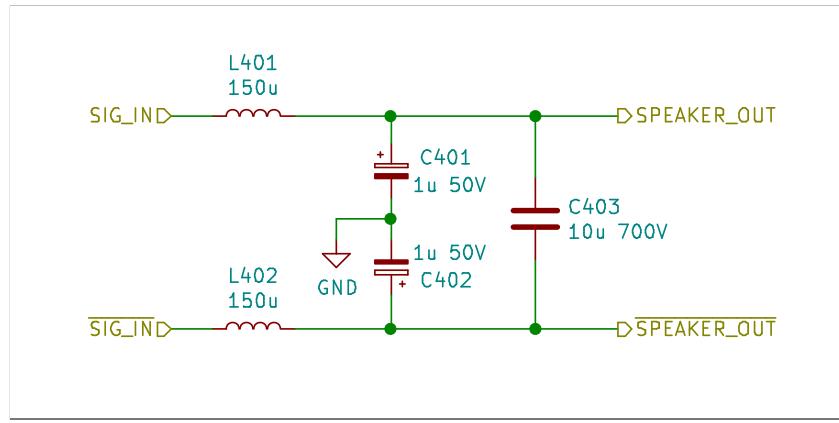


Figure 7: Final output filter schematic

3.1 PCB Layout

3.2 Gate Driving and Bridge Output

4 Results

Here I would expect to see the results of the whole amp, for example: an output wave, analysis of the efficiency, discuss maximum power output (which may be frequency dependent), and THD.

| Frequency (Hz) | THD (%) |
|----------------|---------|
| 30 | 1.8 |
| 50 | 2.2 |
| 100 | 3.2 |
| 200 | 3.3 |
| 300 | 3.5 |
| 500 | 3.2 |

Table 1: Output total harmonic distortion across frequency

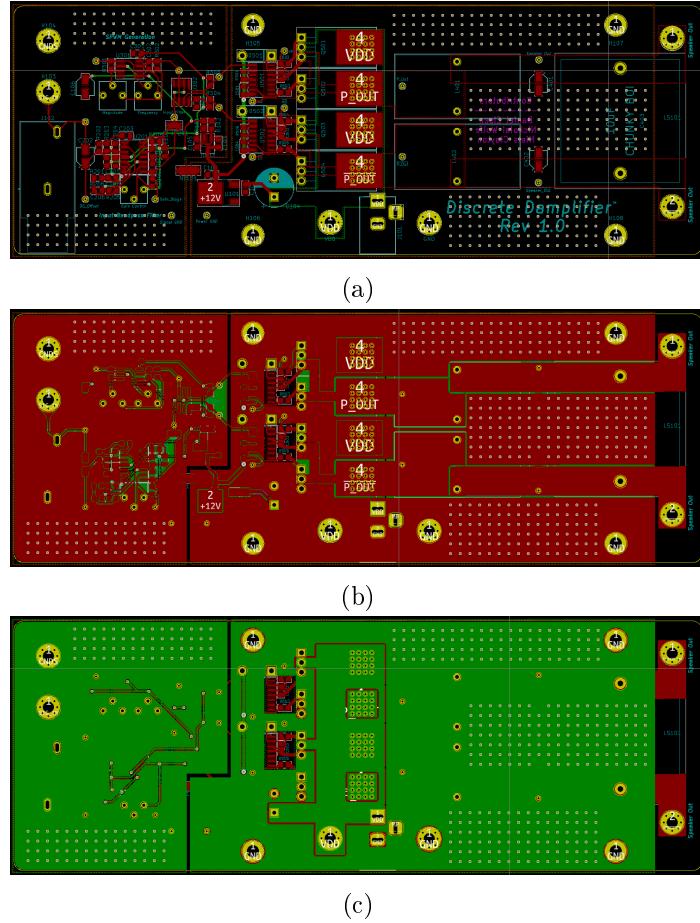


Figure 8

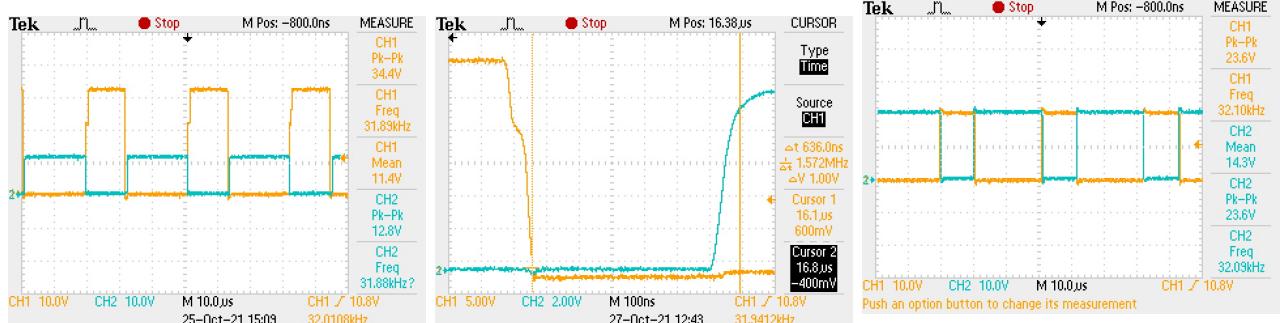


Figure 9

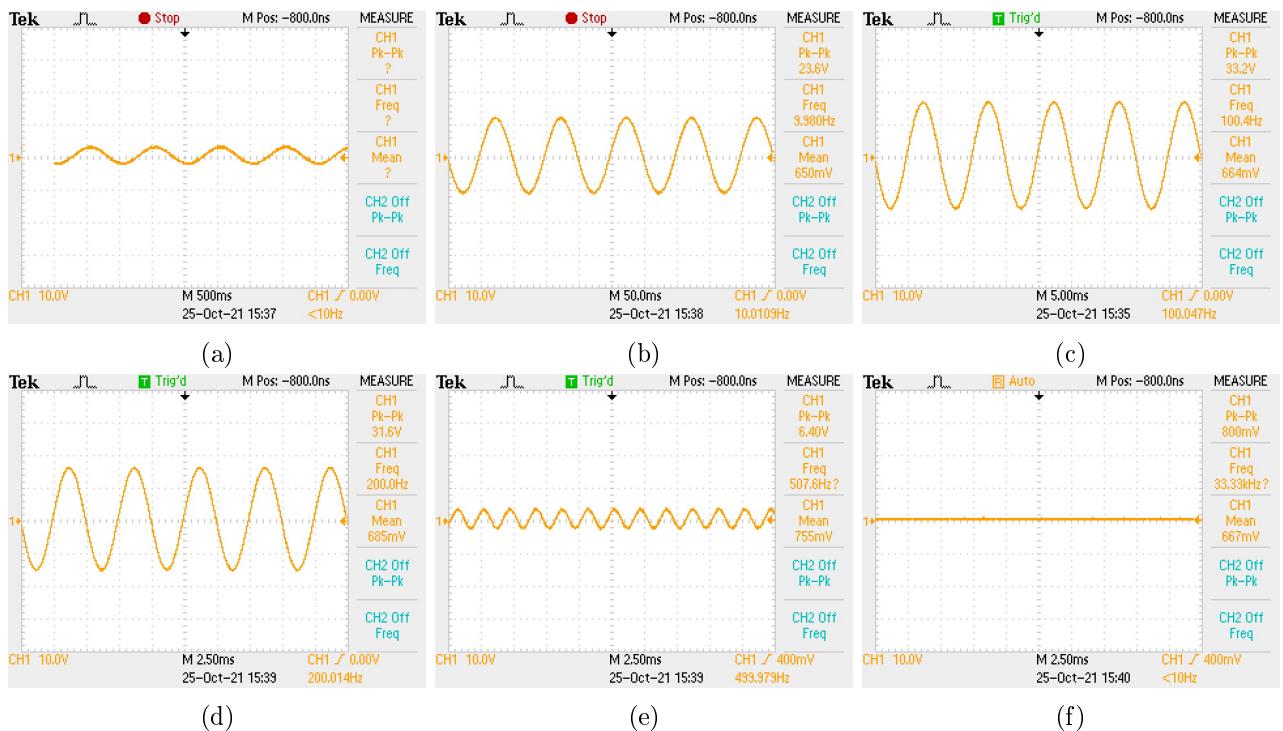


Figure 10

5 Conclusions

What worked, didn't work? How would you change your approach? Any interesting insights?

Per brd the price was kept to the 50 dollar per mark as per this BOM (https://niels-clayton.github.io/D-Class_Amplifier/)

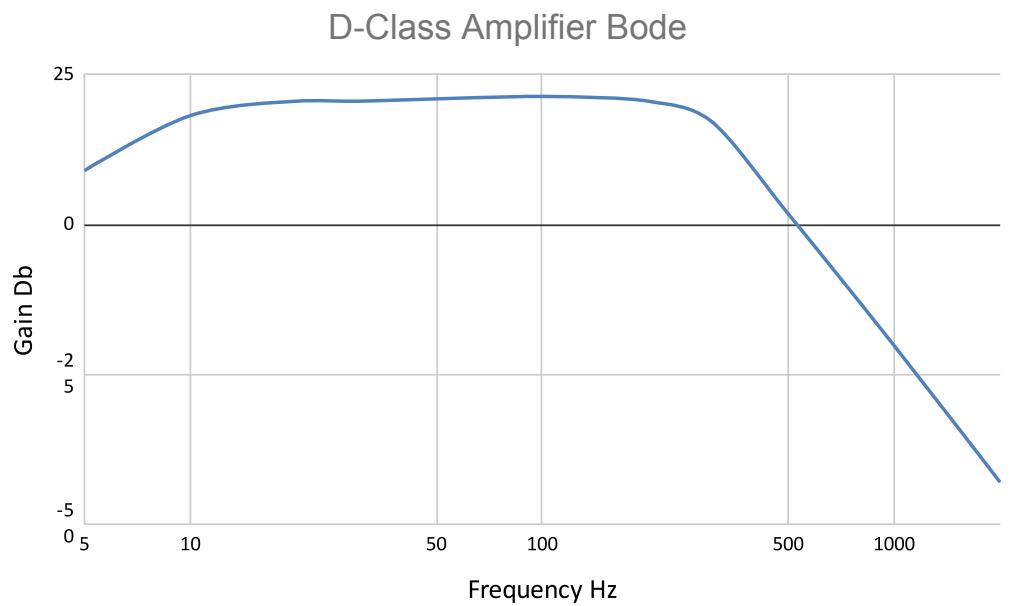


Figure 11

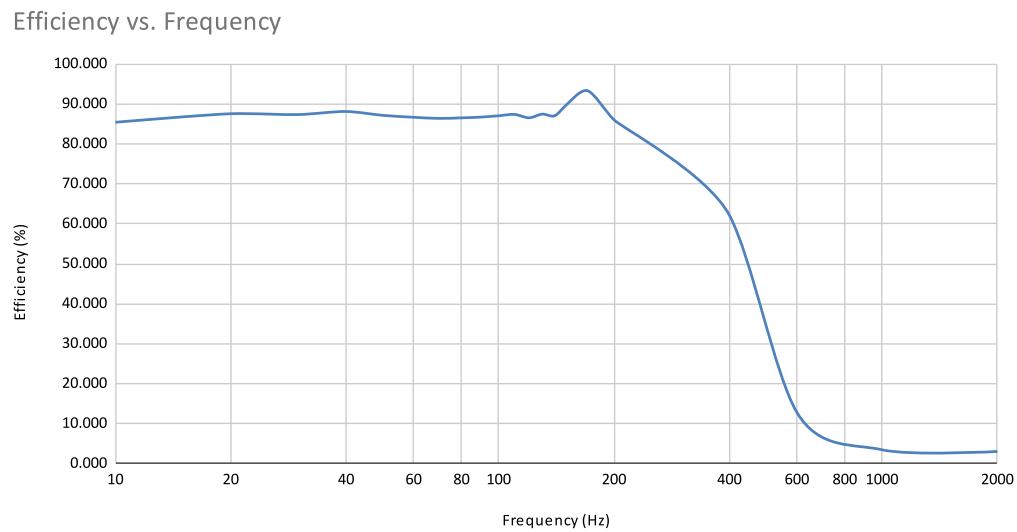


Figure 12

Appendix

Input Filter

Sampling/SPWM

