ECEN302 : Embedded Systems
Assignment 3 Submission

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1. ***You have been asked to design a circuit that can digitize a ±1 V audio signal, band limited to 16 kHz, to within a precision of 50uV. Discuss the key issues here in considering what ADC to use and then suggest a commercially available ADC.***

   For selection of a suitable ADC, the sample rate must be fast enough to enable the capture of the full bandwidth without aliasing, i.e. rated for at or above 16kMhz. It must have a enough output bits to meet the precision required for the given input range and given that is an audio application should not be too noisy. Note that the input signal can be amplified to match the full input range of the selected ADC to preserve precision.

   The AD677 is a 16 bit, 1Mhz, ±5V Sampling ADC.

2. ***Briefly describe the type of ADC typically used in a digital voltmeter or weigh scale. Describe how this type of convertor can reject 50 Hz mains interference.***

   This a Duel Slope ADC. Which operated by first integrating V_{in} for a constant time (T_{int}), after which $-V_{ref}$ [note that $|V_{ref}| > |V_{in}|$] is integrated until the output of the integrator reach's zero again. I.e. a variable slope for a set time against a set slope for a variable time (T2). As the second slope and first integration time are constant the input measured voltage is directly proportional to the second integration time. This is relative measure so eliminates affect of changing RC.

   As the average value of a sinusoidal signal is 0V, setting T_{int} such that in integer number of cycles occur in this time eliminates the interference as this is time where an external signal.

3. ***Briefly describe the operation of a sample and hold unit and suggest when such a device is required. Choose a suitable S&H for the application described in question 1 above, given that an ADC without a S&H was chosen***

   A Sample and Hold unit takes a snapshot of an instantaneous voltage signal and holds that voltage for as long as is required. This values can then be read in an ADC for example.

   The LF198/398 meets the input range requirement, low output noise and wide bandwidth.

4. ***What is the quantisation error of a 12 bit Analogue to Digital converter with an input voltage range of 0 to +1V.***

   $1V/2^{12} = 244.14\mu V \therefore$ quantisation error $\approx \pm 122\mu V$

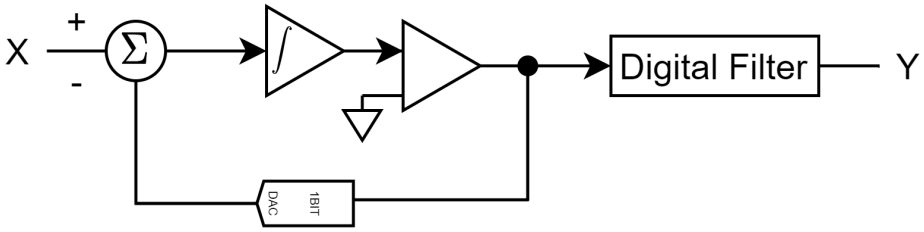
5. ***A 16-bit successive approximation ADC with an input voltage range of $\pm 5V$ is connected to a 16 MHz clock. This ADC is used to convert an input signal of 2.1362V. Determine the digital output and the time for the conversion.***

   Take 16 'guesses', one per clock cycle, therefore the conversion time is $1\mu S$.

   To get nearest output value, assuming 0b0... is -5V:

$$\frac{2.136 + 5}{\frac{10}{2^{16}}} \approx 46768$$

6. ***Sketch a block diagram of a Delta-Sigma ADC and then describe:***



   (a) *The signal that comes out of the comparator and how it relates to the input voltage.*
   The output of the comparator is a serial PWM signal whose proportion of high to low levels is representative of Vin (compared to the input range).

   (b) *How this comparator output signal is then converted into a multi-bit digital output.*
   This signal is then digitally filtered, by oversampling it considerably into a bitstream, taking a rolling average of the bitstream to extract a binary digital value.