ECEN 405
Lab 1 PWM Submission

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Deliverables

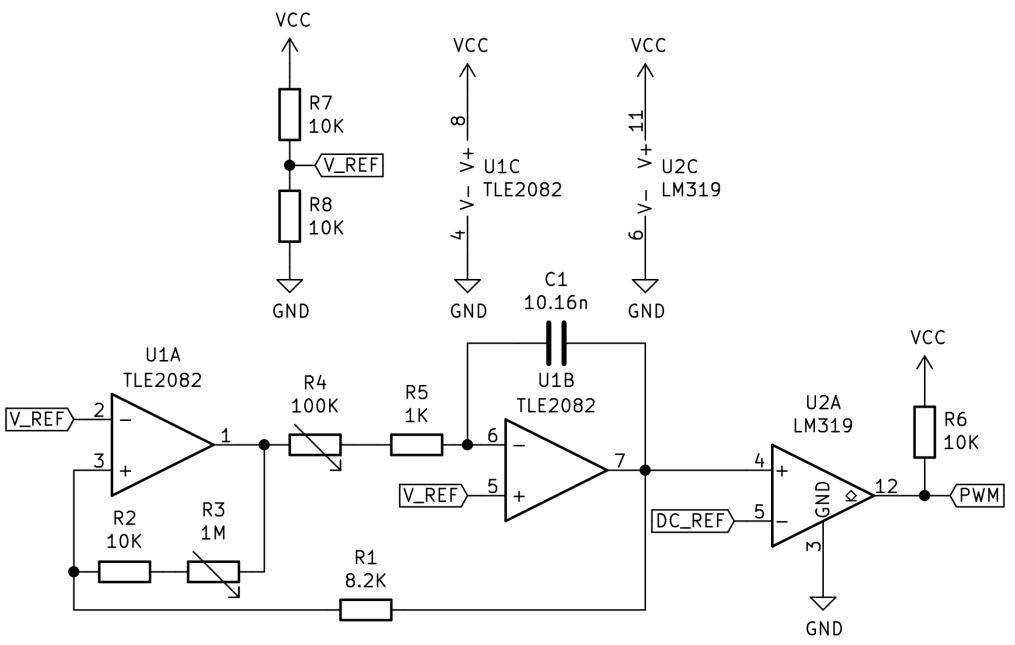
1. Capacitance:

$$\begin{aligned} C_1 &= \frac{10k}{4{\cdot}8.2k{\cdot}1k{\cdot}30kHz} \\ &= 1.016{\times}10^{-8} \\ C_1 &= 10.16nF \end{aligned}$$

2. Frequencies:
   $R_1 = 8.2k,\ R_2 = 10k,\ , R_5 = 1k, C_1 = 10.16nF$

$$F_t = \frac{(R_2 + R_3)}{4R_1(R_4 + R_5)C_1}$$
$$F_t\{R_3 = 1M,\ R_4 = 0\} = 3.03MHz$$
$$F_t\{R_3 = 0,\ R_4 = 100k\} = 297.1Hz$$
$$\text{to match lab value : } F_t\{R_3 = 0,\ R_4 = 1M\} = 29.97Hz$$

3. Schematic:



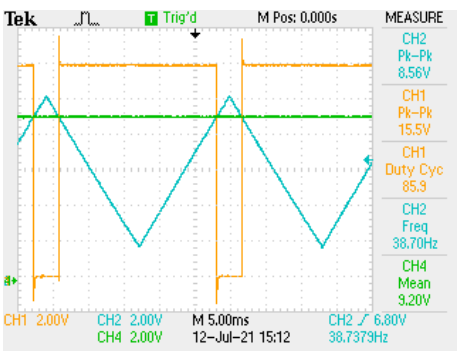
4. IRFBC40APBF: $R_{DS(on)} = 1.2,\ t_{c,on} = 13,\ t_{c,off} = 31$

$$\begin{aligned} \text{Conduction losses} = P_{cond} &= R_{DS(on)}dI^2 \\ &= 1.2{\cdot}0.5{\cdot}1 \\ &= 0.6W \end{aligned}$$
$$\begin{aligned} \text{Switchinglosses} = P_{sw} &= \frac{1}{2}V_{in}I_o \\ @29.97Hz &= 7.91\mu W \\ @297.1Hz &= 78.4\mu W \\ @3.03MHz &= 0.799W \end{aligned}$$

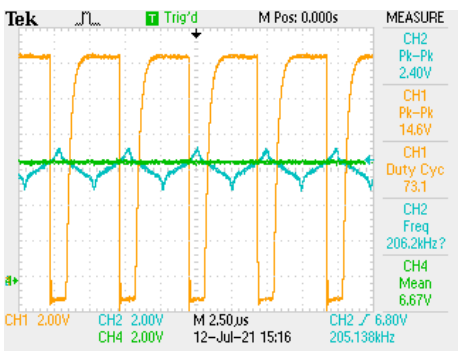
5. Build it:

Danny B's approval of breadboarded circuit

6. Test it:



Lowest Frequency

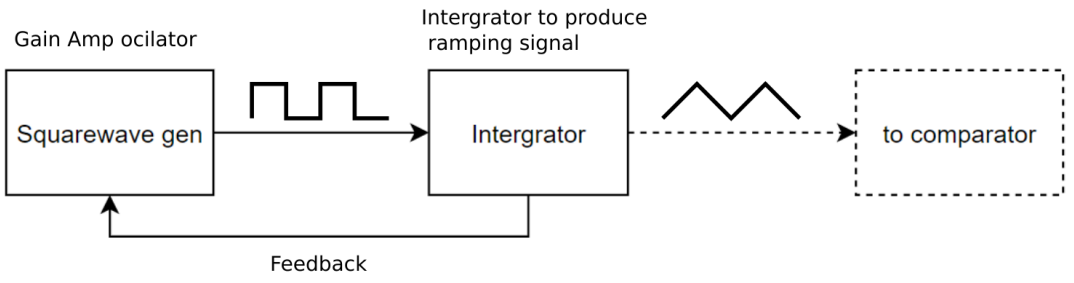


Highest Frequency

7. This circuit is constructed in the real world on a breadboard. So it differs from ideal with parasitic capacitance, imperfect slew rates from the op-amps and comparators and possibly other non-ideal factors. Due to this the upper theoretical frequency (3Mhz) was could not be achieved, with only a recorded max of 200kHz.

8. The LM319 is a duel comparator chip, so to add an inverted output to the circuit the input just need to be switched and fed into the second comparator pins and its out also pulled up.

9. This circuit consists of two main subcircuits.



Sub-circuits: Gain Amp Oscillator and Integrator:
