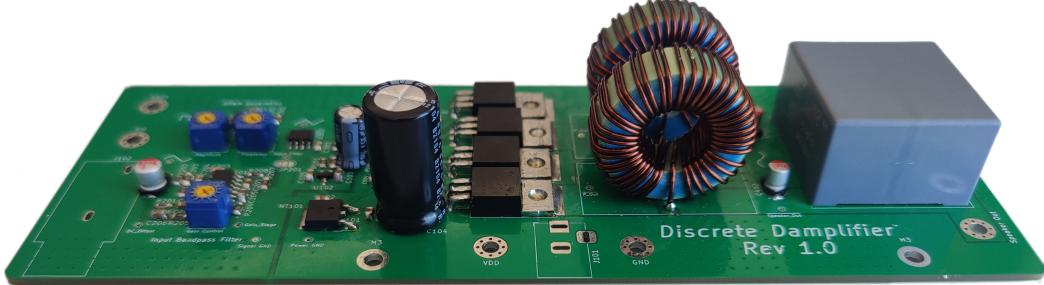


ECEN 405 - D Class Amplifier

"What a buck convertor would say if it could talk"

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1 Introduction

In the realm of audio amplifiers the D Class offers a method of supplying a high power loads with very high efficiency (especially when compared to other classes). Classes A, AB offer high power output with very low signal distortion but suffer greatly in the efficiency department due to continuous linear conduction times and resulting losses in their amplifying elements/transistors. D class amplifiers can achieve up to 90-95% power efficiency by taking advantage of a switching approach but require a more complex design process and circuit.

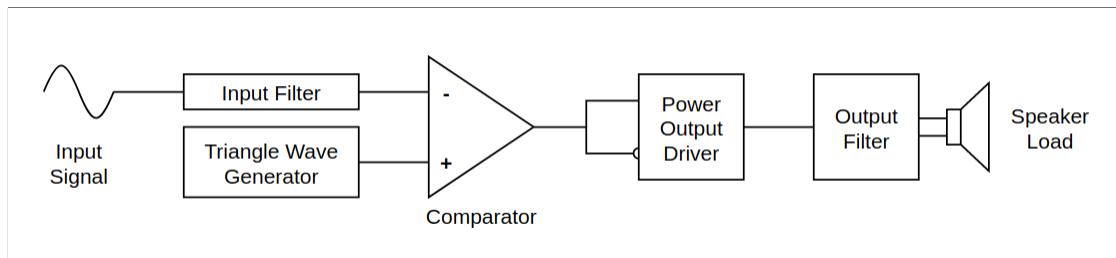


Figure 1: General Block Diagram of a D Class Amplifier

A D class design can be broken up and explained with a series of blocks illustrated above in fig. 1. An input signal is sampled with a triangular wave into a high frequency SPWM carrier signal that is then amplified to high power by switching a MOSFET bridge and the carrier frequency is removed with a low pass filter. As the switching elements are either ON or OFF the continuous conduction losses are eliminated*.

This report outlines and discusses the specifics in design, implementation and results of constructing a D-class amplifier project to the specifications outlined below in section 1.

Specifications

- $P_{out} = 80W$ for $R_L = 4\Omega$
- 10Hz to 200Hz Bandwidth
- Input sensitivity of 1V for maximum output (interpreted as 1V amplitude, 2V pk-pk)
- Maximum costs: \$50 per person

2 Design

A D-class amplifier operates on the signal sampling, switching amplification, and signal reconstruction as briefly described above. This project practically realised this approach with the high level design shown in fig. 2.

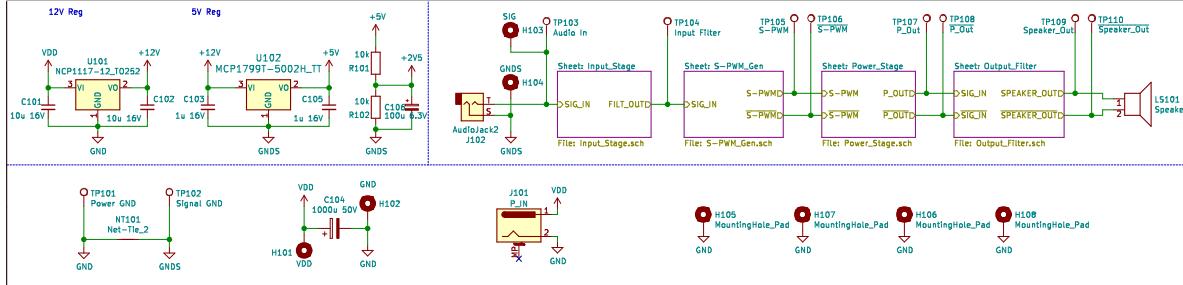


Figure 2: Top Level Design Schematic

As the intended load is a sub-woofer and there is a required bandwidth, the input audio signal must undergo some filtering and other preconditioning. This is handled by the input stage and was designed by Nickolai Wolfe. This stage band-passes the audio to meet the frequency range requirement, and otherwise adjusts gain and reference levels to make it suitable for the sampling stage.

The Sampler or Sinusoidal pulse width modulation (SPWM) generation stage was designed by Niels Clayton and encodes the audio signal into a high frequency carrier PWM signal. This signal is output (non-inverted and inverted for positive and negative output channel) at the correct voltage level for the driving circuitry as the switching control signal to the Power Amplifying Stage.

The last stage(s) of the D-Class is the Amplifying Bridges and reconstruction (Low pass) filters and their design was handled by myself. This project utilised two independent MOSFET bridges to amplify both SPWM signals and the reconstruction filter then strips out the high frequency carrier PWM to output the desired audio signal to the load.

2.1 Top Level Design Decisions

Topology

First is a topology choice. D-class amplifiers come in two main "flavours", Full and Half Bridge. Full Bridge amplifiers dedicate a whole bridge (1 driver, 2 MOSFETs) for each of a channels output rails. A Half bridge on the other hand has a single bridge that drives both the positive and negative sides of the output signal.

As the half bridge does not have independent bridges it will therefore require double the supply voltage (and is usually dual rail) to achieve the same output power. Its configuration also resulting in the commutation current being pumped back through the power supply, resulting in fluctuation and often the need for implementation a closed loop feedback system to maintain output stability.

For the above drawbacks of the half-bridge as well as the fact that we are producing a mono output channel we decided to use an open loop full bridge topology to make breaking up the design simpler, maintain a single supply rail and sacrifice the required component duplication as a compromise.

Power Supply

Now that the project confirmed as Full Bridge, to meet the required output power to the 4 Ohm load the required VDD needs to be set.

$$\begin{aligned} V_{DD} &= \sqrt{2 \cdot R_L \cdot P_{out}} = 25.298V \\ &= 26V(\min) \end{aligned}$$

Another addition that was made as an extension to the scope the inclusion of 2 linear regulators to power the drivers and logic circuitry such that this project would produce a more cohesive final product. These are included in fig. 2.

2.2 Input Bandpass Filter

Nickolai designed the input stage that consists of 4th order Butterworth active low pass and a 2nd order active high pass filter with corner frequencies at 10Hz and 300Hz to meet the bandwidth specification in section 1 with no attenuation at 200Hz. This stage additional imposes the signal on a mid-rail reference voltage of 2.5V to enable the entire logic side of this project to utilise a single ended 5V supply and also utilised a spare op-amp (from single quad package) as an adjustable gain stage for fine control and tuning.

All this is shown in fig. 3 as the final design.

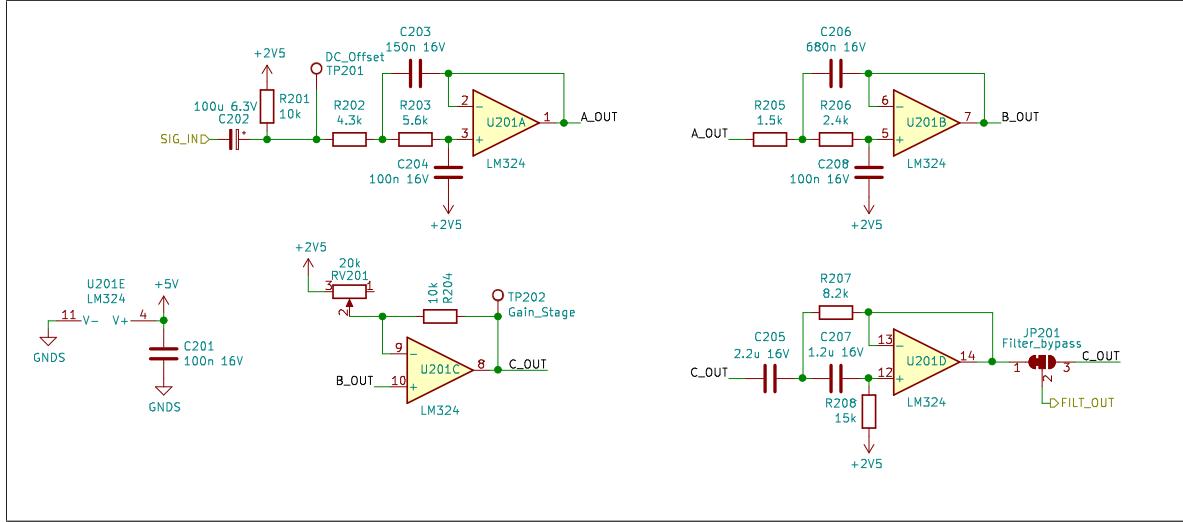


Figure 3: Input filtering schematic

2.3 Audio Sampling and SPWM

Niels designed the circuitry required to generate the high frequency triangle wave required to sample the processed input audio with the duel comparators to produced an inverted and non-inverted Sinusoidal Pulse-width-modulated signal at the required 5V level for controlling the gate drivers.

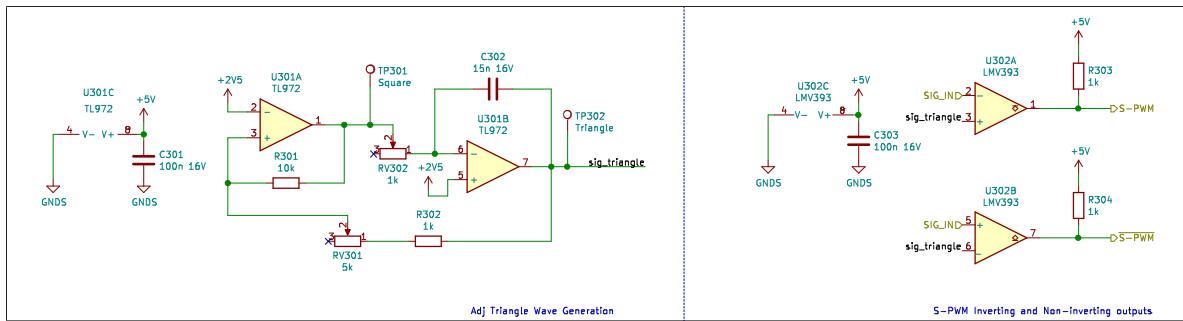


Figure 4: Sampling triangle wave & SPWM generation schematic

It basically operates by comparing the current signal level to the triangle wave and encoding that in the width of the SPWM. This circuit also integrates both adjustable triangle wave frequency and scale to tune the switching speed and signal enveloping for best performance.

2.4 Power Stage and Output Filter

These sections are required to amplify the generated 5V SPWM from the sampler filter out the carrier frequency to reproduce the audio signal.

They consist of two symmetric MOSFET bridges (non-inverted and inverted SPWM amplifiers) that forming the full bridge topology and a low pass reconstruction filter to decode the audio signal. Each of these require following a design procedure to meets specification and the optimisation of component choice to minimise losses, maintain signal integrity and add protection.

Power Amplifying Bridge

In order the successfully amplify the SPWM encoded audio the MOSFET bridges must be switched quickly and efficiently, minimising conduction losses and retaining signal clarity. The design of such an effective amplifying bridge relies on three main aspects:

- Correct MOSFET Selection
- Gate Drivers for fast gate charging
- Bootstrapping and switching dead time

The finalised design of both bridges is shown here in fig. 5 accepting the 5V SPWM signals and outputting the POUT amplified signal for filtering.

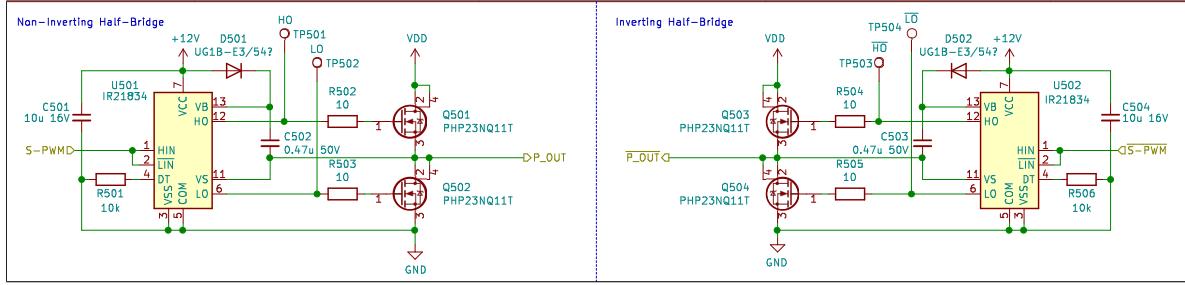


Figure 5: Gate driver schematic

Before component selection can occur the FET voltage rating must be calculated:

$$BV_{dss} = \frac{\sqrt{2 \cdot P_{out} \cdot R_L}}{0.85} \cdot 1.5 = 44.6V \quad (1)$$

The selected FETs for the project are the PHP23NQ11T. These were selected for their combination of very low $R_{ds(on)}$ of $49m\Omega$ and very low gate charge of $10nC$. These factors work to minimise gate charge time as well as reduce the on state conduction power loss. They exceed the voltage rating at 110V and have an ambient power dissipation of 100W so will be comfortably operating at maximum quarter power.

The IR21834PBF in SMD packaging were selected as the gate driving ICs as they integrate a large all the necessary features for proper bridge control. Each is a dedicated half-bridge driver designed of the required bootstrap operation to properly reference the high-side MOSFET to allow for successful switching. It can supply the gate outputs with up to 1.8A of charge current for nominal gate ON/OFF times of 40ns and 20ns. It is also 5V input to be compatible with the SPWM generation stage and features a matched preparation delay between each channel to prevent phase drift/offset and inter-channel interference in the filter stage.

Most importantly these drivers support a programmable dead time to prevent VDD to GND shoot through across the FETs and allows for tuning the project overall THD by changing the control resistance, nominally set to 10K for a 63nS dt.

Reconstruction Filter

This D-class is designed around a minimum switching/carrier frequency of 30kHz therefore a filter is required on the bridges output to attenuate this and restore the audio signal for output and driving the sub-woofer. Even though the carrier frequency is outside the audible range and the sub-woofer could not accurately reproduce it, leaving it unfiltered could degrade the efficiency and well as cause EMI issues.

As audio signal integrity is a priority the chosen topology is a low-pass Butterworth filter to maintain a flat gain in the passband and good phase response. Specifically the configuration chosen is the Alternate Balanced 2-Pole Filter shown in fig. 6. This utilises dual matched inductors (L) to eliminate common-mode swing, a single full rail unpolarised capacitor (C_L) for improved rejection and two addition balancing capacitors ($C_{a,b}$) that provide a HF ground shorts.

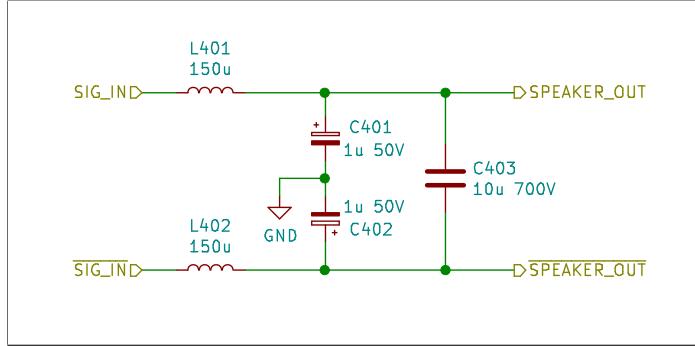


Figure 6: Alternate Balanced 2-Pole LPF

The calculation of these values are all derived from the load (R_L) and selected cutoff frequency. This was placed one decade before the minimum switching frequency of 30kHz to ensure a -40dB attenuation.

$$f_0 = 3 \text{ kHz}, \omega_0 = 18850 \text{ rad.s}^{-1} \quad (2)$$

$$C_L = \frac{1}{R_L w_o \sqrt{2}} = 9.38 \mu F \quad (3)$$

$$C_{a,b} = 0.2 C_L = 1.88 \mu F \quad (4)$$

$$L = \frac{R_L \sqrt{2}}{2 w_o} = 150 \mu H \quad (5)$$

These exact values are obviously not directly available for purchase and obtaining the inductors is the main limiting factor. Therefore the above values were used as the starting off point in component selection, and the recalculated values to match the available inductors were simulated to ensure functionality was retained.

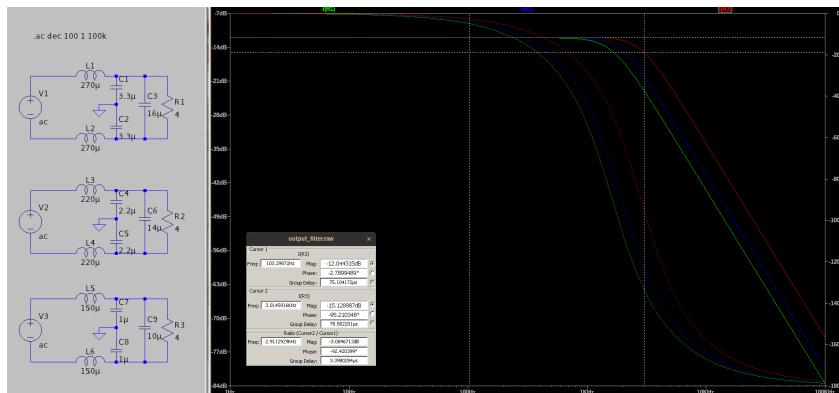


Figure 7: Output filter option simulations

In fig. 7 you can see the 3 real world attainable circuits (based of real component values in stock) simulated. These all still match in topology performance and all have a corner frequency (-3dB) of under 3kHz thus retaining the intended attenuation. All these values were found in the same or very similar product series. The inductors were sourced as high current (5A), shielded core signal transformers to ensure a constant inductance across the expected output current, the main capacitor was a unpolarised film capacitor for signal quality, tight tolerances and closer to ideal characteristics.

From these the final values were selected to help meet the price specification.

3 Implementation

3.1 PCB Layout

With each of the amplifiers stages fully designed and top-level connective schematic complete, the next step is to implement it by laying out an integrated PCB. This can be seen in fig. 8 showing the full layout the projects deliverable.

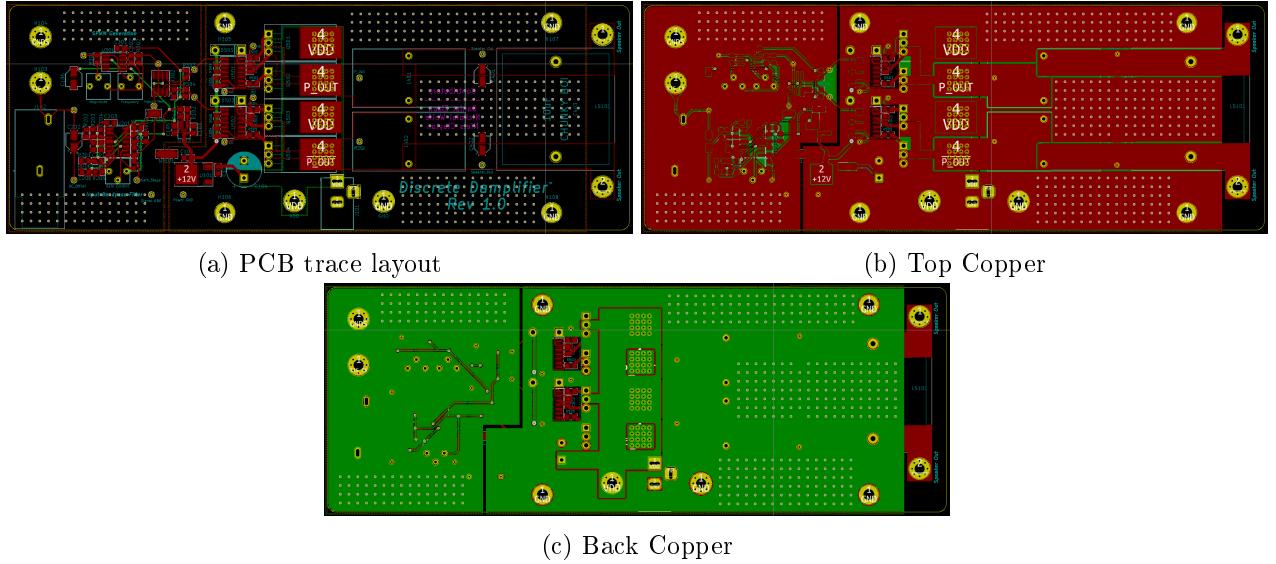


Figure 8: Final Full PCB

By design this project includes a mix of sensitive signal processing at the input, and high power, high frequency switching at the output. This represents and important requirement to isolation of grounds and management of current return paths.

This is primarily achieved by completely separating the Power and Signal ground planes on both sides and providing a single return path for signal currents to via a net-tie from signal to power ground. This completely prevents any high currents from the amplification bridges from returning around/under the sensitive op amps. Figure 8 b&c's copper pour shows this isolation and return path.

Adjacent to this approach, this project heavily utilised copper pour zones and heavy via stitching to ensure constant ground references and very low impedance current paths for the high power output. To match these custom zones we also made custom FET footprints that allows us to dissipate excess heat into the board.

Finally we defined explicit pour keepout zones under the output terminals to prevent connectors shorting to the ground plane and under the output half both gate drivers to prevent noise coupling into the gate input signals.

3.2 Gate Driving and Bridge Output

The bridge driving sections functionality was confirmed by examining the generated gate signals, dead-time and the resulting amplified signals. In ?? you can observe the high side gate signal (a) being correctly bootstrapped

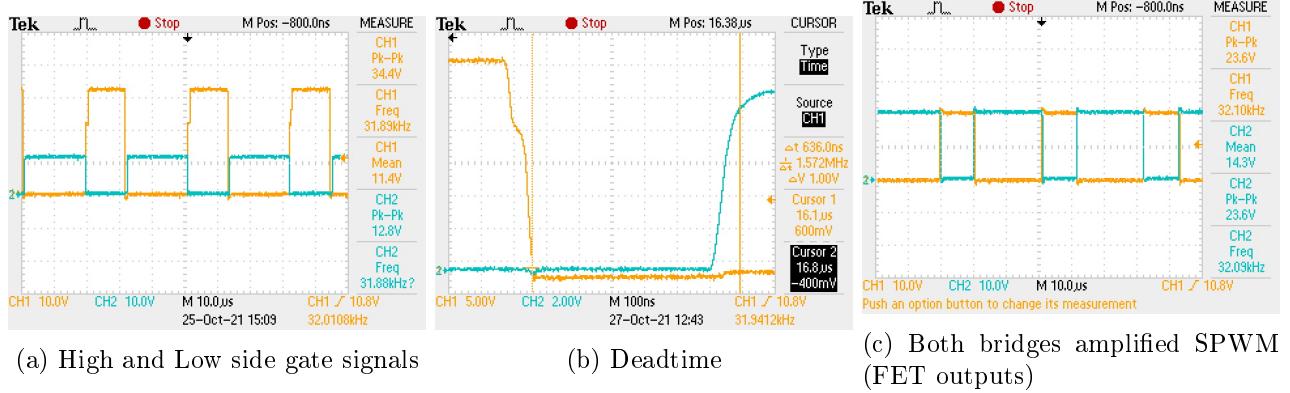


Figure 9

up and the Miller charge plateau can even be seen, the deadtime (b) is also successfully being set at 63ns as outlined in section 2.4, and successfully results in a non-inverted and inverted amplified SPWM (c).

3.3 Reconstruction Filter

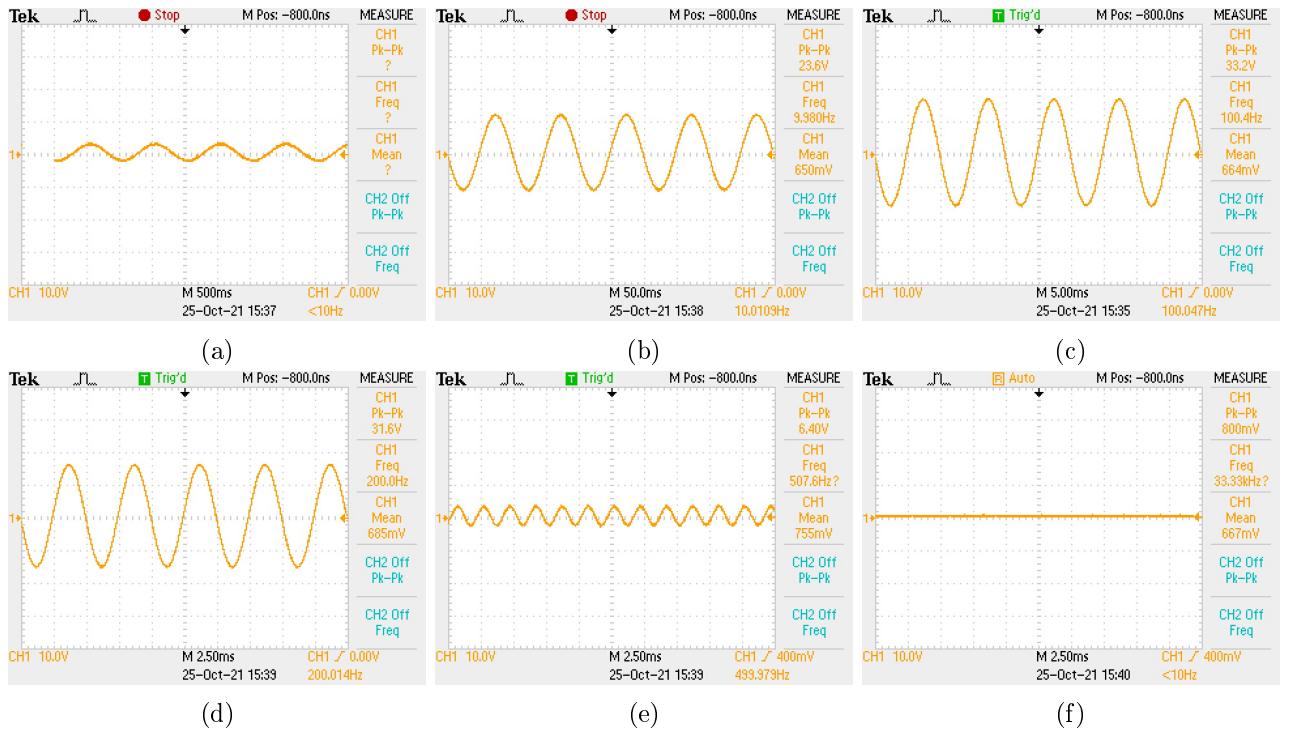


Figure 10: Output from Reconstruction filter at various frequencies

To show the reconstruction filter successfully removed the carrier frequency and retain the correct bandwidth attenuation to meet the specification in section 1 the input signal was varied from 10Hz to 2kHz and the results are very successfully shown in fig. 10.

Extra

The only changes made in testing was the addition of an $100\mu F$ smoothing capacitor on the mid-rail voltage reference for the input signal processing to prevent oscillations.

4 Results

To finalise and summarise the overall performance of this Class D amplifier a series of frequency sweeps were undertaken and the measurements relevant to section 1 were taken.

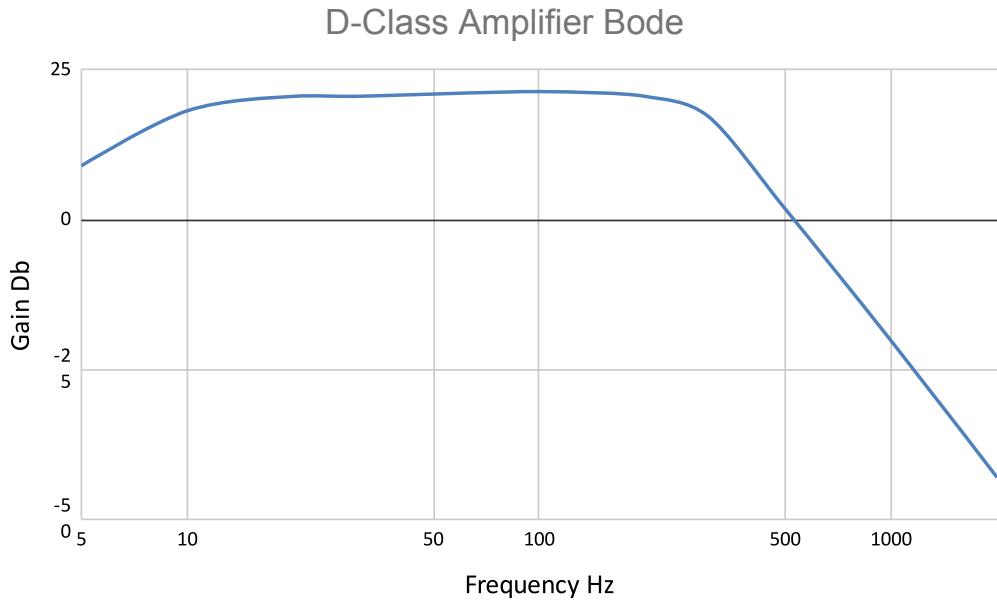


Figure 11

By taking an FFT of the output signal (loaded) the Bode plot fig. 11 shows a flat passband matching the 10Hz to 200Hz specification.

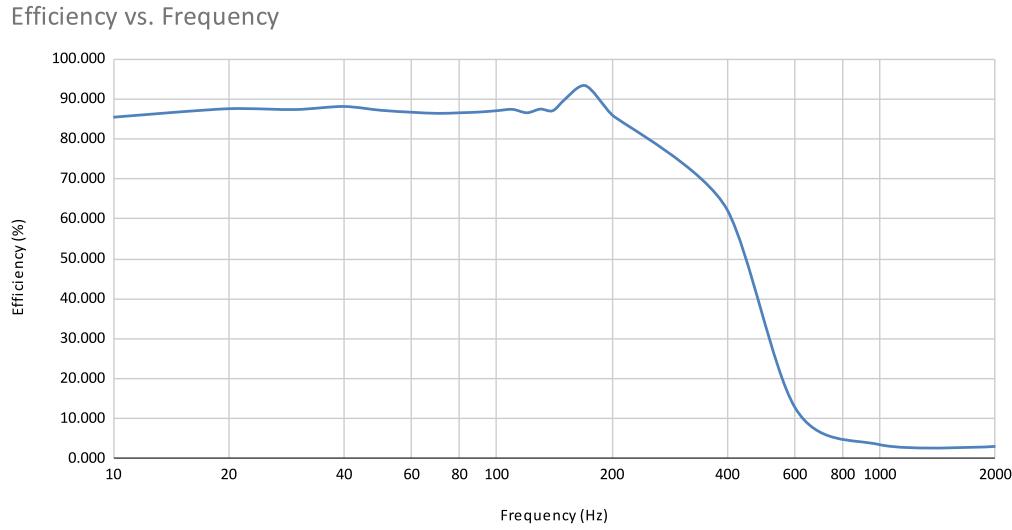


Figure 12

fig. 12 shows that by utilising the D class approach to power amplification, a very high efficiency could be achieved across the operating range. Sustaining 85% to 95%.

This %THD was also measured across the measurable range (table 1) of the meter and shows what was approximately expected for a deadtime of 63ns. It could be possible to reduce this to sub %1 by dropping down to 40ns but this was not explored.

Frequency (Hz)	THD (%)
30	1.8
50	2.2
100	3.2
200	3.3
300	3.5
500	3.2

Table 1: Output total harmonic distortion across frequency

5 Conclusions

In conclusion our segmented and thorough approach to design and careful layout consideration resulted in this project very successfully producing a D-Class amplifier to the given specifications in section 1. We were also able to maintain the \$50 per board cost and order and construct 3 working devices, outlined in this [Interactive BOM](#).

The feeling of which can be accurately summarised by fig. 13.

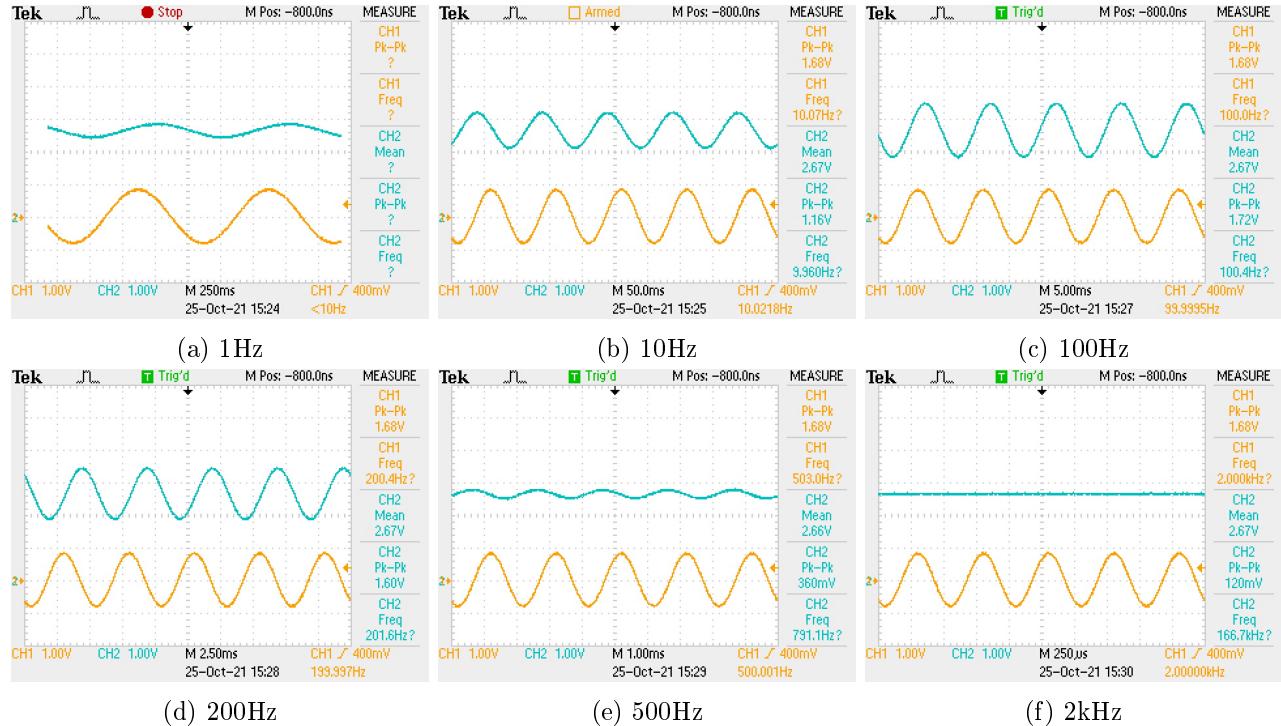


Figure 13

Appendix

Implementation results of other team members stages.

Input Filter



Sampling/SPWM

