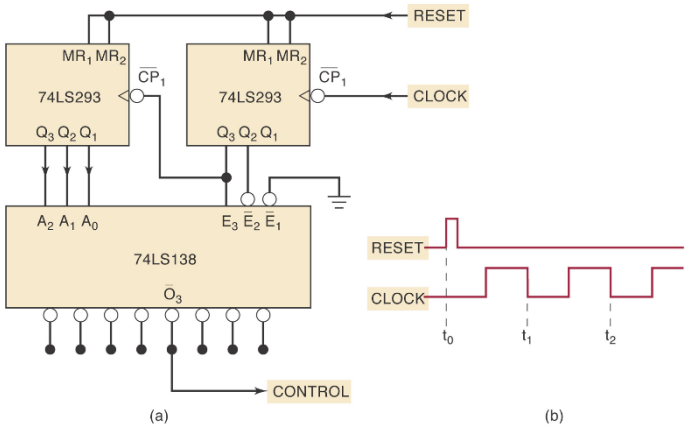
ECEN202 **Assignment 3**

Due Monday 29 April 2019

1. Use J-K flip flops to design a synchronous counter that will go through the following sequence: 000, 010, 101, 110 and repeat. The undesired (unused) states must always go to 000 on the next clock pulse.

2. Redesign the counter of (Q1) without any requirement on the unused states, so that their next state can be a don't care state. Compare to the previous counter design.

3. Look at the circuit below, identify each of the ICs used and explain the operation of the circuit. Now modify the circuit so that it will produce a control signal that will remain LO from CLK t_{20} to t_{24}.



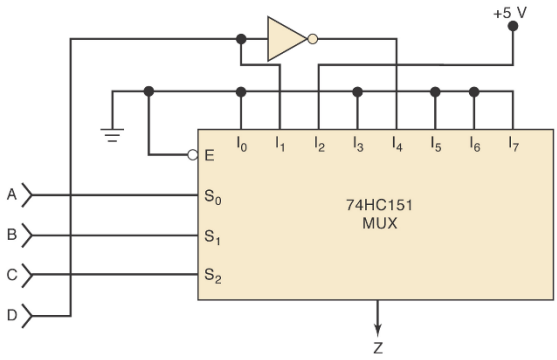
4. The circuit below shows how an eight input MUX can be used to generate a four variable logic function, even though the MUX has only three inputs.

(a) Check that you understand the operation of the circuit and then draw up a truth table showing the O/P Z for the 16 possible I/P combinations.

(b) Set up a truth table showing the output Z for all the input combinations.

(c) Write and the sum of products expression for Z and simplify to show that:

$$Z = \overline{C}.B\overline{A} + D.\overline{C}.\overline{B}.A + \overline{D}.C.\overline{B}.\overline{A}$$



5. In class we looked at the structure of a CMOS NAND gate. Now sketch a similar structure for a CMOS NOR gate and use a truth table to show which of the transistors will be ON or OFF for each of the input states and that it will yield the required NOR gate logic.