ECEN303 : Test 2
Circuits, Op amp limitations, Noise, Stability, Oscillators

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Question 1

a) c)

b) c)

c) d)

d) c)

e) a)

f) a)

g) b)

h) a)

i) d)

j) c)

k) c)

l) a)

Question 2

Assume $T = 25°C$, $298.15K$:

i) $e_n = \sqrt{4KTR}$
$e_{R1} = e_{RP} = 4.057nV/\sqrt{Hz}$
$e_{R2} = 27.81nV/\sqrt{Hz}$

ii) $v_n = 15nV/\sqrt{Hz}$, $i_n = 7pA/\sqrt{Hz}$, $A_+ = 48$, $A_- = 47$

$R_{PN} = e_{RP} \cdot A_+ = 194.47nV/\sqrt{Hz}$
$R_{1N} = e_{R1} \cdot A_- = 190.67nV/\sqrt{Hz}$
$R_{2N} = e_{R2} = 27.81nV/\sqrt{Hz}$
$O_n = v_n \cdot A_+ = 720nV/\sqrt{Hz}$
$i_+ = i_n \cdot R_1 \cdot A_+ = 336nV/\sqrt{Hz}$
$i_- = i_n \cdot R_2 = 329nV/\sqrt{Hz}$

Total $= \sqrt{R_{PN}^2 + R_{1N}^2 + R_{2N}^2 + O_n^2 + i_+^2 + i_-^2} = 902.54nV/\sqrt{Hz}$

iii) $B = 999.95$
$V_{out}\ Noise = Total \cdot B = 902.5\mu V$

Question 3

i) To deal with I_B we set $R_P + R_A = R_1//R_2 = 957\Omega$
To stick with standard resistor values, $R_P = 910\Omega$, $R_A = 47\Omega$
Input voltage offset max: $3 + (957 * 0.00003) = 3.02871$ but allow for $\pm 4mV$ of control.
$\frac{V_x}{V_y} = \frac{R_A}{R_A + R_B} = \frac{4mV}{15V} \therefore R_B = \frac{47}{\frac{4 \cdot 10^{-3}}{15}} - 47176.2K \approx 170K$ for more control.
$R_c << R_B$ thus 10K

ii) The process in time consuming and expensive, difficult to automate, the offset drift of an op amp with temperature will vary with the setting of its offset adjustment.

iii) Can use a programmable DAC for external trimming.

Question 4

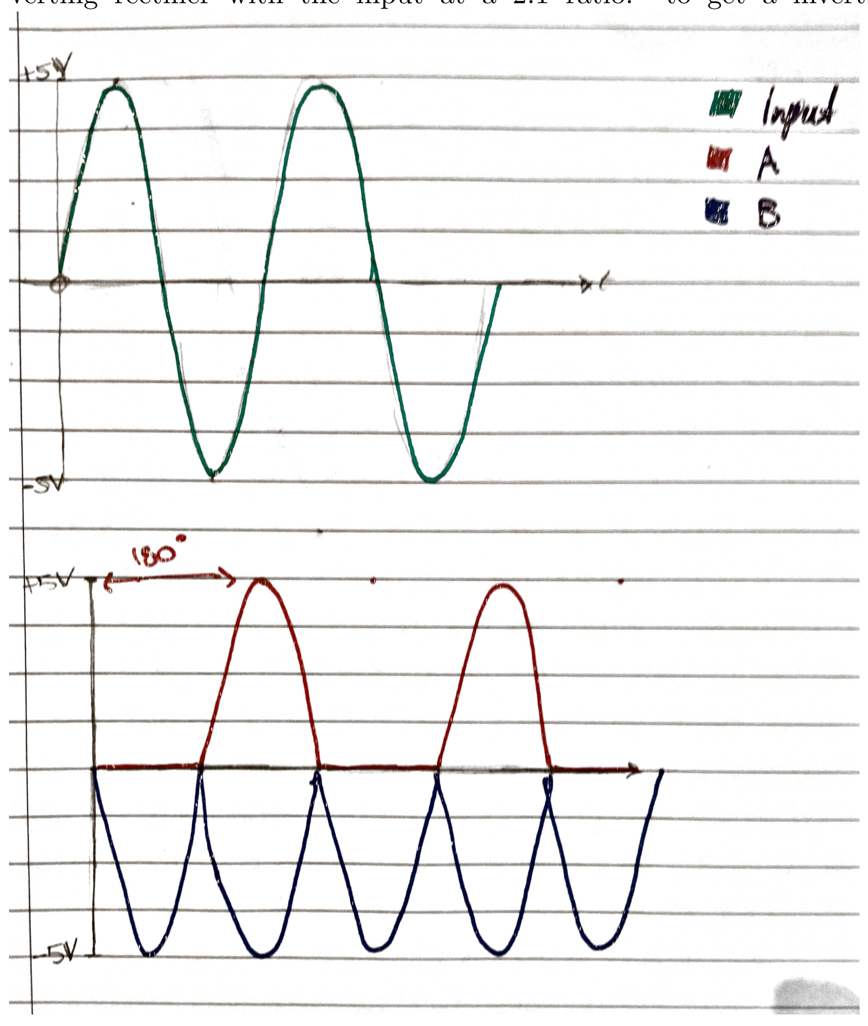
i) The Vo is saturated at 1 rail, until the output crosses the threshold set be R1, R2, and then Vo snaps to the other rail.

ii) $V_T = \pm 0.25V$, $V_T = \pm 0.25V$
$V_T = \frac{R_1}{R_1 + R_2} V_O$
Choose $R_1 = 1K$ then $R_2 = \frac{R_1}{\frac{V_T}{V_O}} - R_1 = 51K$

iii) Can be used to compensate for contact switch bonusing and cutting out noise, ie for a audio noise gate.

Question 5

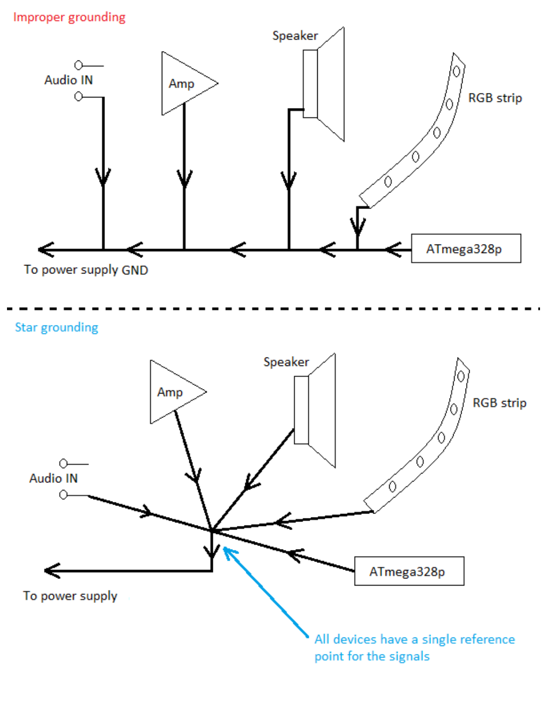
i) The circuit has a initial stage of an half wave rectifier that is then combined at the inverting rectifier with the input at a 2:1 ratio. to get a inverted full wave rectification.



ii) This is an inverting full wave rectifier.

Question 6

i) This is grounding scheme that is used to prevent ground loops. It involves have components referencing the **same** point, not intermediate points.



ii) A pole placed at an appropriate low frequency in the open-loop response reduces the gain of the amplifier to one (0 dB) for a frequency at or just below the location of the next highest frequency pole. This is to allow for greater open loop bandwidth while still maintaining amplifier closed loop stability.

iii) To do this we increase the phases rate of change, to do this we add poles in the form of an RC chain.