ECEN303 Analogue Electronics
Lab 2 - LTspice Laboratory - Submission

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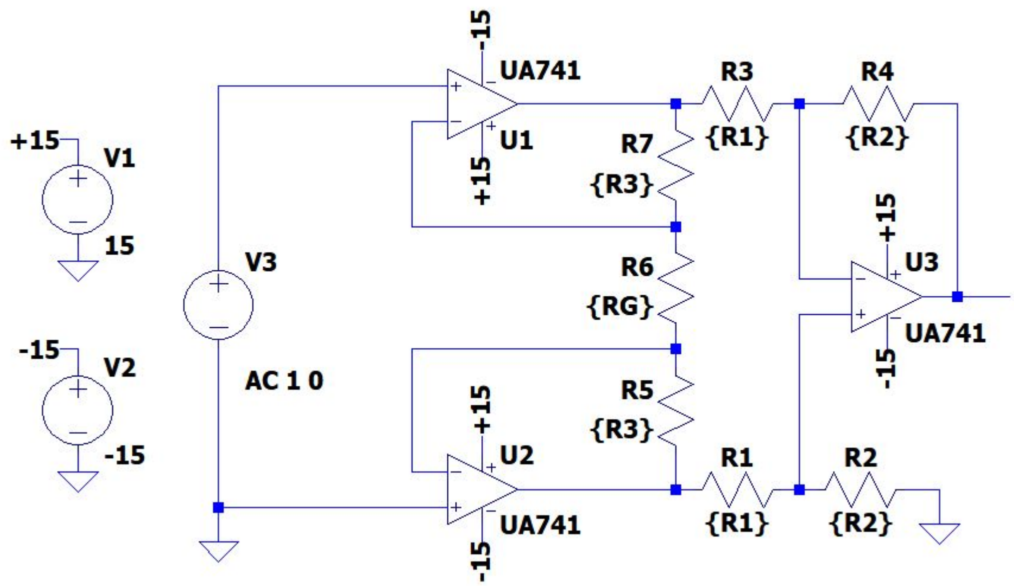
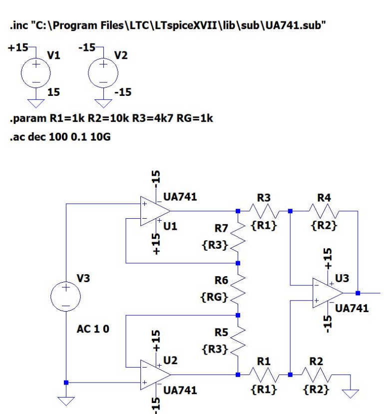
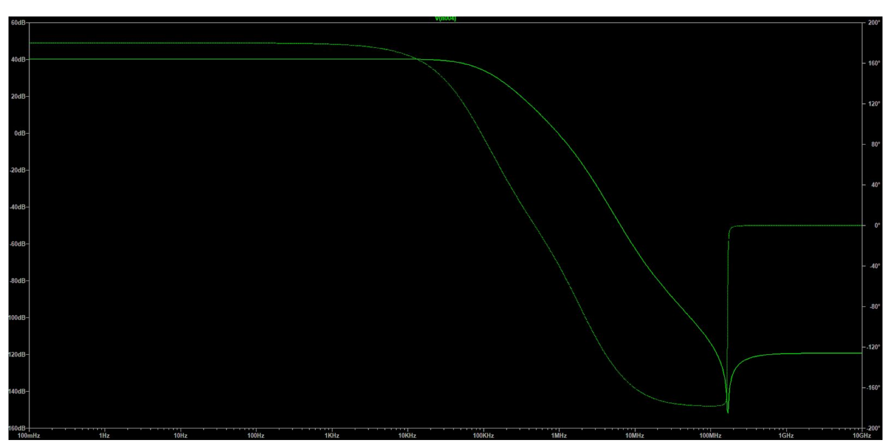
1. Schematic Entry



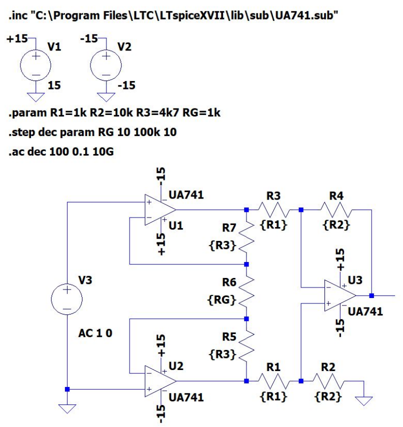
2. Circuit Simulation

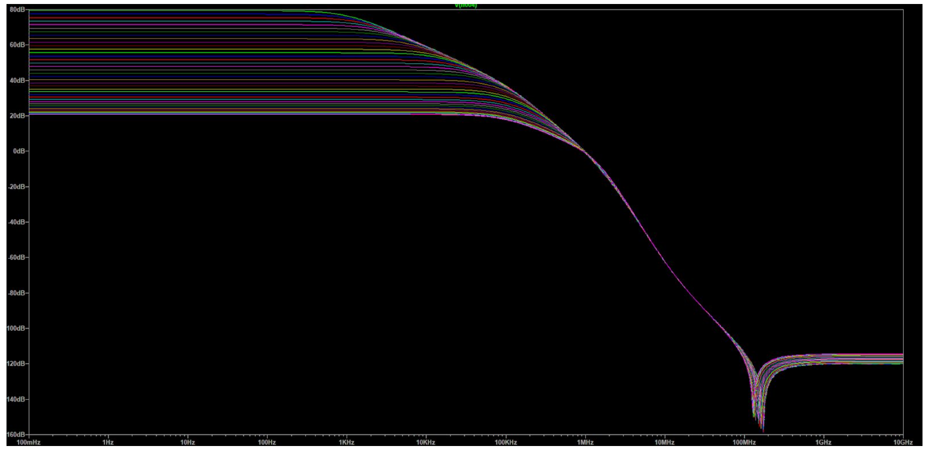
A.



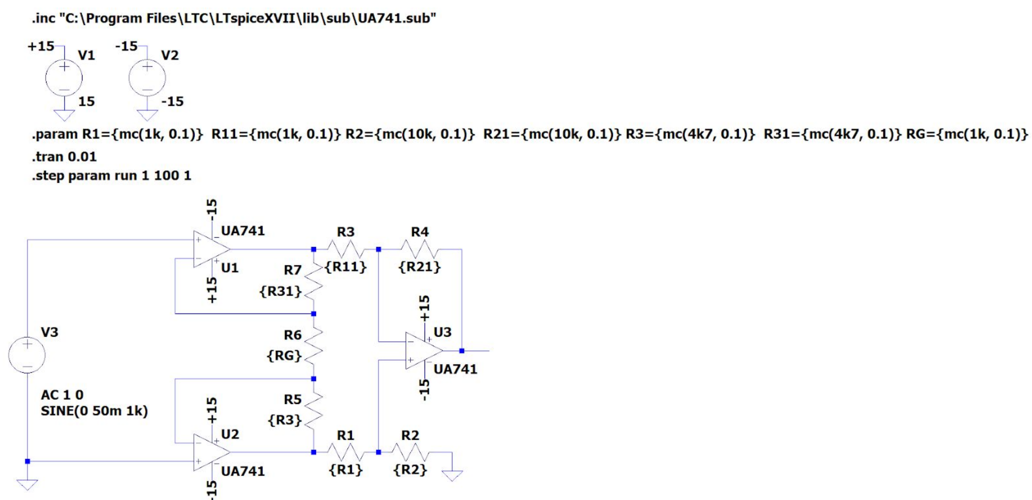


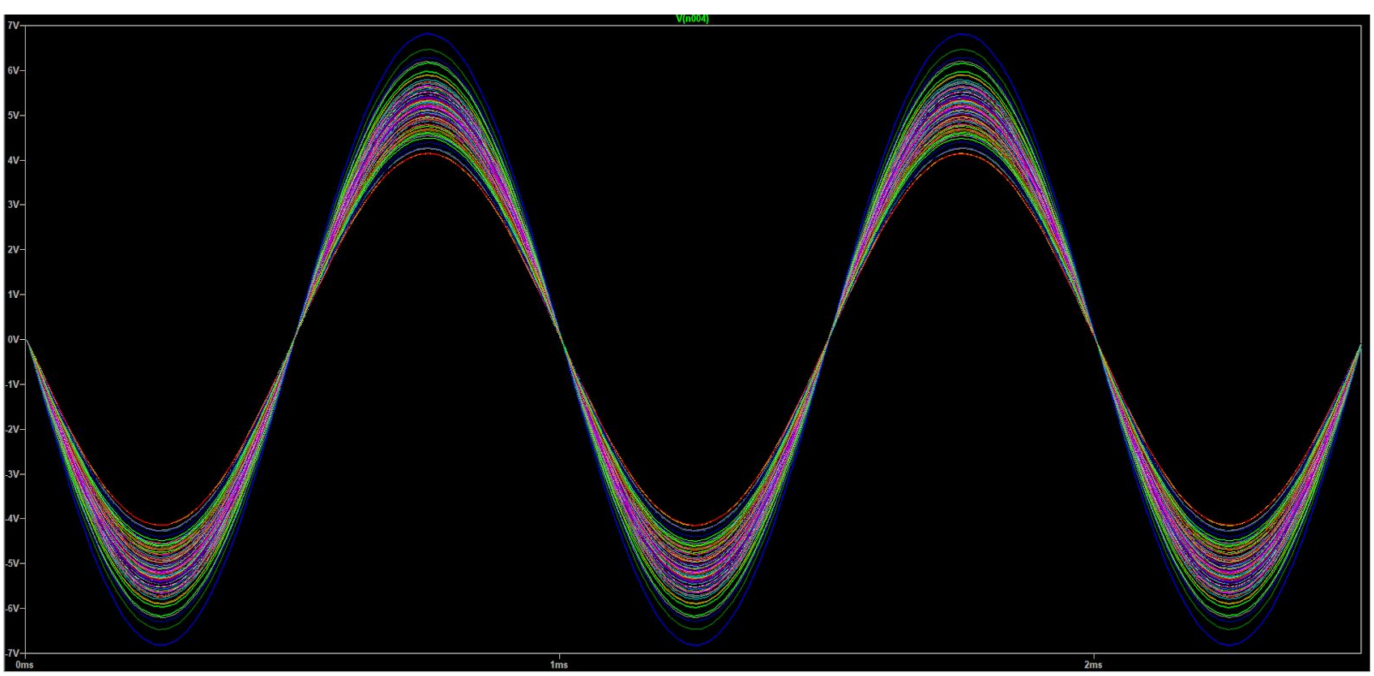
B.


.inc "C:\Program Files\LTC\LTspiceXVII\lib\sub\UA741.sub"
+15 V1 15
-15 V2 -15
.param R1=1k R2=10k R3=4k7 RG=1k
.step dec param RG 10 100k 10
.ac dec 100 0.1 10G
UA741 U1 R3 {R1} R4 {R2} R7 {R3} R6 {RG} R5 {R3} U3 UA741 V3 AC 1 0 U2 UA741 R1 {R1} R2 {R2}



C.


.inc "C:\Program Files\LTC\LTspiceXVII\lib\sub\UA741.sub"
+15 V1 15
-15 V2 -15
.param R1={mc(1k, 0.1)} R11={mc(1k, 0.1)} R2={mc(10k, 0.1)} R21={mc(10k, 0.1)} R3={mc(4k7, 0.1)} R31={mc(4k7, 0.1)} RG={mc(1k, 0.1)}
.tran 0.01
.step param run 1 100 1
UA741 U1 R3 {R11} R4 {R21} R7 {R31} R6 {RG} R5 {R3} U3 UA741
V3 AC 1 0 SINE(0 50m 1k)
U2 UA741 R1 {R1} R2 {R2}


V(n004)
0ms
1ms
2ms

3. Analysis and Critical Thinking

A.

$$\begin{aligned}\frac{V_o}{V_i} &= \frac{R_2}{R_1}(1+\frac{R_3}{R_G}) \\ &= \frac{10k}{1k}(1+\frac{4k7}{1k}) \\ \frac{V_o}{V_i} &= 57 \\ \text{Amplitude Amp Factor} &= 20log(\frac{V_o}{V_i}) \\ &= 35.1175\text{dB}\end{aligned}$$

B. This series of outputs shows a correspondence between maximum gain and the range/bandwidth of meeting that maximum gain. Such that a higher gain is inversely proportional to bandwidth of the max gain.

C. As seen by look at the output waveforms of the MC simulation, it can be seen that the |voltage| output can vary significantly for the varied resistor values. So by running the monte carlo analysis to cover the bases of real world resistor variance to determine if the design is within the desired output. (eg between a minimum and hitting the rails).