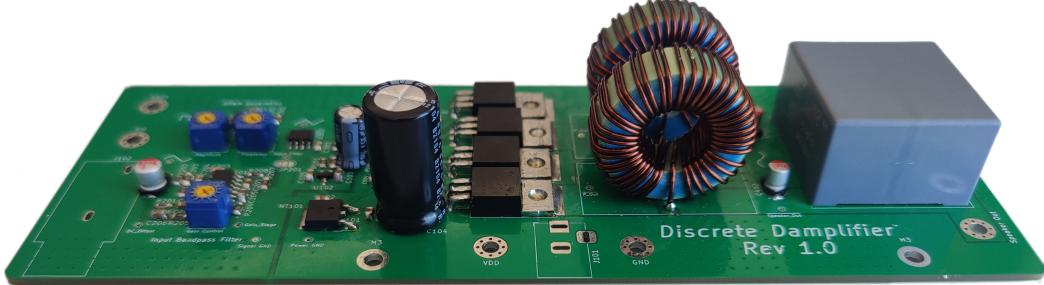


ECEN 405 - D Class Amplifier

"What a buck convertor would say if it could talk"

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Team members: Niels Clayton & Nickolai Wolfe



1 Introduction

In the realm of audio amplifiers the D Class offers a method of supplying a high power loads with very high efficiency (especially when compared to other classes). Classes A, AB offer high power output with very low signal distortion but suffer greatly in the efficiency department due to continuous linear conduction times and resulting losses in their amplifying elements/transistors. D class amplifiers can achieve up to 90-95% power efficiency by taking advantage of a switching approach but require a more complex design process and circuit.

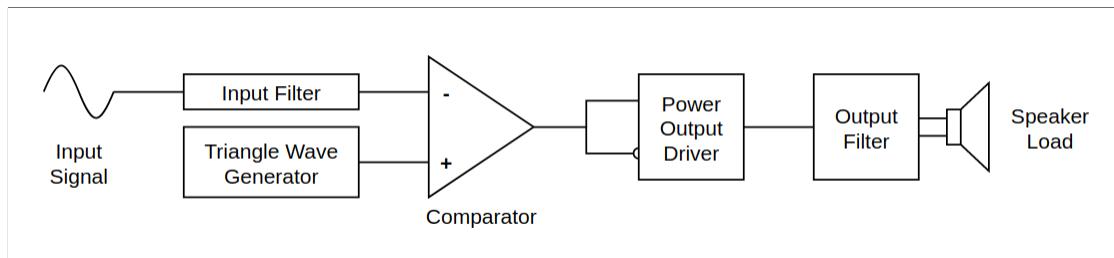


Figure 1: General Block Diagram of a D Class Amplifier

A D class design can be broken up into and explain with a series of blocks illustrated above in fig. 1. An input signal is sampled with a triangular wave into a high frequency SPWM carrier signal that is then amplified to high power by switching a MOSFET bridge and the carrier frequency is removed with a low pass filter. As the switching elements are either ON or OFF the continuous conduction losses near eliminated*.

This report outlines and discussed the specifics in design, implementation and results of constructing a D-class amplifier project to the specifications outlined below in section 1.

Specifications

- $P_{out} = 80W$ for $R_L = 4\Omega$
- 10Hz to 200Hz Bandwidth
- Input sensitivity of 1V for maximum output (interpreted as 1V amplitude, 2V pk-pk)
- Maximum costs: \$50 per person

2 Design

A D-class amplifier operates on the signal sampling, switching amplification, and signal reconstruction as briefly described above. This project practically realised this approach with the high level design shown in fig. 2.

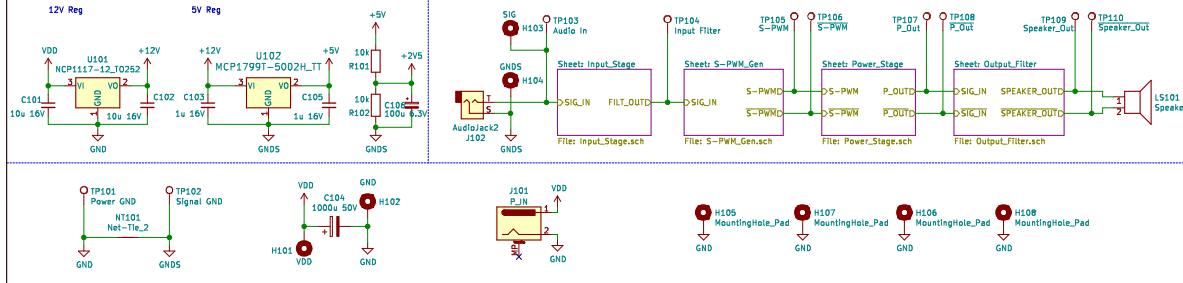


Figure 2: Top Level Design Schematic

As the intended load is a sub-woofer and there is a required bandwidth, the input audio signal must undergo some filtering and other preconditioning. This is handled by the input stage and was designed by Nickolai Wolfe. This stage band-passes the audio to meet the frequency range requirement, and otherwise adjusts gain and reference levels to make it suitable for the sampling stage.

The Sampler or Sinusoidal pulse width modulation (SPWM) generation stage was designed by Niels Clayton and encodes the audio signal into a high frequency carrier PWM signal. This signal is output (non-inverted and inverted for positive and negative output channel) at the correct voltage level for the driving circuitry as the switching control signal to the Power Amplifying Stage.

The last stage(s) of the D-Class is the Amplifying Bridges and reconstruction (Low pass) filters and their design was handled by myself. This project utilised two independent MOSFET bridges to amplify both SPWM signals and the reconstruction filter then strips out the high frequency carrier PWM to output the desired audio signal to the load.

2.1 Top Level Design Decisions

Topology

First is a topology choice. D-class amplifiers come in two main "flavours", Full and Half Bridge. Full Bridge amplifiers dedicate a whole bridge (1 driver, 2 MOSFETs) for each of a channels output rails. A Half bridge on the other hand has a single bridge that drives both the positive and negative sides of the output signal.

As the half bridge does not have independent bridges it will therefore require double the supply voltage (and is usually dual rail) to achieve the same output power. Its configuration also resulting in the commutation current being pumped back through the power supply, resulting in fluctuation and often the need for implementation a closed loop feedback system to maintain output stability.

For the above drawbacks of the half-bridge as well as the fact that we are producing a mono output channel we decided to use an open loop full bridge topology to make breaking up the design simpler, maintain a single supply rail and sacrifice the required component duplication as a compromise.

Power Supply

Now that the project confirmed as Full Bridge, to meet the required output power to the 4 Ohm load the required VDD needs to be set.

$$\begin{aligned} V_{DD} &= \sqrt{2 \cdot R_L \cdot P_{out}} = 25.298V \\ &= 26V(\min) \end{aligned}$$

Another addition that was made as an extension to the scope the inclusion of 2 linear regulators to power the drivers and logic circuitry such that this project would produce a more cohesive final product. These are included in fig. 2.

2.2 Input Bandpass Filter

Active Bandpass filter with adjustable gain stage to pass 10Hz to 200Hz.

this is what is was designed to do to meet these spec with this method, with these nice additions

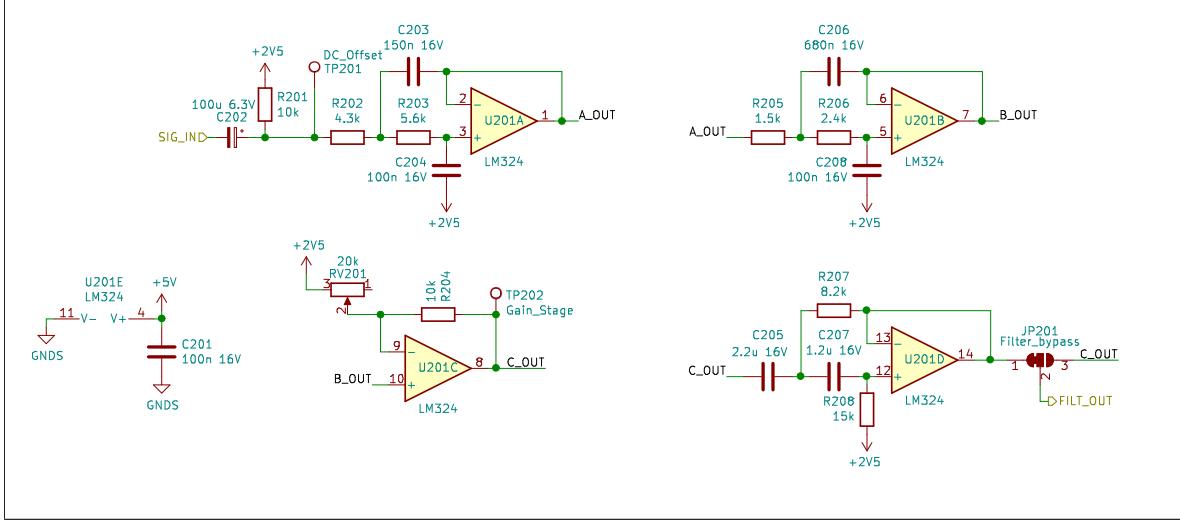


Figure 3: Input filtering schematic

2.3 Audio Sampling and SPWM

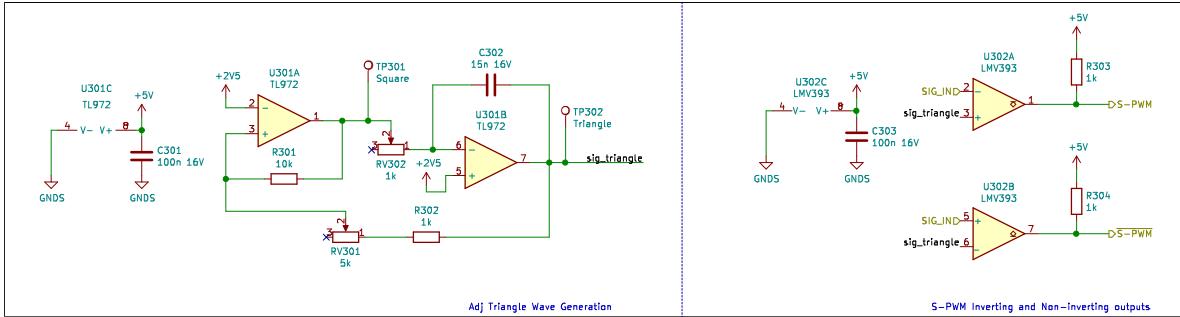


Figure 4: Sampling triangle wave & SPWM generation schematic

2.4 Power Stage and Output Filter

These sections are required to amplify the generated 5V SPWM from the sampler filter out the carrier frequency to reproduce the audio signal.

They consist of two symmetric MOSFET bridges (non-inverted and inverted SPWM amplifiers) that forming the full bridge topology and a low pass reconstruction filter to decode the audio signal. Each of these require following a design procedure to meets specification and the optimisation of component choice to minimise losses, maintain signal integrity and add protection.

Power Amplifying Bridge

- FET selection
- Driver selection
- Bootstrapping and dead time

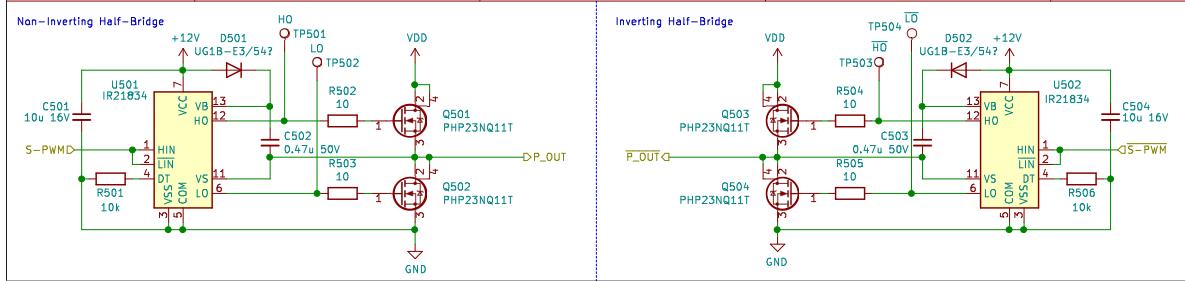


Figure 5: Gate driver schematic

Reconstruction Filter

This D-class is designed around a minimum switching/carrier frequency of 30kHz therefore a filter is required on the bridges output to attenuate this and restore the audio signal for output and driving the sub-woofer. Even though the carrier frequency is outside the audible range and the sub-woofer could not accurately reproduce it, leaving it unfiltered could degrade the efficiency and well as cause EMI issues.

As audio signal integrity is a priority the chosen topology is a low-pass Butterworth filter to maintain a flat gain in the passband and good phase response. Specifically the configuration chosen is the Alternate Balanced 2-Pole Filter shown in fig. 6. This utilises dual matched inductors (L) to eliminate common-mode swing, a single full rail unpolarised capacitor (C_L) for improved rejection and two addition balancing capacitors ($C_{a,b}$) that provide a HF ground shorts.

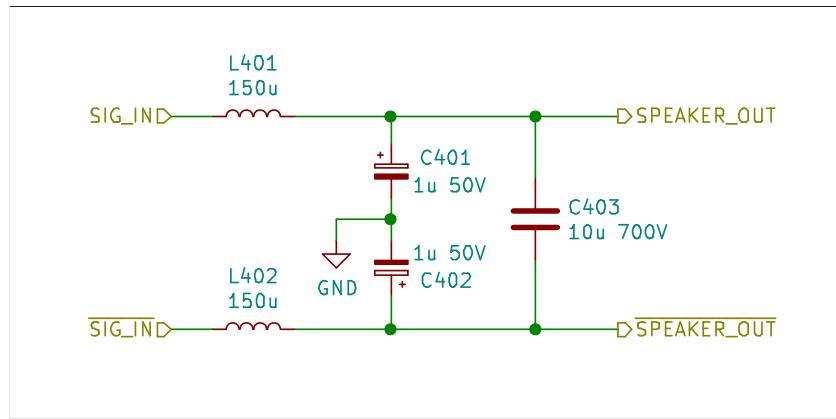


Figure 6: Alternate Balanced 2-Pole LPF

- Topology and Design
- Simulation and Part selection

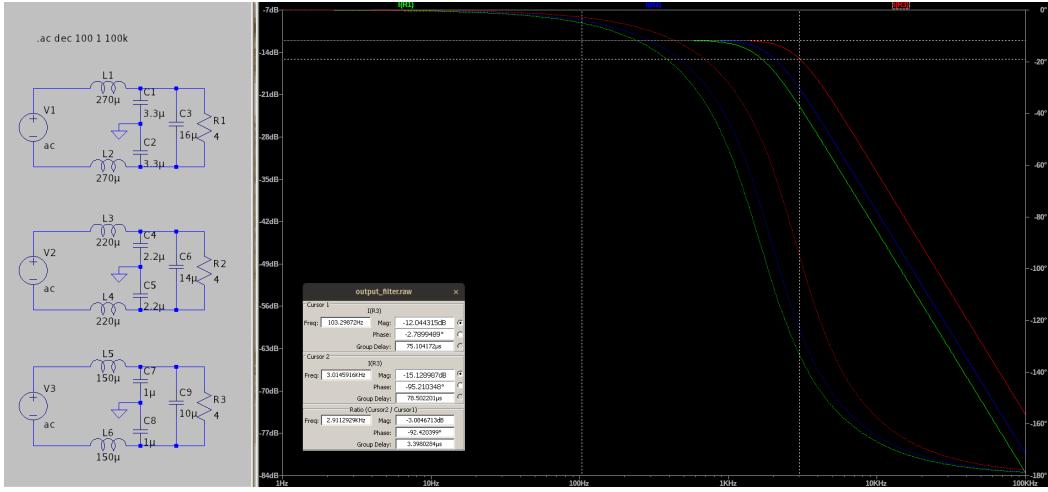


Figure 7: Output filter option simulations

3 Implementation

Here you should discuss the assembly of the amplifier and any problems you faced as a team building the amplifier. Here, the individual components should also be characterised. For example: if you have a filter, what is the response and how does it compare to the calculated? If you have a triangle wave, how does it look? Is it doing what I should? Why? Why not? How do the inputs/outputs of your comparator look? How does the square wave on the gate of the MOSFETs look?

3.1 PCB Layout

3.2 Gate Driving and Bridge Output

4 Results

Here I would expect to see the results of the whole amp, for example: an output wave, analysis of the efficiency, discuss maximum power output (which may be frequency dependent), and THD.

Frequency (Hz)	THD (%)
30	1.8
50	2.2
100	3.2
200	3.3
300	3.5
500	3.2

Table 1: Output total harmonic distortion across frequency

5 Conclusions

What worked, didn't work? How would you change your approach? Any interesting insights?

Per brd the price was kept to the 50 dollar per mark as per this BOM (https://niels-clayton.github.io/D-Class_Amplifier/)

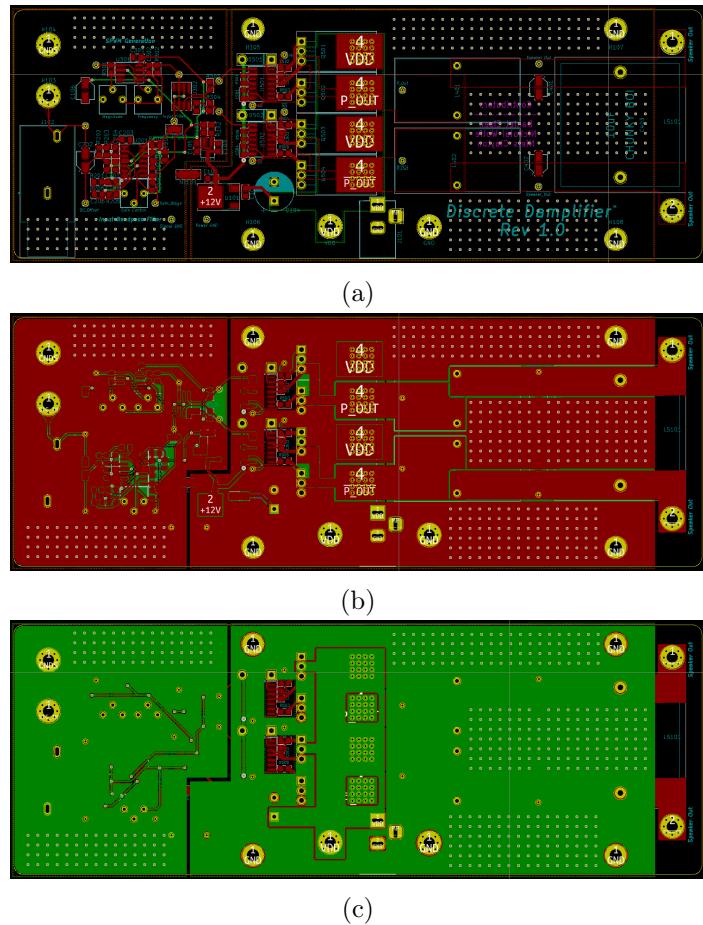


Figure 8

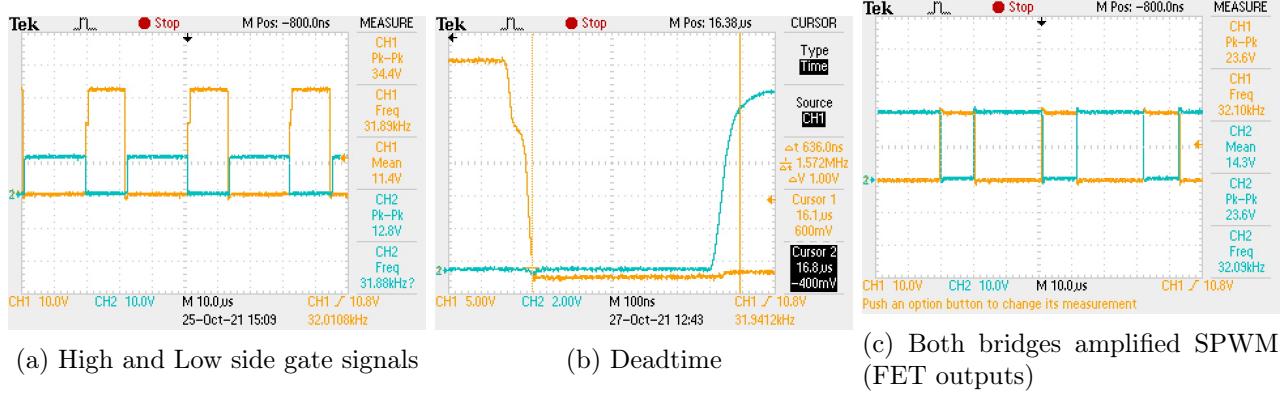


Figure 9

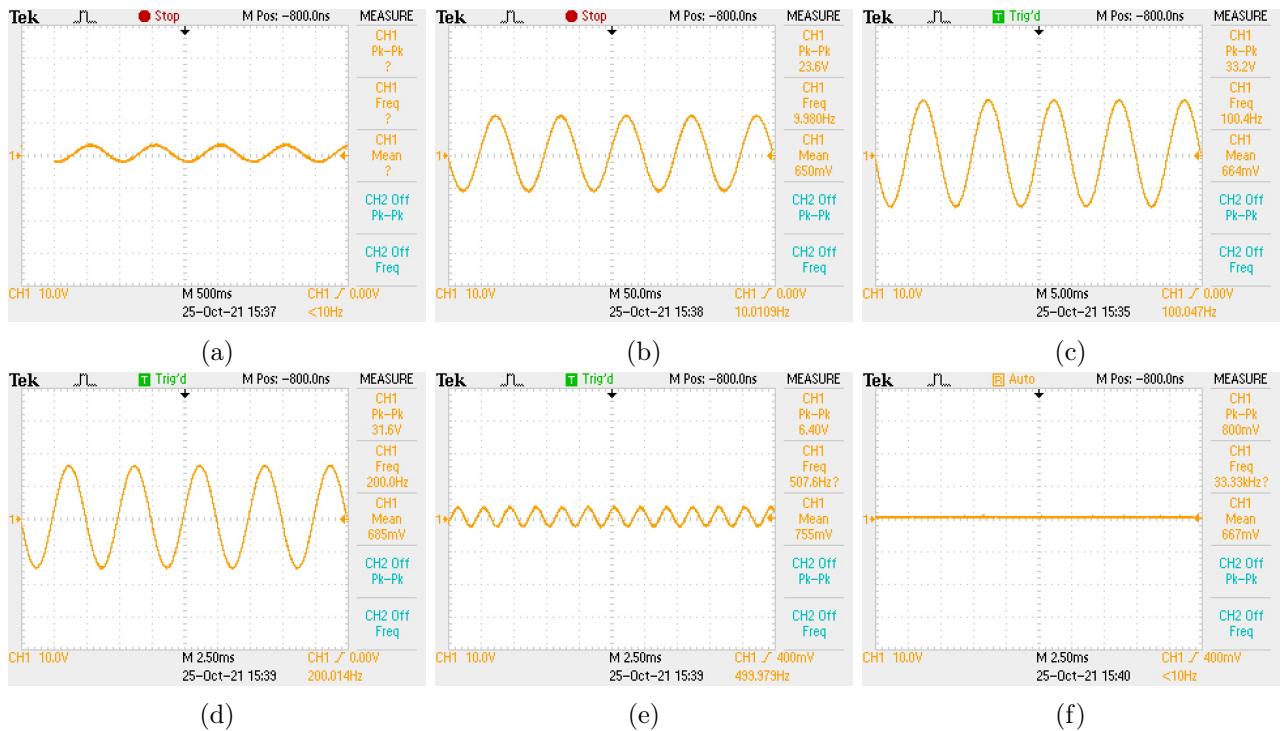


Figure 10

Appendix

Input Filter

Sampling/SPWM

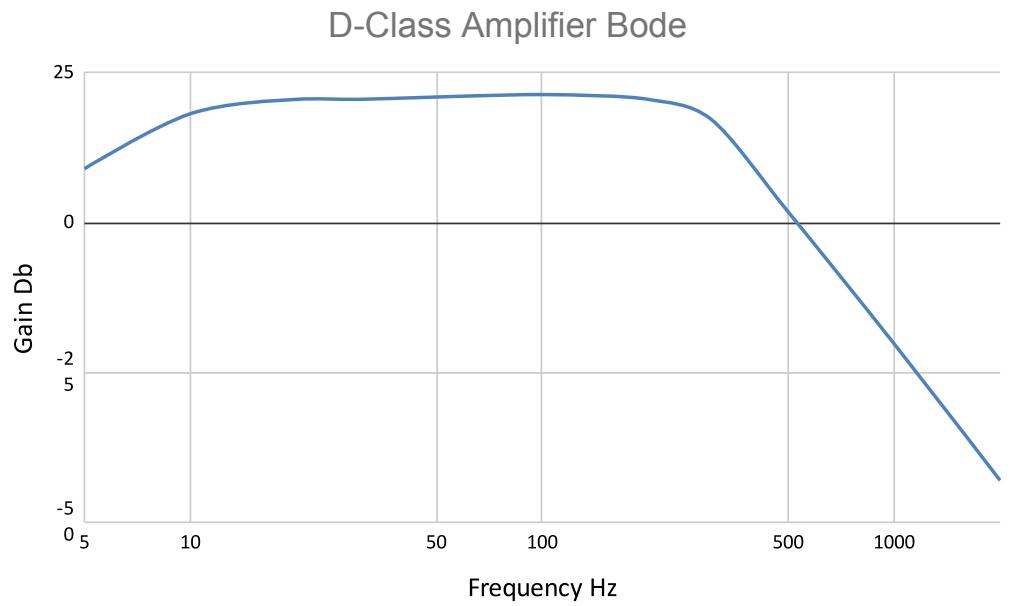


Figure 11

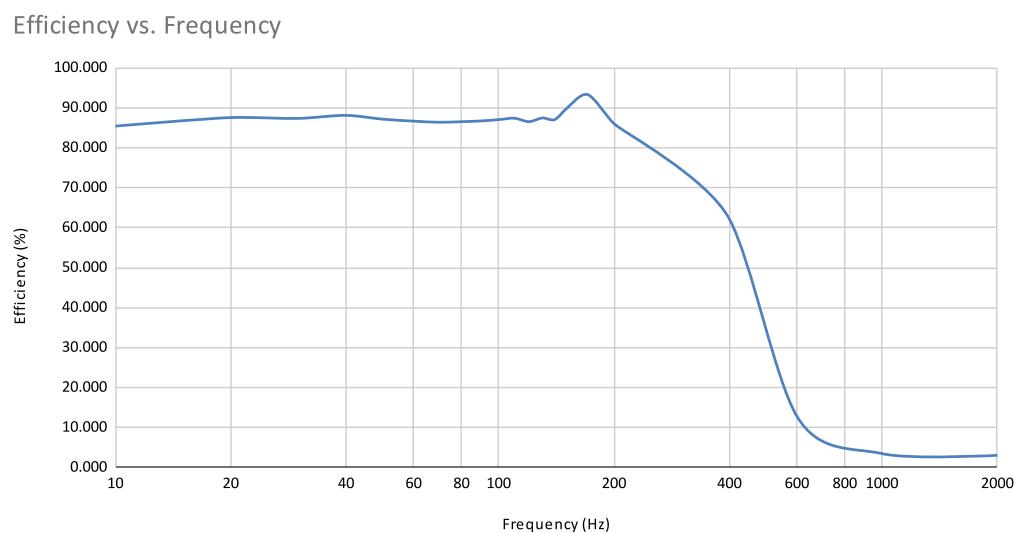


Figure 12



Figure 13

