ECEN 202 Test **18 August 2016**

Attempt all questions – use the test book supplied.

Total = 70 marks

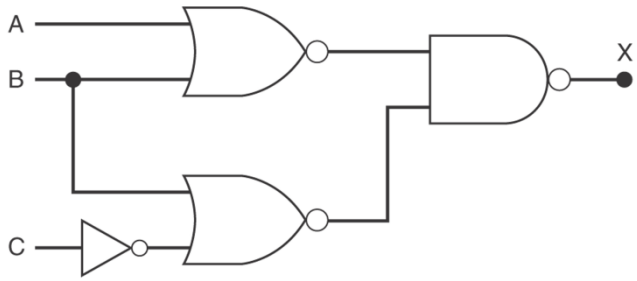
Time allowed: 90 minutes

Data sheets attached at back.

Question 1: Combinatorial Logic [20 marks]

a. (i) Write down a logic expression for the logic represented by the circuit below. (1)

(ii) Now use De Morgan's Theorems to simplify this expression. (3)



b. Consider the following sum of products expression:

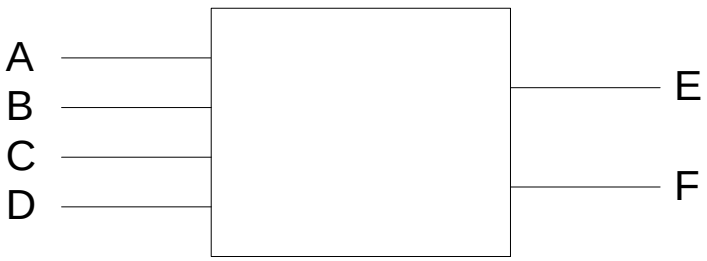
$$\overline{B}.\overline{C}.\overline{D} + \overline{A}.B.\overline{C}.\overline{D} + A.B.\overline{C}.\overline{D} + \overline{A}.\overline{B}.C.D + A.\overline{B}.C.D + \overline{A}.\overline{B}.C.\overline{D} + \overline{A}.B.C\overline{D} + A.B.C.\overline{D} + A.\overline{B}.C.\overline{D}$$

(i) Generate a truth table for the logic (2)

(ii) Use a Karnaugh map to minimise this expression (3)

c. A logic circuit is used to compare the magnitudes of two 2-bit binary numbers, AB and CD. The circuit has two outputs, E and F and functions in such a way that:

- The O/P E will be HI whenever AB = CD and LO when AB ≠ CD.
- The O/P F will be HI when CD > AB and LO when CD < AB. When AB = CD (E = HI) it will then F will be in a "don't care" state.



You must now design the logic to implement the output F.

(i) Use the Karnaugh map method to find the logic function describing F.

(5)

(ii) Sketch the logic circuit needed to implement F. (2)

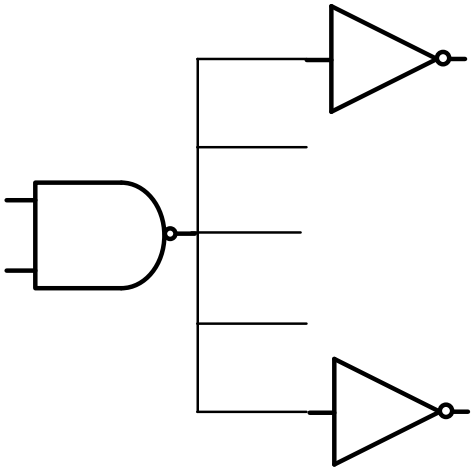
(iii) When you want to construct the logic circuit, you find out that you only have NAND gates available. Sketch a logic circuit for the circuit to be constructed from NAND gates only. (4)

Question 2: Properties of logic ICs [20 marks]

a. Attached are extracts from the datasheets for 74LS00 quad two-input NAND gates and the 74LS04 hex inverter.

(i) Calculate the noise margin for this logic family. (2)

(ii) You want to connect the O/P of one NAND gate to drive a number of parallel inverters. Calculate the maximum number of inverters that you will be able to drive ? (4)

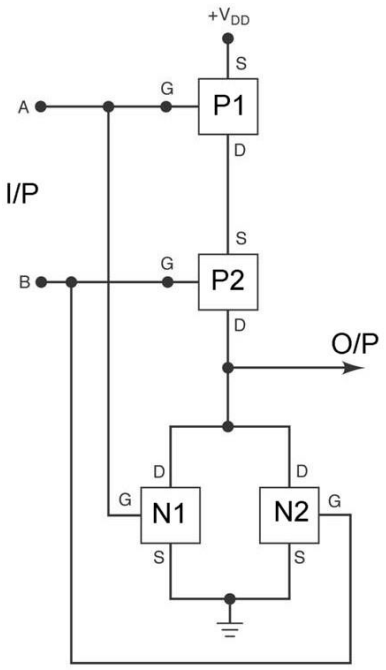


After construction of the circuit in (ii) you now need to calculate the maximum time it will take for a change in the input to the NAND gate to be observed on the output of the NOT gate:

(iii) What will this time be if the one input to the NAND gate is held HI while the other input makes a LO to HI transition ? (1)

(iv) What will this time be if the one input to the NAND gate is held LO while the other input makes a LO to HI transition ? (1)

b. Study the following circuit below made from MOSFET transistors:



(i) Draw up a table as shown below and fill in the table below to indicate the status (ON or OFF) of each of the two PMOS transistors (P1 and P2) as well as the two NMOS transistors (N1 and N2) for each of the possible input conditions. (4)

(ii) Also fill in the output logic (HI or LO) that will result from the status of the transistors for each input. (2)

(iii) Identify this logic gate. (1)

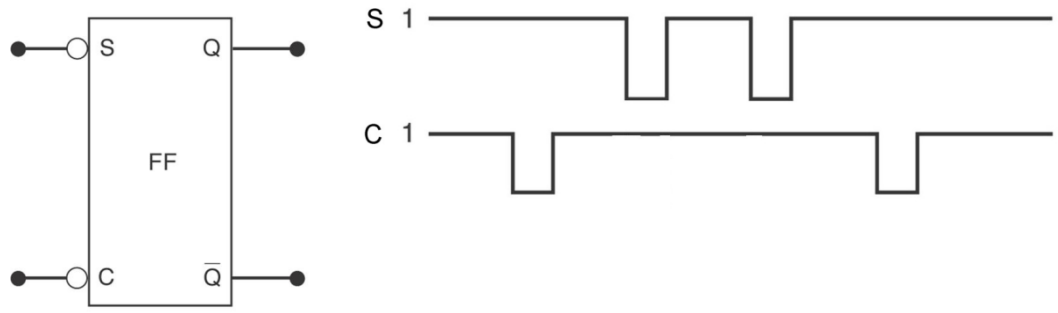
(iv) Show how this gate can be converted to a tri-state enabled logic gate of the same function as previous. The tri-state input should be active LO. (3)

A	B	P1	P2	N1	N2	O/P
0	0					
0	1					
1	0					
1	1					

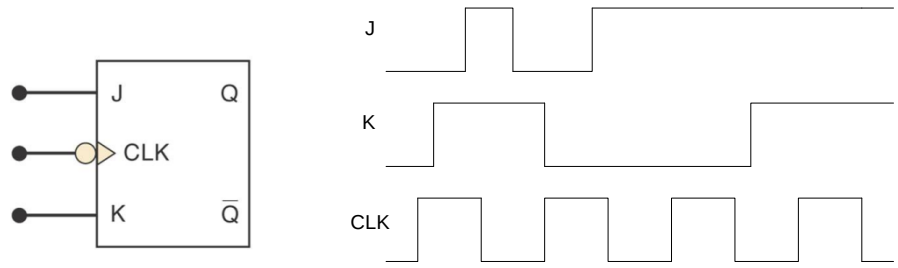
Question 3: Sequential logic: Latches and Flip-Flops [20 marks]

a. For each of the devices or circuits below, sketch the timing diagram of the output Q that will result from the given input conditions. In all cases assume that the flip flop is initially in the RESET state.

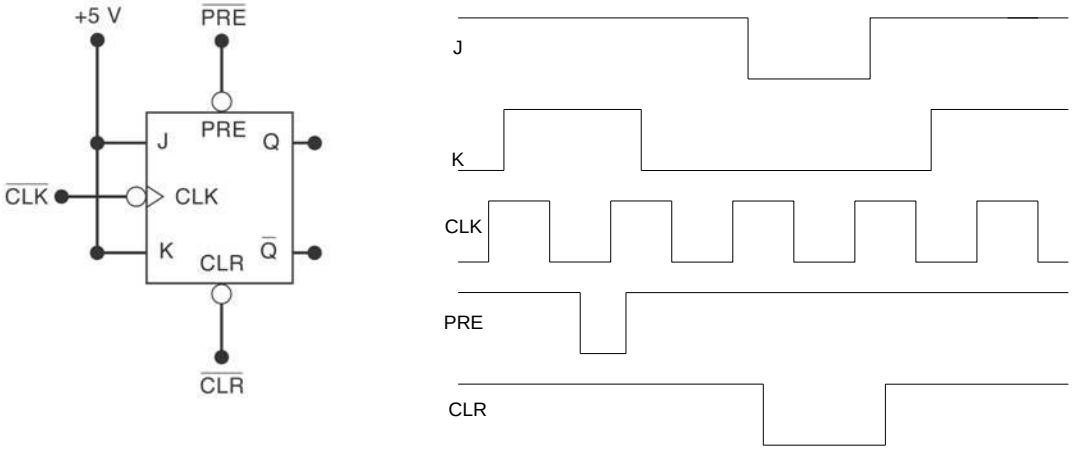
(i) Sketch Q (2)



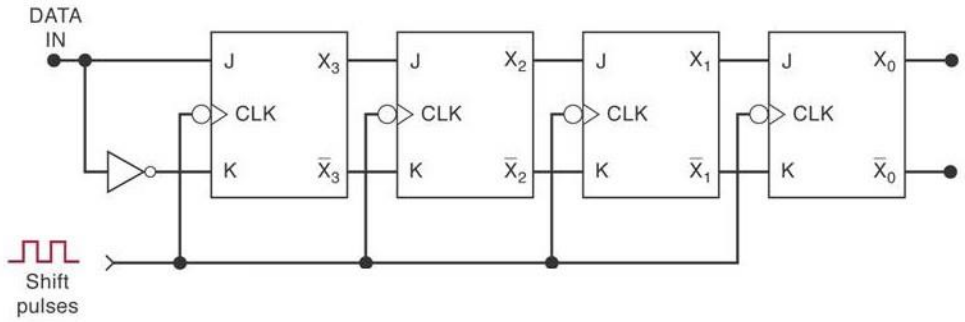
(ii) Sketch Q (2)

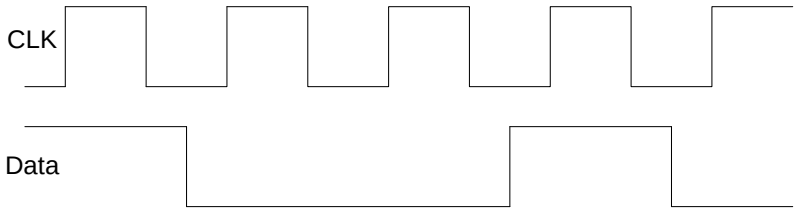


(iii) Sketch Q (2)

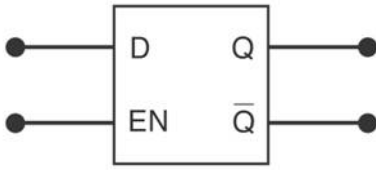


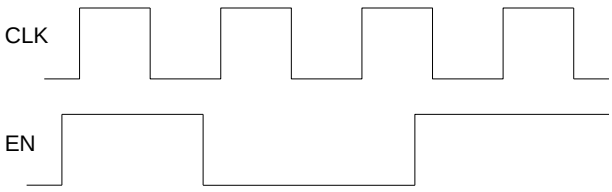
(iv) Sketch the waveforms at X_0, X_1, X_2 and X_3. (4)



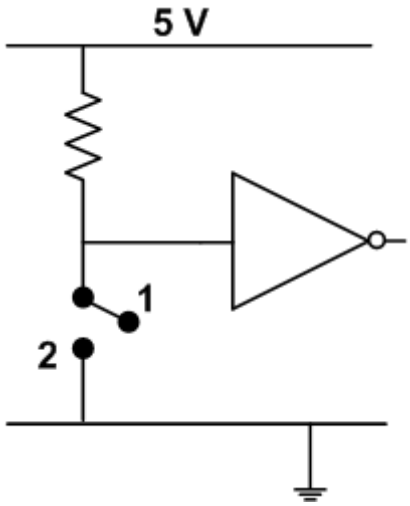


(v) Sketch Q (2)





b. In the circuit below, the logic level to the input to the inverter is controlled by a mechanical switch.



(i) The switch is initially in position 1 (open) , then changes to position 2 for 1 second (closed) and then returns to position 1. Sketch a timing diagram that shows the theoretical logic levels at the input and the output of the inverter during this time. (2)

(ii) Also sketch a timing diagram that will show the most likely actual logic level at the input and the output of the inverter during this process. What is this effect called and why is it observed? (2)

(iii) Show how you will implement a SC latch to solve this problem (ii). (4)

Question 4: Sequential logic: Counters [10 marks]

You need to construct a 1 Hz clock signal from a 20 Hz reference signal. Assume that this reference signal has the appropriate voltage range for digital logic. Sketch diagrams to show how you will construct a counter for this task using:

(i) Generic J-K flip-flops with active LO CLEAR inputs. Sketch the logic diagram. (4)

(ii) 74LS293 decade counter(s) as in the attached datasheet. Sketch a circuit diagram that will show pin numbers and pin functions. (6)