ECEN302 : Integrated Digital Electronics
Lab 5 Submission

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September 18, 2020

1 Overview

A lot of HDL coding is respective, boilerplate code that is pretty much always necessary for the project function. I.e. counters, clock sources at specified frequencies, and other basic parts. For this it is less efficient and more error prone to write the HDL code in full, instead the Vivado environment offers the IP catalogue and wizards component creation to build up a base more easily and efficiently.

2 Methodology

The first design was a pulse generator, for this I used the clock wizard to generate a high speed 5Mhz input clock. Using the wizard allows for intuitive easy implementation and selection of clocking parameters and frequency, this generates IP that can be directly instigated in the HDL project code. A basic resettable, rising edge counter to count the edges and output a high/low signal across a 1 second period. This was done by counting the edges and outputting a low if count ¡ 2500000 and high otherwise, resetting every 5000000.
For the second design, the above 5Mhz to 1 second increment design was used to drive a second utilised 0 to 9 4 bit counter that was imported as from the IP catalogue and customised to reset/enable correctly to output to the seven segment display. The display different values to 2 modules similtationly another divided clock rate must be used to scan across the modules, i.e the refresh rate.