ECEN302 : Integrated Digital Electronics
Lab 6 Submission : Vitis and the MicroBlaze IP

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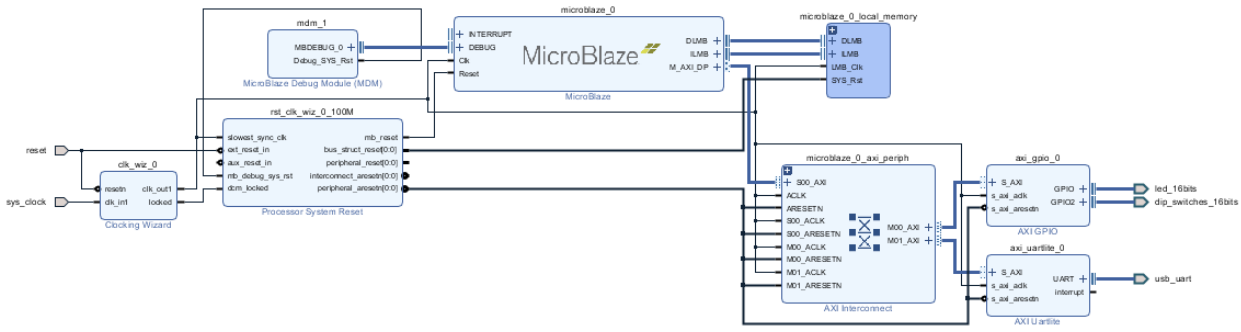
1 Overview

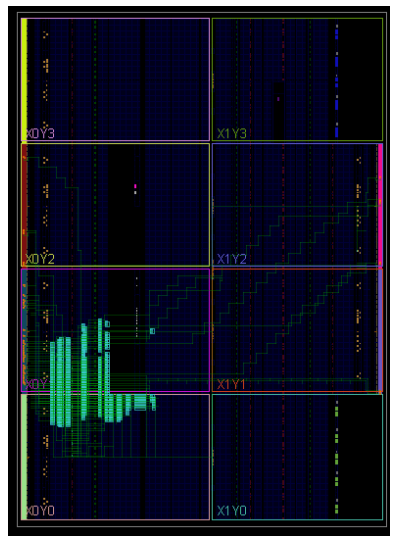
FPGA design is much more that simple logic definitions using small sequential and/or combinatorial designs. The Xilinx suit also allows, via the IP catalogue system, to include and entire microprocessor core directly to a devices fabric.
Doing this allows the 'softcore' processer to be use in a management role of much more complex designed and larger applications.
This lab covers how to add and setup the MicroBlaze softcore processer as a vivado project and then export that implemented hardware to the Vitis IDE so that the processer can be developed for in plain C code.

2 Methodology

Firstly, a Vivado project is setup with a block diagram into which the MicroBlaze IP block is added. This allowed for device specific blocks and ports to be added, such as a reset and clock pin as well and configurable GPIO block.
From this Vivado can run multiple steps of automated design/connections to add blocks required by the included IP, MicroBlaze memory and peripherals, and map the net connections correctly.



From that a VHDL wrapper can be generated and the design fully implemented. As seen below this design consumes a fair bit more resources than the previously labs smaller designs but there is still plenty of silicon left to construct the rest of a more complex deign, such as signal processing units, hardware accelerators, video processers etc that can be monitors/managed by the softcore.



From the implemented design and bitstream the project can export the hardware and Vitis can launched and setup to develop for that exports onboard MicroBlaze, for which we did the customary Hello World then made the LED's flash.