ECEN202 **LAB 1**

Logic Gates and Combinatorial Logic

1. Learning Objectives

The purpose of this lab is to:

a. serve as a review of the characteristics of basic logic gates.

b. allow the construction of basic digital circuits using a breadboard and design station

c. use the basic logic gates as combinatorial building blocks to synthesize complex logic functions.

d. use multiplexers to implement logic function

2 Introduction.

2.1 Building real logic circuits using integrated circuit logic gates

In this lab we will start to build logic circuits using digital integrated circuits (ICs). All the ICs we will use are based on CMOS (**c**omplementary **m**etal **o**xide **s**emiconductor) oxide technology. The technology and characteristics of these devices will be discussed in more detail in class. We will specifically use the 74HCT family of ICs, which makes them totally compatible with older TTL (transistor-transistor logic) devices. The IC number should normally look as follows:

AA 74HCT XXX B or in the simpler form 74HCTXXX.

This number can be decoded as follows:

AA: Typically a two letter code that indicates the manufacturer

74 or 54: The temperature range over which the IC will work. Commercial devices (74) have a temperature range of typically 0 – 70 ºC, while military specified devices (54) will have a temperature range of -55 to 125 ºC.

HCT: Indicates the logic family, in this case CMOS with specific characteristics. Al members of this family should have identical operating characteristics, for example the supply voltage required or the HI-LO voltage ranges.

XXX: We then have two or three digits that indicate the device function, for example 00 would indicate a NAND gate, while the number 153 would indicate a dual four-input

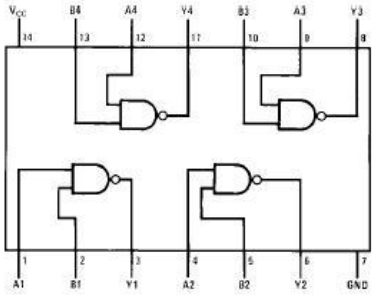
multiplexer.

B: The last part of the number may be a single letter that indicates the type of package of the device.

The logic gates that we use are designed as part of an integrated circuit, which is then packaged to produce an IC with typically 14 pins. These pins provide electrical connection between the external circuit and the internal logic gates. This enables multiple logic gates to be included on the same package and in the figure below the internal arrangement of a 74HCT00 CMOS NAND gate is shown. It can be seen that the internal structure consists of four two-input NAND gates, which thus needs twelve of the fourteen pins of the package. Of course the IC also needs power to enable these gates to work, and a power and ground is supplied in pins 14 and 7 respectively.

74HCT00 Quad 2-Input NAND Gate

LOGIC SYMBOL



2.2 Use of device datasheets

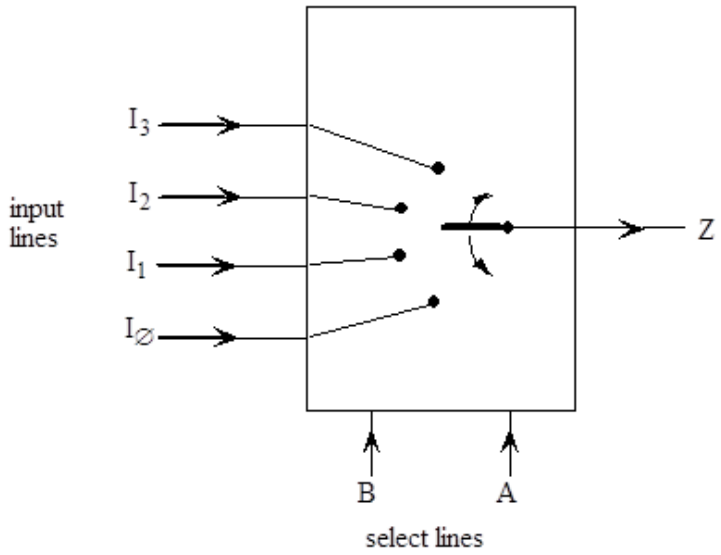
All the information we should need on the use of a particular integrated circuit should be available in the datasheet supplied by the manufacturer. **It is then essential that we refer to these datasheets when we construct a circuit.** Datasheets are available on the web; for example search for "74HCT00" and you will come across datasheets from different manufacturers for the device. Device properties between different manufacturers are typically very similar, and will provide you with all the electrical, timing and mechanical characteristics you need to use the IC.

2.3 Use of the design station and breadboard.

In these laboratories we will mostly use a commercial design station and breadboard to prototype your circuits. The functions and use of these will be explained to you at the start of the laboratory.

2.4 Implementing logic functions with a multiplexer (MUX)

A multiplexer is one of the special function integrated circuits that will be discussed in more detail later in the course. It has multiple inputs, a single output and a number of "input select lines" that will determine which one of the multiple input lines will be switched through to the output. It behaves like a rotary switch in that one of these inputs is steered through to the output depending upon the status of "input select" lines (also called control lines). This process is illustrated below for a 4:1 MUX. We can now hardwire a logic function on the MUX by connecting the input lines to the logic value that will be required as the output value Z for the given inputs A and B.



3. Pre-lab Preparations

3.1 Reading

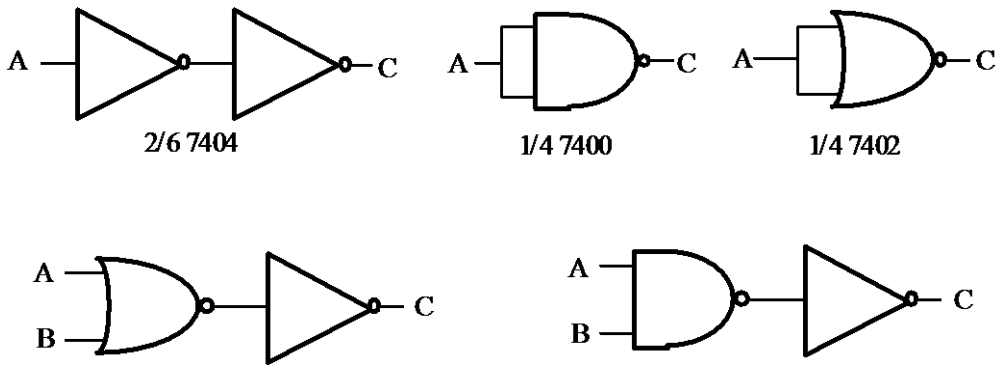
Read through Sections 1a,b and c (Review Sections) of your class notes.

3.2 Complete the following work in your lab notebook before you attend the lab.

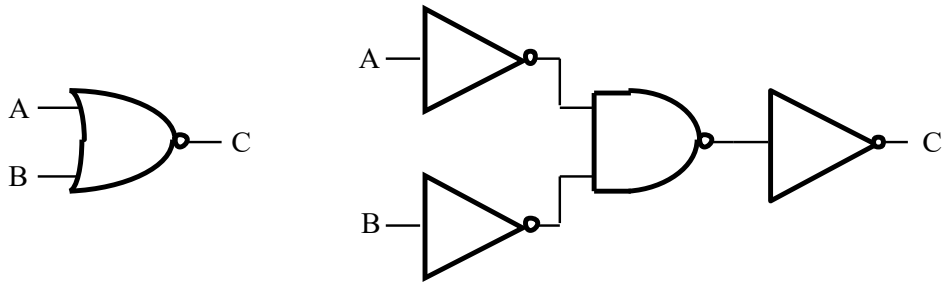
3.2.1 Draw up the truth tables for one of the four gates on each of the 74HCT00, 74HCT02 & 74HCT04 packages.

3.2.2 Use data sheets (available on the web) to sketch the pin-outs for each of the devices 74HCT00, 74HCT02 and 74HCT04. Note that (i) pin #1 is marked by a dot on the IC case, and the pins are numbered anticlockwise when viewed from above, (ii) pin #14, usually (but not always) reserved for the +5V power supply, and pin #7, usually common, are at opposite corners of the IC.

3.2.3 Establish truth tables relating the inputs A and B to the output C for the circuits below. Summarise the truth tables with algebraic expressions which reflect the relevant theorems of Boolean algebra.



3.2.4 Demonstrate one of De Morgan's two laws by establishing truth tables for the two circuits below. Write down algebraic expressions for the outputs C in both cases and show them to be equal by reference to their truth tables.



3.2.5 A One-Bit Half Adder

Write down the truth table for a one-bit adder with inputs A, B, and outputs CARRY & SUM. Write expressions for the two outputs, and sketch the logic circuit that you will construct to implement this function.

3.2.6 The 74HCT153 MUX

Get the data sheet of the above dual 4:1 MUX and study the operation of this device. Pay particular attention to the use of the ENABLE inputs. Explain what function this has in the operation of the IC. Now sketch in your lab book the logic levels that needs to be connected to the input lines in order to make this 4:1 MUX function as (i) a NAND gate and (ii) an XOR gate.

4 In the laboratory

4.1 Using the design station

Ensure that you are familiar with the functions and use of the design station and the breadboard. Use your digital multimeter in resistance function (alarm) and establish the contact pattern across the breadboard. Sketch this contact pattern in your lab notebook.

6.2 Evaluating the 74HCT00, 74HCT02 and 74HCT04 Integrated Circuits

Establish a +5 V (red wire) bus on the outer perimeter rail of the breadboard and a common rail (green wire) on the inner perimeter rail. Place a 74HCT00 IC on the breadboard, and make the appropriate power connections. Connect V_{ext} to +5 V on the SDS, and the inputs for one of the four gates on the package to the logic level switches (UP = HI). Connect the gate output to a logic indicator (ON = HI) with the logic selector set to "TTL". Briefly confirm the operation of the gate in terms of LO's & HI's. Repeat for each of the other two gates.

6.3 Construction of some simple logic functions.

Construct each of the logic function from Section 3.2.3 above using the appropriate logic gates. Establish truth tables relating the inputs A and B to the output C for these circuits, using logic switches and LED logic indicators. (Note that "2/6 7404" means "two of the six gates in a 7404 chip", etc.) To aid in wiring up the circuits, sketch them in your log book with the inclusion of pin numbers. Check that their operation agrees with your expected truth table.

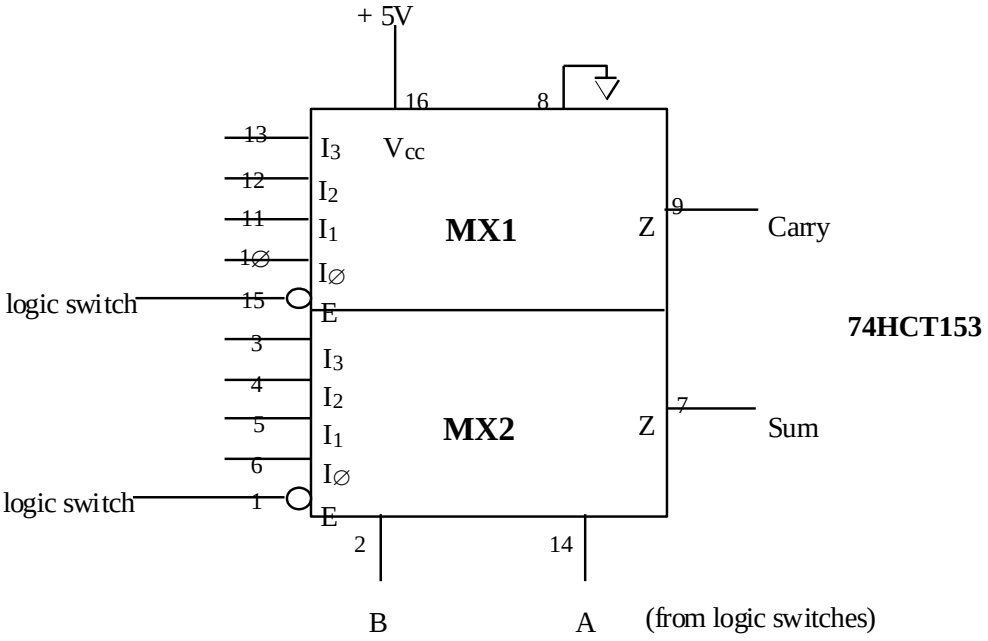
Now demonstrate one of De Morgan's two laws by building the two logic circuits from Section 3.2.4 and checking that your circuit operation agrees with your truth table.

6.4 Construction of a One-Bit Half Adder using discrete logic gates.
Construct this circuit that you designed in Section 3.2.6 using any of the three types of logic gates. Check the circuit operation.

6.5 Implementing logic functions with a multiplexer (MUX)

Wire up the MUX with correct logic level on the input lines in order to make this 4:1 MUX function as (i) a NAND gate and (ii) an XOR gate. Check that it is operating correctly.

6.6 Construction of a One-Bit Half Adder using a multiplexer solution
The true convenience of using multiplexers is that we can use them in implementing arbitrary logic functions. To demonstrate this capability, we will use the 74HCT153 dual 4 line to 1 line MX to implement the one-bit adder:-



Use your truth table to set the inputs (I_0...I_3) for CARRY & SUM to 1's (+5V) or 0's (common) by direct connection. With E1 & E2 set LO, check the operation of the adder.

Investigate the effect of the ENABLE inputs (labelled E on the diagram) on the device operation. Note that the bubble symbols on the enable inputs indicate that they are **active low.**

7. Post lab tasks – some more complex designs
As we have discussed in class, we can use our basic logic gates to synthesize much more complex logic functions. Look at the following:

7.1 Designing and building a prime number detector.
You must design a logic circuit that looks at a three-bit binary code (CBA) and output a HI signal if the decimal equivalent of the code represents a prime number.

(i) Draw up a truth table that represents this logic and determine the SOP expression.

(ii) Simplify this expression in order to use the least possible number of gates.

(iii) Also use a K-map to represent and simplify this logic. Does the simplified logic of the K-map agree with that from the algebraic simplification ?

(iii) Show how you will construct this circuit using the appropriate logic gates available on the tray (it does not need to be NAND, NOR or NOT).

(iv) If you should have time available in the lab construct this circuit and check that the circuit provides the correct logic function. Demonstrate your circuit to the lab demonstrator.

7.2 MUX implementation of prime number detector

Can you implement the logic function of the previous problem (7.1) using the 74HCT153 4:1 MUX instead of logic gates ? You are allowed to add external gates(s) to the MUX to enable your design. Sketch both the logic diagram as well as the circuit diagram to show how you will wire up this circuit.

Hint: You may need to change your dual 4:1 MUXes into a single 8:1 MUX.

8. Report

Use a short report to show the following results:

8.1 Show the truth table for your one-bit half adder (Section 3.2.5) and then show how you implemented this function by (i) discrete logic gates (Section 6.4) and by use of the 74HCT153 MUX (Section 6.5).

8.2 (i) Describe the basic operation of a multiplexer by describing the operation of a 4:1 MUX. Show the truth table for such a device and explain how the device can be used to implement arbitrary logic functions.

(ii) What would the internal structure of a MUX look like ? Sketch the likely internal structure for a 2:1 MUX.

(iii) Briefly discuss the operation of the 74HCT153 MUX by presenting the truth table. Explain the function of the ENABLE inputs.

8.3 Show your design for a prime number detector by showing the truth table and any simplifications you have made. Now show your logic circuits as based on (i) discrete logic gates and (ii) the 74LS153 MUX. Which one of these two options would be result in the minimum number of ICs to be used ?

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