ECEN302 : Integrated Digital Electronics
Assignment 1 Submission

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1. **Look up the data sheet for the device we are using in the laboratory and then answer the following questions:**

   The device on the Nexys4 DDR and A7 boards if is the Artix-7 100T.

   (a) *How many CLBs are there?*
   There are 7925 CLB's (15850 logic slice pairs).

   (b) *How many I/O pins?*
   The max supported single ended I/O is 300, but on the CSG324 package there are **210** user available I/O pins.

   (c) *What I/O voltages can be accommodated and how is this configured?*
   1.2V, 1.5V, 1.8V, 2.5V and, 3.3V. These are selected by setting the IOSTANDARD in I/O planning or in the constraints file of your project.

   (d) *What is the physical footprint?*
   The CSG324 package is 15x15 mm.

   (e) *What does "speed grade" mean?*
   Xilinx defines the 'Speed Grade" of specifically FPGA devices to be a general indication of the timing performance of that device. These are specified as relative rating with a device family. Ie -1,-2,-3 etc from slowest to fastest. Each speed grade level represents around a 10-15% performance difference.

2. **With reference to the CLB:**

   (a) *How is combinatorial logic typically implemented?*

   (b) *What is the main purpose of the flipflops/latches?*

   (c) *What is the carry chain and what is it used for?*

   (d) *What is the deference between a SLICEM and a SLICEL?*

   (e) *How are the CLBs connected to other CLBs?*

3. **With regard to FPGA design:**

   (a) *Describe the principle of pipelining and why it is often necessary?*

   (b) *Explain "setup" and "hold" timing?*

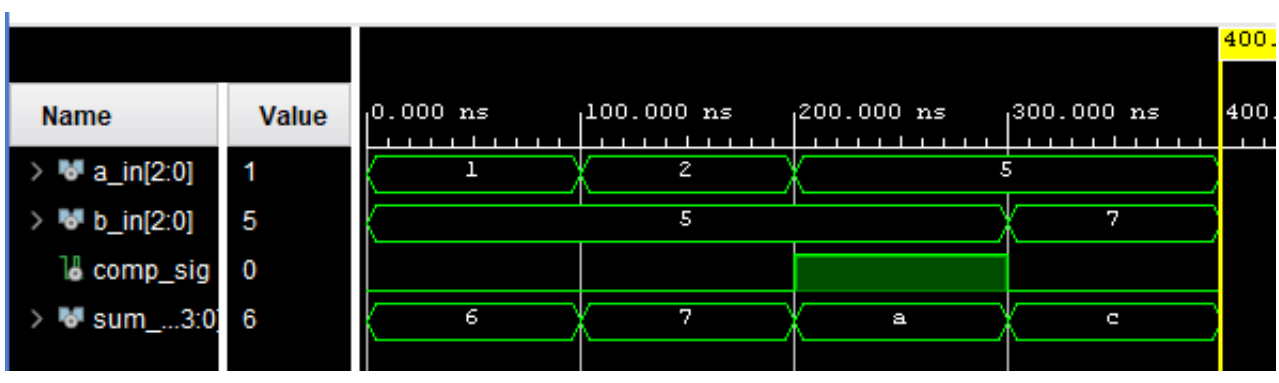
   (c) *What is metastability and what are the two main causes of it?*

   (d) *How do we typically deal with metastability?*

   (e) *Describe the difference between Mealy and Moore FSMs*

4. **VHDL design. Compare and Add Circuit.**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity comp_add is
    port(
        a : in unsigned(2 downto 0);
        b : in unsigned(2 downto 0);
        comp : out std_logic;
        sum : out unsigned(3 downto 0)
        );
end comp_add;

architecture Behavioral of comp_add is

begin

process (a,b) begin
    if (a = b) then
        comp <= '1';
    else
        comp <= '0';
    end if;
    sum <= ('0' & a) + ('0' & b);
end process;

end Behavioral;
```




```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity comp_add_tb is
--  Port ( );
end comp_add_tb;

architecture Behavioral of comp_add_tb is

component comp_add
    port(
        a : in unsigned(2 downto 0);
        b : in unsigned(2 downto 0);
        comp : out std_logic;
        sum : out unsigned(3 downto 0)
        );
end component;

signal a_in : unsigned(2 downto 0) := (others => '0');
signal b_in : unsigned(2 downto 0) := (others => '0');

signal comp_sig : std_logic  := '0';
signal sum_sig : unsigned(3 downto 0) := (others => '0');

begin

ca0: comp_add port map (
    a => a_in,
    b => b_in,
    comp => comp_sig,
    sum => sum_sig
);

process begin
    a_in <= "001";
    b_in <= "101";
    wait for 100 ns;
    a_in <= "010";
    wait for 100 ns;
    a_in <= "101";
    wait for 100 ns;
    b_in <= "111";
    wait for 100 ns;
end process;

end Behavioral;
```

5. **Below is a list of tools or methods that can assist and/or accelerate the development and debugging of code for FPGAs. For each one describe the process and its benefit to the developer. (note: it is expected that you write at least a quarter of an A4 page on each item. Feel free to include pictures).**

   (a) *Schematic generation of synthesised and routed designs*

   (b) *Test bench simulation*

   (c) *Timing analyser*

   (d) *Integrated Logic Analyser (ILA)*