ECEN405: Design Considerations of Converters



- What do we design for?
 - Cost
 - Size
 - Weight
 - Energy efficiency
 - Reliability



- What do we design for?
 - Cost
 - Size
 - Weight
 - Energy efficiency
 - Reliability
- What are our tools?
 - Switching frequency (already discussed)
 - Transistor/diode selection (already discussed)
 - Magnetic components
 - Capacitor selection
 - Thermal design



- Magnetic components
 - Size depends on switching frequency
 - Finite values (unless you wind your own)
 - Current rating and saturation
 - Resistance
 - Many types (different cores, toroidal low magnetic flux)



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 - Again, different types
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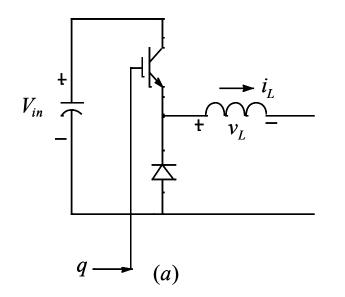
- Capacitor Selection

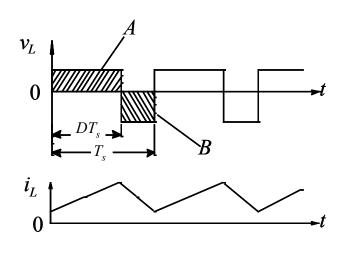
- Equivalent series resistance (ESR)
- Again, different types
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Thermal design

- Switching losses = heat
- Resistance in a circuit = heat
- Heat sinks increase size but also reliability
- Normal air convection, forced and liquid
- Increases cost
- Will talk about heat calculations in more depth later 6



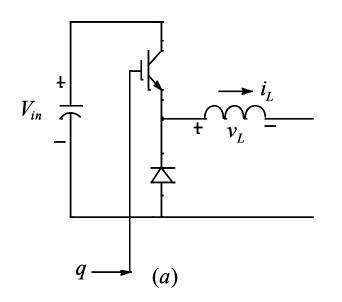


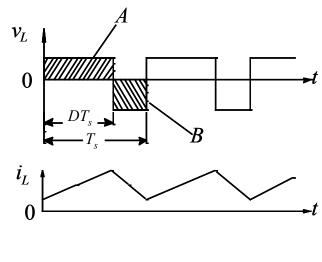


(b)



- We make some assumptions
 - Load = constant
 - Input voltage = constant
- Waveforms repeat with the period T_s
- Let's consider the inductor of a switching power-pole
- If the waveform repeats, the current at $i(T_s) = i(0)$
- The average inductor voltage over $T_s = 0$:





(b)



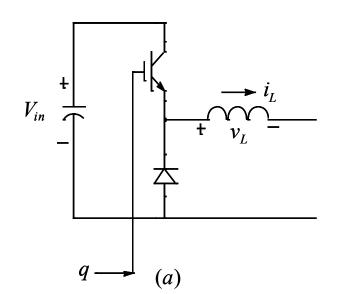
The average inductor voltage over $T_s = 0$:

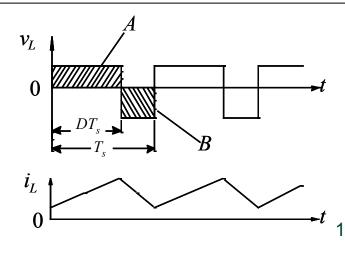
$$v_L = L rac{di_L}{dt} \quad \Rightarrow \quad i_L(t) = rac{1}{L} \int_{ au} v_L \cdot d au \qquad \qquad \qquad i_L(t) = i_L(0) + rac{1}{L} \int_0^t v_L \cdot d au$$

$$i_L(t) = i_L(0) + rac{1}{L} \int\limits_0^t v_L \cdot d au$$

$$i_L(T_s)=i_L(0)$$

$$\frac{1}{L} \int_{0}^{T_{s}} v_{L} \cdot d\tau = 0 \quad \Rightarrow \quad V_{L} = \frac{1}{T_{s}} \left(\int_{0}^{DT_{s}} v_{L} \cdot d\tau + \int_{DT_{s}}^{T_{s}} v_{L} \cdot d\tau \right) = 0$$



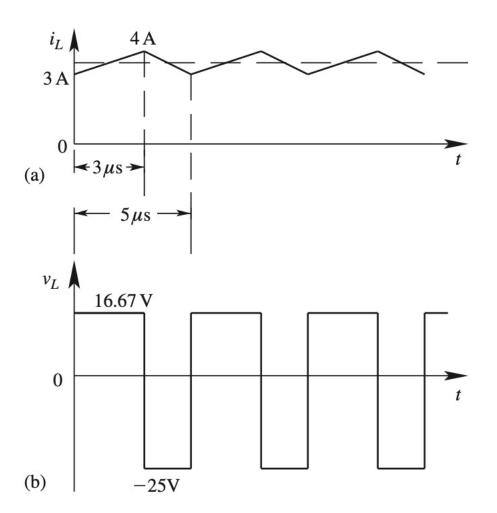


(b)



Lets do an example: We have a 50uH inductor...

$$v_L = L \frac{di_L}{dt} \quad \Rightarrow \quad i_L(t) = \frac{1}{L} \int_{\tau} v_L \cdot d\tau$$

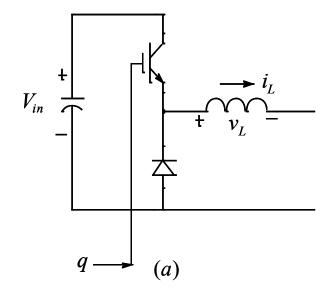


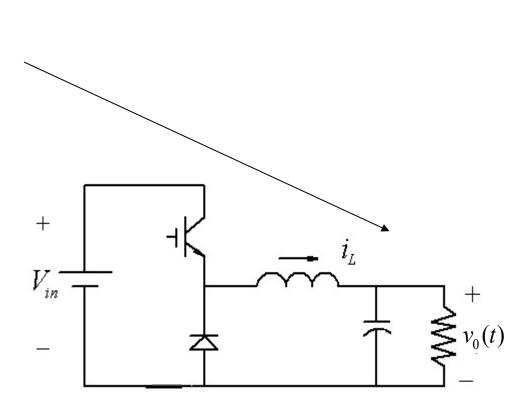


And for the capacitor?



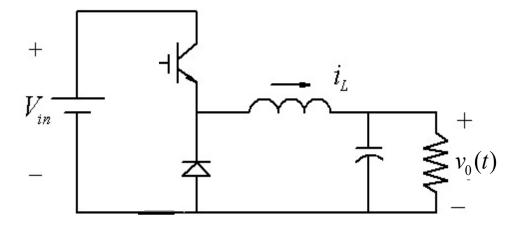
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And for the capacitor?

- Similar analysis to inductor



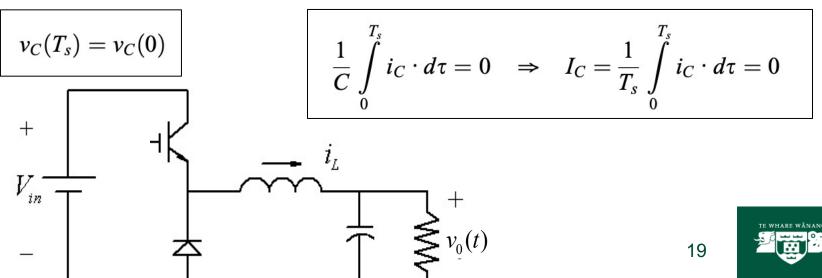


And for the capacitor?

- Similar analysis to inductor

$$i_C = C \frac{dv_C}{dt} \quad \Rightarrow \quad v_C(t) = \frac{1}{C} \int_{\tau} i_C \cdot d\tau$$

$$v_C(t) = v_C(0) + \frac{1}{C} \int_0^t i_C \cdot d\tau$$



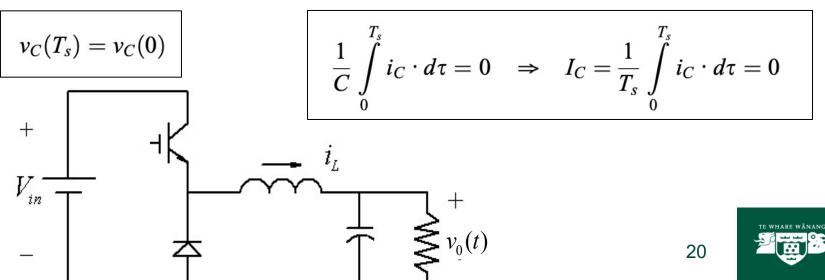


And for the capacitor?

- Similar analysis to inductor
- At $v(T_s)$ the voltage is the same as v(0)
- The average current integral over 1 period is 0

$$i_C = C \frac{dv_C}{dt} \quad \Rightarrow \quad v_C(t) = \frac{1}{C} \int_{\tau} i_C \cdot d\tau$$

$$v_C(t) = v_C(0) + rac{1}{C} \int\limits_0^t i_C \cdot d au$$



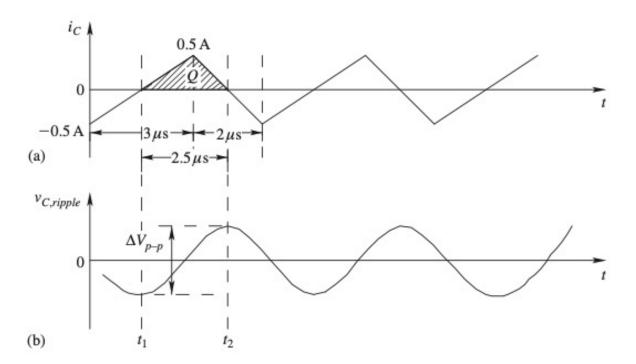


$$i_C = C \frac{dv_C}{dt}$$
 \Rightarrow $v_C(t) = \frac{1}{C} \int_{\tau} i_C \cdot d\tau$ $v_C(t) = v_C(0) + \frac{1}{C} \int_{0}^{t} i_C \cdot d\tau$

$$v_C(t) = v_C(0) + \frac{1}{C} \int_0^t i_C \cdot d\tau$$

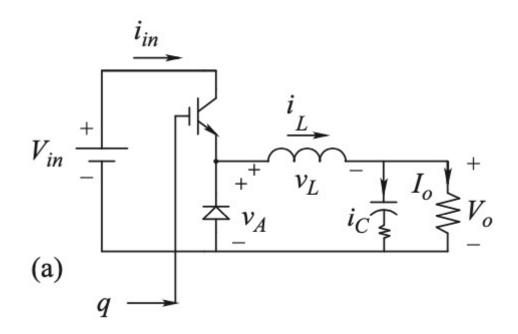
$$v_C(T_s)=v_C(0)$$

$$rac{1}{C}\int\limits_0^{T_s}i_C\cdot d au=0 \quad \Rightarrow \quad I_C=rac{1}{T_s}\int\limits_0^{T_s}i_C\cdot d au=0$$



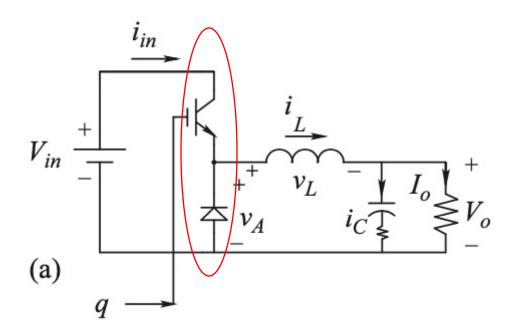


- Buck converter decreases input voltage



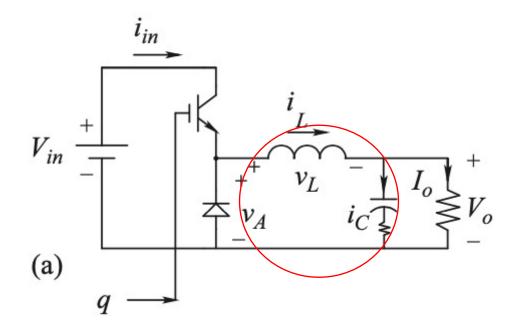


- Buck converter decreases input voltage
- Switching pole



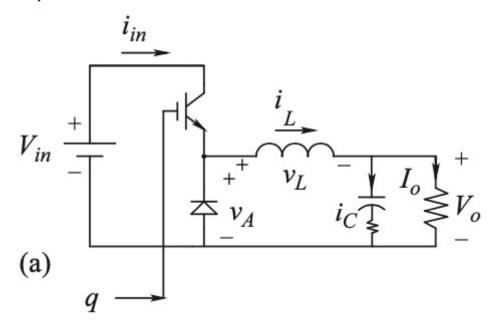


- Buck converter decreases input voltage
- Switching pole
- Second order low pass filter





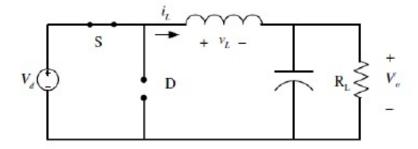
- Buck converter decreases input voltage
- Switching pole
- Second order low pass filter
- For analysis we make some assumptions:
 - Inductor current is continuous
 - Average inductor voltage is zero
 - Average capacitor current is zero
 - Ideal components





Switching analysis

When the switch is closed (transistor turned on)



- · Diode is reverse biased
- · Switch conducts inductor current
- This results in positive inductor voltage, i.e.

$$v_L = V_d - V_o$$

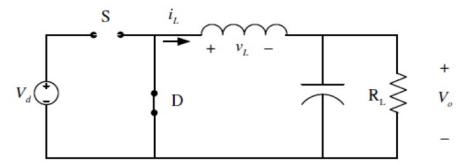
· Causes linear increase in inductor current:

$$v_L = L \frac{di_L}{dt} \Rightarrow i_L = \frac{1}{L} \int v_L dt$$



Switching analysis

When the switch is open (transistor turned off)



- Because of inductive energy storage, i_L continues to flow
- Diode is forward biased
- Current now flows (freewheeling) through the diode
- Inductor voltage is $v_L = -V_o$

Switching analysis

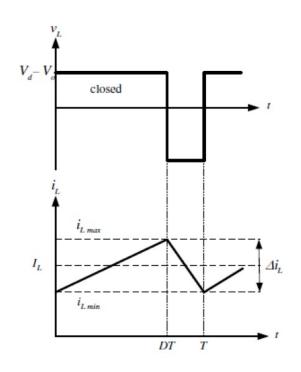
$$\Rightarrow (\Delta i_L)_{\text{closed}} = \left(\frac{V_d - V_o}{L}\right) DT \qquad \bigvee_{V_d - V_d} V_d$$

For switch opened:

$$v_{L} = -V_{o} = L \frac{di_{L}}{dt}$$

$$\Rightarrow \frac{di_{L}}{dt} = \frac{-V_{o}}{L}$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{(1-D)T} = \frac{-V_o}{L}$$



$$\Rightarrow \left(\Delta i_L\right)_{\text{opened}} = \left(\frac{-V_o}{L}\right)(1-D)T$$

$$v_L = L \frac{di_L}{dt} \quad \Rightarrow \quad i_L(t) = \frac{1}{L} \int_{\tau} v_L \cdot d\tau$$

$$i_C = C \frac{dv_C}{dt} \quad \Rightarrow \quad v_C(t) = \frac{1}{C} \int_{\tau} i_C \cdot d\tau$$



So the change of i_L over one period must be zero

$$\left(\Delta i_L\right)_{\text{closed}} + \left(\Delta i_L\right)_{\text{opened}} = 0$$

$$\left(\frac{V_d - V_o}{L}\right) DT + \left(\frac{-V_o}{L}\right) (1 - D)T = 0$$

$$V_o = DV_d$$

eqn 7.3

Neglecting circuit losses, input power = output power

so
$$V_dI_d = V_oI_o$$

$$\frac{I_o}{I_d} = \frac{V_d}{V_o} = \frac{1}{D}$$

eqn 7.4



- Filter design
 - We want to smooth output voltage



Filter design

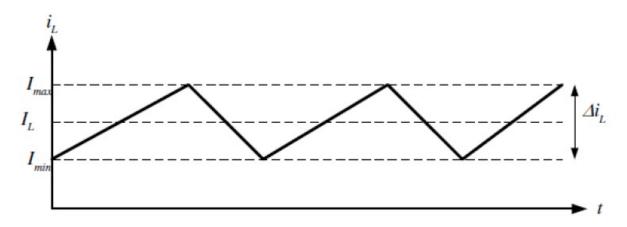
- We want to smooth output voltage
- Need to consider tolerable limits (user defined)
- Typically communicated as a percentage
- CCM, inductor ripple must be positive (also usually defined)



- Filter design
 - We want to smooth output voltage
 - Typically communicated as a percentage
 - CCM, inductor ripple must be positive (also usually defined)
 - Equations usually give you exact values assuming ideal...
 - Must size for realistic conditions



Maximum, Minimum and Average Inductor Current



Average inductor current = average current in RL

$$\Rightarrow I_L = R_L = \frac{V_o}{R}$$

Maximum and minimum currents:

$$I_{\text{max}} = I_L + \frac{\Delta i_L}{2} = \frac{V_o}{R} + \frac{1}{2} \left(\frac{V_o}{L} (1 - D)T \right)$$

$$I_{\text{min}} = I_L - \frac{\Delta i_L}{2}$$

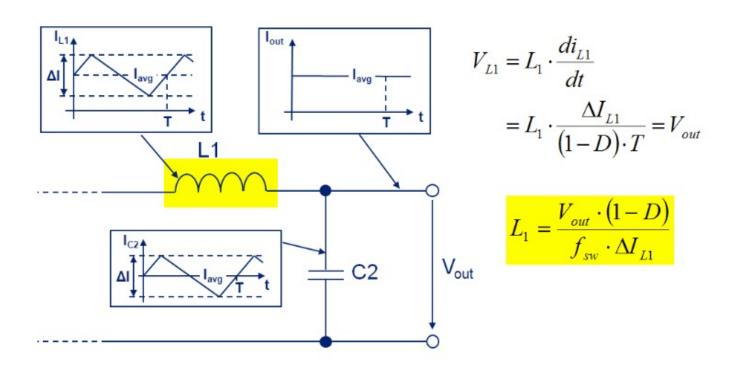
$$= V_o \left(\frac{1}{R} + \frac{(1 - D)}{2Lf} \right)$$

$$= V_o \left(\frac{1}{R} - \frac{(1 - D)}{2Lf} \right)$$

$$\begin{split} I_{\min} &= I_L - \frac{\Delta i_L}{2} \\ &= V_o \left(\frac{1}{R} - \frac{(1-D)}{2Lf} \right) \end{split}$$



- Filter design



- Filter design

$$L = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN} \cdot f_{sw} \cdot \Delta I_L}$$

$$L_{1} = \frac{V_{out} \cdot (1 - D)}{f_{sw} \cdot \Delta I_{L1}}$$

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 - Capacitor needs to keep a constant output voltage
 - ESR and capacitance influence ripple
 - Should select low ESR capacitors



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$$C_{out} = \frac{I_{L(max)}^2 L}{(V_o + V_{os})^2 - V_0^2}$$

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 - Capacitor needs to keep a constant output voltage
 - ESR and capacitance influence ripple
 - Should select low ESR capacitors
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- Should also have an input capacitor to reduce switching noise
 - We are more concerned with output filter in the course



- Filter design
 - Inductor

$$L = \frac{V_O(1-D)}{f_{sw}\Delta I_L}$$

- Capacitor

$$C_{out} = \frac{I_{L(max)}^2 L}{(V_o + V_{os})^2 - {V_0}^2}$$