ECEN202 Test 21 August 2014

Total = 50 Maximum time allowed: 75 minutes

Name……. Student No…….

Attempt all questions. Please use the page to the left of the questions to continue when needed. An extra page is provided at the back.

1. Simplify the following expressions using Boolean algebra:

$\overline{A}.B.C + A.\overline{B}.\overline{C} + \overline{A}.\overline{B}.\overline{C} + A.\overline{B}.C + A.B.C$ (4)

2. Use the Karnaugh map below to minimise the following sum-of-products expression:

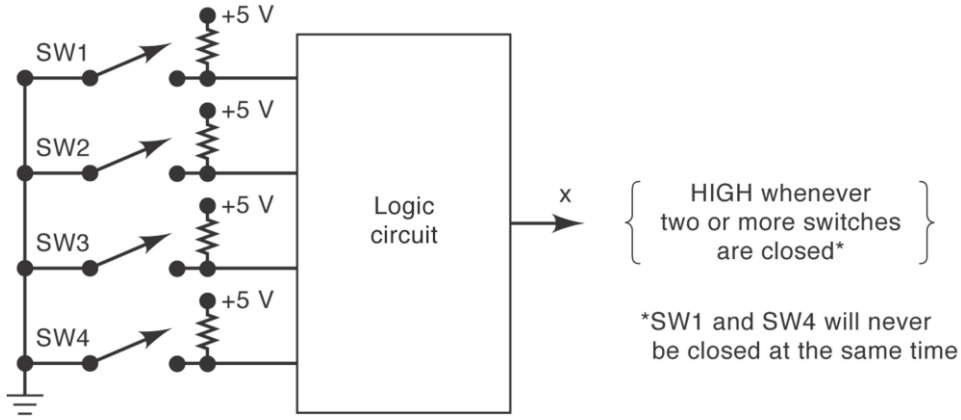
$\overline{B}.\overline{C}.\overline{D} + \overline{A}.B.\overline{C}.\overline{D} + A.B.\overline{C}.\overline{D} + \overline{A}.\overline{B}.C.D + A.\overline{B}.C.D + \overline{A}.\overline{B}.C.\overline{D} + \overline{A}.B.C\overline{D} + A.B.C.\overline{D} + A.\overline{B}.C.\overline{D}$ (6)

	/C/D	/C D	C D	C/D
/A/B				
/A B				
A B				
A/B				

3. The diagram below shows four switches that are part of the control circuitry in a photocopy machine. The switches are at various locations along the path of the copy paper. Each switch would be normally open and as the paper passes over a switch, the switch closes. It is impossible for switches SW1 and SW4 to be closed at the same time. You now need to design a logic circuit to produce a HI O/P whenever two or more switches are closed at the same time. Do this by:

(i) Drawing up a truth table that relates the O/P, X, to the state of the four switches.
(ii) Use a Karnaugh map to produce a simplified logic equation.
(iii) Sketch a logic diagram for a circuit to implement this function.

(10)



4. Explain what we mean by "current sourcing" and "current sinking" for a digital IC driving subsequent logic gates. Assume a totem pole TTL output configuration and use simple sketches to explain the direction of current flow for each of the two cases. Use the attached data sheet of the 74LS04 inverter and determine the maximum current that can flow in each case. (5)

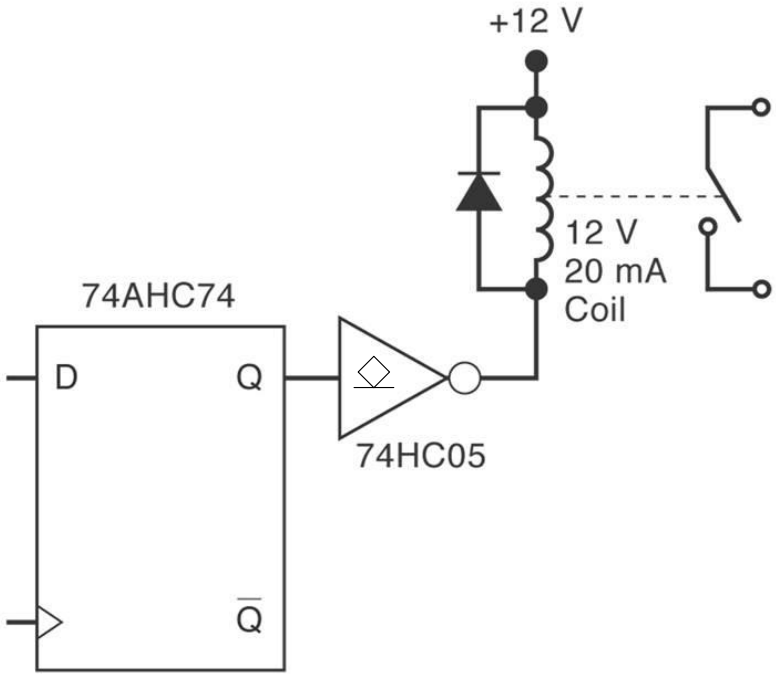
5. Show how PMOS and NMOS transistors can be combined to produce a CMOS tri-state inverter. The ENABLE input should be an active HI, i.e. when this input is HI the device will function as a normal inverter, and when it is LO the device will be in the high-Z state. (5)

6. Show how an edge triggered J-K flip-flop can be constructed from a basic NAND S – C latch. Also show the design of the edge detector circuitry for the detection of a negative-going transition. (5)

7. (i) Sketch the design of an asynchronous four-bit up counter using J-K flip flops. (3)

(ii) The data sheet for the J-K flip flop gives values of t_{PLH} = 16 ns and t_{PHL} = 24 ns. Calculate the maximum frequency that can be reliably used on your counter. (2)

8. (NOT DONE 2019)The following circuit is used to switch a relay (an electromechanical switch) on or off. Study the circuit and answer the following questions. (The 74HC74 is a D flip-flop and the 74HC05 is an open-drain inverter)



(i) What sequence of logic events would be necessary to activate and deactivate the relay ? (2)
(ii) Why do we not connect the relay directly to the output of the D flip-flop ? (2)
(iii) What is the purpose of the 74HC05 in the circuit ? How does it solve the problem(s) in (ii) ? (2)
(iv) What is the purpose of the diode in the circuit ? Is the polarity of the diode correct ? Explain. (2)
(v) Switching on the relay can also simply be achieved with the correct logic level on the inverter, eliminating the flip-flop. Give a reason why the designer may have wanted to use the D flip-flop in this circuit. (2)

****End of Test****