**Eitan Lukin**

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**SKILLS AND QUALIFICATIONS**

* **3+ years of VLSI Backend Circuit Design experience at Intel Corporation in Intel Big Core.**
* **2 years of Logic Design at NextSilicon (System Verilog, worked with 3rd party IP’s).**
* **Highly experienced in creating infrastructures from scratch to process and analyze data (Python).**
* **Product Owner and Group Representative in lead engineers’ forum (FUB Forum) at Intel Corp.**
* Final B.Sc. project included **front end implementation of DEFLATE algorithm (LZ77 + Huffman Encoding).**
* Experienced in: Python, System Verilog, multiple UNIX scripting languages. Familiar with: C, C++
* Multicultural (lived in Argentina, Venezuela, USA, and Israel) and fluent in English, Spanish, and Hebrew.

**WORK EXPERIENCE**

2019-2020 Logic Design **– NextSilicon.**  Tel-Aviv, Israel

* **Logic design of various blocks in design.**
* Provide automation for TTM improvements in accordance with SIRC (Samsung Israel Research Center) methodology.

2019-2019 Logic Design **– Samsung Electronics, SIRC**  Tel-Aviv, Israel

* **Create logic blocks for real-time image processing and noise reduction for Samsung Image Sensors.**
* Provide automation for TTM improvements in accordance with SIRC methodology.

2017-2018 **FUB Forum and Product Owner –** Intel Corporation, Intel Big Core Haifa, Israel

* **Member of lead engineers’ forum (FUB Forum) and product owner of central flow used worldwide at Intel.**
* Representative of Execution Cluster and a core leader in central partition runs.
* Advise and consult in matters of TFM (Tool Flow Methodologies).
* Perform large scale analysis on Core level simulations – includes developing in **python** for process automation.
* Assisted in core level analysis for interconnect capacitance improvements on metal layers.

2015-2018 **Circuit Designer –** Intel Corporation, Intel Big Core Haifa, Israel

* Full BE flow including Circuit Implementations, Logic Verification, STA, Reliability Verification, Noise, DRC, etc.
* Implemented, verified and signed off several partitions in **High Speed Environment** for **4 generations** of Intel Core products (7th Generation, 8th Generation and more).
* Design partitions with highly intricate logic (core execution units) and large memory units (static arrays).
* **Lead numerous studies** on group level activities including: top-down collateral effects on signal integrity of all partitions, cycle time change analysis for all partitions, and assist in the development of in-house design tools.

### Education

2012-2017 **Technion, Israel Institute of Technology** Haifa, Israel

**Bachelor of Science, Faculty of Electrical Engineering – Software and Computer Engineering**

* **Final project** was conducted in the field of VLSI (block diagram to GDSII) and involved implementing the **DEFLATE** compression algorithm. Industry standard results were achieved and verified with Calgary Corpus.
* Member of 2015 Technion Israel Institute of Technology Dean’s Delegation to the United States.

### Military SERVICE (IDF)

2009 **Air Force Academy**

2010-2012 **Armored Corps.**

Main Battle Tank gunner, radio communications operator for 9th Battalion (401st Brigade) commander and deputy commander; Rank at discharge: Staff Sergeant.