E151 - Design Project 2

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Goals:

- **Design a gain stage for an op-amp (featuring active loading!)**
- **Connect differential, gain, and output stages to create a functional op-amp**
- **Explore stability of our constructed amplifier**

Data for this project can be viewed on the following spreadsheet:
https://docs.google.com/spreadsheets/d/1KRs_CRuB5lPmXmJWg6F44qMbzHGFOkDwtSLigfG3_b0/edit?usp=sharing

Note: In all experimental scope traces, yellow traces correspond to input and green traces correspond to output

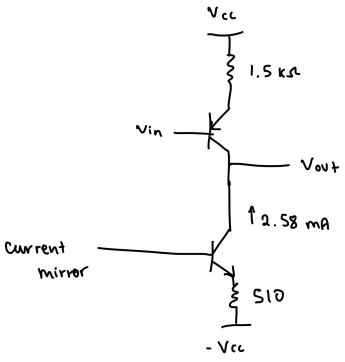
Overview:
When constructing the op amp, we had the following required design specifications:

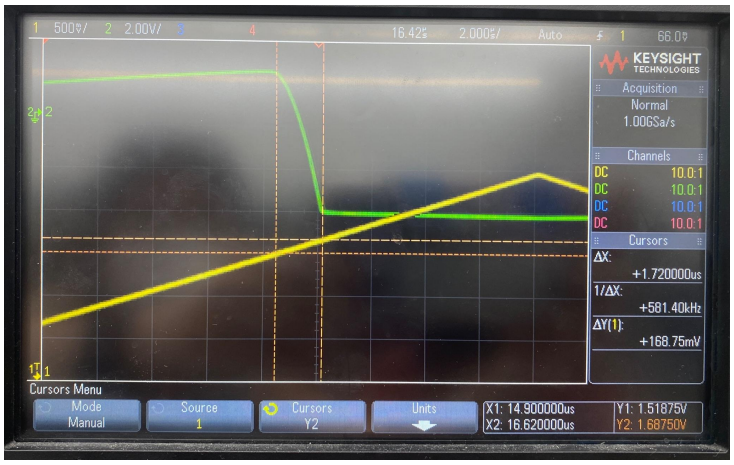
- Open loop gain of 50 or higher
- Use a +6V to -6V supply rail
- Be able to operate with DC input voltages

For our op amp design, we chose to use our differential stage from lab 9 and class AB output stage from lab 10. So, to complete our design, we needed to create a gain stage and figure out how to bias it appropriately to connect all three stages. Once our design was complete, we validated the design by looking at the gain stage and the open loop gain/stability. We then looked at unity gain, non-inverting gain, slew rate, step response time constant, steady state error, and the maximum capacitive load of our amplifier.

Setup, Gain Stage Design:
For our gain stage, we chose to use an actively loaded common emitter with degeneration (active loading yayyyyyy). Our design used a pnp transistor, and the current was biased using the current mirror from our differential stage.

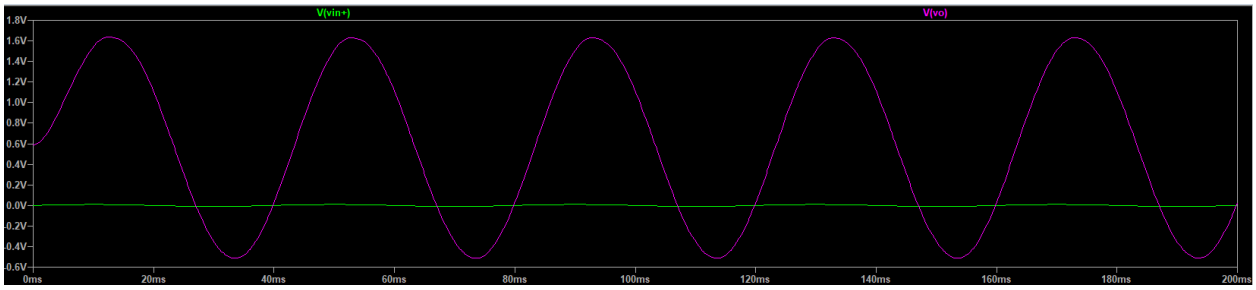
To select the emitter's resistor value, we started by looking at the expected bias point of the differential stage. Based on a mirror current of 2.58mA and a 3.9kΩ resistor, we expected the output to be biased around 1V, since we expected about 1.28mA going through the resistor. So, we chose a 1.5kΩ resistor for our emitter to be above 1.7V (6V - (1.5kΩ)(2.58mA)). However, since we were actively loading the gain stage, the gain stage had a small acceptable input swing range. So, we chose to create a transfer characteristic by using a ramp input. The resulting transfer characteristic is shown below:





After testing this approach, we realized that it would be difficult to appropriately bias the voltage to properly amplify the input, as the gain stage would also be influenced by the other stages since there were no coupling capacitors between the stages. So, we changed our approach to using simulation to determine what resistor would properly bias the gain stage. We started by using a parameter sweep across the gain stage, ranging from 1kΩ to 2kΩ. Based on the sweep

results, we found that a 1620Ω resulted in a gain stage that appropriately amplified the signal. The plot below shows the simulated result:

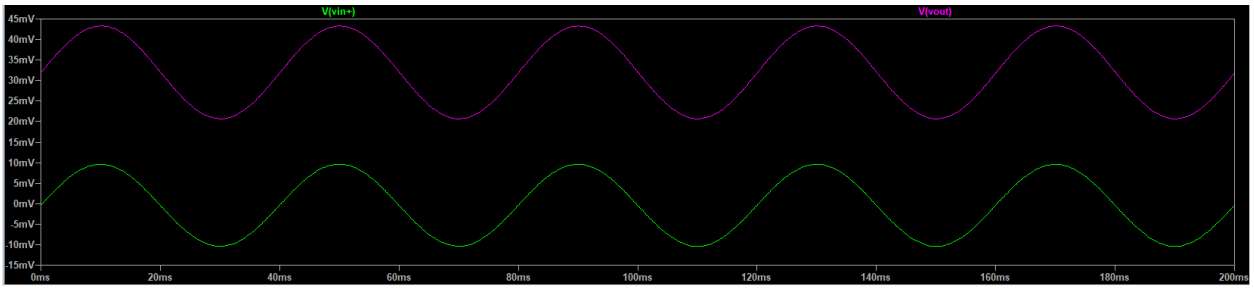


We decided that when building the gain stage, it would be best to use a potentiometer so that we could adjust it until we saw amplification. We chose to use a 1kΩ potentiometer in series with an 820Ω resistor, so we would have a reasonable resistor range to test with.

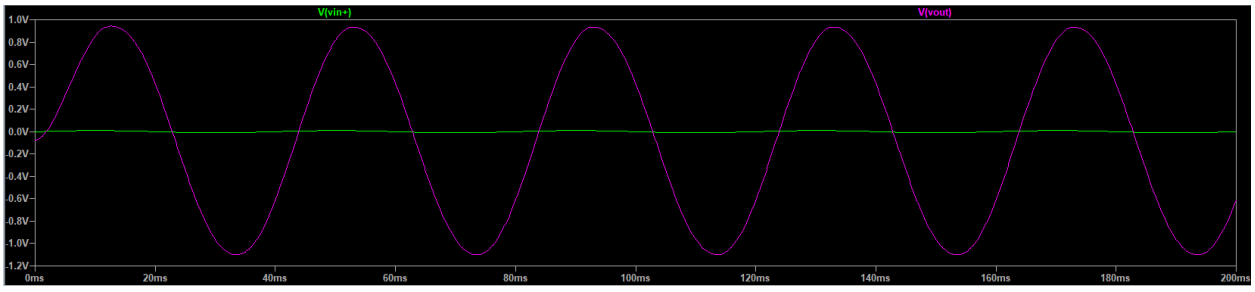
Additional Modifications:

After verifying in simulation that the gain stage functioned properly, we connected the output stage. We immediately noticed that when scoping the output, the signal was no longer amplified. To fix this problem, we included an emitter follower buffer with a 3.9kΩ emitter resistor in between the gain stage and output stage.

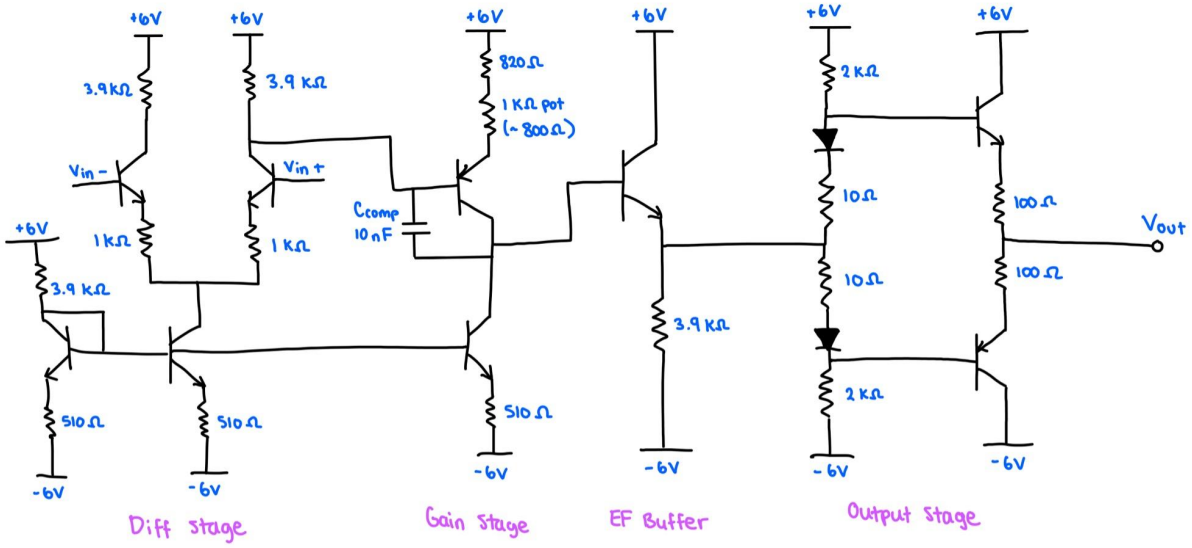
Without buffer:



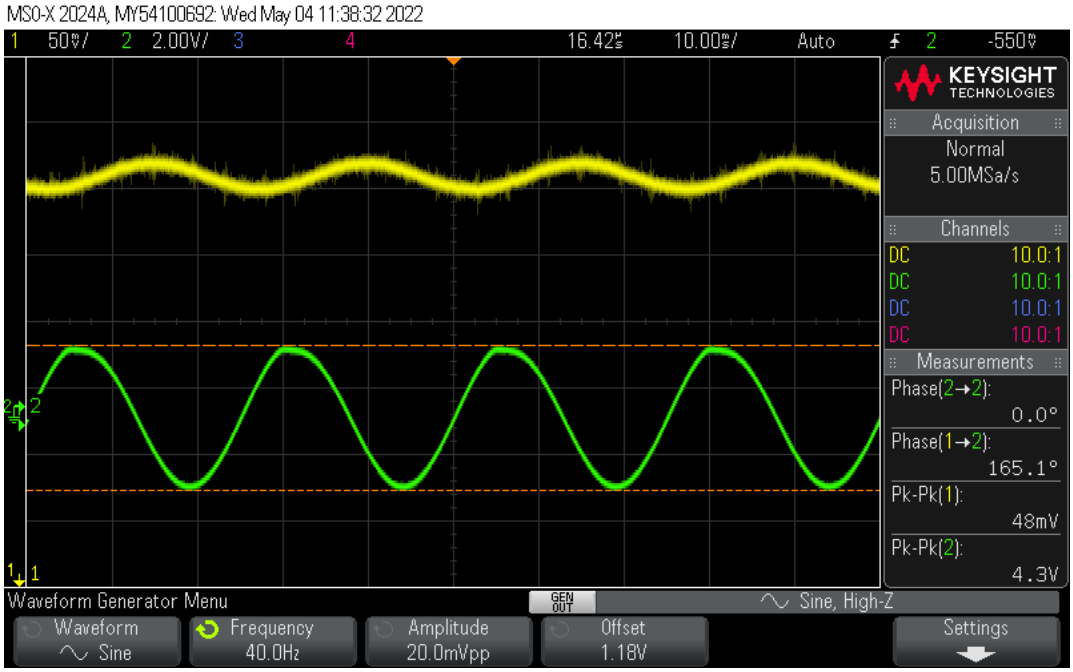
With buffer:



Circuit Schematic:
Below is a drawing of our overall op amp schematic



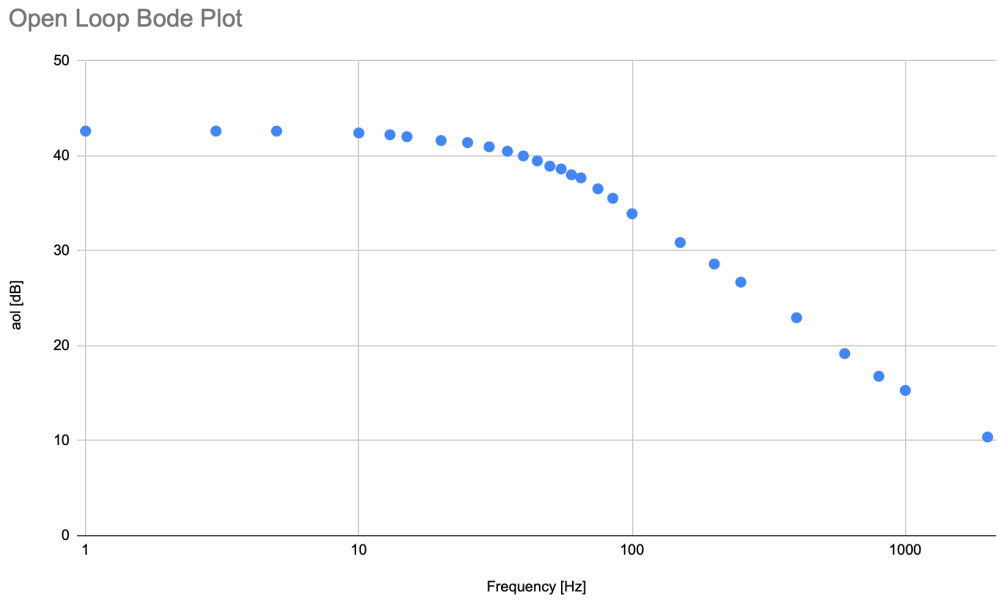
Verifying Gain Stage:
The first thing we did experimentally was test the op amp's gain stage. We did this by inputting a signal at the base of the pnp and scoping the input and output of the gain stage. We included an offset in our input signal to model the DC coupling that would occur due to the other stages. Based on the scope trace shown below, the gain stage successfully amplified the DC coupled input signal and had a gain greater than 50.



Open Loop:

Bode Plot/Verifying Design Spec:

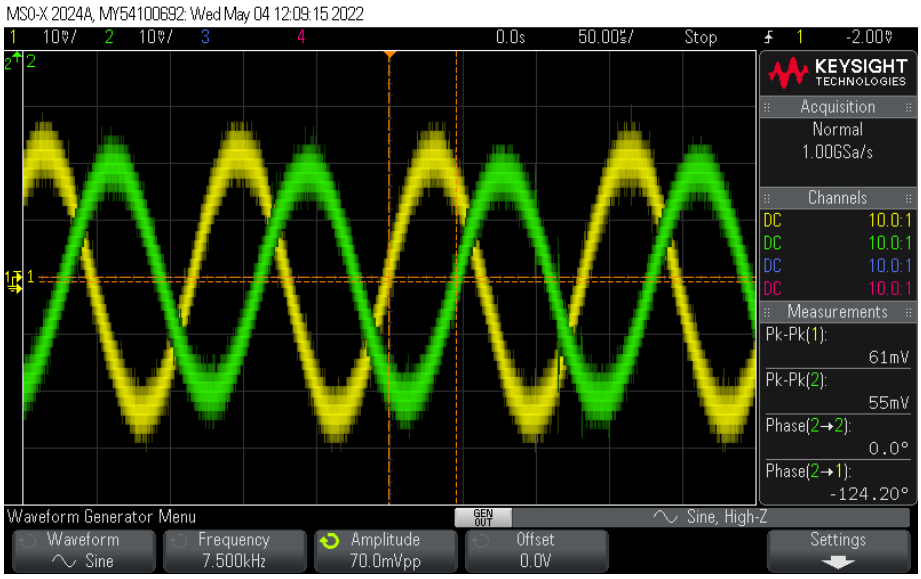
To measure the open loop gain, we first grounded the inverting input of our op amp and connected the function generator to the non-inverting input. We added an attenuating resistor to the input because we did not want the output signal to be clipped. To determine the resultant input amplitude when using a 20mVpp signal, we measured the attenuation factor by using a large input signal and scoping the corresponding input signal. We then took measurements of the input and output peak to peak values and calculated the resulting gain. Because of the 10nF compensation capacitor, we expected the dominant pole of the open loop response to be at a very low frequency. So, we made our bode plot by taking input and output measurements starting from a 1Hz frequency



The bode plot's behavior matched what we were expecting. There was a dominant pole at about 45Hz. Based on the constant gain we observed from 1Hz to 10Hz, we found the open loop gain to be approximately a_{ol} = 42.548dB = 134. So, we verified that our op amp design satisfied the design parameter of having an open loop gain of 50 or higher.

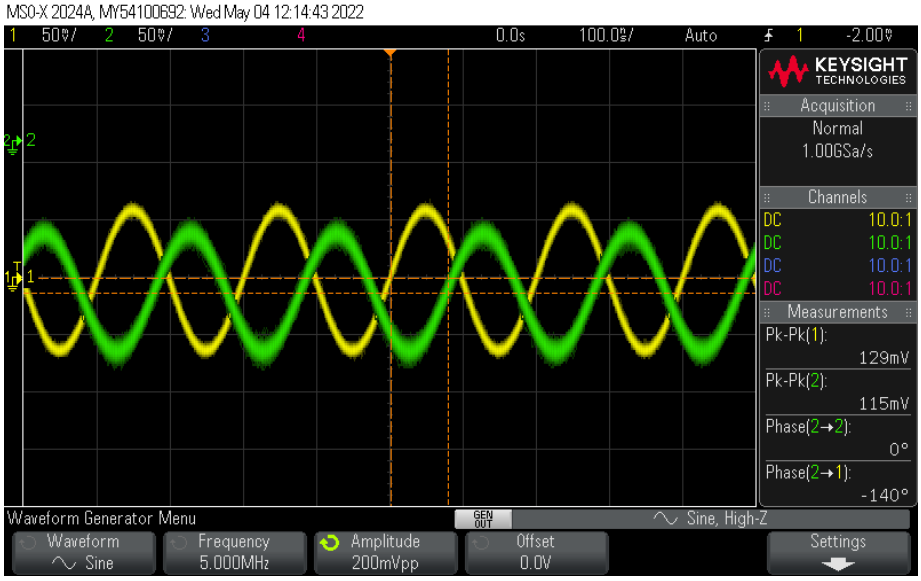
Stability with compensation capacitor:

To check the open loop stability, we increased the input frequency until we saw that the output signal was slightly smaller than the input, indicating that the 0dB gain crossover frequency had been passed. We then used the scope to measure the phase shift, and added 180° to compute the phase margin. Based on the scope measurements picture below, we got an open loop phase margin of 55.8°. Since the phase margin was positive, we verified that the amplifier was open-loop stable.

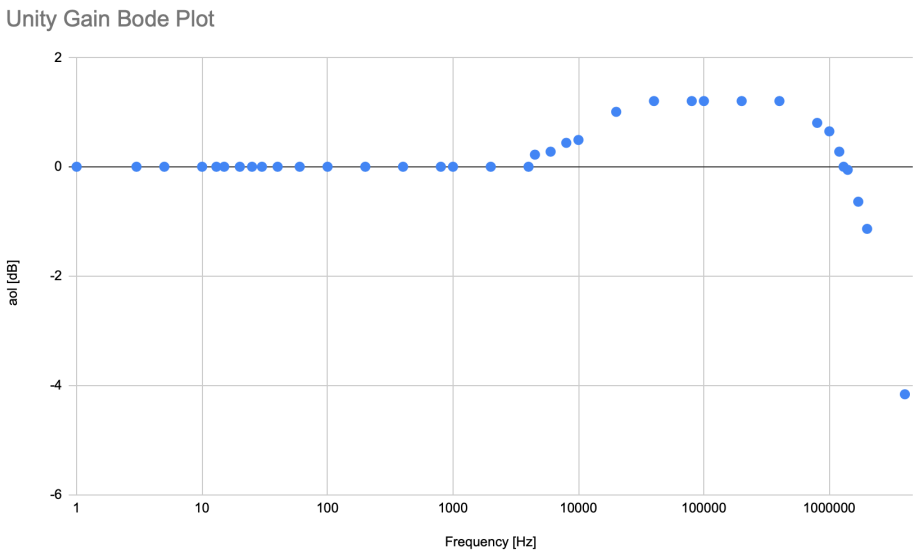


Stability without compensation capacitor:

We removed the compensation capacitor and repeated the process we used previously to determine stability. We observed that without the compensation capacitor, a much larger input frequency was needed to reach the crossover frequency. Based on the scope measurements picture below, we got an open loop without compensation capacitor phase margin of 40°. This phase margin was smaller, but it was still positive. Therefore, even without the compensation capacitor, the op amp was open-loop stable.

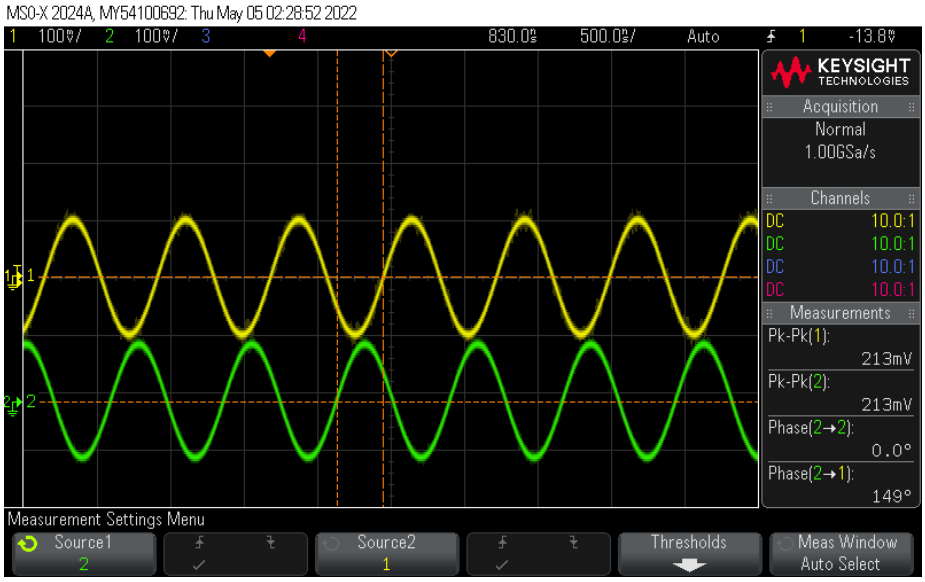


Unity Gain:
To configure our op amp for unity gain feedback, we switched from grounding our inverting input to connecting it to the output of our op amp. We then took input and output measurements to create our bode plot. Based on the definition of a unity gain buffer, we expected the input and output signals to be equal. The unity gain bode plot is below:



Looking at the bode plot, the behavior matched what we expected, with the gain being 1 at lower frequencies.

To assess stability, we looked at the phase shift at a 1.3MHz input frequency, which was the frequency where the gain returned to 0dB. Using scope readings, the phase shift was 149°, which is equivalent to -211°. Based on this phase shift, the phase margin of the unity gain configuration was -31°. Since the phase margin was negative, we concluded that the op amp was not unity gain stable.



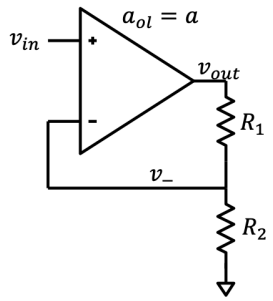
Comparison of Unity Gain to Open Loop :

The peak gain for the open loop Bode plot at 43dB is achieved by lower frequencies in the range tested. The peak gain for the unity gain Bode plot at near 1dB is achieved by higher frequencies in the range tested and indicates the frequencies at which unity gain is not achieved. Overall, the unity gain configuration has a larger range of frequencies (up to 4kHz) where the desired behavior is achieved. In addition, the comparison shows the tradeoffs that come with introducing feedback. While the unity gain configuration controlled the gain well, it also led to instability.

Non-Inverting Gain:

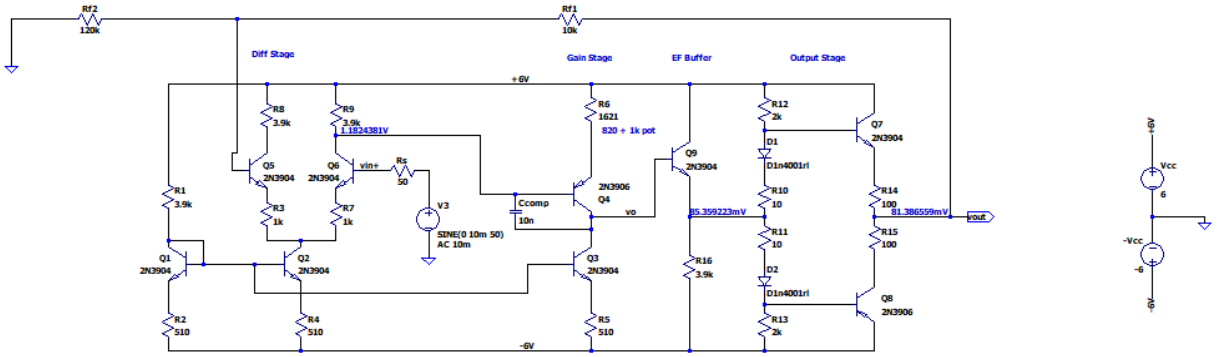
Design:

Since our unity gain feedback configuration was not stable, we configured our op amp for non-inverting gain, using the following setup.

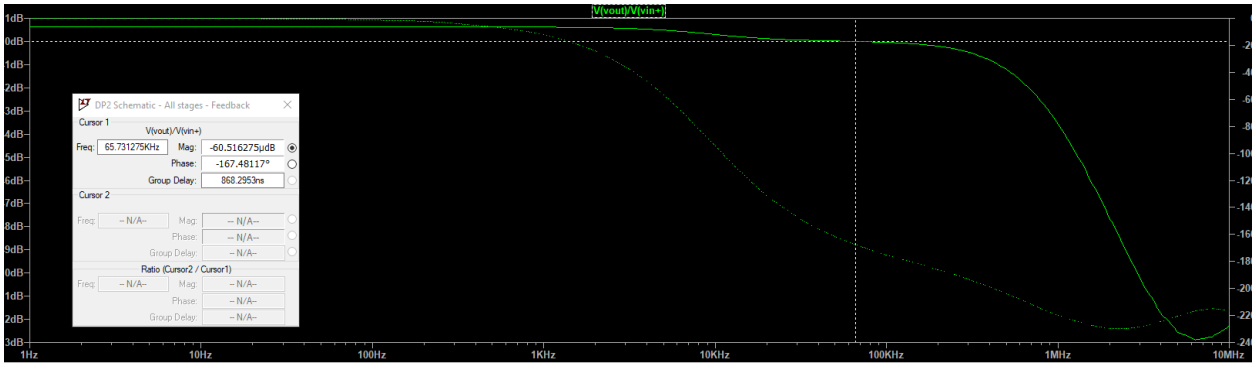


We chose R1 and R2 values that would minimally affect the gain while also shifting the crossover frequency such that the system would be stable. We chose R1 = 10kΩ and R2 = 120kΩ. Before building our non-inverting gain configuration, we tested the design on simulation to verify that it was stable. The simulation results are shown below:

LTspice schematic:

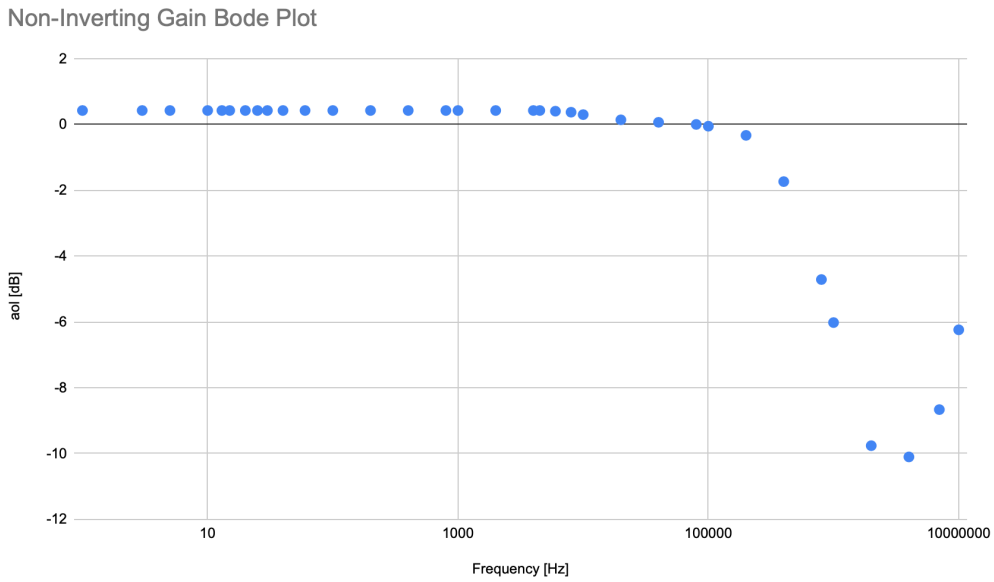


Bode plot:



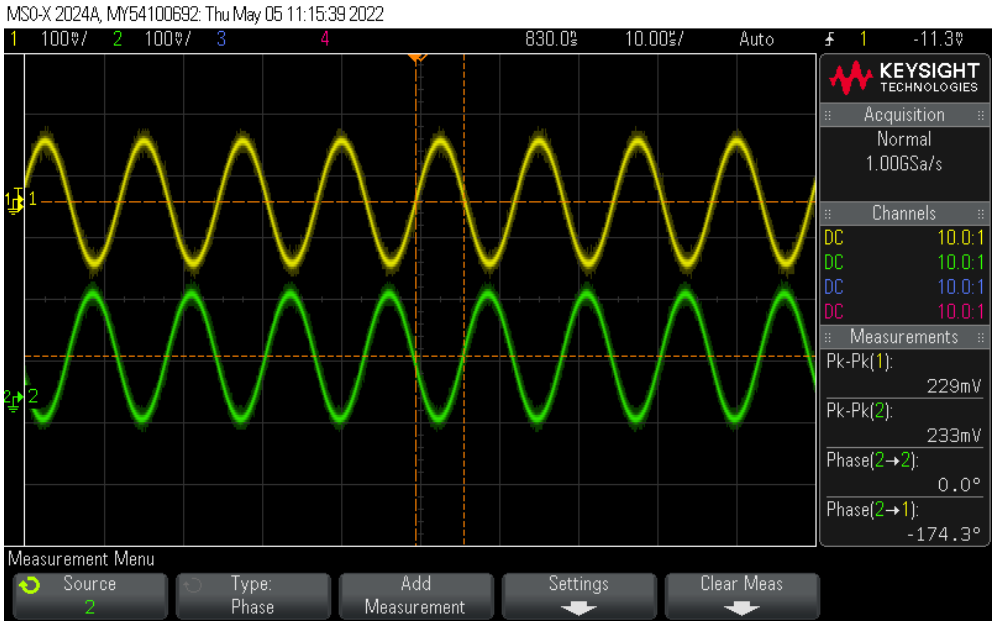
Based on the simulation, the phase margin of the feedback system was approximately 12.52°, verifying that it was closed loop stable.

Experimental:
We repeated our previous process, taking input and output measurements to create a bode plot for the non-inverting gain amplifier.



The bode plot behavior matched that of the simulated response, with the gain being slightly above 0dB. An interesting observation we made was that there was a high frequency pole present, which we will discuss further when looking at the step response.

To assess stability, we looked at the phase shift at a 80kHz input frequency, which was the frequency where the gain reached 0dB. Using scope readings, the phase shift was -174.3°. Based on this phase shift, the phase margin of the non-inverting gain configuration was 5.7°. Since the phase margin was positive, we had proof of stability in feedback.

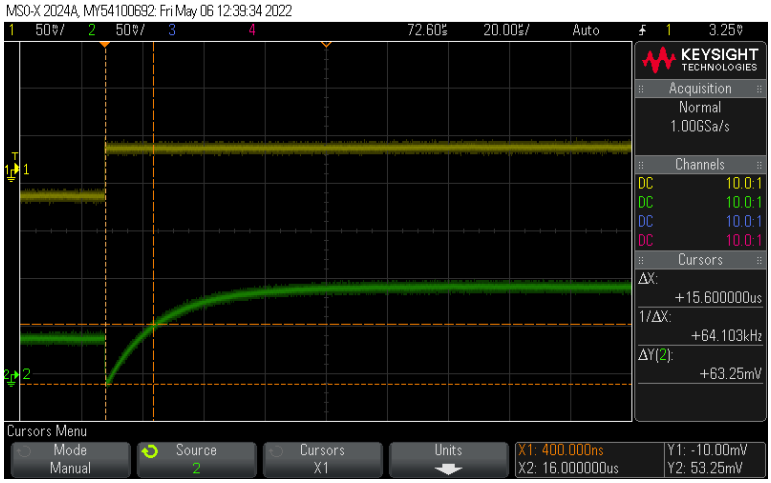


Closed Loop Step Response Overview:
To determine the time constant and steady state error, we used a small input amplitude. To determine the slew rate, we used a large input amplitude.

Time constant:
Analytical:
To compute the time constant, we looked at our non-inverting gain bode plot to determine the frequency of the dominant pole. We estimated the pole to be at approximately 10kHz. Using the dominant pole's frequency, we calculated the expected time constant as:

$$\tau = \frac{1}{2\pi(10000\ Hz)} \simeq 15.91\mu s$$

Experimental:
To measure the time constant, we used a small signal input amplitude. The first thing we noticed when looking at the step response was the sudden downward spike. We attributed this behavior to the high frequency pole that our feedback has, which we found when creating our bode plot for the non-inverting amplifier. To determine the time constant, we looked at the response that occurred after the fast high frequency pole response, using the cursors to determine the time it took for the response to reach 63% of its steady state value. Our experimental results returned a time constant of τ = 15.6μs.



Comparison:
The expected vs measured results matched reasonably well, with a <2% error.

SSE:

Analytical:

To calculate the expected steady state error, we used the following expression,

$$\epsilon_{ss} = (\frac{1}{f} - \frac{v_{out}}{v_{in}})f$$

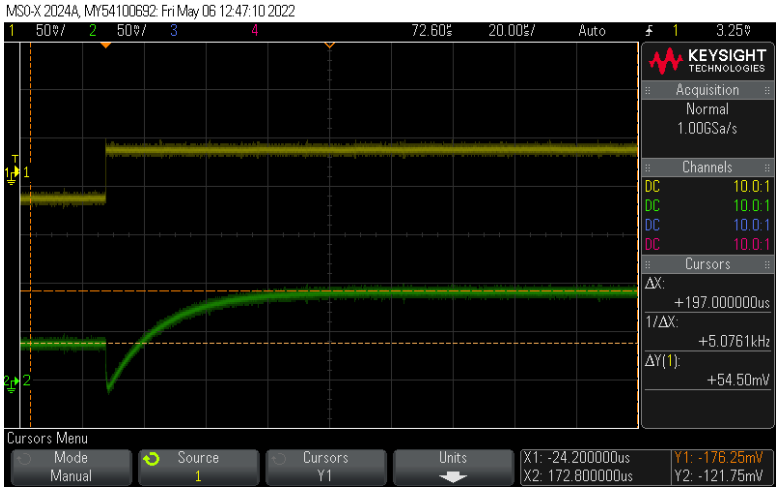
In this expression, $\frac{v_{out}}{v_{in}} = 1.05$, the gain of of non-inverting amplifier, and

$f = \frac{R2}{R1+R2} = \frac{120000}{130000} \simeq 0.923.$

Plugging in our parameters, we find the expected steady state error to be ϵ_{ss} = 3.08%.

Experimental:

To measure the steady state error, we look at the same step response that we used to determine the time constant. We measured the peak to peak amplitudes of the input and output signals, and then computed the error between them. When measuring the output signal, we did not include the drop that was due to the high frequency response, since it would not be present if a low pass filter was included. Based on the measured amplitudes, we got an experimental steady state error of ϵ_{ss} = 6.34%.



Comparison:

The measured steady state error is approximately double the error we expected. However, due to experimental limitations in how precise our measurements were, this appears to be reasonable. For example, our calculations used an input of 51.25mV$_{pp}$ and an output of 54.5mV$_{pp}$. Were we to have instead used an output of 53mV$_{pp}$, this would have decreased the steady state error to 3.41%.

Slew Rate:

Analytical:

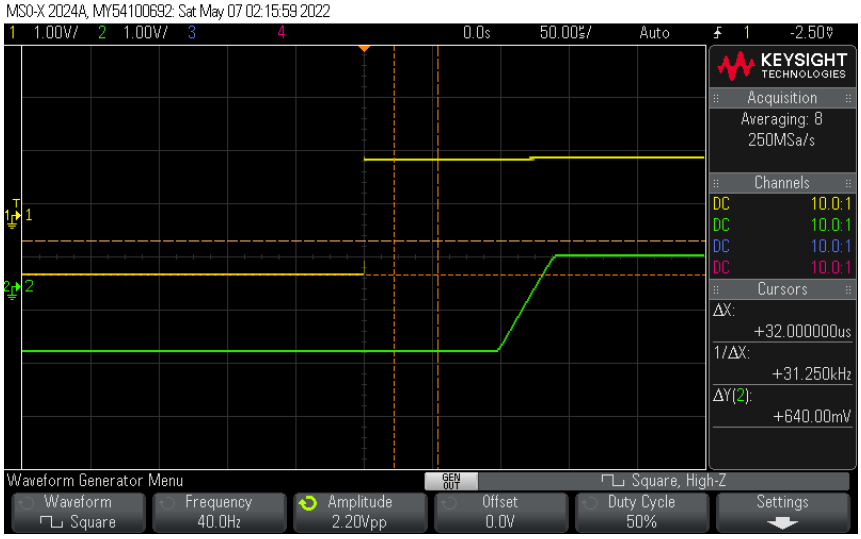
To calculate the expected slew rate, we used the following expression,

$$SR = \frac{I_{mirror}}{C_{comp}}$$

Based on this expression, we calculated the slew rate to be SR = 256818 V/s. We used the compensation capacitance of 10nF and the mirror biasing current of 2.568mA.

Experimental:

In order to be able to observe slewing, we used a large signal input amplitude. The observed step response had a linear rising edge, which was different from the behavior we saw with the small signal input. To determine the experimental slew rate, we measured the slope of the response's rising edge. From this, we found the experimental slew rate to be SR = 20000 V/s.



Comparison:

The experimental slew was significantly smaller than what we expected, being about 2/25 of our expected slew rate. We believe that this can be attributed to the limiting factor of the input's response. Since the input response does not spontaneously jump to its peak value, the slew rate is limited. For sanity check, we measured the gain stage's bias current while the op amp was slew rate limited. We found the current to be 2.58mA, which reasonably matched the current we used in our analytical calculation.

Max Capacitive Load:

Analytical:

In Mastery Problem 12a, we derived the following expression for maximum capacitive load,

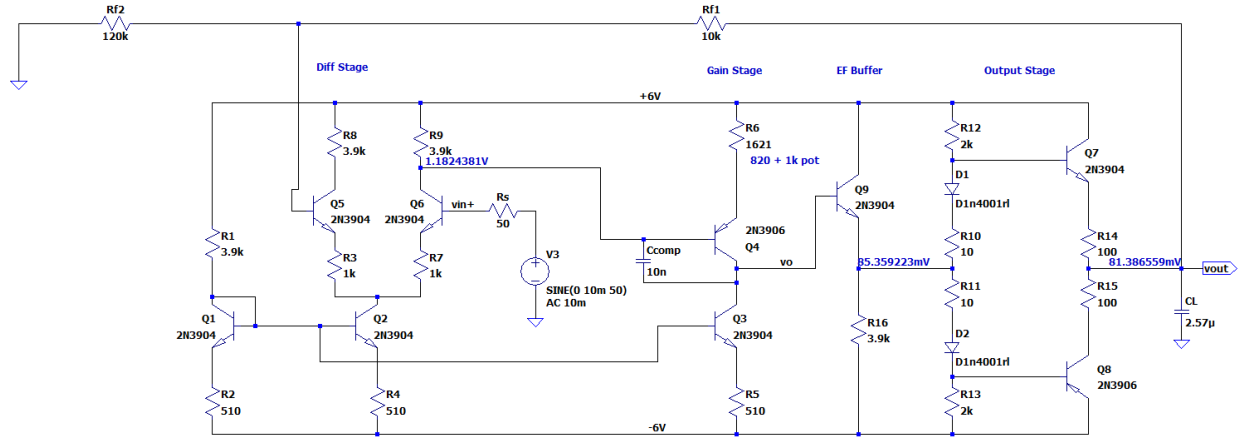
$C_{L,max} = \frac{100\tau}{r_{out} a_{ol} f}$, using the assumptions R1 + R2 << r_{out} and $r_{out}C_L$ << τ

Plugging in our values, using our experimental a_{ol} and expected τ, we find the analytical maximum capacitive load to be $C_{L,max}$ = 0.257μF.

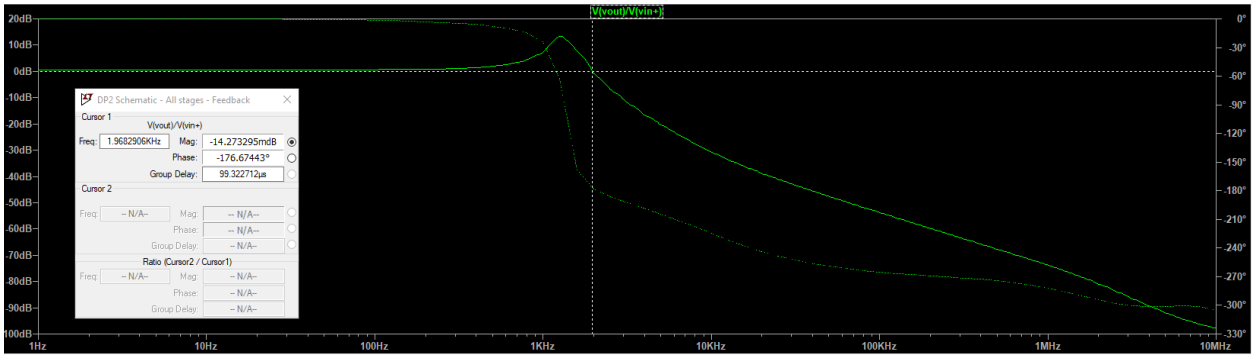
Simulated:

To verify our calculation, we first simulated the bode plot with the 0.257μF load capacitor on LTspice. We wanted to check the stability of the amplifier and assess that if it was stable, how close was it to becoming unstable. Based on the simulated bode plot, a 0.257μF load capacitor resulted in a phase margin of <3°, which is really close to the 0° phase margin stability limit. Therefore, we were satisfied with our chosen $C_{L,max}$ value.

LTspice schematic:

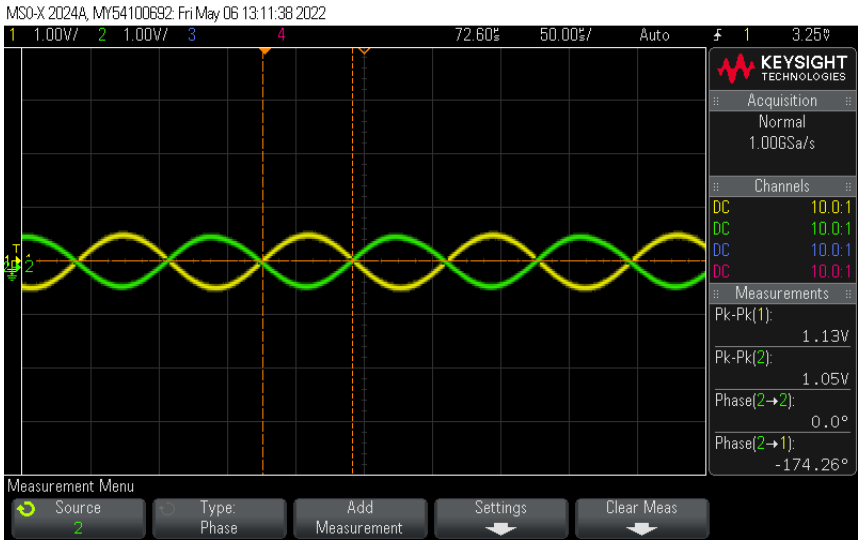


Bode plot:



Experimental:

For experimental purposes, we choose to round down to $C_{L,max}$ = 0.25μF. To test our maximum capacitive load, we chose to create a 2.5μF by connecting four 1μF capacitors in series, connecting the load capacitor from the output to ground. We then tested the stability, repeating the process we've used throughout the project. Using scope readings, the phase shift was -174.36°. Based on this phase shift, the phase margin of the non-inverting gain configuration was 5.64°. Since the phase margin was positive, we had proof of stability in feedback with our capacitive load. We also verified that with a load of 0.25μF, the phase margin was <10° away from being unstable, confirming that 0.25μF was nearing instability.



Commentary on $C_{L,max}$:

The maximum capacitive load is in the appropriate range for the circuit. It is because Anuragini said so.