PSEC4A

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Overview

This document provides an overview of the PSEC4A ASIC designed in late 2016 and early 2017 and submitted for fabrication on a MOSIS 0.13 μm CMOS MPW in February, 2017. The PSEC4A ASIC is intended for the 'analog down-conversion' of wide-bandwidth ($\sim$2 GHz) analog signals, achieved through fast sampling (1-11 gigasamples-per-second [GSPS]) followed by a relatively slow digitization and readout process ($\mathcal{O}$100 MHz). Thus, PSEC4A requires a trigger signal to capture the signal-of-interest, either from an external source or generated using the PSEC4A internal discriminators.

The PSEC4A has 8 signal input channels. Each channel has 1056 samples, which are randomly addressable in blocks of 132 samples. The sampling rate is set by an external clock input, which is locked on-chip using a delay-locked loop (DLL). When successfully locked, one input clock period spans the primary sampling array and the sampling rate is equal to 132*f, where f is the input clock frequency.

Features

- **'Fast' and 'Slow' DLL modes to allow a wide range of stable sampling rates, from $\sim$1 GSPS to 11 GSPS.**
- **Improved input coupling to extend analog bandwidth**
- **Simultaneous sampling / digitization / readout functionality to reduce dead-time induced latency**
- **Multi-buffering via addressable switched-capacitor banks.**
- **On-chip 10-bit DACs for biases and thresholds**
- **Each channel with a threshold-level discriminator and trigger output pin**
- **11-bit ramp-compare ADC using on-chip 1.5 GHz clock generator**
- **Can be powered through a single 1.2V supply**

Absolute Maximum ratings

spec	max	nominal	comment
Supply Voltage ($\mathrm{V_{dd}}$)	1.5 V	1.2 V	may be possible to increase $\mathrm{AV_{dd}}$ only to increase dynamic range
IO voltage	$\mathrm{V_{dd}}$	1.2 V	Over/under voltage protection diodes on most pins. (**Not** on signal inputs)
Signal range voltage	0-$\mathrm{AV_{dd}}$	0.1-1.1 V	about a 1 V usable range

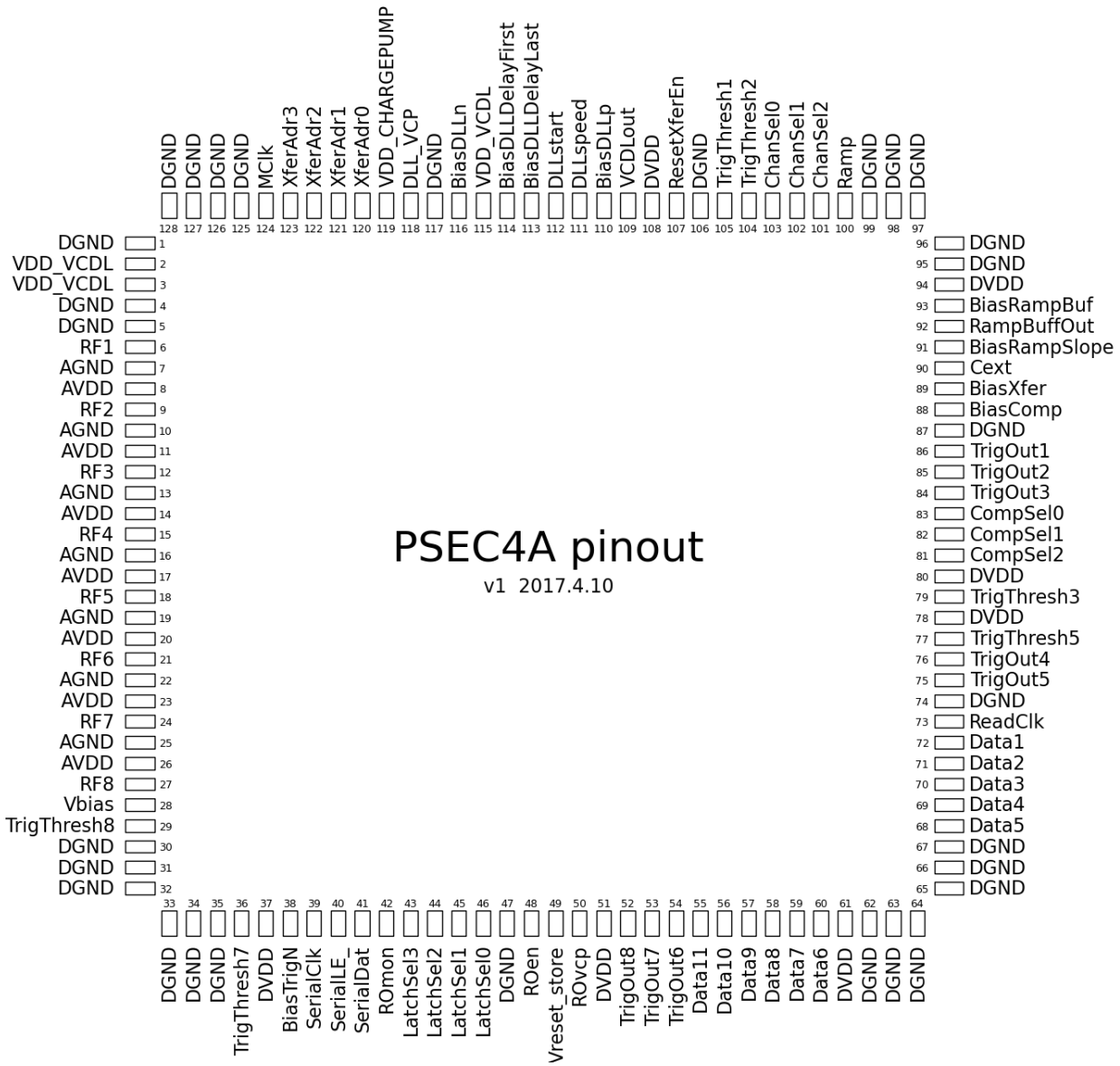

Figure 1: PSEC4A pinout in LQFP128 package

I/O Descriptions

The PSEC4A pinout, as housed in the LQFP128 package, is shown in Figure 1.

Power

The PSEC4A has four separate +1.2 V V_{dd} rails and two GND returns. These can be tied to a single power supply (+1.2 V, GND), but there may (potentially) be performance benefits when taking care to provide some isolation between these rails.

power rail	ref	comment
DV_{dd}	DGND	power rail for digital circuitry
$V_{dd}VCDL$	DGND	power rail for timing generation circuits (VCDL and chip-wide timing drivers)
$V_{dd}ChargePump$	DGND	power rail for DLL feedback circuit
AV_{dd}	AGND	power rail for analog circuits and DACs

It is likely that using a single PCB GND plane for both DGND and AGND will be satisfactory. For a conservative design, it is suggested that:
1) AV_{dd} be generated by a separate regulator
2) $V_{dd}VCDL$ be isolated from the DV_{dd} plane using an appropriate ferrite.
3) $V_{dd}ChargePump$ be independently generated or further isolated from $V_{dd}VCDL$ using a ferrite. $V_{dd}ChargePump$ should draw no more than a couple mA.

Digital I/0s

pin #	pin name	type	description
39	SerialClk	IN	clock for serial interface
40	SerialLE_	IN	Load signal (active low) for serial interface
41	SerialDat	IN	data line for serial interface
43	LatchSel3	IN	Internal latch select decoder, bit 3 (MSB)
44	LatchSel2	IN	Internal latch select decoder, bit 2
45	LatchSel1	IN	Internal latch select decoder, bit 1
46	LatchSel0	IN	Internal latch select decoder, bit 0 (LSB)
45	ROen	IN	Enable fanout buffers for ring oscillator chip-wide ADC clock
52	TrigOut8	OUT	Trigger bit output on channel 8 (may be left open if not using self trigger)
53	TrigOut7	OUT	Trigger bit output on channel 7 (may be left open if not using self trigger)
54	TrigOut6	OUT	Trigger bit output on channel 6 (may be left open if not using self trigger)
55	DataOut11	OUT	ADC data
56	DataOut10	OUT	ADC data
57	DataOut9	OUT	ADC data
58	DataOut8	OUT	ADC data
59	DataOut7	OUT	ADC data
60	DataOut6	OUT	ADC data
68	DataOut5	OUT	ADC data
69	DataOut4	OUT	ADC data
70	DataOut3	OUT	ADC data
71	DataOut2	OUT	ADC data
72	DataOut1	OUT	ADC data
73	ReadClk	IN	Clock for data readout
75	TrigOut5	OUT	Trigger bit output on channel 5 (may be left open if not using self trigger)

76	TrigOut4	OUT	Trigger bit output on channel 4 (may be left open if not using self trigger)
81	CompSel2	IN	Internal comparator select decoder, bit 2 (MSB)
82	CompSel1	IN	Internal comparator select decoder, bit 1
83	CompSel0	IN	Internal comparator select decoder, bit 0 (LSB)
84	TrigOut3	OUT	Trigger bit output on channel 3 (may be left open if not using self trigger)
85	TrigOut2	OUT	Trigger bit output on channel 2 (may be left open if not using self trigger)
86	TrigOut1	OUT	Trigger bit output on channel 1 or the OR of all 8 trigger outputs as selected in the Serial Interface (may be left open if not using self trigger)
100	Ramp	IN	Start ADC ramp
101	ChanSel2	IN	Internal channel select decoder, bit 2 (MSB)
102	ChanSel1	IN	Internal channel select decoder, bit 1
103	ChanSel0	IN	Internal channel select decoder, bit 0 (LSB)
107	ResetXferEn	INOUT	Enable or disable the reset stage of the analog storage caps. Nominally set in the Serial Interface.
109	VCDLout	OUT	Delayed-by-148 samples MClk output (primarly for debugging)
111	DLLspeed	INOUT	Pick fast or slow DLL mode. Nominally set in the Serial Interface.
112	DLLstart	IN	Reset/start DLL
120	XferAdr0	IN	Internal analog transfer address decoder, bit 0 (LSB)
121	XferAdr1	IN	Internal analog transfer address decoder, bit 1
122	XferAdr2	IN	Internal analog transfer address decoder, bit 2
123	XferAdr3	IN	Internal analog transfer address decoder, bit 3 (MSB)
124	MClk	IN	Sampling clock

Analog I/0s

RF inputs

- Pins 6,9,12,15,18,21,24,27 are signal inputs 1 through 8, respectively.
- These are not ESD protected.
- Each signal line should be terminated with the appropriate impedance (typically a 50 ohm 0402 resistor) as close as possible to these inputs.
- Each signal line should be AC coupled before this termination and a DC pedestal bias (between 0.2 and 1.0V) should be applied to the signal-return side of the termination resistor or inductor.

PSEC4A DAC debugging outputs

Most of the analog biases required to run the chip can be generated on-chip with 17 digital-to-analog converters (DAC) that are programmed through the Serial Interface. The DC voltages of most of these DACs are sent to external pads for debugging purposes. If issues arise with the PSEC4A DAC design or Serial Interface, these DAC pins may be over-ridden using a low-impedance buffer amplifier.

This also allows additional decoupling capacitors to be added to these analog levels,if necessary.

The PSEC4A DACs and associated package pins, if applicable, are listed in the following table:

DAC #	DAC/pin name	pin #	description
1	ROvcp	50	Bias voltage for ring oscillator clock speed (V=0 fastest)
2	BiasTrigN	38	Bias voltage for self-trigger discrimators (V=1.2 max current bias)
3	BiasXfer	89	Bias voltage for analog transfer buffer
4	BiasRampBuf	93	Bias voltage for ramp buffer in each cell
5	BiasComp	88	Bias voltage for ADC comparators
6	BiasDllDelayLast	113	Delay tuning for last timing cell
7	BiasDllDelayLast	114	Delay tuning for first sample cell [1]
8	BiasDLLp	110	Tuning voltage for DLL pFET charge pump current
9	BiasDLLn	116	Tuning voltage for DLL nFET charge pump current
10	TrigThresh1	105	Trigger threshold voltage for channel 1
11	TrigThresh2	104	Trigger threshold voltage for channel 2
12	TrigThresh3	79	Trigger threshold voltage for channel 3
13	TrigThresh4	–	Trigger threshold voltage for channel 4
14	TrigThresh5	77	Trigger threshold voltage for channel 5
15	TrigThresh6	–	Trigger threshold voltage for channel 6
16	TrigThresh7	36	Trigger threshold voltage for channel 7
17	TrigThresh8	29	Trigger threshold voltage for channel 8
18	BiasRampSlope	91	Bias voltage to tune the ADC ramp slope

[1] together with BiasDLLDelayLast, this allows the wraparound sample (sample 132 back to sample 1 in the primary sampling array) to be tuned to a specific duration