

# PSEC4A

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## Overview

This document provides an overview of the PSEC4A ASIC designed in late 2016 and early 2017 and submitted for fabrication on a MOSIS 0.13  $\mu\text{m}$  CMOS MPW in February, 2017. The PSEC4A ASIC is intended for the ‘analog down-conversion’ of wide-bandwidth ( $\sim 2$  GHz) analog signals, achieved through fast sampling (1-11 gigasamples-per-second [GSPS]) followed by a relatively slow digitization and readout process ( $\mathcal{O}100$  MHz). Thus, PSEC4A requires a trigger signal to capture the signal-of-interest, either from an external source or

generated using the PSEC4A internal discriminators.

The PSEC4A has 8 signal input channels. Each channel has 1056 samples, which are randomly addressable in blocks of 132 samples. The sampling rate is set by an external clock input, which is locked on-chip using a delay-locked loop (DLL). When successfully locked, one input clock period spans the primary sampling array and the sampling rate is equal to  $132 \cdot f$ , where  $f$  is the input clock frequency.

## Features

- ‘Fast’ and ‘Slow’ DLL modes to allow a wide range of stable sampling rates, from  $\sim 1$  GSPS to 11 GSPS.
- Improved input coupling to extend analog bandwidth
- Simultaneous sampling / digitization / readout functionality to reduce dead-time induced latency
- Multi-buffering via addressable switched-capacitor banks.
- On-chip DACs
- Each channel with a threshold-level discriminator and trigger output pin
- 11-bit ramp-compare ADC using on-chip 1.5 GHz clock generator
- Powered through a single 1.2V supply

## Absolute Maximum ratings

spec	max	nominal	comment
Supply Voltage (Vdd)	1.5 V	1.2 V	may be possible to increase AVdd only to increase dynamic range
IO voltage	Vdd	1.2 V	Over/under voltage protection diodes on most pins. ( <b>Not</b> on signal inputs)
Signal range voltage	0-AVdd	0.1-1.1 V	about a 1 V usable range

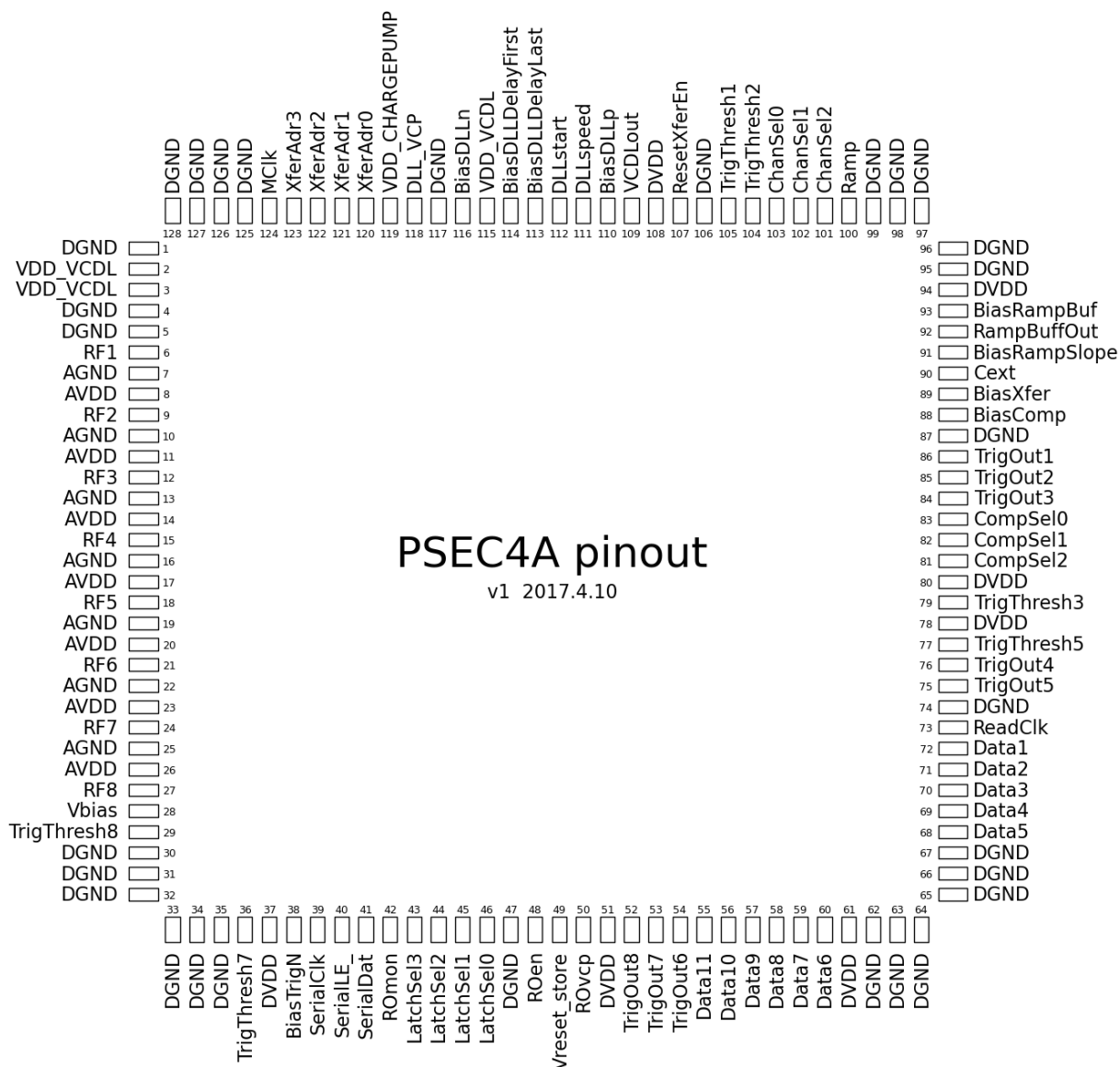


Figure 1: PSEC4A pinout in LQFP128 package

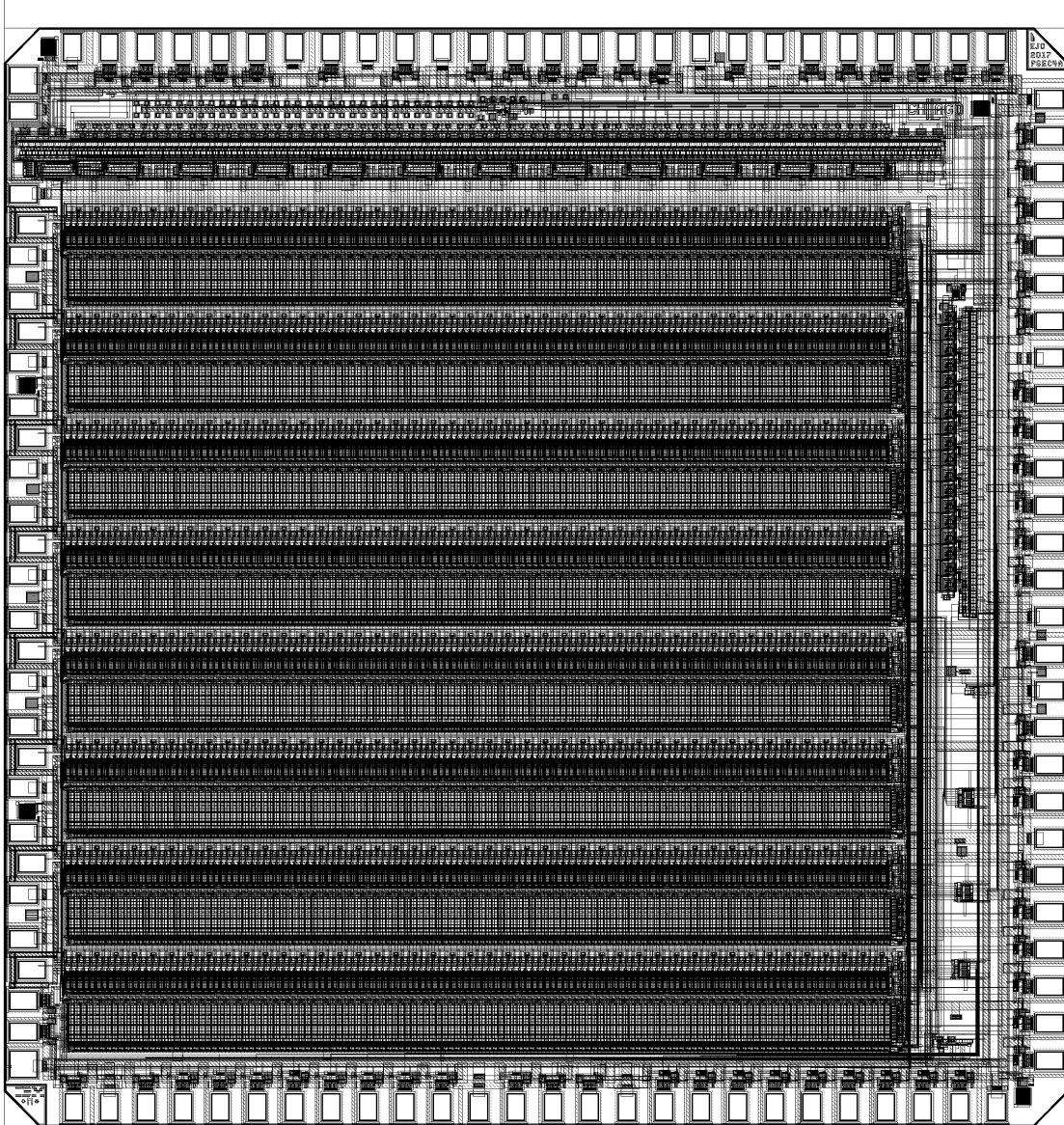


Figure 2: PSEC4a black-and-white layout capture. The die has 107 pads. The layout has an area of  $3800 \times 3920 \mu m^2$ .