In [2]:
```
%matplotlib inline
import matplotlib.pyplot as plt
```

In [19]:
```
##starting up the SURFv5...
##
## The board has just been programmed
##
## The calibration file is empty:
##      the cal file calibrations/surf_calibrations.json is an
##      empty file with just 2 curly brackets:
##        {}
##
## import the useful functions:
import surf_board
import calibrations.surf_calibrations as sc
reload(sc)
```

Out[19]:
```
<module 'calibrations.surf_calibrations' from 'calibrations/surf_calibrations.py'>
```

In [10]:
```
## verify that the surf_calibrations.json file is, in fact, empty:
sc.read_cal()  #when calling this function without any arguments,
               #it returns the name of the boards in the cal file
```

In [11]:
```
## run the surf_board module for the board 'CANOES':
surf_board.do('CANOES')
```

```
identify:
Identification Register: 53354137 (S5A7)
Version Register: 0.2.12 compiled 22/27
Device DNA: 70b0cc13d9705c
path: /sys/class/uio/uio0
Using default VadjN
Using default VadjP of 2700.
setting default values
Found sync edge: 2469
Found WR_STRB edge on LAB0: 3744
Found WR_STRB edge on LAB1: 3770
Found WR_STRB edge on LAB2: 3756
Found WR_STRB edge on LAB3: 3767
Found WR_STRB edge on LAB4: 3738
Found WR_STRB edge on LAB5: 3800
Found WR_STRB edge on LAB6: 3820
Found WR_STRB edge on LAB7: 3822
Found WR_STRB edge on LAB8: 3720
Found WR_STRB edge on LAB9: 3696
Found WR_STRB edge on LAB10: 3810
Found WR_STRB edge on LAB11: 3906
adding board to calibration json file..
scanning for Vadjp..
LAB4D# 0 Trial: vadjp 2720 width 602.000000 target 543.000000
LAB4D# 0 Trial: vadjp 2710 width 565.000000 target 543.000000
LAB4D# 0 Trial: vadjp 2700 width 522.000000 target 543.000000
LAB4D# 0 Trial: vadjp 2705 width 543.000000 target 543.000000
LAB4D# 1 Trial: vadjp 2680 width 511.000000 target 542.000000
LAB4D# 1 Trial: vadjp 2690 width 550.000000 target 542.000000
LAB4D# 1 Trial: vadjp 2685 width 532.000000 target 542.000000
LAB4D# 1 Trial: vadjp 2687 width 540.000000 target 542.000000
LAB4D# 2 Trial: vadjp 2720 width 561.000000 target 531.000000
LAB4D# 2 Trial: vadjp 2710 width 516.000000 target 531.000000
LAB4D# 2 Trial: vadjp 2715 width 538.000000 target 531.000000
LAB4D# 2 Trial: vadjp 2713 width 531.000000 target 531.000000
LAB4D# 3 Trial: vadjp 2720 width 604.000000 target 535.000000
LAB4D# 3 Trial: vadjp 2710 width 566.000000 target 535.000000
LAB4D# 3 Trial: vadjp 2700 width 526.000000 target 535.000000
LAB4D# 3 Trial: vadjp 2705 width 545.000000 target 535.000000
LAB4D# 3 Trial: vadjp 2703 width 541.000000 target 535.000000
LAB4D# 3 Trial: vadjp 2701 width 530.000000 target 535.000000
LAB4D# 3 Trial: vadjp 2702 width 534.000000 target 535.000000
LAB4D# 4 Trial: vadjp 2680 width 483.000000 target 556.000000
LAB4D# 4 Trial: vadjp 2690 width 531.000000 target 556.000000
LAB4D# 4 Trial: vadjp 2700 width 567.000000 target 556.000000
LAB4D# 4 Trial: vadjp 2695 width 548.000000 target 556.000000
LAB4D# 4 Trial: vadjp 2697 width 556.000000 target 556.000000
LAB4D# 5 Trial: vadjp 2720 width 507.000000 target 507.000000
LAB4D# 6 Trial: vadjp 2720 width 518.000000 target 494.000000
LAB4D# 6 Trial: vadjp 2710 width 479.000000 target 494.000000
LAB4D# 6 Trial: vadjp 2715 width 497.000000 target 494.000000
LAB4D# 6 Trial: vadjp 2713 width 488.000000 target 494.000000
LAB4D# 6 Trial: vadjp 2714 width 493.000000 target 494.000000
LAB4D# 7 Trial: vadjp 2680 width 454.000000 target 509.000000
LAB4D# 7 Trial: vadjp 2690 width 496.000000 target 509.000000
LAB4D# 7 Trial: vadjp 2700 width 519.000000 target 509.000000
LAB4D# 7 Trial: vadjp 2695 width 506.000000 target 509.000000
LAB4D# 7 Trial: vadjp 2697 width 512.000000 target 509.000000
LAB4D# 7 Trial: vadjp 2696 width 507.000000 target 509.000000
LAB4D# 8 Trial: vadjp 2720 width 624.000000 target 584.000000
LAB4D# 8 Trial: vadjp 2710 width 580.000000 target 584.000000
LAB4D# 8 Trial: vadjp 2715 width 603.000000 target 584.000000
LAB4D# 8 Trial: vadjp 2713 width 591.000000 target 584.000000
LAB4D# 8 Trial: vadjp 2711 width 585.000000 target 584.000000
LAB4D# 9 Trial: vadjp 2720 width 669.000000 target 614.000000
LAB4D# 9 Trial: vadjp 2710 width 619.000000 target 614.000000
LAB4D# 9 Trial: vadjp 2700 width 579.000000 target 614.000000
LAB4D# 9 Trial: vadjp 2705 width 599.000000 target 614.000000
LAB4D# 9 Trial: vadjp 2710 width 621.000000 target 614.000000
LAB4D# 9 Trial: vadjp 2708 width 613.000000 target 614.000000
LAB4D# 10 Trial: vadjp 2720 width 576.000000 target 521.000000
LAB4D# 10 Trial: vadjp 2710 width 545.000000 target 521.000000
LAB4D# 10 Trial: vadjp 2700 width 506.000000 target 521.000000
LAB4D# 10 Trial: vadjp 2705 width 527.000000 target 521.000000
LAB4D# 10 Trial: vadjp 2703 width 517.000000 target 521.000000
LAB4D# 10 Trial: vadjp 2704 width 518.000000 target 521.000000
LAB4D# 10 Trial: vadjp 2705 width 523.000000 target 521.000000
LAB4D# 11 Trial: vadjp 2720 width 509.000000 target 447.000000
LAB4D# 11 Trial: vadjp 2710 width 460.000000 target 447.000000
LAB4D# 11 Trial: vadjp 2700 width 417.000000 target 447.000000
LAB4D# 11 Trial: vadjp 2705 width 440.000000 target 447.000000
LAB4D# 11 Trial: vadjp 2710 width 461.000000 target 447.000000
LAB4D# 11 Trial: vadjp 2708 width 452.000000 target 447.000000
LAB4D# 11 Trial: vadjp 2706 width 445.000000 target 447.000000
Saving VadjP for board CANOES
no entry matching input key
setting default values
Clock Status: LAB4 Clock is enabled (CLKSEL[1] = 1)
            : LAB4 Driving Clock is FPGA Clock (CLKSEL[0] = 0)
            : Local Clock is enabled (CLKSEL[2] = 0)
            : FPGA System Clock PLL is running (PLLCTRL[0] = 0/PLLCTRL[2] = 0)
            : FPGA System Clock is Local Clock (PLLCTRL[1] = 0)
 Int Status : 00000000
 LED        : Internal value 000, Key value 000
 Full LED   : 00000000
 Int Mask   : 00000000
**********************
Reading from MCP4728...
DAC channel A (RFP_VPED_0):  register is set to 0x9c4, EEPROM is set to 0x9c4
DAC channel B (RFP_VPED_1):  register is set to 0x578, EEPROM is set to 0x578
DAC channel C (RFP_VPED_2):  register is set to 0x578, EEPROM is set to 0x578
DAC channel D (VPED)      :  register is set to 0x76c, EEPROM is set to 0x76c
**********************
LAB4 runmode: not enabled
LAB4 testpat: not enabled
```

Out[11]:
```
<SURF at /sys/class/uio/uio0>
```

In [13]:
```
## recheck the surf_calibrations.json file
sc.read_cal()
```

```
board in cal file: CANOES
```

In [15]:
```
## load up the surf_data class:
import surf_data
reload(surf_data)
dev=surf_data.SurfData()
```

In [20]:
```
## check the calibration data available for CANOES:
sc.read_cal(dev.dev.dna())
```

```
vadjp
DNA
```

In [21]:
```
## the board DNA, and vadjP are in the cal file
##
## let's take some pedestal data:
dev.pedestalRun()
```

```
Saving pedestals for board CANOES...
```

Out[21]:
```
array([[1638, 1809, 1631, ..., 1719, 1654, 1660],
       [1645, 1828, 1633, ..., 1748, 1665, 1711],
       [1632, 1827, 1607, ..., 1721, 1664, 1699],
       ...,
       [1640, 1874, 1612, ..., 1733, 1693, 1497],
       [1616, 1860, 1637, ..., 1740, 1664, 1467],
       [1633, 1837, 1623, ..., 1698, 1669, 1454]])
```

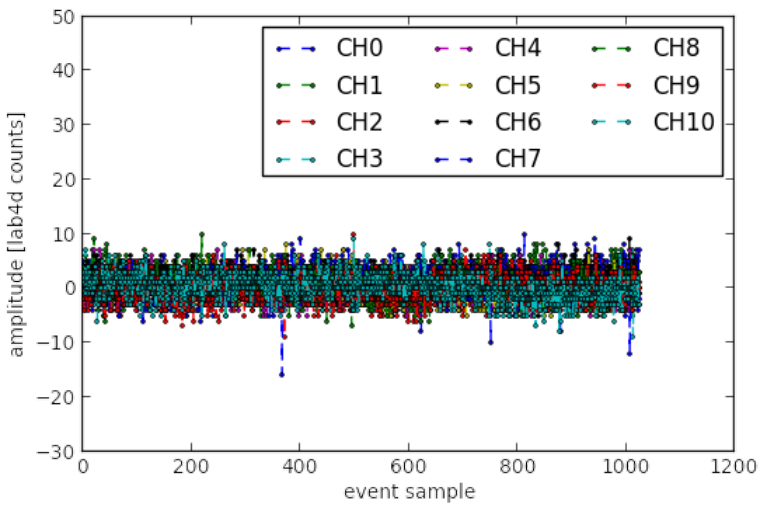
In [22]:
```
##OK, lets check the cal file again for CANOES:
sc.read_cal(dev.dev.dna())
```

```
pedestals
vadjp
DNA
```

In [23]:
```
## good, the pedestal data was added as expected
##
## now let's check to see if the data is sensible. Take 5 events:
data = dev.log(5, save=False)
```

In [30]:
```
for i in range(11):
    plt.plot(data[1][i], 'o--', ms=2, label='CH{:d}'.format(i))
plt.xlabel('event sample')
plt.ylabel('amplitude [lab4d counts]')
plt.ylim([-30, 50])
plt.legend(ncol=3)
```

Out[30]:
```
<matplotlib.legend.Legend at 0xbf30aec>
```



In [ ]:
```
```