Synchronous Sequential Logic: Gray Code Up/Down Counter

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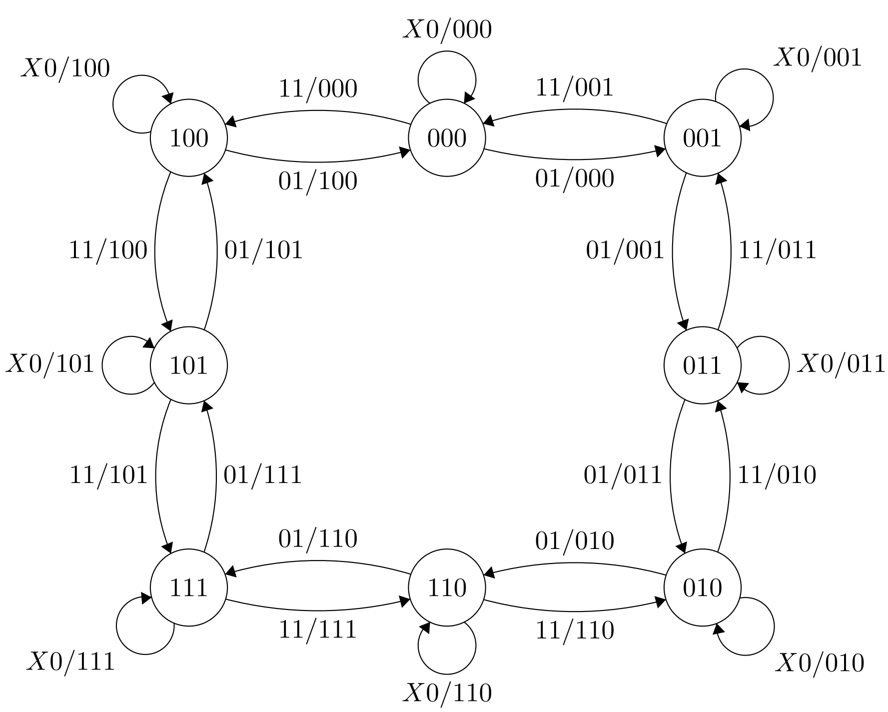
The Problem

Create a synchronous sequential logic diagram that implements a Gray Code counter. The circuits will have a *Direction* input and an *Enable* input. The Gray Code will have 3 outputs for each bit which then wraps around once it reaches the end 100 (7 in decimal).

State Diagram



Input, Outputs and Number of Flip-Flops

Inputs

There are 2 inputs:

1. *Direction*: The input which increments/decrements the Gray Code.
2. *Enable*: The input which allows the *Direction* input to increment/decrement the Gray Code.

Outputs

There will be *3 outputs*, one for each bit in the 3-bit Gray Code.

Flip-Flops

There will be *3 JK flip-flops* for each bit in the 3-bit Gray Code.

Excitation Table

The table is found on the next page.

Present State			Input		Next State			JK Flip-Flop Input					
A	B	C	D	E	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	0	0	0	0	X	0	X	0	X
0	0	0	0	1	0	0	1	0	X	0	X	1	X
0	0	0	1	0	0	0	0	0	X	0	X	0	X
0	0	0	1	1	1	0	0	1	X	0	X	0	X
0	0	1	0	0	0	0	1	0	X	0	X	X	0
0	0	1	0	1	0	1	1	0	X	1	X	X	0
0	0	1	1	0	0	0	1	0	X	0	X	X	0
0	0	1	1	1	0	0	0	0	X	0	X	X	1
0	1	0	0	0	0	1	0	0	X	X	0	0	X
0	1	0	0	1	1	1	0	1	X	X	0	0	X
0	1	0	1	0	0	1	0	0	X	X	0	0	X
0	1	0	1	1	0	1	1	0	X	X	0	1	X
0	1	1	0	0	0	1	1	0	X	X	0	X	0
0	1	1	0	1	0	1	0	0	X	X	0	X	1
0	1	1	1	0	0	1	1	0	X	X	0	X	0
0	1	1	1	1	0	0	1	0	X	X	1	X	0
1	0	0	0	0	1	0	0	X	0	0	X	0	X
1	0	0	0	1	0	0	0	X	1	0	X	0	X
1	0	0	1	0	1	0	0	X	0	0	X	0	X
1	0	0	1	1	1	0	1	X	0	0	X	1	X
1	0	1	0	0	1	0	1	X	0	0	X	X	0
1	0	1	0	1	1	0	0	X	0	0	X	X	1
1	0	1	1	0	1	0	1	X	0	0	X	X	0
1	0	1	1	1	1	1	1	X	0	1	X	X	0
1	1	0	0	0	1	1	0	X	0	X	0	0	X
1	1	0	0	1	1	1	1	X	0	X	0	1	X
1	1	0	1	0	1	1	0	X	0	X	0	0	X
1	1	0	1	1	0	1	0	X	1	X	0	0	X
1	1	1	0	0	1	1	1	X	0	X	0	X	0
1	1	1	0	1	1	0	1	X	0	X	1	X	0
1	1	1	1	0	1	1	1	X	0	X	0	X	0
1	1	1	1	1	1	1	0	X	0	X	0	X	1

Circuit output functions and flip-flop input functions using the map method

Karnaugh Map for J_A

A = 0

BC \ DE	00	01	11	10
00	0	0	1	0
01	0	0	0	0
11	0	0	0	0
10	0	1	0	0

A = 1

BC \ DE	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

$J_A = BC'D'E + B'C'DE$

Karnaugh Map for K_A

A = 0

BC \ DE	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

A = 1

BC \ DE	00	01	11	10
00	0	1	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	1	0

$K_A = B'C'D'E + BC'DE$

Karnaugh Map for J_B

A = 0

BC \ DE	00	01	11	10
00	0	0	0	0
01	0	1	0	0
11	X	X	X	X
10	X	X	X	X

A = 1

BC \ DE	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

$J_B = A'CD'E + ACDE$

Karnaugh Map for K_B

A = 0

BC \ DE	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	1	0
10	0	0	0	0

A = 1

BC \ DE	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	1	0	0
10	0	0	0	0

$K_B = A'CDE + ACD'E$

Karnaugh Map for J_C

A = 0

BC \ DE	00	01	11	10
00	0	1	0	0
01	X	X	X	X
11	X	X	X	X
10	0	0	1	0

A = 1

BC \ DE	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	1	0	0

$J_C = A'B'D'E + A'BDE + ABD'E + AB'DE$

Karnaugh Map for K_C

A = 0

BC \ DE	00	01	11	10
00	X	X	X	X
01	0	0	1	0
11	0	1	0	0
10	X	X	X	X

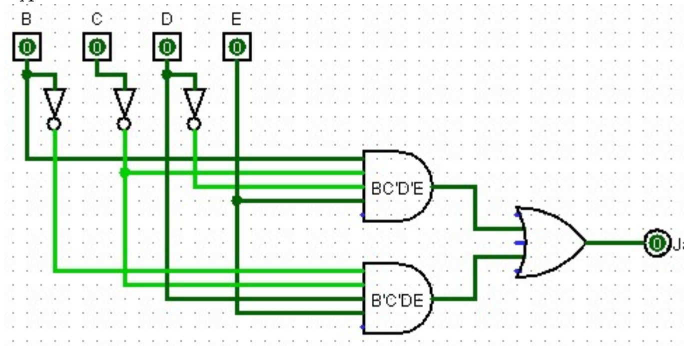
A = 1

BC \ DE	00	01	11	10
00	X	X	X	X
01	0	1	0	0
11	0	0	1	0
10	X	X	X	X

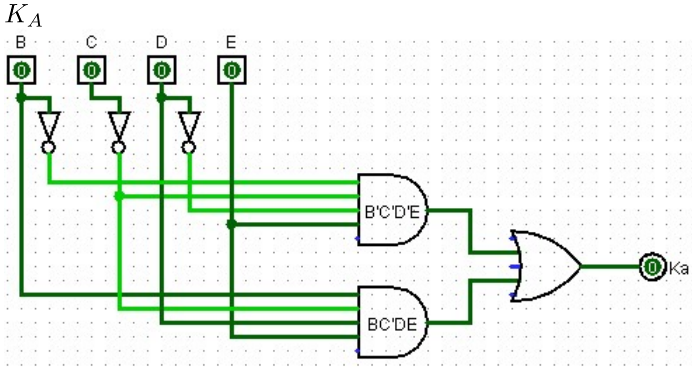
$K_C = A'BD'E + A'B'DE + AB'D'E + ABDE$

Logic Diagrams

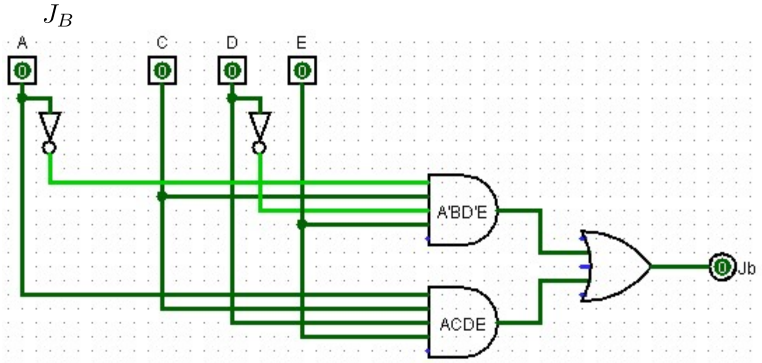
J_A



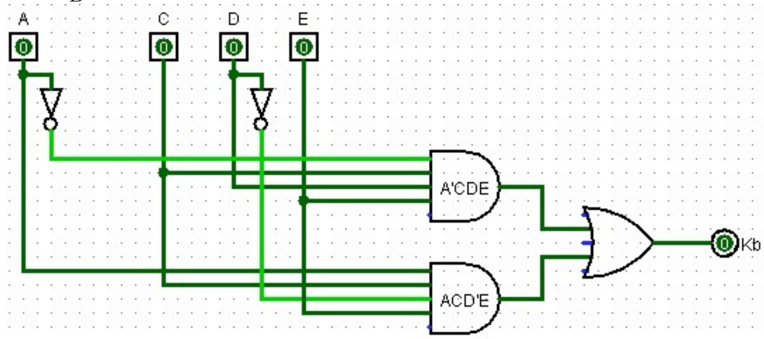
K_A



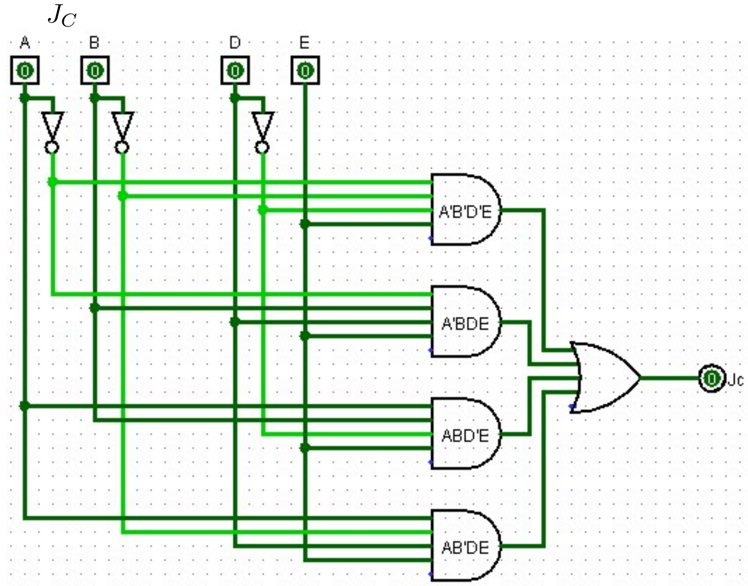
J_B



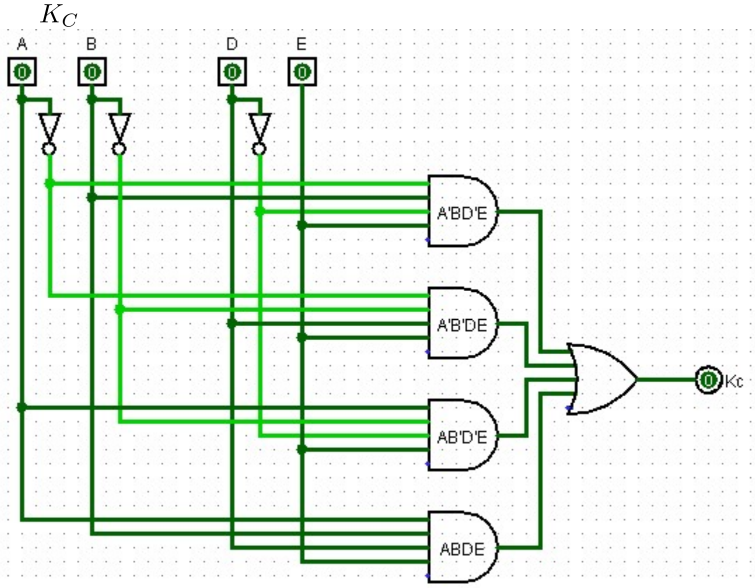
K_B



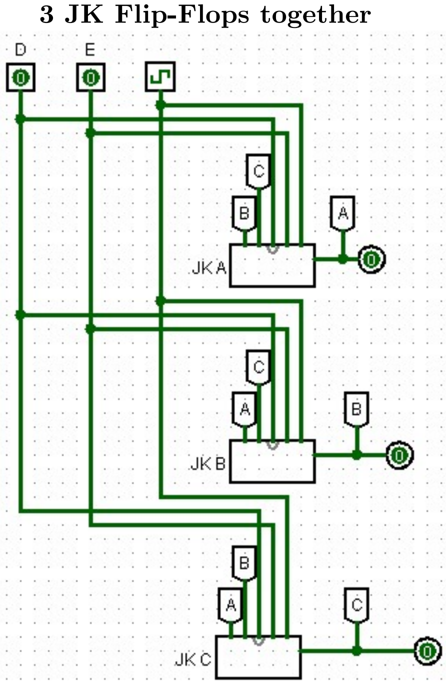
J_C



K_C



3 JK Flip-Flops together



T Flip-Flop Bonus

Input, Outputs and Number of Flip-Flops

Inputs

There are 2 inputs:

1. *Direction*: The input which increments/decrements the Gray Code.
2. *Enable*: The input which allows the *Direction* input to increment/decrement the Gray Code.

Outputs

There will be *3 outputs*, one for each bit in the 3-bit Gray Code.

Flip-Flops

There will be *3 T flip-flops* for each bit in the 3-bit Gray Code.

Excitation Table

The table is found on the next page.

Present State			Input		Next State			T Flip-Flop Input		
A	B	C	D	E	A	B	C	T_A	T_B	T_C
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1	0	0	1
0	0	0	1	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	1	0	0
0	0	1	0	0	0	0	1	0	0	0
0	0	1	0	1	0	1	1	0	1	0
0	0	1	1	0	0	0	1	0	0	0
0	0	1	1	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0	0	0
0	1	0	0	1	1	1	0	1	0	0
0	1	0	1	0	0	1	0	0	0	0
0	1	0	1	1	0	1	1	0	0	1
0	1	1	0	0	0	1	1	0	0	0
0	1	1	0	1	0	1	0	0	0	1
0	1	1	1	0	0	1	1	0	0	0
0	1	1	1	1	0	0	1	0	1	0
1	0	0	0	0	1	0	0	0	0	0
1	0	0	0	1	0	0	0	1	0	0
1	0	0	1	0	1	0	0	0	0	0
1	0	0	1	1	1	0	1	0	0	1
1	0	1	0	0	1	0	1	0	0	0
1	0	1	0	1	1	0	0	0	0	1
1	0	1	1	0	1	0	1	0	0	0
1	0	1	1	1	1	1	1	0	1	0
1	1	0	0	0	1	1	0	0	0	0
1	1	0	0	1	1	1	1	0	0	1
1	1	0	1	0	1	1	0	0	0	0
1	1	0	1	1	0	1	0	1	0	0
1	1	1	0	0	1	1	1	0	0	0
1	1	1	0	1	1	0	1	0	1	0
1	1	1	1	0	1	1	1	0	0	0
1	1	1	1	1	1	1	0	0	0	1

Circuit output functions and flip-flop input functions using the map method

Karnaugh Map for T_A

A = 0

BC \ DE	00	01	11	10
00	0	0	1	0
01	0	0	0	0
11	0	0	0	0
10	0	1	0	0

A = 1

BC \ DE	00	01	11	10
00	0	1	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	1	0

$T_A = A'BC'D'E + A'B'C'DE + AB'C'D'E + ABC'DE$

Karnaugh Map for T_B

A = 0

BC \ DE	00	01	11	10
00	0	0	0	0
01	0	$\boxed{1}$	0	0
11	0	0	$\boxed{1}$	0
10	0	0	0	0

A = 1

BC \ DE	00	01	11	10
00	0	0	0	0
01	0	0	$\boxed{1}$	0
11	0	$\boxed{1}$	0	0
10	0	0	0	0

$T_B = A'B'CD'E + A'BCDE + ABCD'E + AB'CDE$

Karnaugh Map for T_C

A = 0

BC \ DE	00	01	11	10
00	0	1	0	0
01	0	0	1	0
11	0	1	0	0
10	0	0	1	0

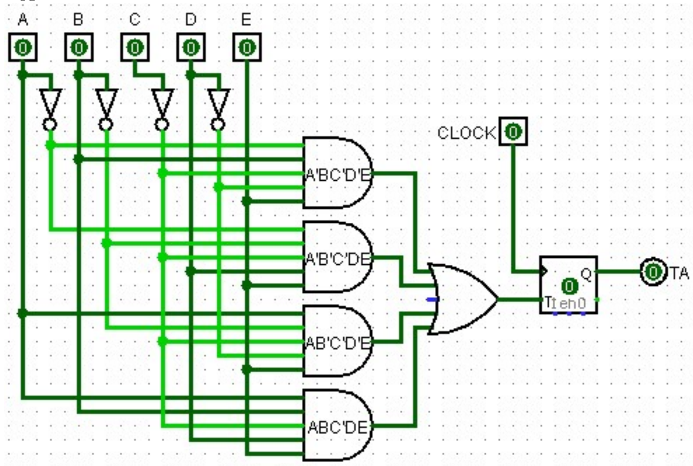
A = 1

BC \ DE	00	01	11	10
00	0	0	1	0
01	0	1	0	0
11	0	0	1	0
10	0	1	0	0

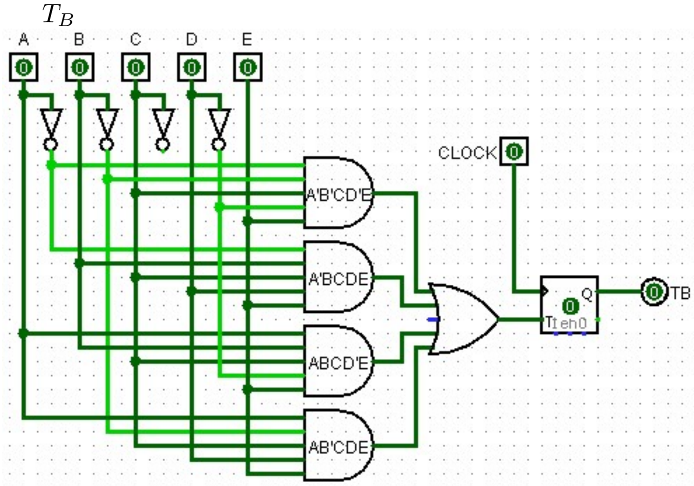
$T_C = A'B'C'D'E + A'BCD'E + A'B'CDE + A'BC'DE + AB'CD'E + ABC'D'E + AB'C'DE + ABCDE$

Logic Diagrams

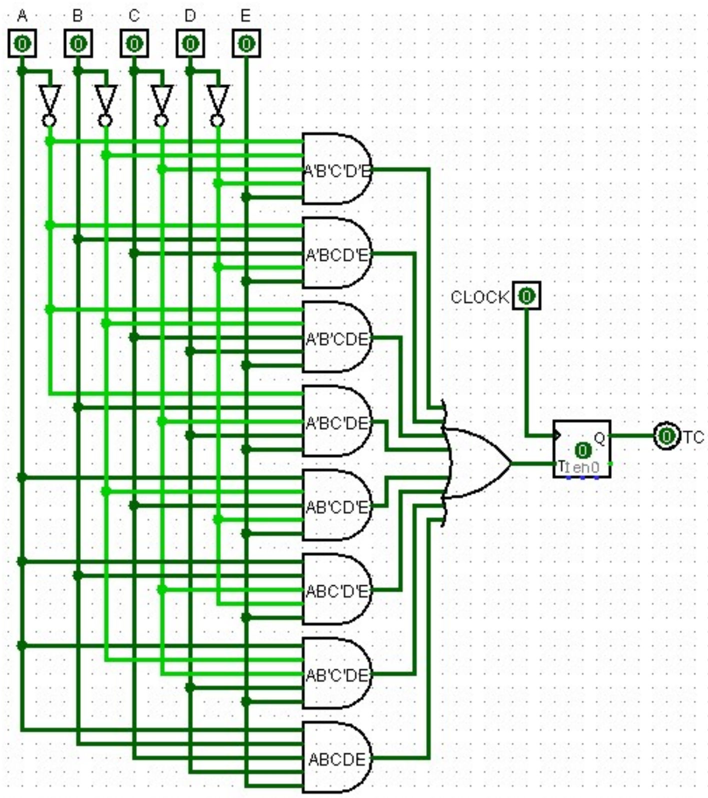
T_A



T_B



T_C



A
B
C
D
E
A'B'C'D'E
A'BCD'E
A'B'CDE
A'BC'DE
AB'C'D'E
ABC'D'E
AB'C'DE
ABCDE
CLOCK
Q
T
en
TC

3 T Flip-Flops together