Combinational Logic: Binary-to-Seven-Segment Decoder

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Design Method

1 State the problem in words

Design a combinational logic circuit that takes a 4-bit binary number as an input and produces 7 outputs, one each for the 7 segments of the display unit to show the corresponding hexadecimal number.

2 Determine the input and output variables

4-bit Input variables:

- bit - 3 (w)
- bit - 2 (x)
- bit - 1 (y)
- bit - 0 (z)

Output variables:

- A
- B
- C
- D
- E
- F
- G

3 Assign letter symbols to the variables.

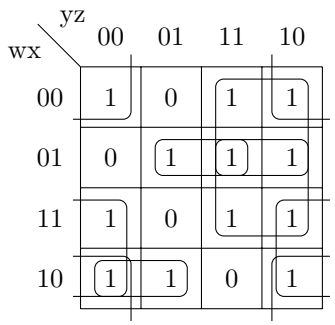
The 4-bit input variables will be represented by w, x, y, z respectively.

4 Create the truth table that defines the relationships between inputs and outputs.

w	x	y	z		A	B	C	D	E	F	G
0	0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	1	0	1	1	0	0	0	0
0	0	1	0	2	1	1	0	1	1	0	1
0	0	1	1	3	1	1	1	1	0	0	1
0	1	0	0	4	0	1	1	0	0	1	1
0	1	0	1	5	1	0	1	1	0	1	1
0	1	1	0	6	1	0	1	1	1	1	1
0	1	1	1	7	1	1	1	0	0	0	0
1	0	0	0	8	1	1	1	1	1	1	1
1	0	0	1	9	1	1	1	1	0	1	1
1	0	1	0	A	1	1	1	0	1	1	1
1	0	1	1	b	0	0	1	1	1	1	1
1	1	0	0	C	1	0	0	1	1	1	0
1	1	0	1	d	0	1	1	1	1	0	1
1	1	1	0	E	1	0	0	1	1	1	1
1	1	1	1	F	1	0	0	0	1	1	1

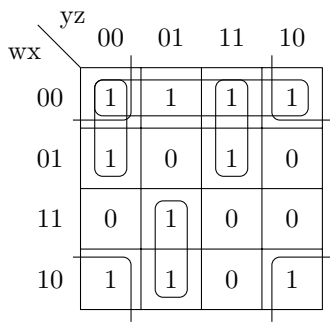
5 Obtain the simplified function for each output (show all steps for this, whether done algebraically or using the map method).

Karnaugh Map for A



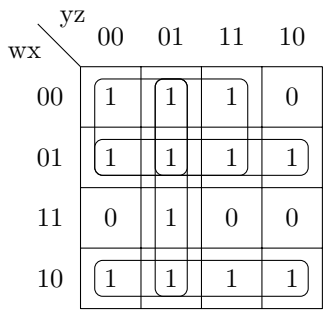
A = wz' + x'z' + wx'y' + w'xz + w'y + xy

Karnaugh Map for B



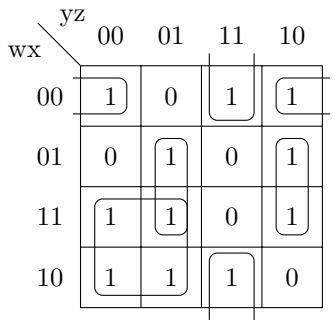
B = x'z' + w'x' + w'y'z' + w'yz + wy'z

Karnaugh Map for C



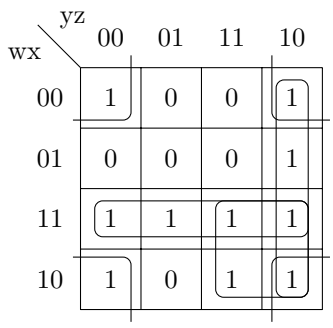
C = y'z + wx' + w'x + w'y' + w'z

Karnaugh Map for D



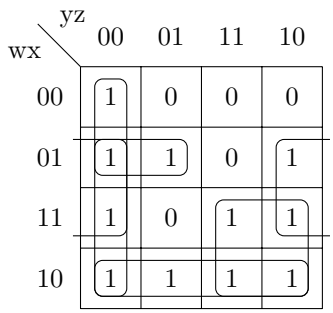
D = wy'+ x'yz + xy'z + w'x'z' + xyz'

Karnaugh Map for E



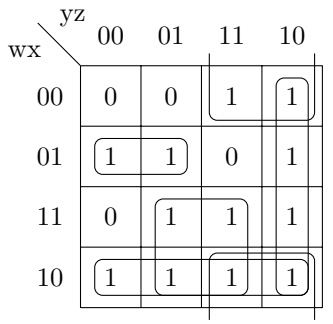
E = x'z' + yz' + wx + wy

Karnaugh Map for F



F = wx' + xz' + wy + y'z' + w'xy'

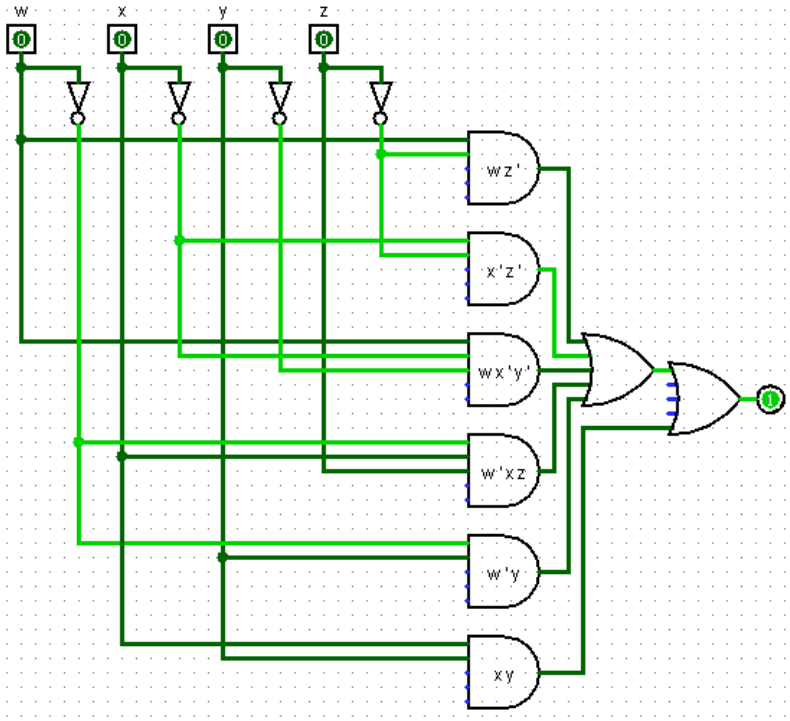
Karnaugh Map for G



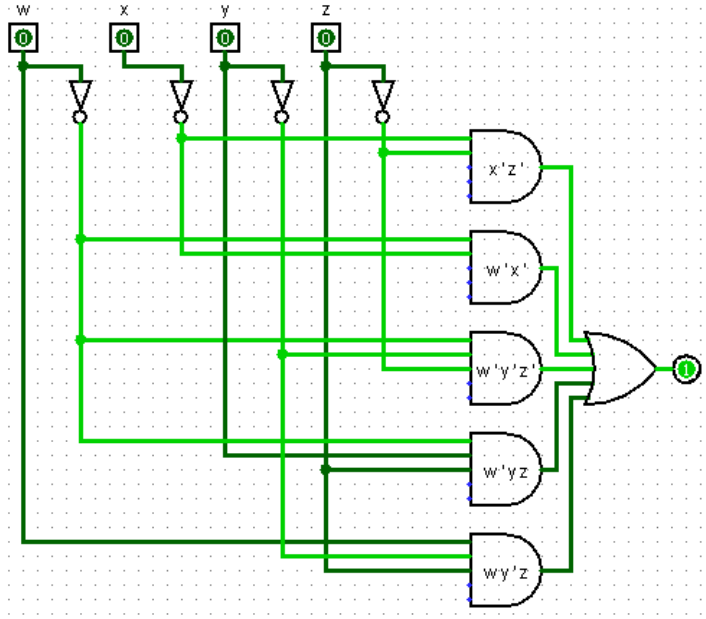
G = x'y + wx' + yz' + wz + w'xy'

6 Implement the functions using the appropriate gates (show a logic diagram for this).

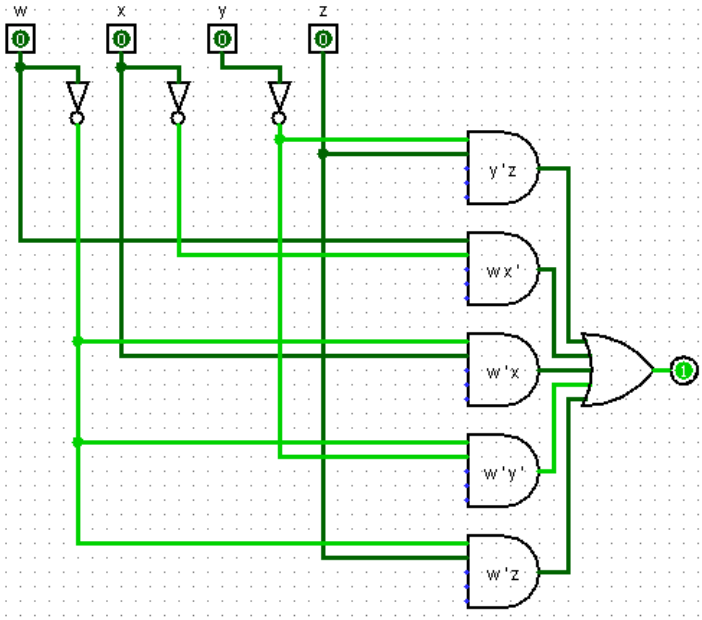
Logic Diagram for A



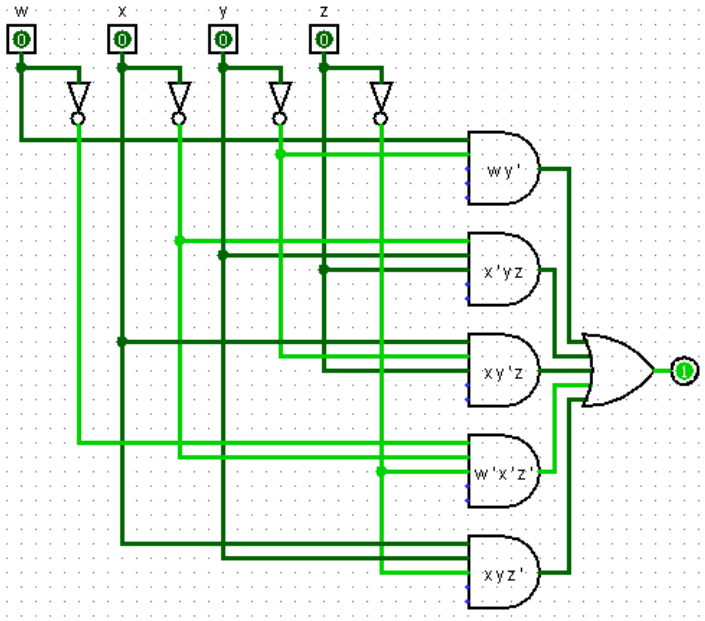
Logic Diagram for B



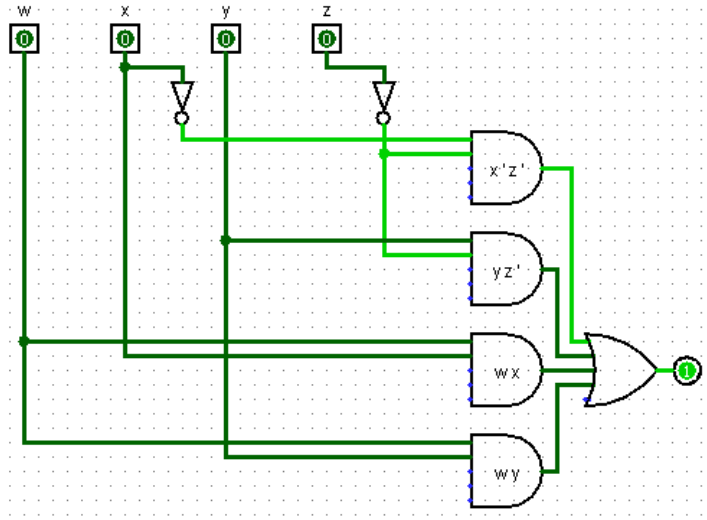
Logic Diagram for C



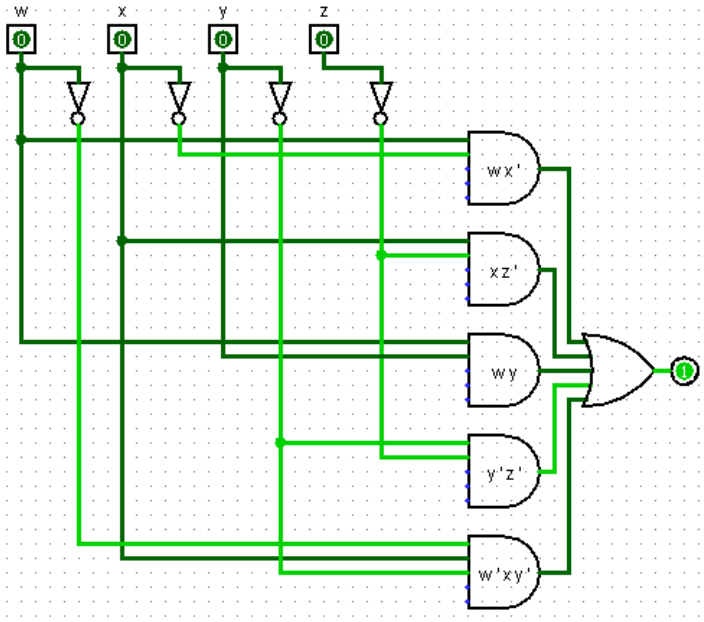
Logic Diagram for D



Logic Diagram for E



Logic Diagram for F



Logic Diagram for G