**Objective**

To exploit this unique data set by reporting in detail on the magnitudes, and also the temporal structure, of delays on high capacity links with nontrivial congestion. The result is one of the most comprehensive pictures of router delay performance that we are aware of. As our analysis is based on empirical results, it is not reliant on assumptions on traffic statistics or router operations.

Our second aim is to use the completeness of the data as a tool to investigate how packet delays occur inside the router. In other words, we aim to provide a physical model capable of explaining the observed delay and congestion. Working in the context of the popular store and forward router architecture, we are able to justify the commonly held assumption that the bottleneck of such an architecture is in the output buffers, and thereby validate the fluid output queue model relied on routinely in the field of active probing.

To define a refined model with an accuracy close to the limits of time stamping precision, which is robust to many details of the architecture under reasonable loads.

Our third contribution is an investigation of the origins of such episodes, driven by the question, “What is the dominant mechanism responsible for delays?” We use a powerful methodology of virtual or “semi-” experiments, that exploitsboth the availability of the detailed packet data, and the fidelity of the router model. We identify, and evaluate the contributions of, three known canonical mechanisms: i) reduction in link bandwidth from core to access; ii) multiplexing of multiple input streams; iii) burstinessof the input traffic stream(s).