BQ25798 I²C Controlled, 1-4 Cell, 5-A Buck-Boost Solar Battery Charger with Dual-Input Selector and MPPT for Small Photovoltaic Panel

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1 Features

- High power density, high integration buck-boost charger for 1-4 cell batteries supporting any USB PD 3.0 profile
  - Integrates four switching MOSFETs, BATFET
  - Integrates input and charging current sensing
- Highly efficient
  - 750-kHz or 1.5-MHz switching frequencies
  - charging current with 10-mA resolution
    - 97.5% converter efficiency charging 12V battery at 1.5A from 12V PV Panel input
- Supports a wide range of input sources
  - MPPT algorithm for charging from small photovoltaic panel
  - 3.6-V to 24-V wide input operating voltage range with 30-V absolute maximum rating
  - Detects USB BC1.2, SDP, CDP, DCP, HVDCP and non-standard adapters
- Dual-input power mux controller (optional)
- Narrow voltage DC (NVDC) power path management
- Powers USB port from battery (USB OTG)
  - OTG output voltage with 10-mV resolution to support USB-PD Programmable Power Supply
  - OTG output current regulation up to 3.32 A with 40-mA resolution
- Flexible autonomous and I²C mode for optimal system performance
- Integrated 16-bit ADC for voltage, current and temperature monitoring
- Low battery quiescent current
  - 21-µA for battery only operation
  - 600 nA in charger shutdown mode
- High accuracy
  - +0.65% to -0.85% charge voltage regulation for 2s-4s batteries
  - ±5% charge current regulation
  - ±5% input current regulation
- Safety
  - Thermal regulation and thermal shutdown
  - Input/battery OVP and OCP
  - Converter MOSFETs OCP
  - Charging safety timer
- Package
  - 29-Pin 4mm × 4mm QFN

2 Applications

- Video Doorbell, Smart Home Control
- Grid Infrastructure, Robotic Lawn Mower
- Asset Tracking, Electronic point of sales (EPOS)

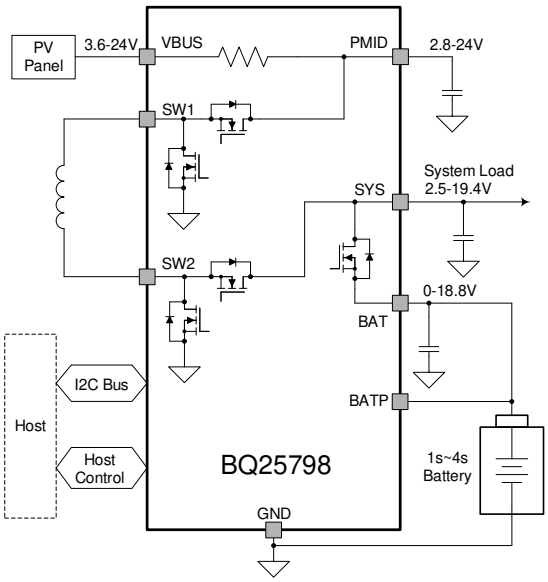
3 Description

The BQ25798 is a fully integrated switch-mode buck-boost charger for 1-4 cell Li-ion batteries and Li-polymer batteries. The integration includes 4 switching MOSFETs (Q_1, Q_2, Q_3, Q_4), input and charging current sensing circuits, the battery FET (Q_{BAT}) and all the loop compensation of the buck-boost converter. It uses NVDC power path management, regulating the system slightly above the battery voltage without dropping below a configurable minimum system voltage. When system power exceeds the input source rating, battery supplement mode supports the system without overloading the input source. BQ25798 provides a simple interface to small photovoltaic panels using its built-in V_{OC} scaling MPPT algorithm.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
BQ25798	QFN (29)	4.0 x 4.0 mm²

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

DATE	REVISION	NOTES
December 2020	*	Advance Information Release

5 Pin Configuration and Functions

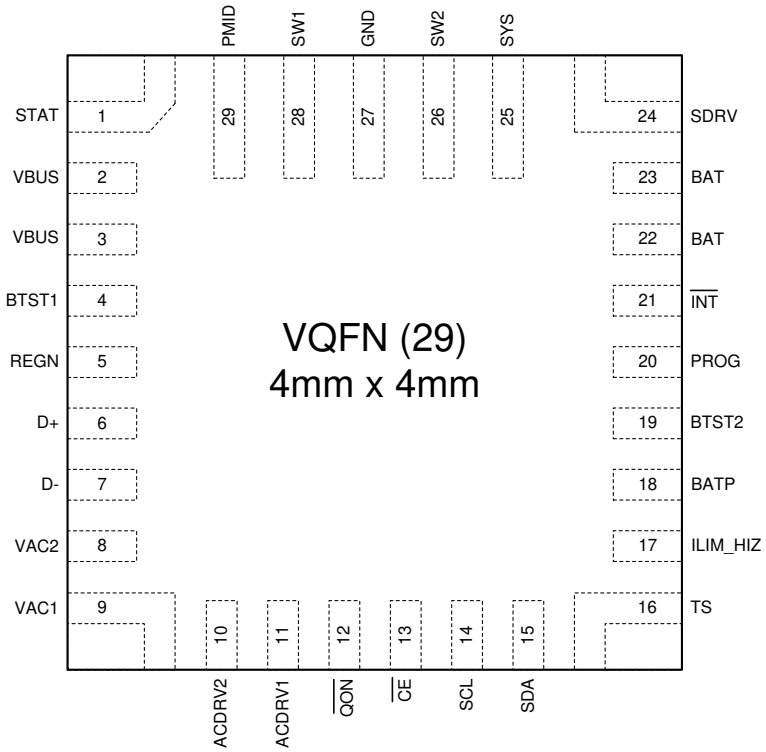

Figure 5-1. RQM Package 29-Pin VQFN Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
STAT	1	DO	**Open Drain Charge Status Output –** It indicates various charger operations. Connect to the pull up rail via a 10kΩ resistor. LOW indicates charging in progress. HIGH indicates charging completed or charging disabled. When any fault condition occurs, STAT pin blinks at 1Hz. The STAT pin function can be disabled when DIS_STAT bit is set to 1.
VBUS	2-3	P	**Charger Input Voltage –** The power input terminal of the charger. An input current sensing circuit is connected between VBUS and PMID. The recommended capacitors at VBUS are 2 pieces of 10µF and one piece of 0.1µF ceramic capacitors. Place the 0.1µF ceramic capacitor as close as possible to the charger IC.
BTST1	4	P	**Input High Side Power MOSFET Gate Driver Power Supply –** Connect a 10V or higher rating, 47nF ceramic capacitor between SW1 and BTST1 as the bootstrap capacitor for driving high side switching MOSFET (Q1).
REGN	5	P	**The Charger Internal Linear Regulator Output –** It is supplied from either VBUS or BAT dependent on which voltage is higher. Connect a 10V, 4.7µF ceramic capacitor from REGN to power ground. The REGN LDO output is used for the internal MOSFETs gate driving voltage and the voltage bias for TS pin resistor divider.
D+	6	AIO	**Positive Line of the USB Data Line Pair –** D+/D- based USB host/charging port detection for VIN1 input. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and the adjustable high voltage adapter.
D-	7	AIO	**Negative Line of the USB Data Line Pair –** D+/D- based USB host/charging port detection for VIN1 input. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and the adjustable high voltage adapter.
VAC2	8	P	**VAC2 Input Detection –** When a voltage between and 24V is applied on VAC2, it represents a valid input being plugged into port #2. Connect to VBUS if the ACFET2 and RBFET2 are not installed.
VAC1	9	P	**VAC1 Input Detection –** When a voltage between and 24V is applied on VAC1, it represents a valid input being plugged into port #1. Connect to VBUS if the ACFET1 and RBFET1 are not installed.

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Table 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
ACDRV2	10	P	**Input FETs Driver Pin 2 –** The charge pump output to drive the port #2 input N-channel MOSFET (ACFET2) and the reverse blocking N-channel MOSFET (RBFET2). The charger turns on the back-to-back MOSFETs by increasing the ACDRV2 voltage 5V above the common drain connection of the ACFET2 and RBFET2 when the turn-on condition is met. Tie ACDRV2 to GND if no ACFET2 and RBFET2 installed.
ACDRV1	11	P	**Input FETs Driver Pin 1 –** The charge pump output to drive the port #1 input N-channel MOSFET (ACFET1) and the reverse blocking N-channel MOSFET (RBFET1). The charger turns on the back-to-back MOSFETs by increasing the ACDRV1 voltage 5V above the common drain connection of the ACFET1 and RBFET1 when the turn-on condition is met. Tie ACDRV1 to GND if no ACFET1 and RBFET1 installed.
$\overline{QON}$	12	DI	**Ship FET Enable or System Power Reset Control Input –** When the device is in ship mode or in the shutdown mode, the SDRV turns off the external ship FET to minimize the battery leakage current. A logic low on this pin with t_{SM_EXIT} duration turns on ship FET to force the device to exit the ship mode. A logic low on this pin with t_{RST} duration resets system power by turning off the ship FET for t_{RST_SFET} (also setting the charger in HIZ mode when VBUS is high) and then turning on ship FET (also disabling the charger HIZ mode) to provide full system power reset. During t_{RST_SFET} when the ship FET is off, the charger applies a 30mA discharging current on SYS to discharge system voltage. The pin contains an internal pull-up to maintain default high logic.
$\overline{CE}$	13	DI	**Active Low Charge Enable Pin –** Battery charging is enabled when EN_CHG bit is 1 and $\overline{CE}$ pin is LOW. $\overline{CE}$ pin must be pulled HIGH or LOW, do not leave floating.
SCL	14	DI	**I^2C Interface Clock –** Connect SCL to the logic rail through a 10 kΩ resistor.
SDA	15	DIO	**I^2C Interface Data –** Connect SDA to the logic rail through a 10 kΩ resistor.
TS	16	AI	**Temperature Qualification Voltage Input –** Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin voltage is out of range. Recommend a 103AT-2 10kΩ thermistor.
ILIM_HIZ	17	AI	**Input Current Limit Setting and HIZ Mode Control Pin –** Program ILIM_HIZ voltage by connecting a resistor divider from pull up rail to ILIM_HIZ pin to ground. The pin voltage is calculated as: V_{ILIM_HIZ} = 1V + 800mΩ × IINDPM, in which IINDPM is the target input current. The input current limit used by the charger is the lower setting of ILIM_HIZ pin and the IINDPM register. When the pin voltage is below 0.75V, the buck-boost converter enters non-switching mode with REGN on. When the pin voltage is above 1V, the converter resumes switching.
BATP	18	P	**Positive Input for Battery Voltage Sensing –** Connect to the positive terminal of battery pack. Place 100Ω series resistance between this pin and the battery positive terminal.
BTST2	19	P	**Output High Side Power MOSFET Gate Driver Power Supply –** Connect a 10V or higher rating, 47nF ceramic capacitor between SW2 and BTST2 as the bootstrap capacitor for driving high side switching MOSFET (Q4).
PROG	20	AI	**Charger POR Default Settings Program –** At power up, the charger detects the resistance tied to PROG pin to determine the default switching frequency and the default battery charging profile. The surface mount resistor with ±1% or ±2% tolerance is recommended. Please refer to more details in the section of PROG Pin Configuration.
$\overline{INT}$	21	DO	**Open Drain Interrupt Output. –** Connect the $\overline{INT}$ pin to a logic rail via a 10kΩ resistor. The $\overline{INT}$ pin sends an active low, 256μs pulse to the host to report the charger device status and faults.
BAT	22-23	P	**The Battery Charging Power Connection –** Connect to the positive terminal of the battery pack. The internal charging current sensing circuit is connected between SYS and BAT. The recommended capacitors at BAT are 2 pieces of 10μF ceramic capacitors.
SDRV	24	P	**External N-channel Ship FET (SFET) Gate Driver Output –** The driver pin of the external ship FET. The ship FET is always turned on when the ship mode is disabled, and it keeps off when the charger is in ship mode or shutdown mode. Connect a 1nF, 50V rated, 0402 package, ceramic capacitor from SDRV to GND when the ship FET is not used.
SYS	25	P	**The Charger Output Voltage to System –** The internal N-channel high side MOSFET (Q4) is connected between SYS and SW2 with drain on SYS and source on SW2. The recommended capacitors at SYS are 5 pieces of 10μF and one piece of 0.1μF ceramic capacitors. Place the 0.1μF ceramic capacitor as close as possible to the charger IC.
SW2	26	P	**Boost Side Half Bridge Switching Node**
GND	27	P	**Ground Return**
SW1	28	P	**Buck Side Half Bridge Switching Node**

Table 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PMID	29	P	**Q1 MOSFET Drain Connection –** An internal N-channel high side MOSFET (Q1) is connected between PMID and SW1 with drain on PMID and source on SW1. The recommended capacitors at PMID are 3 pieces of 10µF and one piece of 0.1µF ceramic capacitors. Place the 0.1µF ceramic capacitor as close as possible to the charger IC.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range (with respect to GND)	VAC1, VAC2	-2	30	V
	VBUS (converter not switching)	-2	30	V
	PMID (converter not switching)	-0.3	30	V
	ACDRV1, ACDRV2, BTST1	-0.3	32	V
	SYS (converter not switching)	-0.3	23	V
	BATP, BAT	-0.3	20	V
	BTST2	-0.3	29	V
	SDRV	-0.3	26	V
	SW1	-2 (50ns)	30	V
	SW2	-2 (50ns)	23	V
	$\overline{PG}$, $\overline{QON}$, D+, D-, $\overline{CE}$, STAT, SCL, SDA, $\overline{INT}$, ILIM_HIZ, PROG, TS, REGN, BATN	-0.3	6	V
Output Sink Current	$\overline{INT}$, STAT		6	mA
Differential Voltage	BTST1-SW1, BTST2-SW2	-0.3	6	V
	PMID-VBUS	-0.3	6	V
	SYS-BAT	-0.3	16	V
	SDRV-BAT	-0.3	6	V
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VBUS}	Input voltage	3.6		24	V
V_{BAT}	Battery voltage			18.8	V
I_{VBUS}	Input current			3.3	A
I_{SW}	Output current (SW)			5	A
I_{BAT}	Fast charging current			5	A
	RMS discharge current (continuously)			6	A
	Peak discharge current (upto 1 sec)			10	A
T_A	Ambient temperature	-40		85	°C

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Junction temperature	-40		125	°C
C_{VBUS}	Effective VBUS capacitance		2		µF
C_{PMID}	Effective PMID capacitance		4		µF
C_{SYS}	Effective SYS capacitance		6		µF
C_{BAT}	Effective BAT capacitance		3		µF

6.4 Thermal Information

THERMAL METRIC (1)		BQ25798 RQM (QFN) 29-PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
$I_{Q\_BAT\_ON}$	Quiescent battery current (BATP, BAT, SYS) when the charger is in the battery only mode, battery FET is enabled, ADC is disabled	VBAT = 8V, No VBUS, BATFET is enabled, I2C enabled, ADC disabled, not in ship mode or shut down mode, system is powered by battery. T_J < 85 °C		17		µA
$I_{Q\_BAT\_OFF}$	Quiescent battery current (BATP) for when the charger is in ship mode.	VBAT = 8V, No VBUS, I2C enabled, ADC disabled, in ship mode, T_J < 85 °C		11		µA
I_{SD_BAT}	Shutdown battery current (BATP) when charger is in shut down mode.	VBAT = 8V, No VBUS, I2C disabled, ADC disabled, in shut down mode, T_J < 85 °C		0.5		µA
$I_{Q\_BAT\_ON}$	Quiescent battery current (BATP, BAT, SYS) when the charger is in the battery only mode, battery FET is enabled, ADC is enabled	VBAT = 8V, No VBUS, I2C enabled, ADC enabled, not in ship mode or shut down mode, T_J < 85 °C		540		µA
I_{Q_VBUS}	Quiescent input current (VBUS)	VBUS = 15V, VBAT = 8V, charge disabled, converter switching, ISYS = 0A, OOA disabled		3		mA
		VBUS = 15V, VBAT = 8V, charge disabled, converter switching, ISYS = 0A, OOA enabled		5		mA
I_{SD_VBUS}	Shutdown input current (VBUS) in HIZ	VBUS = 15V, HIZ mode, no battery, ADC disabled, ACDRV disabled		386		µA
		VBUS = 15V, HIZ mode, no battery, ADC disabled, ACDRV enabled		590		µA

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6.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{Q_OTG}	Quiescent battery current (BATP, BAT, SYS) in OTG	VBAT = 8V, VBUS = 5V, OTG mode enabled, converter switching, I_{VBUS} = 0A, OOA disabled		3		mA
		VBAT = 8V, VBUS = 5V, OTG mode enabled, converter switching, I_{VBUS} = 0A, OOA enabled		5		mA
VBUS / VBAT SUPPLY						
$V_{VAC\_PRESENT}$	VAC present rising threshold to turn on the ACFET-RBFET	For both VAC1 and VAC2		3.4		V
	VAC present falling threshold to turn off the ACFET-RBFET	For both VAC1 and VAC2		3.2		V
V_{VAC_OVP}	VAC overvoltage rising threshold, when VAC_OVP[1:0]=00	For both VAC1 and VAC2		26		V
	VAC overvoltage falling threshold, when VAC_OVP[1:0]=00	For both VAC1 and VAC2		25.2		V
	VAC overvoltage rising threshold, when VAC_OVP[1:0]=01	For both VAC1 and VAC2		18.0		V
	VAC overvoltage falling threshold, when VAC_OVP[1:0]=01	For both VAC1 and VAC2		17.5		V
	VAC overvoltage rising threshold, when VAC_OVP[1:0]=10	For both VAC1 and VAC2		12		V
	VAC overvoltage falling threshold, when VAC_OVP[1:0]=10	For both VAC1 and VAC2		11.6		V
	VAC overvoltage rising threshold, when VAC_OVP[1:0]=11	For both VAC1 and VAC2		7		V
	VAC overvoltage falling threshold, when VAC_OVP[1:0]=11	For both VAC1 and VAC2		6.8		V
V_{VBUS_OP}	VBUS operating range		3.6		24	V
V_{VBUS_UVLOZ}	VBUS rising for active I2C, no battery	VBUS rising		3.4		V
V_{VBUS_UVLO}	VBUS falling to turn off I2C, no battery	VBUS falling		3.2		V
$V_{VBUS\_PRESENT}$	VBUS to start switching	VBUS rising		3.4		V
$V_{VBUS\_PRESENTZ}$	VBUS to stop switching	VBUS falling		3.2		V
V_{VBUS_OVP}	VBUS overvoltage rising threshold	VBUS rising		25.7		V
V_{VBUS_OVPZ}	VBUS overvoltage falling threshold	VBUS falling		24.4		V
I_{BUS_OCP}	IBUS over-current rising threshold			8.0		A
I_{BUS_OCPZ}	IBUS over-current falling threshold			7.5		A
V_{BAT_UVLOZ}	BAT voltage for active I2C, no VBUS, no VAC	VBAT rising, when the charger is in ship mode		3.40		V
		VBAT rising, when the charger is in normal mode		2.60		V

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6.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT_UVLO}	BAT voltage to turn off I2C, no VBUS, no VAC	VBAT falling, when the charger is in ship mode		3.20		V
		VBAT falling, when the charger is in normal mode		2.40		V
V_{BAT_OTG}	BAT voltage rising threshold to enable OTG mode	VBAT rising		2.8		V
V_{BAT_OTGZ}	BAT voltage falling threshold to disable OTG mode	VBAT falling		2.5		V
$V_{POORSRC}$	Bad adapter detection threshold	VBUS falling		3.4		V
$V_{POORSRC}$	Bad adapter detection threshold hysteresis	VBUS rising above $V_{POORSRC}$		200		mV
$I_{POORSRC}$	Bad adapter detection current source			30		mA
R_{VBUS_PD}	VBUS pull down resistance			6		kΩ
R_{VAC_PD}	VAC pull down resistance	For both VAC1 and VAC2		60		Ω
POWER-PATH MANAGEMENT						
$V_{SYSMAX\_REG\_RNG}$	System voltage regulation range, measured on SYS		3.2		19	V
$V_{SYSMAX\_REG\_ACC}$	System voltage regulation accuracy (when V_{BAT}>V_{SYSMIN}, charging disabled, PFM disabled)	V_{BAT} = 16.8V (4s default)	16.82	17.00	17.25	V
		V_{BAT} = 12.6V (3s default)	12.62	12.80	13.04	V
		V_{BAT} = 8.4V (2s default)	8.44	8.60	8.77	V
		V_{BAT} = 4.2V (1s default)	4.268	4.40	4.550	V
$V_{SYSMIN\_REG\_RNG}$	V_{SYSMIN} regulation range, measured on SYS		2.5		16	V
$V_{SYSMIN\_REG\_STEP}$	V_{SYSMIN} regulation step size			250		mV
$V_{SYSMIN\_REG\_ACC}$	System voltage regulation accuracy (when V_{BAT}<V_{SYSMIN})	4s battery	11.9	12.2	12.5	V
		3s battery	9.0	9.2	9.4	V
		2s battery	7.12	7.2	7.32	V
		1s battery	3.5	3.7	3.9	V
V_{SYS_OVP}	VSYS overvoltage rising threshold	As a percentage of the system regulation voltage, to turnoff the converter.		110.0		%
	VSYS overvoltage rising threshold	V_{SYS_REG} = 17V		18.70		V
	VSYS overvoltage rising threshold	V_{SYS_REG} = 8.6V		9.46		V
	VSYS overvoltage falling threshold	As a percentage of the system regulation voltage, to re-enable the converter.		100		%
	VSYS overvoltage falling threshold	V_{SYS_REG} = 17V		17		V
	VSYS overvoltage falling threshold	V_{SYS_REG} = 8.6V		8.6		V
V_{SYS_SHORT}	VSYS short voltage falling threshold			2.2		V
BATTERY CHARGER						
V_{REG_RANGE}	Typical charge voltage regulation range		3		18.8	V
V_{REG_STEP}	Typical charge voltage step			10		mV
V_{REG_ACC}	Charge voltage accuracy, T_J = –40°C - 85°C	V_{REG} = 16.8V	-0.65		0.55	%
		V_{REG} = 12.6V	-0.85		0.65	%
		V_{REG} = 8.4V	-0.25		0.65	%
		V_{REG} = 4.2V	-0.45		0.95	%

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6.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CHG_RANGE}	Typical charge current regulation range		0.05		5	A
I_{CHG_STEP}	Typical charge current regulation step			10		mA
I_{CHG_ACC}	Typical boost mode PWM charge current accuracy, VBUS < VBAT, T_J = –40°C - 85°C	ICHG = 2.5A; VBAT=8V	-3		7	%
		ICHG = 2A; VBAT=8V	-2		8	%
		ICHG = 1.5A; VBAT=8V	0		10	%
		ICHG = 1A; VBAT=8V	-2		8	%
		ICHG = 0.5A; VBAT=8V	-7.5		7.5	%
I_{CHG_ACC}	Typical buck mode PWM charge current accuracy, VBUS > VBAT, T_J = –40°C - 85°C	ICHG = 4A; VBAT=8V	-5.5		2.5	%
		ICHG = 2A; VBAT=8V	-6.5		3.5	%
		ICHG = 1A; VBAT=8V	-5		5	%
		ICHG = 0.5A; VBAT=8V	-7.5		7.5	%
I_{PRECHG_RANGE}	Typical pre-charge current range		40		2000	mA
I_{PRECHG_STEP}	Typical pre-charge current step			40		mA
I_{PRECHG_ACC}	Typical LDO mode charge current accuracy when V_{BATP}-V_{BATN} below V_{SYSMIN}, VBUS < VBAT, T_J = –40°C - 85°C	IPRECHG = 480mA, VBAT = 6.5V	-8		8	%
		IPRECHG = 200mA, VBAT = 6.5V	-20		20	%
		IPRECHG = 120mA, VBAT = 6.5V	-35		35	%
I_{PRECHG_ACC}	Typical LDO mode charge current accuracy when V_{BATP}-V_{BATN} below V_{SYSMIN}, VBUS > VBAT, T_J = –40°C - 85°C	IPRECHG = 1000mA, VBAT = 6.5V	-4.5		3.5	%
		IPRECHG = 480mA, VBAT = 6.5V	-8		8	%
		IPRECHG = 200mA, VBAT = 6.5V	-20		20	%
		IPRECHG = 120mA, VBAT = 6.5V	-30		30	%
I_{BAT_ACC}	IBAT pin current sensing accuracy with 25µA/A gain. The accuracy is applied to forward charging mode for charging current sensing, T_J = –40°C - 85°C	IBAT = 4A, VBAT = 8V	-5		5	%
		IBAT = 2A, VBAT = 8V	-7		7	%
		IBAT = 1A, VBAT = 8V	-10		10	%
		IBAT = 0.5A, VBAT = 8V	-20		20	%
I_{TERM_RANGE}	Typical termination current range		40		1000	mA
I_{TERM_STEP}	Typical termination current step			40		mA
I_{TERM_ACC}	Termination current accuracy, T_J = –40°C - 85°C	ITERM = 120mA, ICHG < 1000mA	-20		20	%
		ITERM = 480mA, ICHG > 1000mA	-14		14	%
V_{BAT_SHORTZ}	Battery short voltage rising threshold to start pre-charge	VBAT rising		2.25		V
V_{BAT_SHORT}	Battery short voltage falling threshold to stop pre-charge	VBAT falling		2.06		V
I_{BAT_SHORT}	Battery short trickle charging current	VBAT < V_{BAT_SHORTZ}		100		mA
$V_{BAT\_LOWV\_RISE}$	Battery voltage rising threshold to start fast-charge, as percentage of V_{REG}	VBAT_LOWV_1:0=00		15		%
		VBAT_LOWV_1:0=01		63.0		%
		VBAT_LOWV_1:0=10		68.0		%
		VBAT_LOWV_1:0=11		72.5		%
$V_{BAT\_LOWV\_HYS}$	Battery voltage threshold hysteresis to stop fast-charge on falling edge	VBAT falling, as percentage of VREG, VBAT_LOWV_1:0=11		1.4		%
V_{RECHG}	Battery recharge threshold	VBAT falling, VRECHG=0011, VREG=8.4V		200		mV
		VBAT falling, VRECHG=0111, VREG=16.8V		400		mV

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6.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BAT_LOAD}	Battery discharge load current			30		mA
I_{SYS_LOAD}	System discharge load current			30		mA
R_{BATP}	BATP Input Resistance			2.5		MΩ
R_{BATN}	BATN Input Resistance			3.3		MΩ
BATFET						
V_{BATFET_FWD}	BATFET forward voltage in supplement mode	BAT discharging current 10mA		30		mV
R_{BATFET}	MOSFET on resistance from SYS to BAT			8		mΩ
BATTERY PROTECTIONS						
V_{BAT_OVP}	Battery overvoltage threshold	VBAT rising, as percentage of VREG		104		%
		VBAT rising, VREG = 16.8V		17.47		V
		VBAT rising, VREG = 8.4V		8.74		V
		VBAT falling, as percentage of VREG		102		%
		VBAT falling, VREG = 16.8V		17.14		V
		VBAT falling, VREG = 8.4V		8.57		V
V_{BAT_SHORT}	Battery short voltage	VBAT falling, to clamp the charging current as trickle charging current.		2.06		V
		VBAT rising, to release the trickle charging current clamp		2.25		V
I_{BAT_OCP}	Battery discharging over-current rising threshold		9.3			A
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_RANGE}	Typical input voltage regulation range		3.6		22	V
V_{INDPM_STEP}	Typical input voltage regulation step			100		mV
V_{INDPM_ACC}	Input voltage regulation accuracy	VINDPM=18.6V	-2		2	%
		VINDPM=10.6V	-3		3	%
		VINDPM=4.3V	-5		5	%
I_{INDPM_RANGE}	Typical input current regulation range		0.1		3.3	A
I_{INDPM_STEP}	Typical input current regulation step			10		mA
I_{INDPM_ACC}	Input current regulation accuracy	IINDPM = 500mA, VBUS=9V	415	460	500	mA
		IINDPM = 1000mA, VBUS=9V	880	940	1000	mA
		IINDPM = 2000mA, VBUS=9V	1800	1880	1960	mA
		IINDPM = 3000mA, VBUS=9V	2720	2820	2920	mA
$V_{ILIM\_REG\_RNG}$	Voltage range for input current regultion at ILIM_HIZ pin		1		4	V
I_{LEAK_ILIM}	ILIM_HIZ pin leakage current	V_{ILIM_HIZ} = 4V	-1.5		1.5	µA
D+ / D- DETECTION						
$V_{D+\_600MVSRC}$	D+ voltage source (600 mV)		500	600	700	mV
$I_{D+\_10UASRC}$	D+ current source (10 µA)	V_{D+} = 200 mV,	7	10	14	µA
$I_{D+\_100UASNK}$	D+ current sink (100 µA)	V_{D+} = 500 mV,	50	90	150	µA
V_{D+_0P325}	D+ comparator threshold for Secondary Detection	D+ pin rising, DPDM_NSCOMP2	250		400	mV

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6.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{D+_0P8}	D+ comparator threshold for Data Contact Detection	D+ pin rising, DPDM_NSCOMP2	775	850	925	mV
I_{D+_LKG}	Leakage current into D+	HiZ mode	-1		1	µA
$V_{D-\_600MVSRC}$	D- voltage source (600 mV)		500	600	700	mV
$I_{D-\_100UASNK}$	D- current sink (100 µA)	V_{D-} = 500 mV,	50	90	150	µA
V_{D-_0P325}	D- comparator threshold for Primary Detection	D- pin Rising, DPDM_NSCOMP2	250		400	mV
I_{D-_LKG}	Leakage current into D-	HiZ mode	-1		1	µA
R_{D-_19K}	D- resistor to ground (19 kΩ)	V_{D-} = 500mV	14.25		24.8	kΩ
$V_{D+\_2p8\_hi}$	D+ high comparator threshold for 2.8V detection	D+ pin rising, DPDM_NSCOMP2	2.85	3	3.1	V
$V_{D+\_2p8\_lo}$	D+ low comparator threshold for 2.8V detection	D+ pin rising, NSCMP1Z	2.35	2.45	2.55	V
V_{D+_2p8}	D+ comparator threshold for non-standard adapter	(combined $V_{D+\_2p8\_hi}$ and $V_{D+\_2p8\_lo}$)	2.55		2.85	V
$V_{D-\_2p8\_hi}$	D- high comparator threshold for 2.8V detection	D- pin rising, DPDM_NSCOMP2	2.85	3	3.1	V
$V_{D-\_2p8\_lo}$	D- low comparator threshold for 2.8V detection	D- pin rising, NSCMP1Z	2.35	2.45	2.55	V
V_{D-_2p8}	D- comparator threshold for non-standard adapter	(combined VD-_2p8_hi and VD-_2p8_lo)	2.55		2.85	V
$V_{D+\_2p0\_hi}$	D+ high comparator threshold for 2.0V detection	D+ pin rising, DPDM_NSCOMP2	2.15	2.25	2.35	V
$V_{D+\_2p0\_lo}$	D+ low comparator threshold for 2.0V detection	D+ pin rising, NSCMP1Z	1.6	1.7	1.85	V
V_{D+_2p0}	D+ comparator threshold for non-standard adapter	(combined $V_{D+\_2p0\_hi}$ and $V_{D+\_2p0\_lo}$)	1.85		2.15	V
$V_{D-\_2p0\_hi}$	D- high comparator threshold for 2.0V detection	D- pin rising, DPDM_NSCOMP2	2.15	2.25	2.35	V
$V_{D-\_2p0\_lo}$	D- low comparator threshold for 2.0V detection	D- pin rising, NSCMP1Z	1.6	1.7	1.85	V
V_{D-_2p0}	D- comparator threshold for non-standard adapter	(combined $V_{D-\_2p0\_hi}$ and $V_{D-\_2p0\_lo}$)	1.85		2.15	V
$V_{D+\_1p2\_hi}$	D+ high comparator threshold for 1.2V detection	D+ pin rising, DPDM_NSCOMP2	1.35	1.5	1.6	V
$V_{D+\_1p2\_lo}$	D+ low comparator threshold for 1.2V detection	D+ pin rising, NSCPM1Z	0.85	0.95	1.05	V
V_{D+_1p2}	D+ comparator threshold for non-standard adapter	(combined $V_{D+\_1p2\_hi}$ and $V_{D+\_1p2\_lo}$)	1.05		1.35	V
$V_{D-\_1p2\_hi}$	D- high comparator threshold for 1.2V detection	D- pin rising, DPDM_NSCOMP2	1.35	1.5	1.6	V
$V_{D-\_1p2\_lo}$	D- low comparator threshold for 1.2V detection	D- pin rising, NSCMP1Z	0.85	0.95	1.05	V
V_{D-_1p2}	D- comparator threshold for non-standard adapter	(combined $V_{D-\_1p2\_hi}$ and $V_{D-\_1p2\_lo}$)	1.05		1.35	V
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	TREG = 120°C		120		°C
		TREG = 100°C		100		°C
		TREG = 80°C		80		°C
		TREG = 60°C		60		°C

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6.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SHUT}	Thermal shutdown rising threshold	Temperature increasing (TSHUT[1:0]=00)	130	150	170	°C
		Temperature increasing (TSHUT[1:0]=01)	110	130	150	°C
		Temperature increasing (TSHUT[1:0]=10)	100	120	140	°C
		Temperature increasing (TSHUT[1:0]=11)	65	85	105	°C
T_{SHUT_HYS}	Thermal shutdown falling hysteresis	Temperature decreasing by T_{SHUT_HYS}		30		°C
JEITA THERMISTOR COMPARATOR (CHARGE MODE)						
V_{T1_RISE}	T1 comparator rising threshold. Charge is suspended above this voltage.	As Percentage to REGN (0°C w/ 103AT)		73.3		%
V_{T1_FALL}	T1 comparator falling threshold. Charge is re-enabled below this voltage.	As Percentage to REGN (3°C w/ 103AT)		72		%
V_{T2_RISE}	T2 comparator rising threshold.	As Percentage of REGN, JEITA_T2=5°C w/ 103AT		71.1		%
		As Percentage of REGN, JEITA_T2=10°C w/ 103AT		68.4		%
		As Percentage of REGN, JEITA_T2=15°C w/ 103AT		65.5		%
		As Percentage of REGN, JEITA_T2=20°C w/ 103AT		62.4		%
V_{T2_FALL}	T2 comparator falling threshold.	As Percentage of REGN, JEITA_T2=5°C w/ 103AT		69.8		%
		As Percentage of REGN, JEITA_T2=10°C w/ 103AT		67.1		%
		As Percentage of REGN, JEITA_T2=15°C w/ 103AT		64.2		%
		As Percentage of REGN, JEITA_T2=20°C w/ 103AT		61.1		%
V_{T3_RISE}	T3 comparator rising threshold.	As Percentage of REGN, JEITA_T3=40°C w/ 103AT		49.7		%
		As Percentage of REGN, JEITA_T3=45°C w/ 103AT		46.1		%
		As Percentage of REGN, JEITA_T3=50°C w/ 103AT		42.5		%
		As Percentage of REGN, JEITA_T3=55°C w/ 103AT		39		%
V_{T3_FALL}	T3 comparator falling threshold.	As Percentage of REGN, JEITA_T3=40°C w/ 103AT		48.4		%
		As Percentage of REGN, JEITA_T3=45°C w/ 103AT		44.8		%
		As Percentage of REGN, JEITA_T3=50°C w/ 103AT		41.2		%
		As Percentage of REGN, JEITA_T3=55°C w/ 103AT		37.7		%
V_{T5_FALL}	T5 comparator falling threshold. Charge is suspended below this voltage.	As Percentage of REGN (60°C w/ 103AT)		34.2		%
V_{T5_RISE}	T5 comparator rising threshold. Charge is re-enabled above this voltage.	As Percentage of REGN (58°C w/ 103AT)		35.5		%

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6.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COLD / HOT THERMISTOR COMPARATOR (OTG MODE)						
V_{BCOLD_RISE}	TCOLD comparator rising threshold.	As Percentage of REGN (–20°C w/ 103AT)		80.0		%
		As Percentage of REGN (–10°C w/ 103AT)		77.1		%
V_{BCOLD_FALL}	TCOLD comparator falling threshold.	As Percentage of REGN (–20°C w/ 103AT)		78.7		%
		As Percentage of REGN (–10°C w/ 103AT)		75.8		%
V_{BHOT_FALL}	THOT comparator falling threshold.	As Percentage of REGN, (55°C w/ 103AT)		37.7		%
		As Percentage of REGN, (60°C w/ 103AT)		34.4		%
		As Percentage of REGN, (65°C w/ 103AT)		31.3		%
V_{BHOT_RISE}	THOT comparator rising threshold.	As Percentage of REGN, (55°C w/ 103AT)		39.3		%
		As Percentage of REGN, (60°C w/ 103AT)		35.7		%
		As Percentage of REGN, (65°C w/ 103AT)		32.5		%
SWITCHING CONVERTER						
F_{SW}	PWM switching frequency	Oscillator frequency		1.5		MHz
				750		kHz
I_{IN_SS}	Input current limit during converter start up	VSYS below 2.2V, IINDPM above 500mA			500	mA
$V_{BTST\_REFRESH}$	Bootstrap refresh comparator threshold	VBTST1-VSW1 when Q2 refresh pulse is requested, VBUS = 15V		3.0		V
		VBTST2-VSW2 when Q3 refresh pulse is requested, VBUS = 15V		3.0		V
V_{F_D}	Integrated BTST diode forward bias voltage	IF=20mA at 25 °C		0.8		V
				0.8		V
V_{R_D}	Integrated BTST diode reverse breakdown voltage	IR=2µA at 25 °C		20		V
				20		V
SENSE RESISTANCE and MOSFET Rdson						
R_{SNS}	VBUS to PMID input sensing resistance	T_j = -40°C-85°C (typical value is under 25°C)		6		mΩ
R_{Q1_ON}	Buck high-side switching MOSFET turnon resistance between PMID and SW1	T_j = -40°C-85°C (typical value is under 25°C)		24		mΩ
R_{Q2_ON}	Buck low-side switching MOSFET turnon resistance between SW1 and PGND	T_j = -40°C-85°C (typical value is under 25°C)		35		mΩ
R_{Q3_ON}	Boost low-side switching MOSFET turnon resistance between SW2 and PGND	T_j = -40°C-85°C (typical value is under 25°C)		28		mΩ
R_{Q4_ON}	Boost high-side switching MOSFET turnon resistance between SW2 and SYS	T_j = -40°C-85°C (typical value is under 25°C)		17		mΩ
MOSFET CYCLE-BY-CYCLE CURRENT LIMIT						
I_{Q1_CBC}	Q1 cycle by cycle current limit		7.5			A

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6.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{Q2_CBC}	Q2 cycle by cycle current limit		10			A
I_{Q3_CBC}	Q3 cycle by cycle current limit		10			A
I_{Q4_CBC}	Q4 cycle by cycle current limit		7.5			A
OTG MODE CONVERTER						
V_{OTG_RANGE}	Typical OTG mode voltage regulation range		2.8		22	V
V_{OTG_STEP}	Typical OTG mode voltage regulation step			10		mV
V_{OTG_ACC}	OTG mode voltage regulation accuracy	IVBUS = 0A, VOTG = 20V	-3		3	%
		IVBUS = 0A, VOTG = 12V	-2.5		3	%
		IVBUS = 0A, VOTG = 5V	-2		3	%
I_{OTG_RANGE}	Typical OTG mode current regulation range		0.12		3.32	A
I_{OTG_STEP}	Typical OTG mode current regulation step			40		mA
I_{OTG_ACC}	OTG mode current regulation accuracy	IOTG = 3.0A	-2.2		2.2	%
		IOTG = 1.52A	-5		3	%
		IOTG = 0.52A	-15		8	%
V_{OTG_UVP}	OTG mode under voltage falling threshold			2.2		V
V_{OTG_OVP}	OTG mode overvoltage rising threshold	As percentage of VOTG regulation, OTG mode OOA disabled.		113		%
	OTG mode overvoltage falling threshold	As percentage of VOTG regulation		98		%
I_{OTG_BAT}	Battery current regulation in OTG mode	IBAT_REG_1:0 = 00, VBAT=8V, VOTG=9V	2.8	3	3.2	A
		IBAT_REG_1:0 = 01, VBAT=8V, VOTG=9V	3.8	4	4.2	A
		IBAT_REG_1:0 = 10, VBAT=8V, VOTG=9V	4.8	5	5.3	A
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5V, I_{REGN} = 20mA	4.6	4.8	5	V
		V_{VBUS} = 15V, I_{REGN} = 20mA	4.8	5	5.2	V
I_{REGN}	REGN LDO current limit	V_{VBUS} = 5V, V_{REGN} = 4.5V	30			mA
I2C INTERFACE (SCL, SDA)						
V_{IH_SDA}	Input high threshold level, SDA	Pull up rail 1.8V	1.3			V
V_{IL_SDA}	Input low threshold level	Pull up rail 1.8V			0.4	V
V_{OL_SDA}	Output low threshold level	Sink current = 5mA			0.4	V
I_{BIAS_SDA}	High-level leakage current	Pull up rail 1.8V			1	µA
V_{IH_SCL}	Input high threshold level, SDA	Pull up rail 1.8V	1.3			V
V_{IL_SCL}	Input low threshold level	Pull up rail 1.8V			0.4	V
V_{OL_SCL}	Output low threshold level	Sink current = 5mA			0.4	V
I_{BIAS_SCL}	High-level leakage current	Pull up rail 1.8V			1	µA
LOGIC I PIN ($\overline{CE}$, ILIM_HIZ, $\overline{QON}$)						
V_{IH_CE}	Input high threshold level, $\overline{CE}$		1.3			V
V_{IL_CE}	Input low threshold level, $\overline{CE}$				0.4	V
$I_{IN\_BIAS\_CE}$	High-level leakage current, $\overline{CE}$	Pull up rail 1.8V			1	µA

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6.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH_QON}	Input high threshold level, $\overline{QON}$		1.3			V
V_{IL_QON}	Input low threshold level, $\overline{QON}$				0.4	V
V_{QON}	Internal $\overline{QON}$ pull up	$\overline{QON}$ is pulled up internally		3.2		V
R_{QON}	Internal $\overline{QON}$ pull up resistance			200		kΩ
$V_{IH\_ILIM\_HIZ}$	Input high threshold level, ILIM_HIZ		1			V
$V_{IL\_ILIM\_HIZ}$	Input low threshold level, ILIM_HIZ				0.75	V
LOGIC O PIN ($\overline{INT}$, $\overline{PG}$, STAT)						
V_{OL_INT}	Output low threshold level, $\overline{INT}$	Sink current = 5mA			0.4	V
$I_{OUT\_BIAS\_INT}$	High-level leakage current, $\overline{INT}$	Pull up rail 1.8V			1	μA
V_{OL_STAT}	Output low threshold level, STAT	Sink current = 5mA			0.4	V
$I_{OUT\_BIAS\_STAT}$	High-level leakage current, STAT	Pull up rail 1.8V			1	μA
ADC MEASUREMENT ACCURACY AND PERFORMANCE						
t_{ADC_CONV}	Conversion time, each measurement	ADC_SAMPLE[1:0] = 00		24		ms
		ADC_SAMPLE[1:0] = 01		12		ms
		ADC_SAMPLE[1:0] = 10		6		ms
		ADC_SAMPLE[1:0] = 11		3		ms
ADC_{RES}	Effective resolution	ADC_SAMPLE[1:0] = 00	14	15		bits
		ADC_SAMPLE[1:0] = 01	13	14		bits
		ADC_SAMPLE[1:0] = 10	12	13		bits
		ADC_SAMPLE[1:0] = 11	10	11		bits
ADC MEASUREMENT RANGE AND LSB						
ADC_{IBUS_RANGE}	ADC VBUS current reading range (forward and OTG)	Range	0		5	A
ADC_{IBUS_STEP}	ADC VBUS current reading step (forward and OTG)	LSB		1		mA
ADC_{VBUS_RANGE}	ADC VBUS voltage reading range	Range	0		30	V
ADC_{VBUS_STEP}	ADC VBUS voltage reading step	LSB		1		mV
ADC_{VAC_RANGE}	ADC VAC voltage reading range	Range	0		30	V
ADC_{VAC_STEP}	ADC VAC voltage reading step	LSB		1		mV
ADC_{VBAT_RANGE}	ADC BAT voltage reading range	Range	0		20	V
ADC_{VBAT_STEP}	ADC BAT voltage reading step	LSB		1		mV
ADC_{VSYS_RANGE}	ADC SYS voltage reading range	Range	0		24	V
ADC_{VSYS_STEP}	ADC SYS voltage reading step	LSB		1		mV
ADC_{IBAT_RANGE}	ADC BAT current reading range	Range	0		8	A
ADC_{IBAT_STEP}	ADC BAT current reading step	LSB		1		mA
ADC_{TS_RANGE}	ADC TS voltage reading range	Range	0		99.9	%
ADC_{TS_STEP}	ADC TS voltage reading step	LSB		0.098		%
ADC_{TDIE_RANGE}	ADC die temperature reading range	Range	-40		150	°C
ADC_{TDIE_STEP}	ADC die temperature reading step	LSB		0.5		°C

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6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
BATTERY CHARGER						
t_{TOP_OFF}	Top-off timer accuracy		12	15	18	min
			24	30	36	min
			36	45	54	min
t_{SAFETY_TRKCHG}	Charge safety timer in trickle charge		0.9	1	1.1	hr
t_{SAFETY_PRECHG}	Charge safety timer in pre-charge	PRECHG_TMR = 0	1.8	2	2.2	hr
t_{SAFETY}	Charge safety timer accuracy	CHG_TMR[1:0] = 00	4.5	5	5.5	hr
		CHG_TMR[1:0] = 01	7.2	8	8.8	hr
		CHG_TMR[1:0] = 10	10.8	12	13.2	hr
		CHG_TMR[1:0] = 11	21.6	24	26.4	hr
I2C INTERFACE						
f_{SCL}	SCL clock frequency				1000	kHZ
WATCHDOG TIMER						
t_{LP_WDT}	Watchdog reset time	EN_HIZ = 1, WATCHDOG = 160s	100	160		s
t_{WDT}	Watchdog reset time	EN_HIZ = 0, WATCHDOG = 160s	136	160		s

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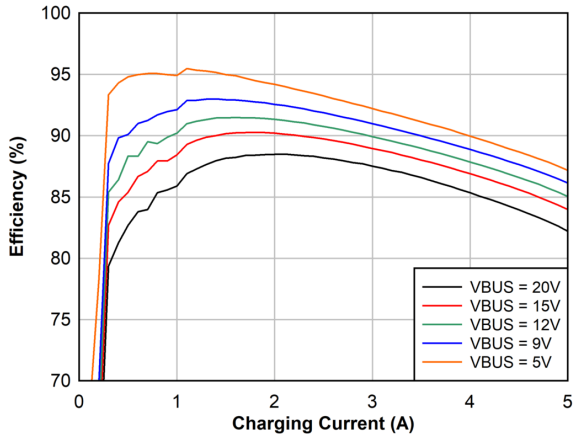
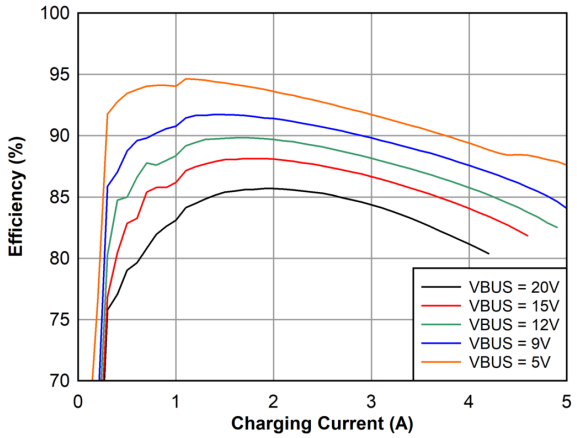
6.7 Typical Characteristics

C_{VBUS} = 2*10µF, C_{PMID}= 3*10µF, C_{SYS} = 5*10µF, C_{BAT} = 2*10µF, L1 = 1µH (SPM6530T-1R0M120) and L2 = 2.2µH (WE-LHMI-74437346022)



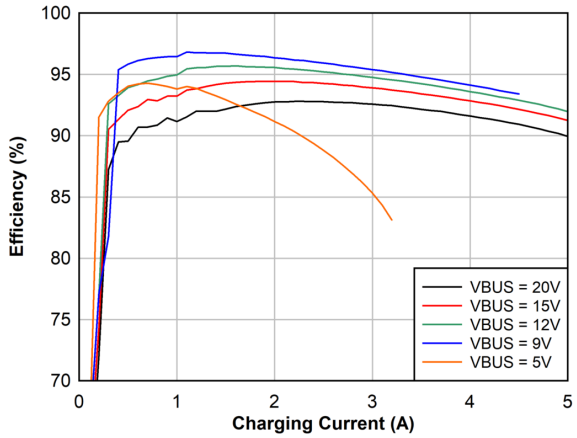
VBAT = 4V, Fsw = 750 kHz with L1 = 2.2µH, PFM disabled

Figure 6-1. 1s Battery Charge Efficiency, 750 kHz



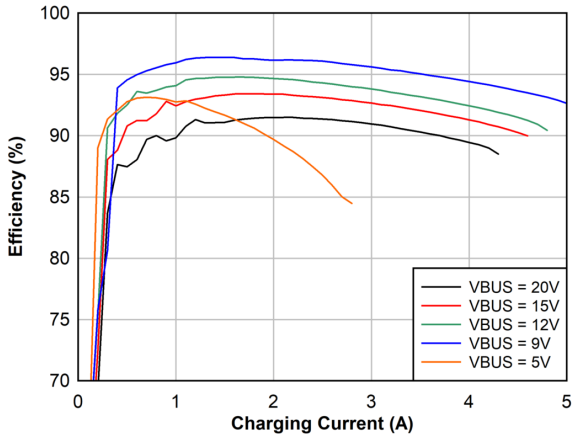
VBAT = 4V, Fsw = 1.5 MHz with L1 = 2.2µH, PFM disabled

Figure 6-2. 1s Battery Charge Efficiency, 1.5 MHz



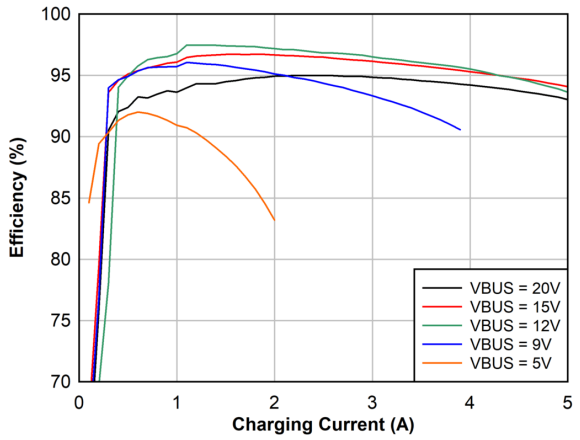
VBAT = 8V, Fsw = 750 kHz with L1 = 2.2µH, PFM disabled

Figure 6-3. 2s Battery Charge Efficiency, 750 kHz



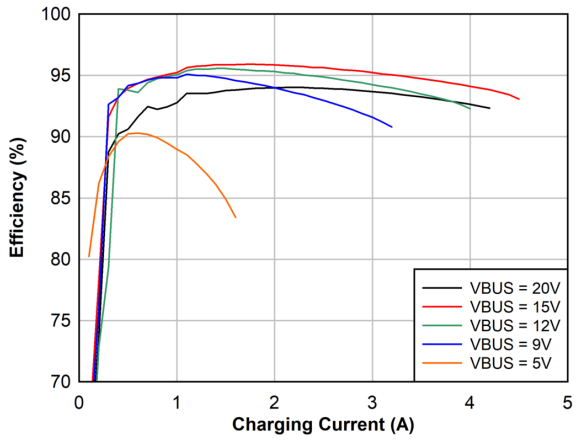
VBAT = 8V, Fsw = 1.5 MHz with L1 = 1µH, PFM disabled

Figure 6-4. 2s Battery Charge Efficiency, 1.5 MHz



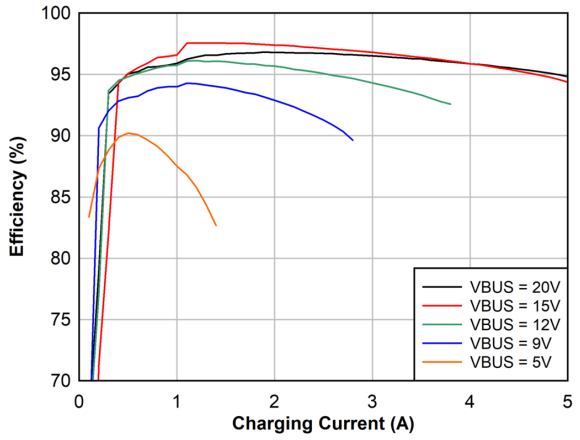
VBAT = 12V, Fsw = 750 kHz with L1 = 2.2µH, PFM disabled

Figure 6-5. 3s Battery Charge Efficiency, 750 kHz



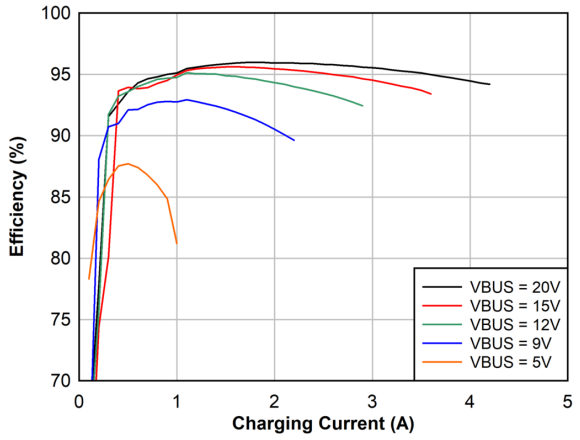
VBAT = 12V, Fsw = 1.5 MHz with L1 = 1µH, PFM disabled

Figure 6-6. 3s Battery Charge Efficiency, 1.5 MHz



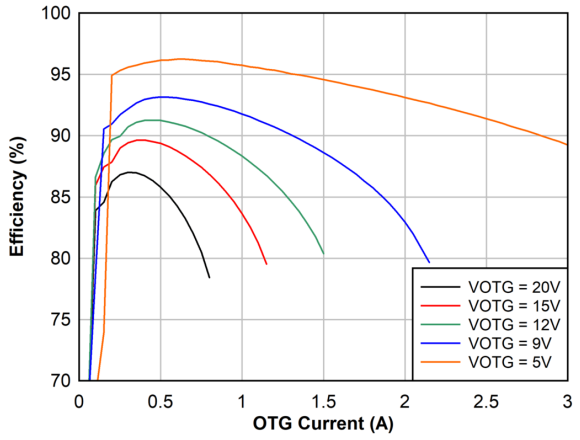
VBAT = 16V, Fsw = 750 kHz with L1 = 2.2µH, PFM disabled

Figure 6-7. 4s Battery Charge Efficiency, 750 kHz



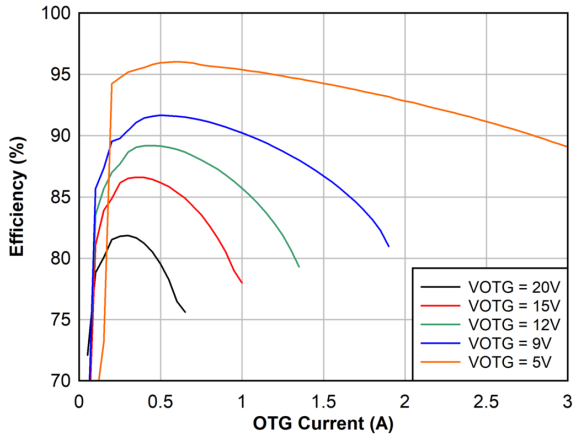
VBAT = 16V, Fsw = 1.5 MHz with L1 = 1µH, PFM disabled

Figure 6-8. 4s Battery Charge Efficiency, 1.5 MHz



VBAT = 4.2V, Fsw = 750 kHz with L1 = 1µH, PFM disabled

Figure 6-9. 1s Battery OTG Efficiency, 750 kHz



VBAT = 4.2V, Fsw = 1.5 MHz with L1 = 1µH, PFM disabled

Figure 6-10. 1s Battery OTG Efficiency, 1.5 MHz

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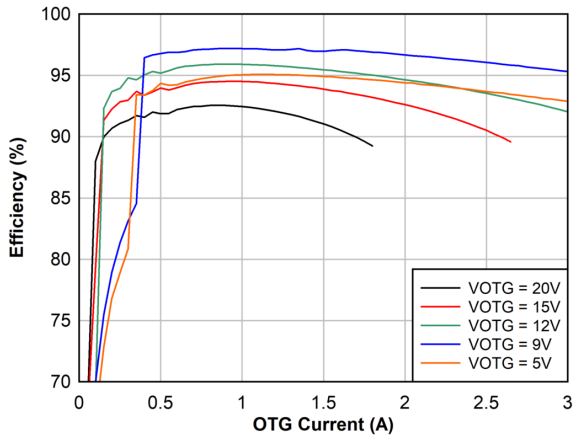
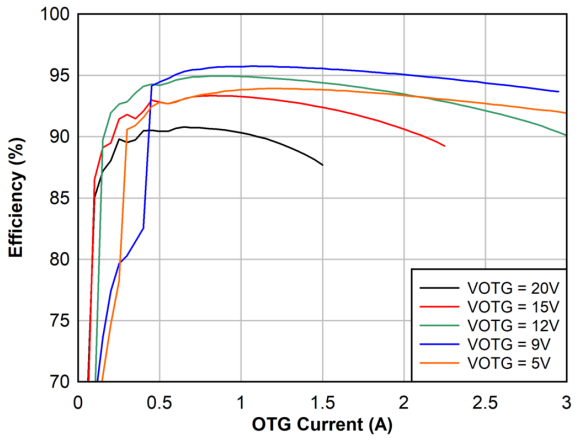


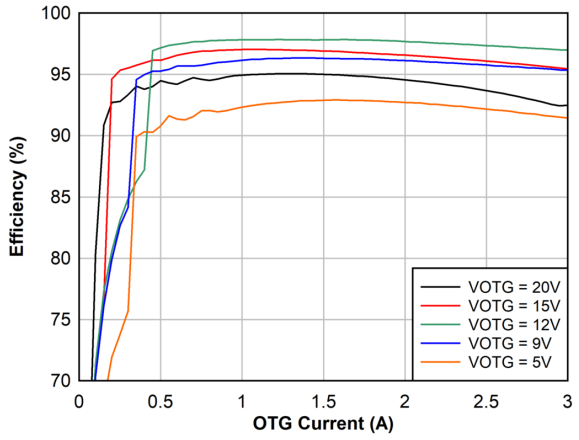
VBAT = 8.4V, Fsw = 750 kHz with L1 = 2.2µH, PFM disabled

Figure 6-11. 2s Battery OTG Efficiency, 750 kHz



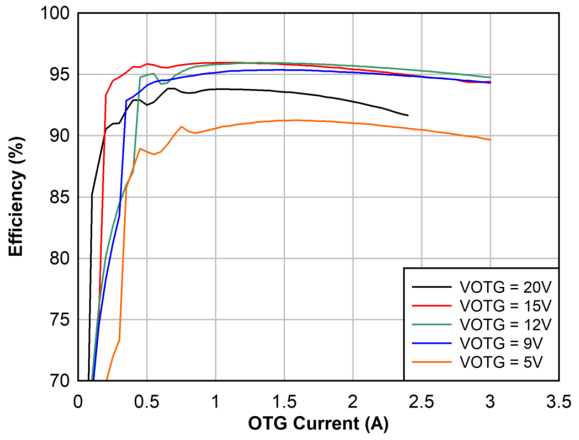
VBAT = 8.4V, Fsw = 1.5MHz with L1 = 1µH, PFM disabled

Figure 6-12. 2s Battery OTG Efficiency, 1.5 MHz



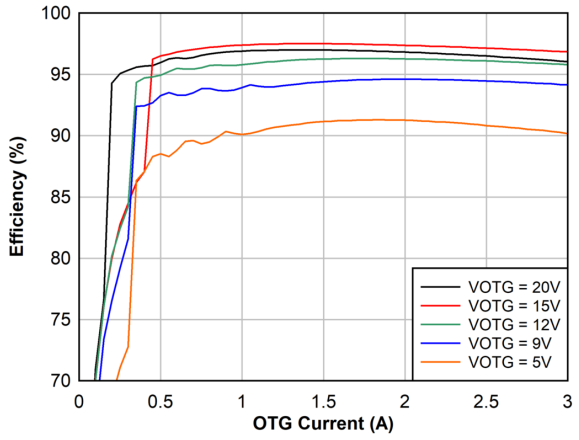
VBAT = 12.6V, Fsw = 750 kHz with L1 = 2.2µH, PFM disabled

Figure 6-13. 3s Battery OTG Efficiency, 750 kHz



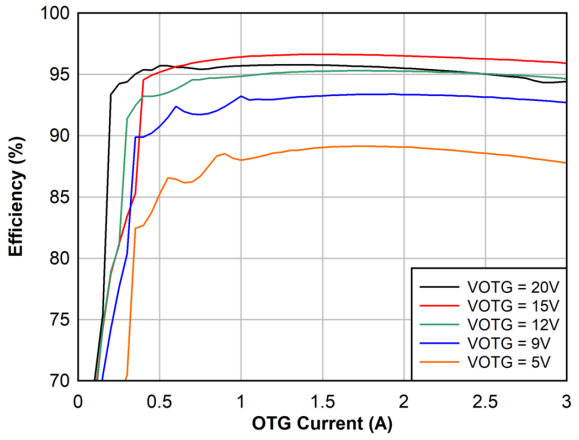
VBAT = 12.6V, Fsw = 1.5 MHz with L1 = 1µH, PFM disabled

Figure 6-14. 3s Battery OTG Efficiency, 1.5 MHz



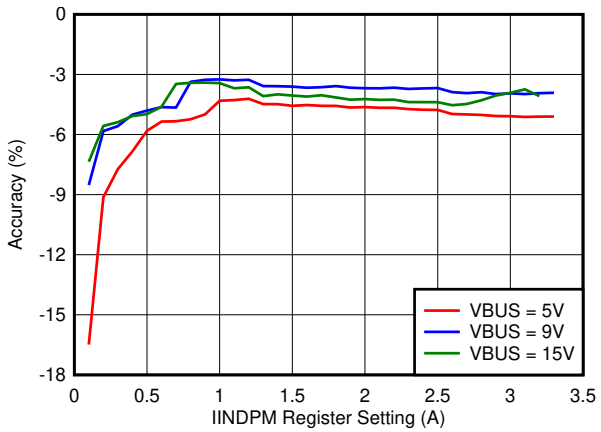
VBAT = 16.8V, Fsw = 750 kHz with L1 = 2.2µH, PFM disabled

Figure 6-15. 4s Battery OTG Efficiency, 750 kHz



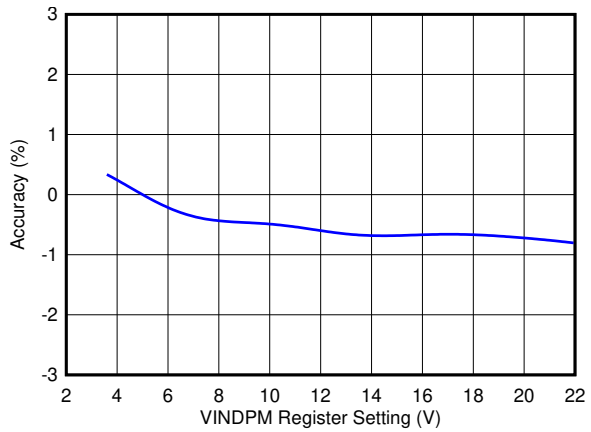
VBAT = 16.8V, Fsw = 1.5 MHz with L1 = 1µH, PFM disabled

Figure 6-16. 4s Battery OTG Efficiency, 1.5 MHz



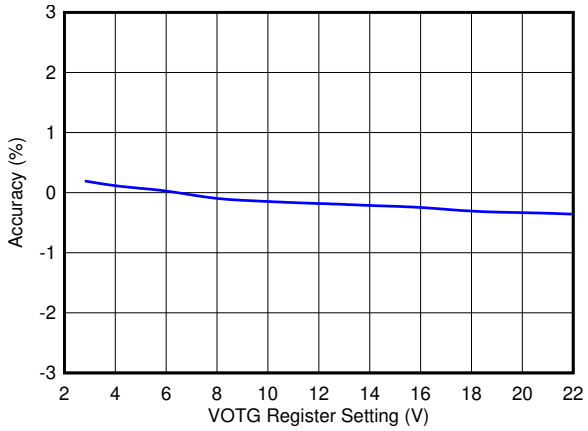
VBAT = 8V, Fsw = 1.5MHz with L1 = 1µH

Figure 6-17. Input Current Regulation (IINDPM) Accuracy



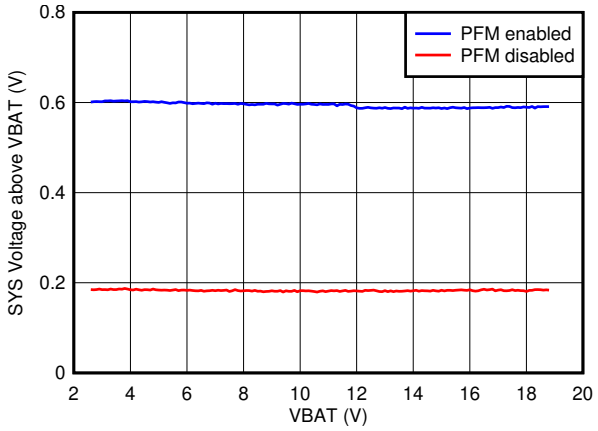
VBAT = 8V, Fsw = 1.5MHz with L1 = 1µH

Figure 6-18. Input Voltage Regulation (VINDPM) Accuracy



VBAT = 8.4V, Fsw = 1.5MHz with L1 = 1µH

Figure 6-19. OTG Voltage Regulation (VOTG) Accuracy



VBUS = 9V, Fsw = 1.5MHz with L1 = 1µH, ISYS = 0A, Charge Disabled

Figure 6-20. Offset Voltage of SYS Regulation above VBAT

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7 Detailed Description

7.1 Overview

The BQ25798 is a fully integrated, switch-mode buck charger for a 1 cell ~ 4 cell Li-ion battery and Li-polymer battery. For compact design and minimum component count, the charger integrates the 4 switching MOSFETs (Q_1, Q_2, Q_3, Q_4), input and charging current sensing circuits, the battery FET (BATFET) and all the loop compensation of the buck-boost converter. It provides high power density and design flexibility to charge batteries across the full input voltage range for USB Type-C™ and USB-PD applications such as digital cameras, drones and mobile printers.

The charger supports narrow VDC (NVDC) power path management, in which the system is regulated at a voltage slightly higher than the battery voltage, without dropping below a configurable minimum system voltage. The system keeps operating even when the battery is completely discharged or removed. When load power exceeds the input source rating, the battery gets into supplement mode and prevents the input source from being overloaded and the system from crashing.

The device charges a battery from a wide range of input sources including legacy USB adapter to high voltage USB-PD adapter and traditional barrel adapter. The charger seamlessly transitions between buck, boost and buck-boost modes based on input voltage and battery voltage without host control. The optional dual-input source selector manages the power flowing from two different input sources, prioritizing the first available input source. The host may manually transition between input sources using I^2C.

To support fast charging using adjustable high voltage adapter (HVDCP), the device provides D+/D- handshake. The device is compliant with USB 2.0 and USB 3.0 power delivery specification with input current and voltage regulation. In addition, the Input Current Optimizer (ICO) allows the detection of maximum power point of an unknown input source. The BQ24798 also features a Maximum Power Point Tracking (MPPT) algorithm to optimize the energy drawn from a low-power photovoltaic panel. This MPPT algorithm measures the open-circuit voltage of the panel on a user-configurable period, then adjusts the VINDPM using the VOC_PCT setting to calculate the maximum power point as a percentage of the measured open-circuit voltage.

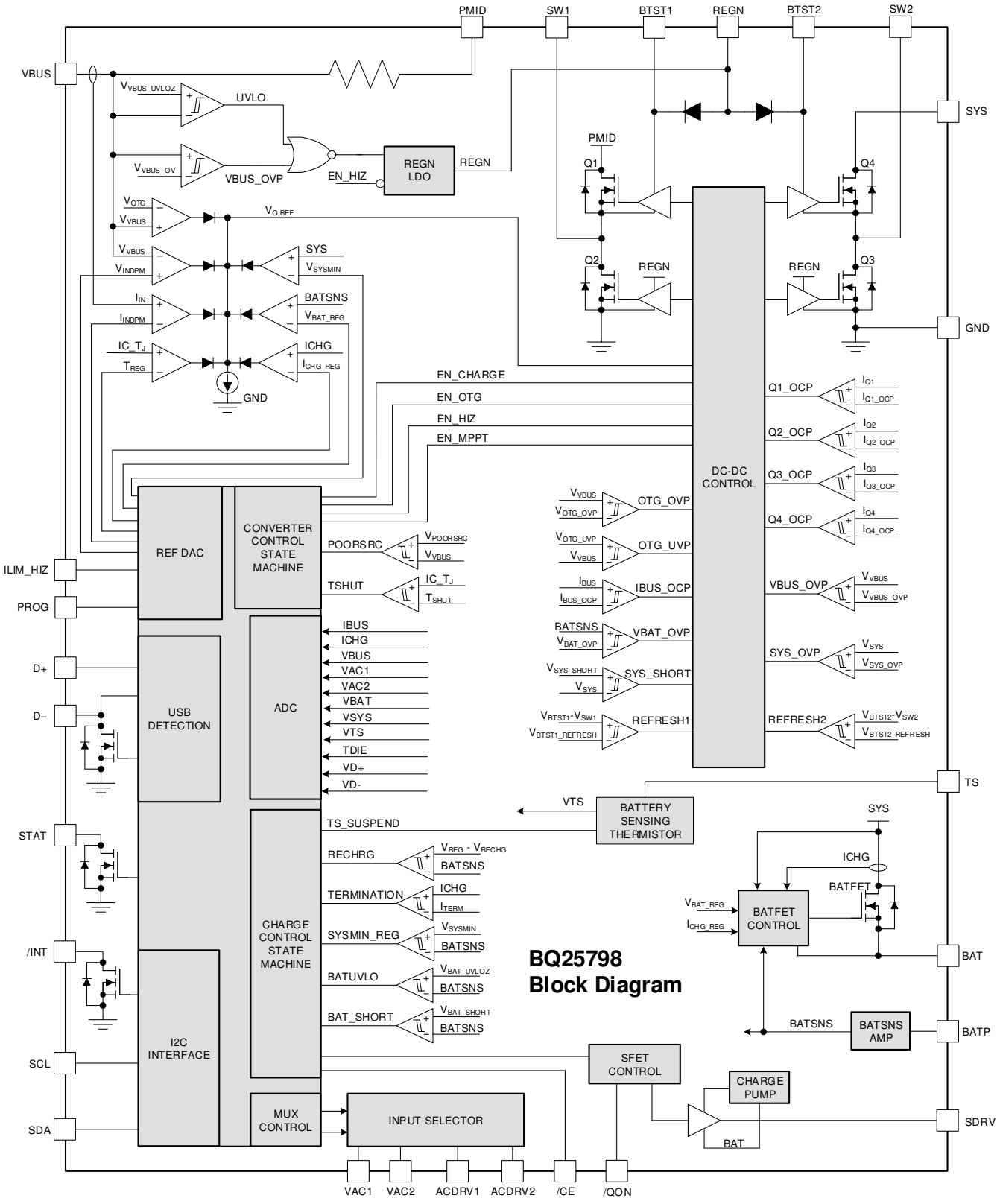
In addition to the I^2C host controlled charging mode, BQ25798 also supports autonomous charging mode. After power up, the charging is defaulted enabled with all the registers default settings. The device can complete a charging cycle without any software engagements. It detects battery voltage and charges the battery in different phases: trickle charging, pre-charging, constant current (CC) charging and constant voltage (CV) charging. At the end of the charging cycle, the charger automatically terminates when the charge current is below a pre-set limit (termination current) in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle.

In the absence of input sources, BQ25798 supports USB On-the-Go (OTG) function, discharging the battery to generate an adjustable 2.8V~22V voltage on VBUS with 10mV step size. This is compliant with the USB PD 3.0 specification defined PPS feature.

The charger provides various safety features for battery charging and system operations, including battery temperature negative thermistor (NTC) monitoring, trickle charge, pre-charge and fast charge timers and over-voltage/over-current protections on the battery and the charger power input pin. The thermal regulation reduces charge current when the die temperature exceeds a programmable threshold. The STAT output of the device reports the charging status and any fault conditions. The $\overline{INT}$ pin immediately notifies the host when a fault occurs.

The device also provides a 16-bit analog-to-digital converter (ADC) for monitoring charge current and input/ battery/system voltages, the TS pin voltage and the die temperature. It is available in a 29-pin 4.0 mm x 4.0 mm QFN package.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Device Power-On-Reset

The internal bias circuits of the BQ25798 are powered from the higher of either V_{VBUS} or V_{BAT} through an integrated power selector. The valid voltage to power up the device has to be greater than V_{VBUS_UVLOZ} when powering from VBUS or V_{BAT_UVLOZ} when powering from BAT. When $V_{VBUS} < V_{VBUS\_UVLOZ}$, $V_{BAT} < V_{BAT\_UVLOZ}$ and a voltage higher than $V_{AC\_PRESENT}$ is present at either VAC1 or VAC2, the device will be powered from V_{AC1} or V_{AC2}, depending on which comes first.

7.3.2 PROG Pin Configuration

At POR, the charger detects the PROG pin pull down resistance, then sets the charger default POR switching frequency and the battery cell count. Please follow the resistance list in Table 7-1 to set the desired POR switching frequency and battery cell count. The surface mount resistor with ±1% or ±2% tolerance is recommended.

Table 7-1. PROG Pin Resistance to Set Default Switching Frequency and Battery Cell Count

SWITCHING FREQUENCY	CELL COUNT	TYPICAL RESISTANCE AT PROG PIN
1.5 MHz	1s	3.0 kΩ
750 kHz	1s	4.7 kΩ
1.5 MHz	2s	6.04 kΩ
750 kHz	2s	8.2 kΩ
1.5 MHz	3s	10.5 kΩ
750 kHz	3s	13.7 kΩ
1.5 MHz	4s	17.4 kΩ
750 kHz	4s	27.0 kΩ

Some of the charging parameters default values are determined by the battery cell count identified by PROG pin configuration, which are summarized in the table below.

Table 7-2. Charging Parameters Dependent on Battery Cell Count

CELL (REG0x0A[7:6])	1s	2s	3s	4s
ICHG (REG0x03/04)	2 A	2 A	1 A	1 A
VSYSMIN (REG0x00[5:0])	3.5 V	7 V	9 V	12 V
VREG (REG0x01/02)	4.2 V	8.4 V	12.6 V	16.8 V
VREG Range	3 V - 4.99 V	5 V - 9.99 V	10 V - 13.99 V	14 V - 18.8 V

After POR, the host can program the ICHG and VSYSMIN registers to any values within the ranges defined in the register tables. However, when programming the battery charging voltage (VREG), the host must ensure the VREG value is in the allowed range associated with the CELL register (REG0x0A[7:6]) setting defined in the table above. When the CELL register is changed, the ICHG, VSYSMIN and VREG registers are reset to the POR default values associated with the CELL setting.

For example, if the PROG pin resistance is a 2s battery configuration, the default POR CELL, ICHG, VSYSMIN and VREG settings will be 2s, 2 A, 7 V and 8.4 V respectively. After POR, the host can change ICHG and VSYSMIN to any values, and can change VREG to any value between 5V and 9.99V. Assuming that the CELL bits remain at the 2s battery configuration, then when the REG_RST bit is set or the watchdog timer expires, the registers are reset to default values with ICHG, VSYSMIN and VREG automatically returing to 2 A, 7V and 8.4V respectively.

When the CELL register is 2s battery configuration, any write out of the range of VREG (5 V - 9.99 V) is ignored by the charger. If VREG needs to be programmed out of the 5 V - 9.9 V range, such as 11 V, the CELL bits have to be changed to the 3s setting. Setting the CELL bits will also cause the ICHG, VSYSMIN and VREG registers to reset to their 3s POR default values of 1 A, 9 V and 12.6 V. Then the host can program VREG in the range of

10 V - 13.99 V. If, after changing the CELL bits to 3S, the REG_RST bit is set or the watchdog timer expires, the ICHG, VSYSMIN and VREG will then be reset to 1 A, 9 V and 12.6 V, regardless of the state of the PROG pin.

7.3.3 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above UVLO threshold (V_{BAT_UVLOZ}), the BATFET turns on and connects the battery to the system. The REGN LDO stays off to minimize the quiescent current. The low $R_{DS(ON)}$ of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The POR sequence when the charger is powered from V_{BAT} is described as below:

1. 5 ms (typical) after $V_{BAT} > V_{BAT\_UVLOZ}$, the charger starts ACFET-RBFET detection, reads the resistance at the PROG pin, and then configures the charger POR register set accordingly.
2. 20 ms (typical) after $V_{BAT} > V_{BAT\_UVLOZ}$, the I^2C registers become accessible to the host..
3. The charger turns the battery FET on to allow the battery to power the system.

7.3.4 Device Power Up from Input Source

When an input source is present at VBUS, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck-boost converter is started. The power up sequence from input source is as listed below:

1. The device begins the POR sequence when $V_{VBUS} > V_{VBUS\_UVLOZ}$ if there is a direct path from input to VBUS, or otherwise when V_{AC1} or $V_{AC2} > V_{AC\_PRESENT}$.
2. 5 ms (typical) after a valid voltage is first present at either VBUS or VAC1/VAC2 pins, the charger starts the ACFET-RBFET detection, reads the resistance at PROG pin, and then configures the charger power on reset (POR) default register settings accordingly.
3. If ACFET-RBFET are detected on the input source pathway, the corresponding ACDRV turns on the pair.
4. 20 ms (typical) after valid voltage voltage presence, the I^2C registers become accessible to the host.
5. As soon as $V_{VBUS} > V_{VBUS\_UVLOZ}$ (in step 1 or after step 3), VBUS_PRESENT_STAT is set to 1. 150 ms (typical) later, REGN is turned on.
6. Once REGN is on, the charger starts the poor source detection. After a good input source is detected (typically 30 ms if there is no retry), PG_STAT is set to 1, then the ADC reads the ILIM_HIZ pin voltage and VBUS voltage and updates the IINDPM and VINDPM registers accordingly.
7. When the poor source detection completes, the charger performs D+/D- detection and updates the VBUS_STAT and IINDPM registers accordingly.
8. 30 ms (typical) after the D+/D- detection completes, the converter starts switching to power SYS and charge the battery.

7.3.4.1 Power Up REGN LDO

When the device is powered up from VBUS, the LDO is turned on when $V_{VBUS\_PRESENT} < VBUS < V_{VBUS\_OVP}$. When the device is powered up from battery only condition, the LDO is turned on at either one of the following conditions:

- The charger is operated in the OTG mode
- VBAT is higher than 3.2V, and ADC TS channel is on (ADC_EN = 1 and TS_ADC_DIS = 0)

The REGN LDO supplies internal bias circuits and the MOSFETs gate drivers. The pull-up rails of ILIM_HIZ, TS, and STAT can be connected to REGN. The $\overline{INT}$ pin pull-up rail is recommended to be an external 1.8V or 3.3V voltage source, rather than REGN, because at battery only condition, the REGN might not be available. Except the charger related pull up rails, the REGN is not recommended to source any other external circuit. The REGN has to power the internal MOSFETs gate drivers, which is very critical for the charger normal operation.

7.3.4.2 Poor Source Qualification

After the REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to move forward to the next power on steps.

1. VBUS voltage below V_{VBUS_OVP}
2. VBUS voltage above $V_{POORSRC}$ when pulling $I_{POORSRC}$ (typical 30 mA)

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Once the conditions are met, the status register bit PG_STAT is set high and the $\overline{INT}$ pin is pulsed to signal the host.

If VBUS_OVP is detected (failing condition 1 above), an $\overline{INT}$ pulse is asserted to alert the host if the VBUS_OVP_MASK = 0 or the PG_MASK = 0. The VBUS_OVP_STAT and VBUS_OV_FLAG fault registers get set, and the PG_STAT bit remains low. The device automatically retries input source qualification once the over-voltage fault goes away.

If a poor source is detected (when pulling $I_{POORSRC}$, the VBUS voltage drops below $V_{POORSRC}$), the EN_HIZ bit is set to 1, PG_STAT bit remains low, PG_FLAG will be set to 1, and an $\overline{INT}$ pulse will be asserted if PG_MASK = 0. The device will repeat the poor source qualification routine every 10 minutes until either the adapter is removed or the source is qualified. Each failed poor source qualification will cause EN_HIZ and PG_FLAG to be set to 1, and an $\overline{INT}$ pulse will be asserted if PG_MASK = 0. In the 10 minute interim between poor source qualification attempts, the host may set EN_HIZ = 0 to force an immediate retry of the poor source qualification. The EN_HIZ bit is cleared automatically when the adapter is plugged in, so cycling the adapter will also force an immediate retry of the poor source qualification.

7.3.4.3 ILIM_HIZ Pin

At POR, before the charger converter starts switching, the charger ADC reads the ILIM_HIZ pin voltage, and calculates the input current limit (ILIM) set by this ILIM_HIZ pin, according to:

$$V_{ILIM\_HIZ} = 1V + 800\ m\Omega \times ILIM \quad (1)$$

The ILIM_HIZ pin sets a high clamp for the IINDPM register. If the IINDPM setting from the D+/D- detection or the POR default 3A IINDPM setting is higher than the ILIM clamp, the IINDPM register stays at this ILIM clamp. In addition, the host cannot program the IINDPM register to any values higher than this ILIM clamp after POR, unless the register bit EN_EXTILIM is set to 0.

The ILIM_HIZ pin can be biased from a resistor voltage divider tied to either REGN or another external voltage source. For both the forward charging mode and the OTG mode, when the ILIM_HIZ pin is pulled lower than 0.75V, the charger stops switching and REGN stays on. The charger resumes switching if the ILIM_HIZ pin voltage becomes higher than 1V.

If the ADC reads the ILIM_HIZ pin voltage is lower than 1.08V (1V + 800 mΩ × 100 mA), the charger considers the ILIM clamp to be 100mA, which is the minimal setting of the IINDPM register.

7.3.4.4 Default VINDPM Setting

In the POR sequence, right after the D+/D- detection, the charger initiates an ADC reading on the VBUS pin voltage without any load current (VBUS at no load condition, $VBUS_0$) before the converter starts switching. The default VINDPM threshold is set to be $VBUS_0$ - 1.4 V ($VBUS_0$ >= 7 V) or $VBUS_0$ - 0.7V ($VBUS_0$ < 7 V).

The $VBUS_0$ can be remeasured at any time by setting the register bit FORCE_VINDPM_DET=1. The converter stops switching, the ADC measures the VBUS voltage, the VINDPM register field is updated, and then the FORCE_VINDPM_DET bit returns to 0. The force VINDPM detection only can be done when VSYS_STAT = 0 (VBAT > VSYSMIN), otherwise stopping the converter would cause VSYS to drop below VSYSMIN. If VSYS_STAT = 1 (VBAT < VSYSMIN), $VBUS_0$ measurement does not start, the FORCE_WINDPM_DET bit resets to 0 and the VINDPM register retains its current value. The host must ensure there is a battery present prior to setting FORCE_VINDPDM_DET = 1, or to allow system to be supported by the battery during detection.

When the measured $VBUS_0$ is out of the VINDPM register range, the changer sets the VINDPM register to the minimum value (3.6V) or maximum (22V) value as appropriate.

7.3.4.5 Input Source Type Detection

After the input source is qualified, the charger runs Input Source Type Detection if AUTO_INDET_EN bit is set (default enabled).

The charger follows the USB Battery Charging Specification 1.2 (BC1.2) to detect SDP/CDP/DCP/HVDC input sources and the non-standard adapters through the USB D+/D- lines. After BC1.2 detection is completed, the BC1.2_DONE_STAT bit is set to 1, and an $\overline{INT}$ pulse and BC1.2_DONE_FLAG are asserted if

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BC1.2_DONE_MASK = 0. In addition, when USB DCP is detected, the charger initiates adjustable high voltage adapter handshake on D+/D- if HVDCP detection is enabled by the host. The input type might be changed after HVDCP detection is completed.

After input source type detection, the following registers are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit
2. VBUS_STAT bits change to reflect the detected source

After detection is completed, the host can over-write IINDPM registers to change the input current limit if necessary. The charger input current is limited by the lower of IINDPM register or ILIM_HIZ pin (when EN_EXTILIM = 1) regardless of Input Current Optimizer (ICO) setting. When AUTO_INDET_EN is disabled, the Input Source Type Detection is bypassed, and the Input Current Limit (IINDPM) register remains unchanged from its previous value.

7.3.4.5.1 D+/D– Detection Sets Input Current Limit

The device contains a D+/D- based input source detection to set the input current limit. The D+/D- detection has four major steps: Data Contact Detect (DCD), Primary Detection, Secondary Detection and High Voltage DCP (HVDCP) detection.

The D+/D- Primary Detection includes standard USB BC1.2 and non-standard adapters. When an input source is plugged in, the device starts standard USB BC1.2 detection first. The USB BC1.2 is capable of identifying Standard Downstream Port (SDP), Charging Downstream Port (CDP) and Dedicated Charging Port (DCP). The non-standard detection is used to distinguish vendor specific adapters based on the unique dividers they apply to the D+/D- pins. The secondary detection is used to distinguish two types of charging ports, CDP and DCP.

A CDP usually requires the attached device to send back an enumeration within 2.5 seconds of CDP plug-in. Otherwise, the port will power cycle back to SDP even the D+/D- detection indicates CDP. This enumeration must be handled externally to the charger.

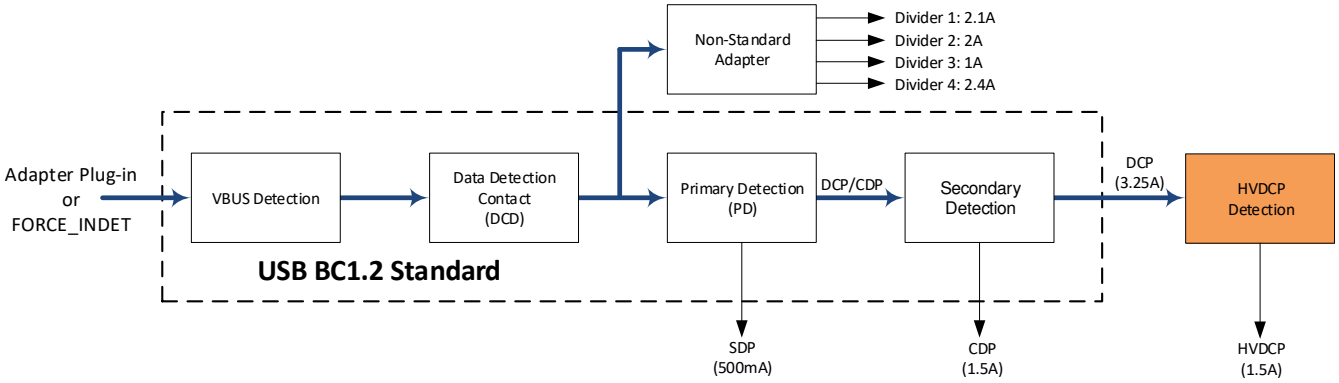

Figure 7-1. D+/D– Detection Flow

Table 7-3. Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D+ THRESHOLD	D– THRESHOLD	INPUT CURRENT LIMIT
Divider 1	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P0_VTH}	2.1 A
Divider 2	V_{D+} within V_{1P2_VTH}	V_{D+} within V_{1P2_VTH}	2A
Divider 3	V_{D+} within V_{2P0_VTH}	V_{D-} within V_{2P8_VTH}	1 A
Divider 4	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P8_VTH}	2.4 A

When a Dedicated Charging Port (DCP) is detected, the charger initiates two high voltage adapter (HVDCP) handshakes to enable the corresponding adapter to output a higher voltage for fast charging. The HVDCP detection can be enabled by setting EN_HVDCP=1 and then setting either EN_9V=1 to increase the input voltage to 9V or EN_12V=1 to increase the input voltage to 12V. When EN_12V and EN_9V are both set to 1, the charger starts 12V first.

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After the input source type detection is done, the DPDM_STAT bit is set to 0, an $\overline{INT}$ pulse and DPDM_DONE_FLAG are asserted if DPDM_DONE_MASK = 0. In addition, REG06_Input_Current_Limit and VBUS_STAT are updated as shown in Table 7-4.

Table 7-4. Input Current Limit Setting from D+/D– Detection

D+/D– DETECTION	INPUT CURRENT LIMIT (IINDPM)	VBUS_STAT_3:0
USB SDP	500 mA	0001
USB CDP	1.5 A	0010
USB DCP	3.25 A	0011
Adjustable High Voltage DCP (HVDCP)	1.5A	0100
Unknown Adapter	3 A	0101
Non-Standard Adapter, Divider 1	2.1 A	0110
Non-Standard Adapter, Divider 2	2 A	0110
Non-Standard Adapter, Divider 3	1 A	0110
Non-Standard Adapter, Divider 4	2.4 A	0110

7.3.4.5.2 HVDCP Detection Procedure

Figure 7-1 shows that an HVDCP source is first qualified as a DCP source in the USB BC1.2 standard detection stage, then qualified in the following HVDCP detection stage as an HVDCP source. When the HVDCP is first qualified as a DCP, the charger sets an IINDPM limit of 3.25A. The IIDPM is then updated to the HVDCP limit of 1.5A after the HVDCP handshake completes. In some cases the higher IINDPM limit of 3.25A may interfere with the source's ability to transition to 9V or 12V if the transition is attemped before the IINDPM is updated to 1.5A.

The recommended procedure for enabling detection of HVDCP sources is completed in the following steps:

- Before adapter insertion, the charger is configured with AUTO_INDET_EN = 1 and HVDCP_EN = 0. EN12V and EN_9V are set as desired for the system.
- When an adapter is inserted, it will be detected as SDP, CDP, DCP or a Non-Standard adapter and an I^2C interrupt is sent to the host. If any detection other than DCP is made, the host proceeds as usual.
- If the adapter is detected as DCP (VBUS_STAT[3:0] = 0011), the host first changes the Input Current Limit register to 1.5A and then changes HVDCP_EN = 1.
- After HVDCP detection is complete, the host sets HVDCP_EN = 0 to disable HVDCP support in preparation for the next input source detection sequence.

7.3.4.5.3 Connector Fault Detection

The host can apply different status on D+ pin including HIZ, 0V, 0.6V, 1.2V, 2.0V, 2.7V, 3.3V or "short to D-", and different status on D- pin including HIZ, 0.6V, 1.2V, 2.0V, 2.7V or 3.3V. The device also provides ADC readings of the D+ and D- pin voltages. The host can use the information to determine if connector is normal or in any faults. The voltage values are set using the DPLUS_DAC and DMINUS_DAC register. The D+/D- pins are only applied at the VAC1 input source. If the DPLUS_DAC or DMINUS_DAC are programmed when the adapter is plugged in and the D+/D- detection is in process, the device will ignore the register programming.

7.3.5 Dual-Input Power Mux

The BQ25798 has two ACDRV drivers to control two optional sets of back-to-back power N-FETs, selecting and managing the power from two different input sources. In the POR sequence, the charger detects whether the ACFETs-RBFETs are present, then updates the ACRB1_STAT or ACRB2_STAT status bits accordingly. The ACFET1-RBFET1 or ACFET2-RBFET2 can be controlled by setting the register bit EN_ACDRV1 or EN_ACDRV2. If the external ACFET-RBFET is not present, then tie VAC1 / VAC2 to VBUS and connect ACDRV1 / ACDRV2 to GND. The power MUX drivers support three different application cases, which are elaborated below.

7.3.5.1 ACDRV Turn On Condition

The ACDRV1 and ACDRV2 control the input power MUX. In order to turn on either ACDRV1 or ACDRV2, all of the following conditions must be valid:

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1. The corresponding ACFET-RBFET was detected at power on: ACDRV is not short to ground.
2. VAC is above $V_{VACpresent}$ threshold
3. VAC is below V_{ACOVP} threshold
4. DIS_ACDRV_BOTH is not set to '1'
5. EN_HIZ is not set to '1'
6. VBUS is below $V_{VBUSpresent}$ threshold

7.3.5.2 VBUS Input Only

In this configuration, only a single input is connected to VBUS, so that no power MOSFETs are required. VAC1 and VAC2 are shorted to VBUS, and ACDRV1 and ACDRV2 are pulled down to GND, as shown in Figure 7-2. At POR, the charger detects that no ACFETs or RBFETs are present by sensing that the ACDRV1 and ACDRV2 pins are both shorted to GND and configures power mux register fields as shown in Table 7-5.

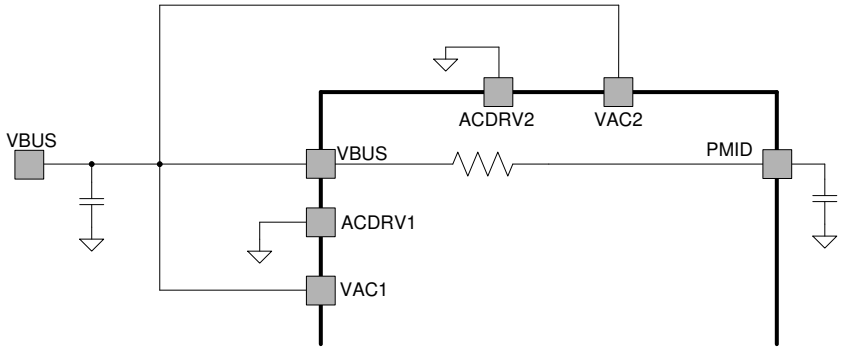

Figure 7-2. Single Input Connected to VBUS Directly Without ACFET-RBFET

Table 7-5. Single Input Configuration Summary

PIN OR REGISTER FIELD	STATE
External MOSFETs	No external power mux MOSFETs.
VAC1 pin	Shorted to VBUS
VAC2 pin	Shorted to VBUS
ACDRV1 pin	Shorted to GND
ACDRV2 pin	Shorted to GND
ACRB1_STAT	0 (Read Only)
ACRB2_STAT	0 (Read Only)
DIS_ACDRV	1
EN_ACDRV1	Locked at 0
EN_ACDRV2	Locked at 0

7.3.5.3 One ACFET-RBFET

In this configuration, only ACFET1-RBFET1 is present, ACFET2-RBFET2 is not. VAC1 is tied to the drain of ACFET1, ACDRV1 is connected to the gates of ACFET1 and RBFET1. VAC2 is shorted to VBUS, ACDRV2 is pulled down to GND. This structure is illustrated in Figure 7-3, which is able to support either single input (one from VAC1 to VBUS through ACFET1-RBFET1) or dual-input (one from VAC1 to VBUS through ACFET1-RBFET1, the other one connected directly to VBUS) applications. At POR, the charger detects only ACFET1-RBFET1 present and configures the power mux register fields as shown in Table 7-6.

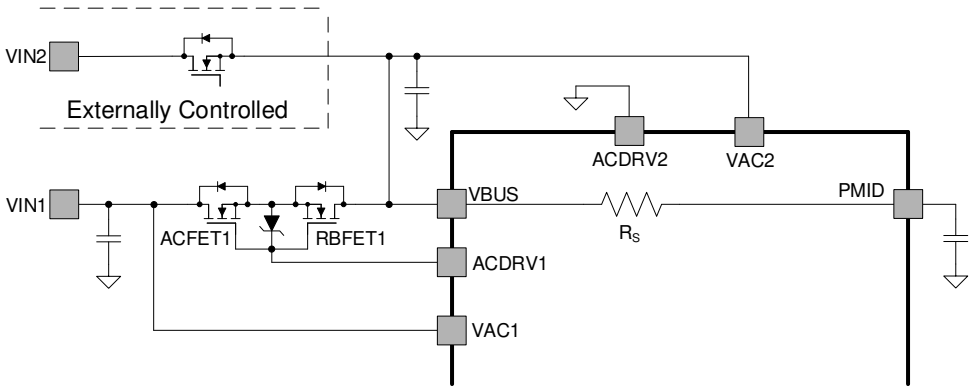

Figure 7-3. One ACFET-RBFET Structure Supporting One Input at VAC1 and/or One Input at VBUS

Table 7-6. Single Input Configuration Summary

PIN OR REGISTER FIELD	STATE
External MOSFETs	ACFET1 and RBFET1 only
VAC1	Connected to input source 1
VAC2	Shorted to VBUS
ACDRV1	Connected to ACFET1/RBFET1 gate terminals
ACDRV2	Shorted to GND
ACRB1_STAT	0: ACFET1/RBFET1 Open (Path Disabled) 1: ACFET1/RBFET1 Closed (Path Enabled)
ACRB2_STAT	0 (Read Only)
DIS_ACDRV	0: Allow ACDRV1 On if all requirements met 1: Force ACDRV1 Off
EN_ACDRV1	0: Force ACDRV1 Off 1: Turn ACDRV1 On if all requirements met
EN_ACDRV2	Locked at 0

When a valid input is presented at VAC1, the charger will set EN_ACDRV1 = 1 and turn ACFET1-RBFET1 on. To swap from the input at VAC1 to the input at VBUS, the host has to turn off the ACFET1-RBFET1 first by setting DIS_ACDRV=1 (forcing EN_ACDRV1 = 0), then enable the other input source which is connected directly to VBUS. To swap from the input at VBUS to the input at VAC1, the host has to disable the input source connected to VBUS, wait for VBUS to fall below $V_{BUS\_PRESENT}$, then turn on the ACFET1-RBFET1 by setting DIS_ACDRV = 0.

7.3.5.4 Two ACFETs-RBFETs

In this scenario, both ACFET1-RBFET1 and ACFET2-RBFET2 are present. VAC1 / VAC2 is tied to the drain of ACFET1 / ACFET2, ACDRV1 / ACDRV2 is connected to the gate of ACFET1 / ACFET2. This structure is developed to support dual-input connected at VAC1 and VAC2. At POR, the charger detects both ACFET1-RBFET1 and ACFET2-RBFET2 present, then updates ACRB1_STAT and ACRB2_STAT to 1.

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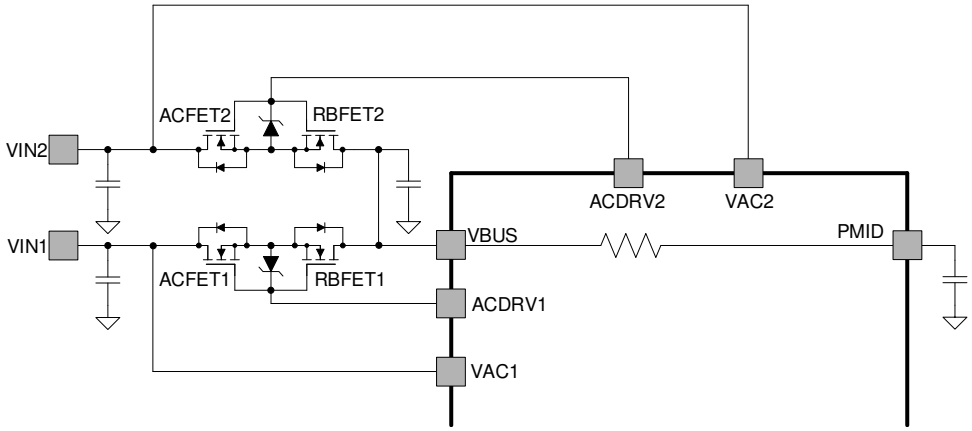

Figure 7-4. Two ACFETs-RBFETs Structure Supporting One Input at VAC1 and One Input at VAC2

Table 7-7. Dual Input Configuration Summary

PIN OR REGISTER FIELD	STATE
External MOSFETs	ACFET1, RBFET1, ACFET2, RBFET2
VAC1 pin	Connected to input source 1
VAC2 pin	Connected to input source 2
ACDRV1 pin	Connected to ACFET1/RBFET1 gate terminals
ACDRV2 pin	Connected to ACFET2/RBFET2 gate terminals
ACRB1_STAT	0: ACFET1/RBFET1 Open (Path Disabled) 1: ACFET1/RBFET1 Closed (Path Enabled)
ACRB2_STAT	0: ACFET2/RBFET2 Open (Path Disabled) 1: ACFET2/RBFET2 Closed (Path Enabled)
DIS_ACDRV	0: Allow ACDRV1 or ACDRV2 on if all requirements met 1: Force ACDRV1 and ACDRV2 off
EN_ACDRV1	0: Force ACDRV1 Off 1: Turn ACDRV1 On if all requirements met
EN_ACDRV2	0: Force ACDRV2 Off 1: Turn ACDRV2 On if all requirements met

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In dual input mode, the ACDRV automatically turns on the ACFET-RBFET of the path where a valid input is first presented, without host intervention. If a valid input is presented on the second path while the first path is already on with a valid input, the ACFET-RBFET of the second path remains off. If desired, the host may manually perform a switch between power paths by switching the values of EN_ACDRV1 and EN_ACDRV2. Both EN_ACDRV bits may be updated in a single I^2C write operation to minimize the transition time. Note that programming EN_ACDRV1 = 1, EN_ACDRV2 = 1 at the same time to turn on both ACFET1-RBFET1 and ACFET2-RBFET2 is not allowed, and will be ignored by the charger.

To transition from one input to the other, the device first turns off the initially active ACFET-RBFET pair, waits until the VBUS voltage drops lower than $V_{BUS\_PRESENT}$, and then enables the new ACFET-RBFET pair. During this change over, the converter stops switching for a short period of time. When no battery is present or the battery is depleted, the system output will fall. The user has to be aware of this and avoid the input source swap when the battery voltage is too low.

If two valid voltages are present at VAC1 and VAC2 and the source on the connected path becomes invalid because of VAC_UVLO, VAC_OV or IBUS_OC, the charger automatically swaps the input without any host

engagement. Any time that the converter autonomously swaps the source paths, it will also update the EN_ACDRV1 and EN_ACDRV2 bits accordingly in order to indicate the active power path.

With only one valid input presented at either VAC1 or VAC2, the ACFET1-RBFET1 and ACFET2-RBFET2 can not be both turned off by setting REG0x13[7:6] = 00. Instead, the host should set DIS_ACDRV = 1 to force both ACFET-RBFET pairs off. With input sources present at both VAC1 and VAC2, the host can turn off the two ACFET-RBFET pairs by setting either REG0x13[7:6] = 00 or DIS_ACDRV = 1.

7.3.6 Buck-Boost Converter Operation

The charger employs a synchronous buck-boost converter that allows charging the 1s to 4s battery from a legacy 5V USB input source, HVDCP and USB-PD power sources. The charger operates in buck, buck-boost or boost mode based on different input voltage and output voltage combinations. The converter can operate uninterruptedly and continuously across the Buck, Buck-boost and Boost operating states.

7.3.6.1 Force Input Current Limit Detection

In host mode, the host can force the device to run Input Current Limit Detection by setting FORCE_INDET bit to 1. After the detection is completed, FORCE_INDET bit automatically returns to 0. After the detection is completed, the input REG06_Input_Current_Limit (IINDPM), and the VBUS_STAT bits may be changed by the device according to the detection result.

7.3.6.2 Input Current Optimizer (ICO)

The device provides Input Current Optimizer (ICO) to identify maximum power point in order to avoid overloading the input source. The algorithm automatically identifies maximum input current limit of an unknown power source and sets the charger IINDPM register properly, in order to prevent from entering the charger input voltage (VINDPM) regulation. This feature is disabled by default at POR (EN_ICO = 0) and only activates when EN_ICO bit is set to 1.

After DCP type input source is detected based on the procedures described in Section 7.3.4.5, the algorithm runs automatically if EN_ICO bit is set. The algorithm can also be forced to execute by setting FORCE_ICO bit regardless of input source type detected. Please note that EN_ICO = 1 is required for FORCE_ICO to work.

The actual input current limit used by the Dynamic Power Management is reported in the ICO_ILIM register whether set by ICO if enabled or IINDPM register if not. In addition, the current limit is clamped by the ILIM_HIZ pin unless EN_EXT_ILIM bit is 0 to disable the ILIM_HIZ pin function.

When V(BAT) > VMINSYS, the ICO algorithm starts with the maximum allowed input current as reported in ICO_ILIM register as 500 mA then continually increases this limit until the optimal limit is found. When VBAT < VSYSMIN, the battery voltage can be too low to supplement a large system load if the charger buck converter is limited to 500 mA and then ramped up by the ICO algorithm. Therefore, when a VBAT < VSYSMIN, the ICO algorithm starts with the maximum allowed input current as reported in ICO_ILIM register to the input current-limit register value in REG0x06 and then continually decreses this limit until the optimal limit is found.

Once the optimal input current is identified, the ICO_STAT[1:0] and ICO_FLAG bits are set. The actual input current is reported in the ICO_ILIM register and does not change unless the algorithm is triggered again by the following events :

1. A new input source is plugged-in, or EN_HIZ bit is toggled
2. IINDPM register is changed
3. VINDPM register is changed
4. FORCE_ICO bit is set to 1
5. VBUS_OVP event

These events also reset the ICO_STAT[1:0] bits to 01

7.3.6.3 Maximum Power Point Tracking for Small PV Panel

The device implements a simple algorithm to track the maximum power point (MPP) when the input source is a solar panel. The I-V and P-V curves of a solar panel are most strongly dependent on irradiation and temperature. The MPP is most commonly located between 70%~90% of the Open Circuit Voltage (VOC) of the solar panel.

The algorithm automatically and periodically detects the charger input source VOC, and sets the VINDPM to be a ratio of the measured VOC. It is recommended to set the charging current to the maximum value, so that the VINDPM is always triggered and activated. The MPPT algorithm is disabled by default at POR (EN_MPPT = 0). The algorithm runs automatically when EN_MPPT bit is set to 1.

Similar to the FORCE_VINDPM_DET feature, when the battery voltage is lower than VSYSMIN (VSYS_STAT = 1), the MPPT algorithm can not be enabled. The EN_MPPT bit will be reset back to 0 if it is written to 1. In the MPPT process, the buck-boost charger stops switching and keeps in the non-switching status for a time period programmed by VOC_DLY[1:0]. When the charger stops switching, the system is powered by the battery discharging. Then the charger measures the VBUS voltage and updates the VINDPM to be VOC_PCT[2:0]*VOC. The converter starts up again for the VOC_RATE[1:0] time interval, stops switching for another VOC_DLY[1:0], measures VOC, and updates the VINDPM register to complete the next cycle. When VBUS goes below $V_{BUS\_PRESENT}$, the EN_MPPT bit will be reset to 0, and forced to be 0 even if the host writes it to 1.

For the EN_ICO, FORCE_VINDPM_DET and EN_MPPT three register bits, only one of them can be set to 1 at a given time. If one of them is enabled, the charger will block the host from enabling the other two features until the first is disabled.

7.3.6.4 Pulse Frequency Modulation (PFM)

In order to improve converter light-load efficiency, the device switches to PFM control at light load condition. The effective switching frequency decreases accordingly as load current decreases. The PFM operation can be disabled by setting PFM_FWD_DIS = 1. With PFM disabled, the converter stays at the PWM mode switching frequency and transitions into DCM operation at light load condition. The minimum effective switching frequency in PFM can be limited to 25 kHz to eliminate the audible noise concern if the out of audio (OOA) feature is enabled by setting DIS_FWD_OOA = 0. The host can disable the OOA by setting DIS_FWD_OOA = 1, which may result in the converter effective switching frequency dropping below 25 kHz at extremely light load. The PFM operation of OTG mode can be independently controlled using the PFM_OTG_DIS and DIS_OTG_OOA bits.

7.3.6.5 Device HIZ State

The charger enters HIZ mode when EN_HIZ bit is set to 1. The HIZ mode refers to a charger state, in which the REGN LDO is off, and the converter stops switching even if the adapter is present. Similar to the battery only condition, the charger is in a low quiescent current mode, turns off the ADC and turns on the BATFET to support the system load. The ADC can be re-enabled during HIZ by setting EN_ADC =1.

Some of the faults like VBUS_OVP, VSYS_OVP, VBAT_OVP and OTG_OVP, force only the converter to stop switching but keep the REGN on. While some of the faults like VSYS_SHORT and IBUS_OCP, force the charger into HIZ mode by setting EN_HIZ=1. More details could be found in the Section 7.3.13 section.

7.3.7 USB On-The-Go (OTG)

7.3.7.1 OTG Mode to Power External Devices

The device supports the OTG operation to deliver power from the battery to other external devices through the USB ports. The OTG voltage regulation is set in VOTG[10:0] register bits. The OTG current regulation is set in IOTG[6:0] register bits. To enable the OTG operation, the following conditions have to be valid:

- The battery voltage is higher than V_{BAT_OTG} rising threshold, and not trigger the VBAT_OVP protection.
- The VBUS is below V_{VBUS_UVLO}.
- The voltage at TS pin is within the range configured by BHOT and BCOLD register bits

The population of ACFET1-RBFET1 and ACFET2-RBFET2 as detected at POR affects the operation of the converter in OTG mode as summarized in Table 7-8.

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Table 7-8. OTG Beahvior by Input Mux State

ACRB1_STAT	ACRB2_STAT	DIS_ACDRV	OTG BEHAVIOR
0	0	0	Converter starts 5 ms after EN_OTG = 1
0	1	0	EN_OTG = 1 does not start converter until EN_ACDRV2 = 1
1	0	0	EN_OTG = 1 does not start converter until EN_ACDRV1 = 1
1	1	0	EN_OTG = 1 does not start converter until either EN_ACDRV1 = 1 or EN_ACDRV2 = 1
X	X	1	Converter starts 5 ms after EN_OTG = 1

For swapping the OTG output from port 1 to port 2, assuming EN_ACDRV2 is already 0, the host has to set EN_ACDRV1 = 0 to turn off ACFET1_RBFET1 first, which causes the converter to stop switching and VBUS to drop below $V_{BUS\_PRESENT}$. The host then sets EN_ACDRV2 = 1, and the converter starts switching again and ACDRV2 turns on ACFET2-RBFET2, which allows VBUS to ramp up. The similar procedure can be applied to the case of swapping the OTG output from port 2 to port 1.

In OTG mode, the converter PFM operation can be disabled by setting PFM_OTG_DIS = 1 and the OOA can be disabled by setting DIS_OTG_OOA = 1.

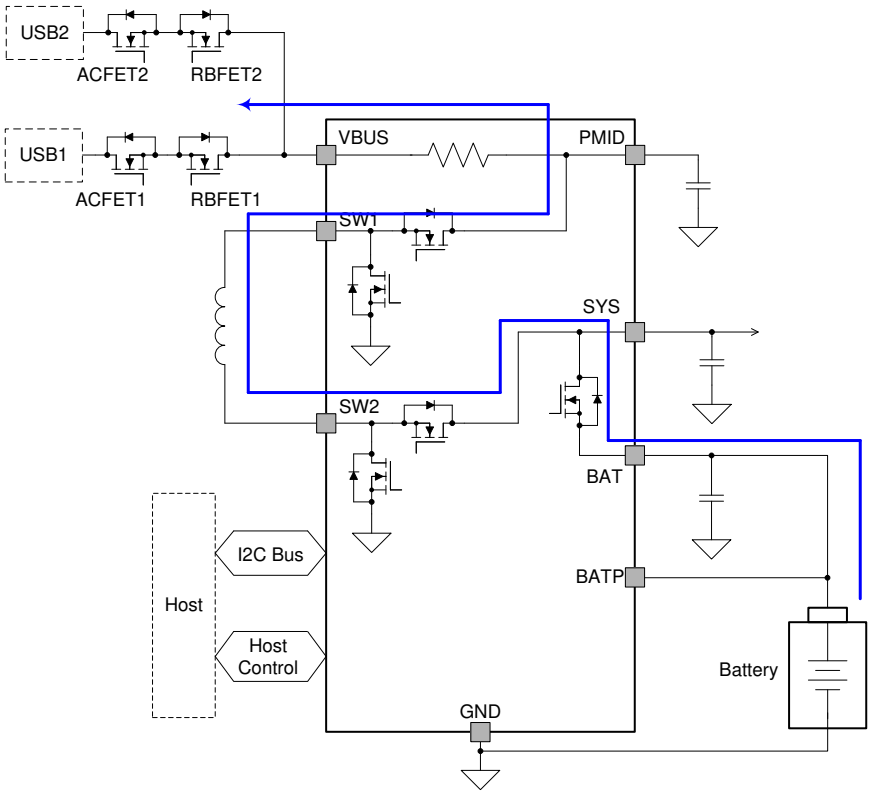

Figure 7-5. The Simplified Application Diagram for the OTG Mode Operation

The simplified application diagram for the OTG mode operation is shown in Figure 7-5, in which the power flow is illustrated by the blue arrows.

The charger regulats the battery discharging current in OTG mode. When IBAT rises higher than the IBAT_REG[1:0] register setting, the charger reduces the OTG output current and prioritizes the system load current if there is any. The IBAT_REG_STAT bit is set to 1 and an $\overline{INT}$ pulse is asserted, and if IBAT_REG_MASK = 0, the IBAT_REG_FLAG is set to 1. If the OTG output current is decreased to zero and the system load pulls even more current, the charger can no longer limit the battery discharging current.

When IBAT_REG[1:0] is set to 00, 01 or 10 (3A, 4A or 5A), there is a soft-start applied to the OTG ouput current. When IBAT_REG[1:0] is set to 11 (Disabled) no soft-start is applied.

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7.3.8 Power Path Management

The device accommodates a wide range of input voltage range from 3.6V to 24V covering the legacy 5V USB input, HVDCP, USB-PD input and the wall adapter. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT) or both.

7.3.8.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by VSYSMIN bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage. The default minimum system voltage at POR is determined according to the PROG pin configuration resistor.

The NVDC architecture also provides charging termination when the battery is fully charged. By turning off the BATFET, the adapter power is prioritized to support the system, which avoids having the battery continuously charged and discharged by the system load even if the adapter is present. This is important for extending the battery life time.

When the battery voltage is below the minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated at around 200 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, the BATFET is fully on and the voltage difference between the system and battery is the $R_{DS(ON)}$ of the BATFET multiplied by the charging current. When battery charging is disabled and VBAT is above the minimum system voltage setting or charging is terminated, the system is always regulated at 200mV (typical, PWM switching) or 600mV (typical, PFM switching) above battery voltage. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

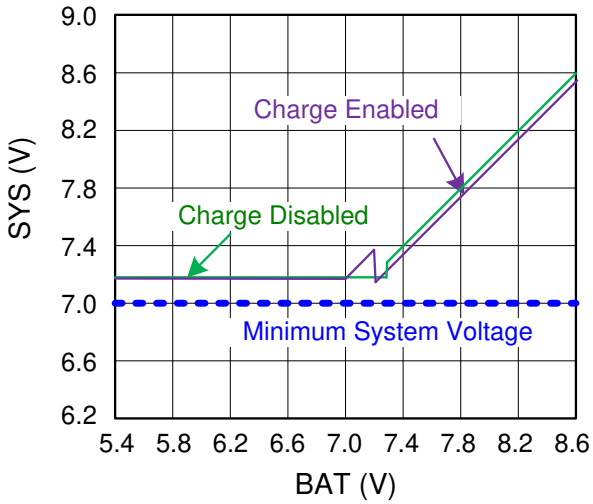

Figure 7-6. Typical System Voltage vs Battery Voltage for a 2S Battery Configuration

7.3.8.2 Dynamic Power Management

To use the maximum available current from the input power source without over loading the adapter, the BQ25798 features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When the input power at the VBUS pin is too low to support the load from SYS pin and the battery charge current from BAT pin, the charger engages either IINDPM to limit its current or VINDPM to prevent further reduction in VBUS pin voltage.

When the system voltage is regulated at VSYSMIN and SYS voltage temporarily drops lower than VSYSMIN, the VSYSMIN loop reduces charging current so that the SYS voltage remains at the VSYSMIN level. If the charge current falls to zero, but the input source is still overloaded, the SYS voltage will drop. Once the SYS voltage falls below the battery voltage, the device automatically enters supplement mode in which the BATFET turns on. The battery starts discharging so that the system is supported from both the input source and battery.

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The battery FET operates in ideal diode mode, driving the battery FET gate voltage to regulate the BATFET V_{DS} at 25 mV for low current. This prevents SYS voltage oscillations from entering and exiting the supplement mode. As the discharge current increases, the ideal diode loop drives the BATFET gate to a higher voltage, in order to reduce the battery FET $R_{DS(ON)}$ until the BATFET is fully turned on. Once the BATFET is fully on, the V_{DS} linearly increases with the discharge current. Figure 7-7 shows the V-I curve of the BATFET ideal diode operation. The BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

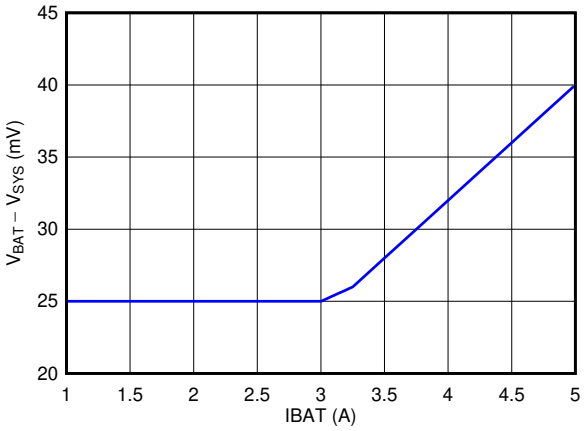

Figure 7-7. BATFET I-V Curve

During DPM mode, the status register bits VINDPM_STAT (VINDPM) and/or IINDPM_STAT (IINDPM) go high. Figure 7-8 shows the DPM response with 5V/3A adapter, 6.4V battery, 1.5A charge current and 6.8V minimum system voltage setting.

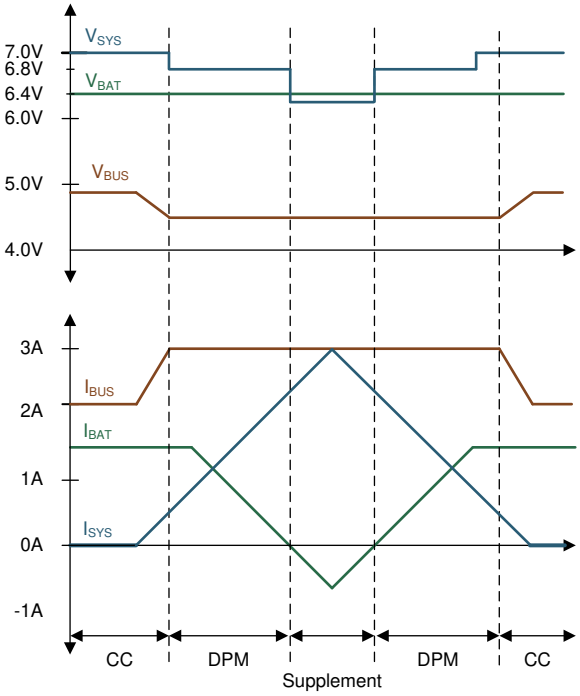

Figure 7-8. DPM Response

7.3.9 Battery Charging Management

BQ25798 charges 1S~4S Li-Ion batteries with up to 5A charge current for high capacity cells. The battery charging in different stages is controlled by the integrated BATFET. The low $R_{DS(ON)}$ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

7.3.9.1 Autonomous Charging Cycle

When battery charging is enabled (EN_CHG bit =1 and $\overline{CE}$ pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table 7-9. The host can always control the charging operation and optimize the charging parameters by writing to the corresponding registers through I^2C.

Table 7-9. Charging Parameter Default Settings

DEFAULT MODE	BQ25798
Charging voltage (REG01_Charge_Voltage_Limit)	4.2 V (1S), 8.4 V (2S), 12.6 V (3S), 16.8 V (4S)
Recharging voltage threshold (VRECHG)	200 mV
Fast charge current (REG03_Charge_Current_Limit)	2 A (1S and 2S), 1 A (3S and 4S)
Pre-charge current (IPRECHG)	120 mA
Trickle charge current (fixed value)	100 mA
Termination current (ITERM)	200 mA
Temperature profile (REG17_NTC_Control_0, REG18_NTC_Control_1)	JEITA
Fast charge safety timer (CHG_TMR)	12 hours
Pre-charge safety Timer (PRECHG_TMR)	2 hours
Trickle charge safety Timer (fixed value)	1 hour

A new charge cycle starts when the following conditions are valid:

- VBUS > $V_{VBUS\_PRESENT}$
- VBAT < VRECHG for TRECHG deglitch time
- Battery charging is enabled by setting register bit EN_CHG = 1 and keeping $\overline{CE}$ pin LOW
- No thermistor fault on TS pin
- No safety timer fault

The charger automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and the device is not in DPM mode or thermal regulation. When a fully charged battery voltage is discharged below recharge threshold (threshold selectable via VRECHG[1:0] bits), the device automatically starts a new charging cycle. After the charging terminates, toggling either $\overline{CE}$ pin or EN_CHG bit initiates a new charging cycle.

The STAT output indicates the charging status of: charging (LOW), charging complete or charging disabled (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting DIS_STAT = 1. In addition, the status register (CHG_STAT) indicates the different charging phases as:

- 000 – Not Charging
- 001 – Trickle Charge (VBAT < V_{BAT_SHORTZ})
- 010 – Pre-charge (V_{BAT_SHORTZ} < VBAT < V_{BAT_LOWV})
- 011 – Fast Charge (CC mode)
- 100 – Taper Charge (CV mode)
- 101 – Reserved
- 110 – Top-off Timer Active Charging
- 111 – Charge Termination Done

When the charger transitions to any of these states, including when the charge cycle completes, an $\overline{INT}$ is asserted to notify the host.

7.3.9.2 Battery Charging Profile

The device charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage, and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current/voltage accordingly.

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Table 7-10. Default Charging Current Setting

VBAT	CHARGING CURRENT	REGISTER DEFAULT SETTING	CHRG_STAT
< V_{BAT_SHORT}	I_{BAT_SHORT}	100 mA (fixed value)	001
V_{BAT_SHORTZ} to V_{BAT_LOWV}	I_{PRECHG}	120 mA	010
> V_{BAT_LOWV}	ICHG	2 A (1S and 2S) 1 A (3S and 4S)	011

If the charger is in DPM regulation or thermal regulation during charging, the actual charging current is less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate, as explained in Section 7.3.9.4.

The BATFET LDO operation can be disabled by setting DIS_LDO = 1. In this state, charge current is regulated according to Table 7-10 and SYS voltage is VBATT plus the IR drop through the BATFET, regardless of battery voltage. No VSYSMIN is maintained. Note that, when in trickle charge, setting DIS_LDO = 1 does not affect I_{BAT_SHORT} or VSYSMIN operation.

V_{BAT_LOWV} is the battery voltage threshold for the transition from pre-charge to fast charge. It is defined as a ratio of battery voltage regulation limit (VREG). The V_{BAT_SHORTZ} is the battery voltage threshold for the transition from trickle charge to pre-charge, which is fixed value 2.2V.

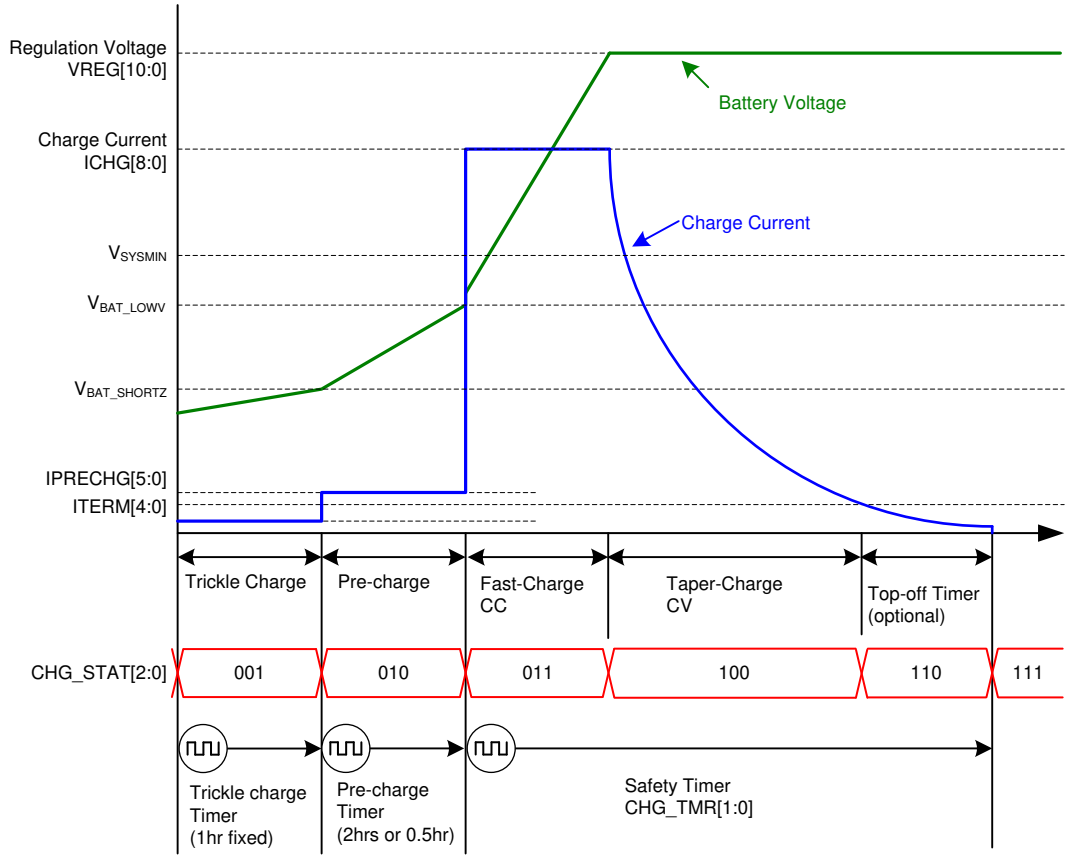

Figure 7-9. Battery Charging Profile

7.3.9.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above the recharge threshold, the converter is operated in the battery constant voltage regulation loop and the current is below the termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system and the BATFET can turn on again if the supplement mode is triggered.

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When termination is done, the status register CHG_STAT is set to 111 and an $\overline{INT}$ pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current (IINDPM), input voltage (VINDPM) or thermal (TREG) regulation. Termination can be permanently disabled by writing 0 to EN_TERM bit prior to charging termination. Writing 0 to EN_TERM when the termination has already occurred or in the top-off charging stage does not disable termination, until the next charging cycle has been restarted. If termination is enabled by setting EN_TERM = 1 during an active charging cycle, the change is applied immediately.

At low termination currents (from 40mA to 160mA), due to the comparator offset, the actual termination current may be up to 20%~40% higher than the termination target. In order to compensate for the comparator offset, a programmable top-off timer (default disabled) can be activated after termination. Whlie the top-off timer is running, the device continues to charge the battery in constant voltage mode (BATFET stays on) until the top-off time expires. The top-off timer follows safety timer constraints, such that if the safety timer is suspended, so is the top-off timer, and if the safety timer is doubled, so is the top-off timer. CHG_STAT reports whether the top off timer is active via the 110 code. Once the top-off timer expires, charging terminates, the CHG_STAT register is set to 111 and an $\overline{INT}$ pulse is asserted to the host.

The top-off timer gets reset (set to 0 and counting resumes when appropriate) for any of the following conditions:

1. Charge disable to enable
2. Termination status low to high
3. REG_RST register bit is set (disables top-off timer)

Once the charger detects termination, the charger reads the top-off timer (TOPOFF_TMR) settings. Programming the top-off timer value after termination has no effect unless a recharge cycle is initiated. The top-off timer only starts to count when the charger's termination criteria are met. If EN_TERM = 0, the charger never terminates charging, so the top-off timer does not start counting, even if it is enabled. An $\overline{INT}$ is asserted to the host when the top-off timer starts counting as well as when the top-off timer expires. All charge cycle related $\overline{INT}$ pulses (including top-off timer $\overline{INT}$ pulse) can be masked by CHG_MASK bit.

7.3.9.4 Charging Safety Timer

The device has a built-in safety timer to prevent an extended charging cycle due to abnormal battery conditions. The user can program the fast charge safety timer through I^2C (CHG_TMR bits). When the fast charge safety timer expires, the fault register CHG_TMR_STAT bit is set to 1, and an $\overline{INT}$ pulse is asserted to the host. The trickle charge timer is fixed 1 hour. The pre-charge safety timer is adjustable 2 hours (POR default) or 0.5 hour. The fast charging timer POR default setting is 12 hours.

The trickle charge, pre-charge and fast charge safety timers can be disabled by setting EN_TRICHG_TMR, EN_PRECHG_TMR or EN_CHG_TMR bit to 0. Each charging safety timer can be enabled anytime regardless of the current charging state. Each timer restarts counting when it is enabled. As soon as each charging stage is initiated, the associated safety timer starts to count, which is illustrated in the battery charging profile chart shown in Section 7.3.9.2.

During input voltage, current or thermal regulation, the safety timer counts at half-clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM_STAT = 1) throughout the whole charging cycle, and the safety timer is set to 5 hours, then the timer will expire in 10 hours. This half-clock rate feature can be disabled by setting TMR2X_EN = 0. If the host disables the half-clock rate while the charger is already running at half-clock rate, the charger keeps running at the half-clock rate and the half-clock rate is not disabled until the charger exit the voltage, current or thermal regulation.

During faults which disable charging or supplement mode, the timer is suspended. Since the timer is not counting in this state, the TMR2X_EN bit has no effect. Once the fault goes away, the safety timer resumes. The pre-charge safety timer and the trickle charge safety timer follow the same rules as the fast charge safety timer in terms of getting suspended, reset and counting at half-rate when TMR2X_EN is set.

The fast charge timer is reset at the following events:

1. Charging cycle stop and restart (toggle $\overline{CE}$ pin, EN_CHG bit, or charged battery falls below recharge threshold after termination)
2. BAT voltage changes from pre-charge to fast-charge or vice versa (in host-mode or default mode)

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3. A change of the value of CHG_TMR[1:0] register bits

The pre-charge timer is reset at the following events:

1. Charging cycle stop and restart (toggle $\overline{CE}$ pin, EN_CHG bit, or charged battery falls below recharge threshold)
2. BAT voltage changes from trickle charge to pre-charge or vice versa, pre-charge to fast charge or vice versa (in host-mode or default mode)
3. A change of the value of PRECHG_TMR register bit.

The trickle charge timer is reset at the following events:

1. Charging cycle stop and restart (toggle $\overline{CE}$ pin, EN_CHG bit, or charged battery falls below recharge threshold)
2. BAT voltage changes from trickle charge to pre-charge or vice versa (in host-mode or default mode)

7.3.9.5 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitoring.

7.3.9.5.1 JEITA Guideline Compliance in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the VT1-VT5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range.

At cool temperature T1-T2, JEITA recommends to reduce the charge current to be lower than half of the charge current at normal temperature T2-T3. BQ2562x provides the programmability of the charge current at T1-T2, to be 20%, 40% or 100% of the charge current at T2-T3 or charge suspend, which is controlled by the register bits JEITA_ISETC.

BQ2562x provides the programmability of the charge voltage at T3-T5, to be with a voltage offset (0mV, 100mV or 200mV) less than charge voltage at T2-T3 or charge suspend, which is controlled by the register bits JEITA_VSET.

The charger also provides flexible voltage/current settings beyond the JEITA requirements. The charge current setting at warm temperature T3-T5 can be configured to be 20%, 40% or 100% of the charge current at T2-T3 or charge suspend, which is programmed by the register bits JEITA_ISETH.

The charge termination is still enabled (when EN_TERM=1) at cool temperature T1-T2 and warm temperature T3-T5. The termination current will be kept as the same in all different temperature ranges. In the normal operation, the charge will be terminated based on the charge current is lower than the termination current, the battery voltage is higher than the battery recharge voltage and the charger is in the battery voltage regulation loop. When the temperature enters T1-T2 or T3-T5, the charge current might drop to 20% or 40% of that at T2-T3, which might be lower than the termination current setting. If at this moment, the battery voltage is already higher than the battery recharge voltage and the charger is in the battery voltage regulation loop, the charge will be terminated.

At warm temperature T3-T5, the battery charge voltage will becomes lower. If the battery voltage is already very close to the battery charge voltage at T2-T3, to reduce the charge voltage by an offset might trigger the VBAT_OVP. The charger should response as the normal VBAT_OVP protection under this scenario.

At cool temperature T1-T2 or warm temperature T3-T5, the charge current will become different from that at the normal temperature range T2-T3, the safety timer should be adjusted accordingly. The safety timer will be suspended when the charge is suspended, and will run at half of the clock rate when the charge current is reduced to 20% or 40%, and will keep the same when the charge current is unchanged.

JEITA charging values are shown in Figure 7-10, in which the blue real line is the default setting and the red dash line is the programmable options.

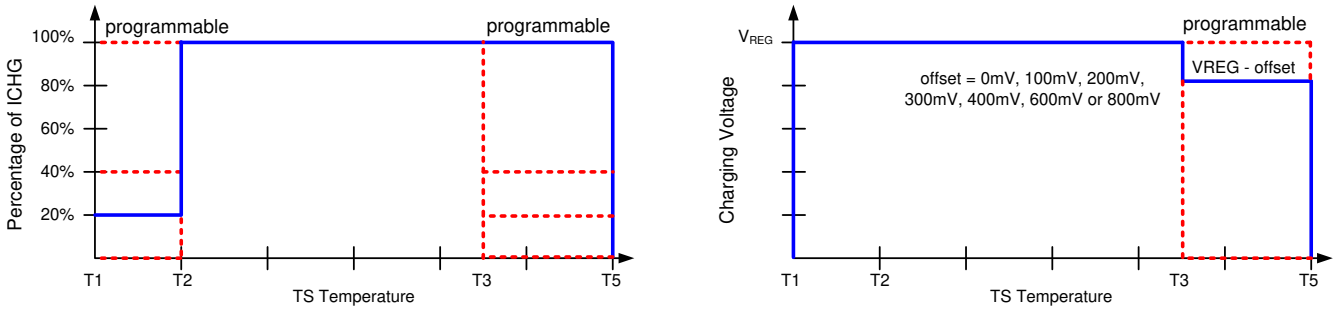

Figure 7-10. TS Charging Values

The NTC monitoring on the battery temperature can be ignored by the charger if TS_IGNORE = 1. When the TS pin feedback is ignored, the charger considers the TS is always good for charging and OTG modes. The TS_STAT including TS_COLD_STAT, TS_COOL_STAT, TS_WARM_STAT and TS_HOT_STAT, always report 000 with TS_IGNORE = 1.

When TS_IGNORE = 0, the charger adjusts the charging profile based on the TS pin feedback information. When the battery temperature crosses from one temperature range to the other one, the associated TS status bits are updated accordingly. The TS flag bits are set for the temperature range for which the TS voltage is reporting, and an $\overline{INT}$ pulse is asserted to alert the host if TS_MASK is low. The FLAG and $\overline{INT}$ pulse can be individually masked by properly setting the associated mask bit, to prevent the $\overline{INT}$ pulse from alerting the host of battery temperature range changes.

The typical TS resistor network is illustrated in Figure 7-11.

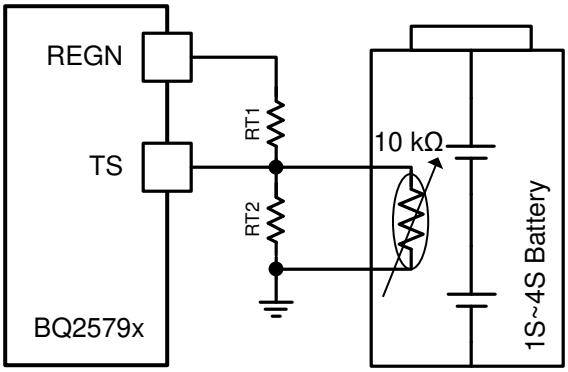

Figure 7-11. TS Resistor Network

Assuming a 103AT NTC thermistor on the battery pack, the value of TSR1 and TSR2 can be determined by:

$$RT2 = \frac{RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{VT1} - \frac{1}{VT5}\right)}{RTH_{HOT} \times \left(\frac{1}{VT5} - 1\right) - RTH_{COLD} \times \left(\frac{1}{VT1} - 1\right)} \quad (2)$$

$$RT1 = \frac{\frac{1}{VT1} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (3)$$

The BQ25798 provides comparators with fixed thresholds for VT1 and VT5, and comparators with programmable thresholds for VT2 and VT3. The thresholds for VT2 and VT3 are controlled by TS_COOL and TS_WARM. This programmability gives more flexibility for the configuration of the JEITA profile. Select T1=0°C and T5=60°C for Li-ion or Li-polymer battery, the RT1 and RT2 are calculated to be 5.24KΩ and 30.31KΩ respectively.

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7.3.9.5.2 Cold/Hot Temperature Window in OTG Mode

For battery protection during OTG mode, the device monitors the battery temperature to be within the VBCOLD to VBHOT thresholds. When RT1 is 5.24 KΩ and RT2 is 31.31 KΩ, TBCOLD default is -10°C and TBHOT default is 60°C. When the temperature is outside of this range, OTG mode is suspended, the converter stops switching. The charger waits in OTG mode (EN_OTG = 1). In addition, the VBUS_STAT bits are set to 000 and the corresponding TS_COLD_STAT or TS_HOT_STAT is reported. Once temperature returns to the normal temperature range, OTG mode is recovered and TS stauts bit is cleared. During TS fault, REGN remains on.

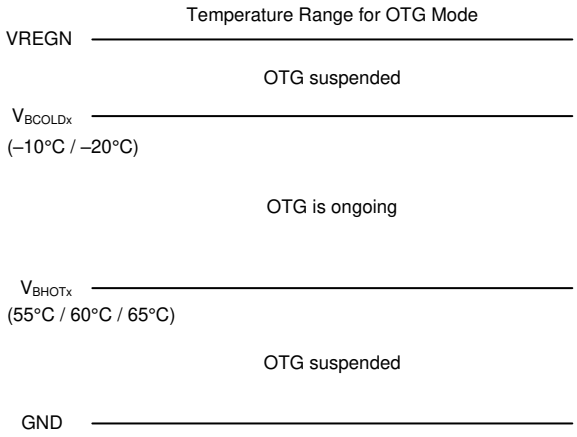

Figure 7-12. TS Pin Thermistor Sense Threshold in OTG Mode

7.3.10 Integrated 16-Bit ADC for Monitoring

The device has an integrated 16-bit ADC to provide the user with critical system information for optimizing the behavior of the charger. The ADC is controlled through the ADC Control register. The ADC_EN bit provides the ability to disable the ADC in order to conserve power dissipation. The ADC_RATE bit allows continuous conversion or one-shot behavior. After a 1-shot conversion finishes, the ADC_EN bit is cleared, and must be re-asserted to start a new conversion. The ADC_AVG bit enables or disables (default) averaging. ADC_AVG_INIT starts average using the existing (default) or using a new ADC value.

To enable the ADC, the ADC_EN bit must be set to 1. The ADC is allowed to operate if either VBUS > 3.4 V or VBAT > 2.9 V is valid. If ADC_EN is set to 1 before VBUS or VBAT reaches its valid threshold, then the ADC conversion is postponed until one of the power supplies reaches the threshold. If the charger is in HIZ mode, the ADC still can be enabled by setting ADC_EN = 1. At battery only condition, if the TS_ADC channel is enabled, the ADC only works when battery voltage is higher than 3.2V, otherwise, the ADC works when the battery voltage is higher than 2.9V.

The ADC_SAMPLE bits control the ADC sample speed, with conversion times of t_{ADC_CONV}. If the host changes the sample speed in the middle of an ADC conversion, the ADC conversion stops the channel being converted, and that channel is reconverted at the new rate. At that point, some of the ADC register values might have been converted with one sample rate and others with a different sample rate.

By default, all ADC channels are enabled with 1-shot or continuous conversion mode unless the channel is disabled in the ADC_Function_Disable_0 or ADC_Function_Disable_1 register. If an ADC channel is disabled by setting the corresponding register bit, then the value in that register is from the last valid ADC conversion or the default POR value (all zeros.) If an ADC channel is disabled in the middle of an ADC measurement cycle, the device finishes the conversion of that channel. Even though no conversion takes place when all ADC channels are disabled, the ADC circuitry is active and ready to begin conversion as soon as one of the bits in the ADC_Function_Disable_0 or ADC_Function_Disable_1 register is set to 0. In order to achieve the lowest quiescent current when disabling all ADC channels, set EN_ADC to 0 instead of disabling with ADC_Function_Disable_0 and ADC_Function_Disable_1.

The ADC_DONE_STAT and ADC_DONE_FLAG bits are set when a conversion is complete in 1-shot mode only. This event produces an $\overline{INT}$ pulse, which can be masked with ADC_DONE_MASK. During continuous conversion mode, the ADC_DONE_STAT and ADC_DONE_FLAG bits have no meaning and remain 0.

ADC conversion operates independently of the faults present in the device. ADC conversion continues even after a fault has occurred. ADC readings are only valid for DC states and not for transients.

If the host wants to exit the ADC more gracefully, it is recommended to write ADC_RATE to one-shot in order to force the ADC to stop at the end of a complete cycle of conversions.

ADC Measurement Channels:

- IBUS (positive in forward converter mode)
- IBAT (positive for charging)
- VBUS
- VPMID
- VBAT
- VSYS
- TS
- TDIE

7.3.11 Status Outputs (STAT, and $\overline{INT}$)

7.3.11.1 Charging Status Indicator (STAT Pin)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive an LED. The STAT pin function can be disabled via the DIS_STAT bit.

Table 7-11. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge and charging in top-off timer)	LOW
Charging complete	HIGH
HIZ mode, charge disable	HIGH
Battery only mode and OTG mode	HIGH
Charge suspend (A fault condition which disable charging)	Blinking at 1 Hz

7.3.11.2 Interrupt to Host ($\overline{INT}$)

In some applications, the host does not always monitor charger operation. The $\overline{INT}$ pin notifies the system host on the device operation. By default, the following events generate an active-low, 256μs $\overline{INT}$ pulse.

1. Good input source detected
   - V_{VBUS} < V_{VBUS_OVP} threshold
   - V_{VBUS} > $V_{POORSRC}$ (typical 3.4 V) when $I_{POORSRC}$ (typical 30 mA) current is applied (not a poor source)
2. VBUS_STAT changes state (VBUS_STAT any bit change)
3. Good input source removed
4. Entering IINDPM regulation
5. Entering VINDPM regulation
6. Entering IC junction temperature regulation (TREG)
7. I^2C Watchdog timer expired
   - At initial power up, this $\overline{INT}$ gets asserted to signal I^2C is ready for communication
8. Charger status changes state (CHRG_STAT value change), including Charge Complete
9. TS_STAT changes state (TS_STAT any bit change)
10. VBUS over-voltage detected (VBUS_OVP)
11. VAC over-voltage detected (VAC_OVP for VAC1 or VAC2)
12. Junction temperature shutdown (TSHUT)

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13.Battery over-voltage detected (BATOVP)
14.System over-voltage detected (VSYS_OVP)
15.IBUS over-current detected (IBUS_OCP)
16.IBAT over-current detected (IBAT_OCP)
17.Charge safety timer expired, including trickle charge and pre-charge and fast charge safety timer expired
18.A rising edge on any of the other *_STAT bits

Each one of these $\overline{INT}$ sources can be masked off to prevent $\overline{INT}$ pulses from being sent out when they occur. Three bits exist for each one of these events:

- The STAT bit holds the *current status* of each $\overline{INT}$ source
- The FLAG bit holds information on which source produced an $\overline{INT}$, regardless of the *current status*
- The MASK bit is used to prevent the device from sending out $\overline{INT}$ for each particular event

When one of the above conditions occurs (a rising edge on any of the *_STAT bits), the device sends out an $\overline{INT}$ pulse and keeps track of which source generated the $\overline{INT}$ via the FLAG registers. The FLAG register bits are automatically reset to zero after the host reads them, and a new edge on STAT bit is required to re-assert the FLAG. This sequence is illustrated in Figure 7-13.

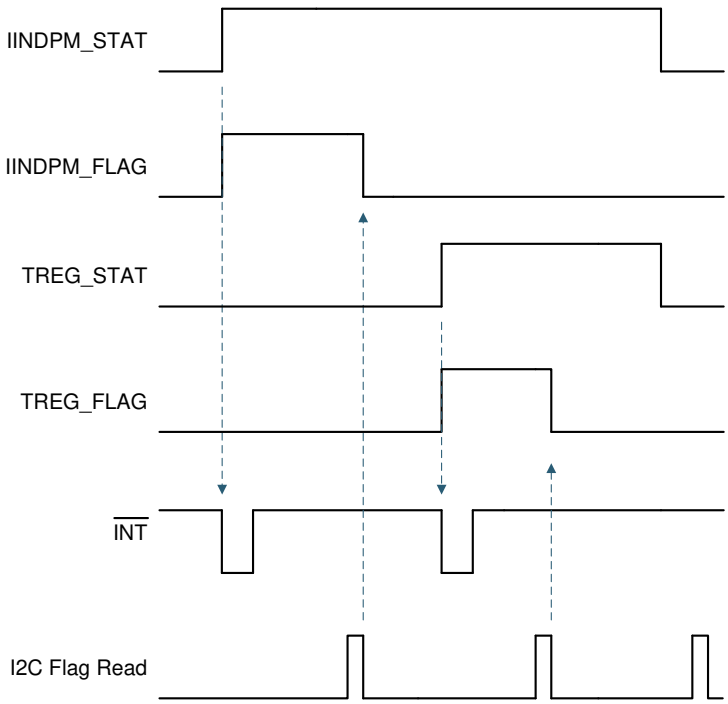

Figure 7-13. $\overline{INT}$ Generation Behavior Example

7.3.12 Ship FET Control

The charger provides an N-FET driving pin (SDRV) to control an external ship FET. When this ship FET is off, it removes leakage current from the battery to the system. The ship FET is controlled by the SDRV_CTRL[1:0] register bits, to support the shutdown mode, ship mode and the system power reset.

- **IDLE Mode** when SDRV_CTRL[1:0] = 00, POR default. The external ship FET is fully on, I^2C is enabled. The internal BATFET status is determined by the charging status. This mode is valid with adapter present, during forward charging, in OTG mode or in the battery only condition.
- **Shutdown Mode** when SDRV_CTRL[1:0] = 01. The ship FET and the internal BATFET are both off. The I^2C is disabled. The charger is totally shutdown and can only be woken up by an adapter plug-in. This mode can only be entered when no adapter is present. If SDRV_CTRL[1:0] is written to 01 with an adapter present, the write is ignored.

- **Ship Mode** when SDRV_CTRL[1:0] = 10. The ship FET and the internal BATFET are both off. The I²C is still enabled. The charger can be woken up by setting SDRV_CTRL[1:0] back to 00, or pulling the $\overline{QON}$ pin low, or an adapter plug-in. This mode can only be entered when no adapter is present. If SDRV_CTRL[1:0] is written to 01 with an adapter present, the write is ignored.
- **System Power Reset** when SDRV_CTRL[1:0] = 11. The ship FET is turned off for typical 350ms to reset the system power (converter goes to HIZ mode if VBUS is high), then the ship FET is fully turned on again. The BATFET keeps the status unchanged during the system power reset. After the reset is done, SDRV_CTRL[1:0] goes back to 00.

When the host changes SDRV_CTRL[1:0] from 00 to the other values, the charger turns off the ship FET immediately or delays by t_{SM_DLY} as configured by SDRV_DLY bit. The application diagram when the battery is connected to the charger through an external ship FET is illustrated in the figure below.

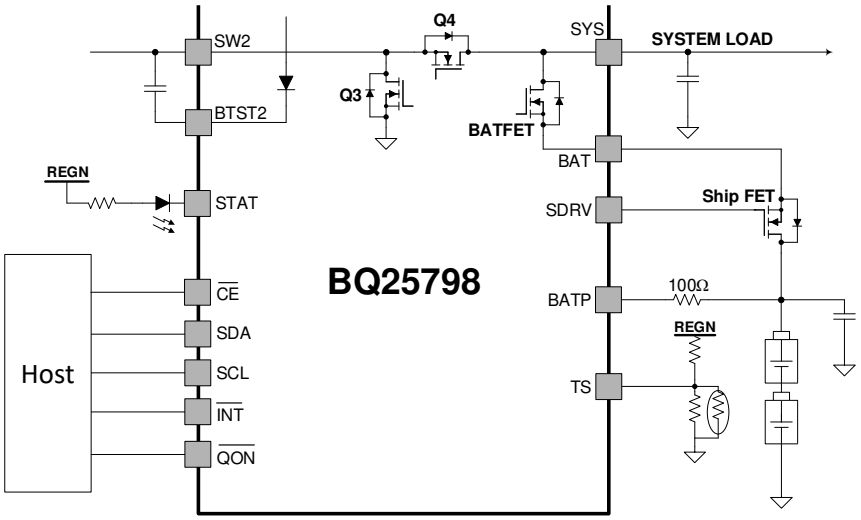

Figure 7-14. The Application Diagram for the External Ship FET

7.3.12.1 Shutdown Mode

To further reduce battery leakage current, the host can shut down the charger by setting the register bits SDRV_CTRL[1:0] to 01. In this mode, the I²C is disabled and the charger is totally shut down. The device can only be woken up by plugging in an adapter.

After the SDRV_CTRL[1:0] is set to 01, the external ship FET turns off either immediately or after waiting for 10s as configured by SDRV_DLY register bit. When VBUS is high because of an adapter being present or the OTG mode being enable, SDRV_CTRL[1:0] will be reset to 00 if the host writes it to 01.

When the device exits shutdown mode, the SDRV_CTRL bits are reset to the POR default values (00).

7.3.12.2 Ship Mode

To extend battery life and minimize the system power loss when system is powered off during idle, shipping or storage, the device can turn off BATFET and external ship FET to minimize the battery leakage current. The ship mode is enabled when the host sets SDRV_CTRL[1:0] to 10. The I²C is still enabled, but the charger system clock slows down to minimize the device quiescent current.

After the SDRV_CTRL[1:0] is set to 10, the external ship FET is turned off either immediately or after waiting 10 seconds as configured by SDRV_DLY register bit. When VBUS is high because of an adapter being present or OTG mode being enabled, SDRV_CTRL[1:0] automatically resets to 00 if the host writes it to 10.

The following events will cause an exit from ship mode:

- Plug in an adapter
- Set SDRV_CTRL[1:0] = 00

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- Set REG_RST = 1, to reset all the registers including SDRV_CTRL bits back to default (00)
- A logic low of t_{SM_EXIT} (typical 1s or 15ms programmed by WKUP_DLY bit) duration on $\overline{QON}$ pin

The charger exits ship mode by turning on the ship FET and internal BATFET to reconnect the battery to the system and resetting SDRV_CTRL bits to their POR default value (00).

7.3.12.3 System Power Reset

The host can reset the system power by:

- Set the register bits SDRV_CTRL[1:0] to 11
- A logic low of t_{RST} (typical 10s) duration on $\overline{QON}$ pin

When the system power reset is enabled, the device turns off the ship FET for t_{RST_SFET} (typical 350ms) and also sets the charger in HIZ mode if VBUS is high. After the t_{RST_SFET} completes, the device then turns on the ship FET and disables the charger HIZ mode. While the SFET is off, the charger applies a 30mA (typical) sink current on SYS to discharge system voltage.

Regardless of whether the charger is at battery only condition or in the forward charging mode with adapter present, the charger resets the system power when the SDRV_CTRL[1:0] bits are set to 11 or the $\overline{QON}$ pin is pulled low for t_{RST} duration.

7.3.13 Protections

7.3.13.1 Voltage and Current Monitoring

7.3.13.1.1 VAC Over-voltage Protection (VAC_OVP)

The charger has a programmable V_{VAC_OVP} threshold. When the VAC1 or VAC2 voltage is higher than V_{VAC_OVP}, the corresponding ACDRV turns off the ACFET-RBFET.

One register field (VAC_OVP[1:0]) sets the VAC_OVP threshold for both VAC1 and VAC2 inputs. However, the faults on each VAC input is reported separately through the register bits VAC2_OVP_STAT and VAC1_OVP_STAT (and corresponding FLAG and MASK bits). When one of the ACFET-RBFET is turned off due to VAC_OVP fault, the device can be still operated from the other VAC input if the voltage at the other input is valid.

During VAC_OVP fault and with VAC_OVP_MASK low, an $\overline{INT}$ pulse is asserted to alert the host, the VAC_OVP_STAT and VAC_OVP_FLAG fault registers get set. The ACDRV automatically turns the ACFET-RBFET on again when the over-voltage condition goes away.

7.3.13.1.2 VBUS Over-voltage Protection (VBUS_OVP)

The charger has a fixed V_{VBUS_OVP} threshold. When the VBUS voltage is higher than V_{VBUS_OVP} (typical 26 V), the device triggers a VBUS over-voltage event. The converter stops switching immediately to protect the internal power MOSFETs.

As the SYS voltage falls below the battery voltage, the BATFET is turned on to supplement the system load. During VBUS over-voltage, an $\overline{INT}$ pulse is asserted to alert the host if the VBUS_OVP_MASK is low, the VBUS_OVP_STAT and VBUS_OV_FLAG fault registers get set. The device automatically starts switching again when the VBUS over-voltage condition goes away.

7.3.13.1.3 VBUS Under-voltage Protection (POORSRC)

If the VBUS voltage falls below $V_{POORSRC}$ during operation, the converter stops switching and the charger considers the input voltage on VBUS as being under-voltage. During the input under-voltage, an $\overline{INT}$ pulse is asserted to alert the host if the PG_MASK is low. The PG_STAT bit is changed from 1 to 0. The PG_FLAG bit is also set to 1 to alert this event. As system falls below battery voltage, the BATFET is turned on to supplement the system load. The device automatically attempts to restart switching when the VBUS voltage is increased higher than $V_{POORSRC}$.

7.3.13.1.4 System Over-voltage Protection (VSYS_OVP)

The VSYS_OVP thresholds are set to be 110% (rising) and 100% (falling) of the system regulation voltage. If the SYS voltage becomes higher than 110% of its regulation point, the converter stops switching immediately to

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protect the internal power MOSFETs and the other external circuits connected to SYS. An $\overline{INT}$ pulse is asserted to alert the host if VSYS_OVP_MASK is low, the VSYS_OVP_STAT and VSYS_OVP_FLAG fault registers get set. When the system voltage falls back lower than the 100% of the system regulation point, the converter starts switching again.

7.3.13.1.5 System Short Protection (VSYS_SHORT)

When the SYS voltage falls below 2.2 V, the charger immediately enters the PFM operation, to limit the output current to approximately 1A or less (regardless of the DIS_VSYS_SHORT bit setting).

If the hiccup mode for SYS short is enabled by setting DIS_VSYS_SHORT = 0, the charger shuts down when the SYS voltage drops below 2.2 V longer than 10ms. After waiting for 500 ms, the charger attempts to restart the converter. After 10 ms of converter operation, if the SYS voltage is still lower than 2.2 V, the charger shuts down the converter for another 500 ms and the cycle repeats. After 90 s from the first short detection, if the converter shuts down for 7 times, the charger latches off the converter by setting the EN_HIZ bit to 1. If the VSYS_SHORT_MASK is low, the device also asserts an $\overline{INT}$ pulse is asserted to alert the host, the VSYS_SHORT_FLAG fault register gets set. The latch off is cleared when EN_HIZ bit is set to 0. If the system voltage is still lower than 2.2 V when the host clears the latch off, the charger enters the hiccup protection again.

If the hiccup mode for system short is disabled by setting DIS_VSYS_SHORT = 1, the converter continues running in forced PFM operation when the SYS voltage is lower than 2.2 V. After 10 ms deglitch time, an $\overline{INT}$ pulse is asserted to alert the host if VSYS_SHORT_MASK is low, the VSYS_SHORT_STAT and VSYS_SHORT_FLAG fault registers get set.

7.3.13.1.6 Battery Over-voltage Protection (VBAT_OVP)

When the battery voltage is detected to be higher than 104% of the battery charging regulation voltage, the charger turns off the converter immediately to prevent the battery voltage from increasing further. When the battery voltage drops below 102% of the battery charging regulation voltage, the converter automatically resumes switching again. The BATFET stays on to allow the battery to supplement the system load when the converter is disabled. An $\overline{INT}$ pulse is asserted to alert the host if the VBAT_OVP_MASK is low, the VBAT_OVP_STAT and VBAT_OVP_FLAG register bits get set.

During the battery over-voltage protection, the charger provides a typical 30mA discharge current at the BAT pin to bring down the battery voltage. The discharging current is controlled by EN_AUTO_IBATDIS and FORCE_IBATDIS register bits. When EN_AUTO_IBATDIS = 1, the discharging current is automatically applied at the BAT pin, without the host engagement, during the battery over-voltage condition. The discharging current is terminated when the battery over-voltage condition goes away. When FORCE_IBATDIS = 1, the discharging current is applied at the BAT pin, regardless of the battery over-voltage condition and the EN_AUTO_IBATDIS bit setting.

7.3.13.1.7 Battery Over-current Protection (IBAT_OCP)

In the battery only case where the external ship FET is present (SFET_PRESENT bit has to be set to 1) and EN_BATOC = 1, if the battery discharging current becomes higher than I_{BAT_OCP}, the charger turns off the external ship FET by setting SDRV_CTRL = 01 to force the charger into the ship mode. The ship FET can be turned on again when the host writes SDRV_CTRL = 00, or pulls low on the $\overline{QON}$ pin (timing follows the same as wake up from ship mode), or re-plugs in an adapter.

In the adapter and battery present case, if the battery supplement current becomes higher than I_{BAT_OCP}, the ship FET enters hiccup mode with 100ms off-time and 1ms on-time, until the battery over-current fault is gone. In OTG mode, if the battery discharging current is higher than I_{BAT_OCP}, the charger exits OTG mode by clearing the EN_OTG bit, then enters ship mode by setting SDRV_CTRL = 01. When the IBAT_OCP event occurs, an $\overline{INT}$ pulse is asserted to alert the host if IBAT_OCP_MASK is low, the IBAT_OCP_STAT and IBAT_OCP_FLAG fault register bits get set.

If the external ship FET is not present (SFET_PRESENT bit stays 0), the EN_BATOC register bit stays at 0. The ship FET driver will not respond to the battery over-current fault.

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7.3.13.1.8 Input Over-current Protection (IBUS_OCP)

When EN_IBUS_OCP = 1, the IBUS over-current protection is enabled. If the input current exceeds the IBUS over-current threshold I_{BUS_OCP} (typical 8 A), the charger latches off the converter by setting the EN_HIZ bit to 1. In addition, the charger sets DIS_ACDRV = 1, to disable both ACDRV1 and ACDRV2. As the SYS voltage falls below the battery voltage, the BATFET turns on to supplement the system load. Setting EN_HIZ and DIS_ACDRV bits to 0 restarts the converter. The adapter removal and replacement also resets the EN_HIZ bit to 0, but VBUS, VAC1 and VAC2 must all fall below UVLO in order for DIS_ACDRV to be reset.

When EN_IBUS_OCP = 0, the IBUS over-current protection is disabled, the EN_HIZ and DIS_ACDRV ignore the IBUS over-current fault and the converter and ACFET-RBFET keep the same status as before the fault occured. Regardless of the EN_ IBUS_OCP bit setting, when the IBUS input current becomes higher than I_{BUS_OCP}, an $\overline{INT}$ pulse is asserted to alert the host if IBUS_OCP_MASK is low, and the IBUS_OCP_STAT and IBUS_OCP_FLAG fault register bits get set.

7.3.13.1.9 OTG Over-voltage Protection (OTG_OVP)

When the VBUS voltage rises above 115% of the VOTG regulation point, the converter stops switching immediately to protect the internal power MOSFETs and the other external circuits connected to VBUS. The converter resumes switching when the VBUS voltage falls back to 100% of the VOTG regulation point. When OTG_OVP is detected, an $\overline{INT}$ pulse is asserted to alert the host if OTG_OVP_MASK is low, the VOTG_OVP_STAT and VOTG_OVP_FLAG fault registers get set.

7.3.13.1.10 OTG Under-voltage Protection (OTG_UVP)

The charger monitors the VBUS voltage in OTG mode to provide under-voltage protection. The OTG mode has built-in constant current regulation to allow the OTG output to support various types of loads. The OTG_UVP hiccup protection is default enabled (DIS_VOTG_UVP = 0). The converter shuts down when the VBUS voltage drops below 2.2 V longer than 10ms. After waiting for 500 ms, the charger attempts to restart the converter. After 10 ms of converter operation, if the VBUS voltage is still lower than 2.2 V, the charger shuts down the converter for another 500 ms and the cycle repeats. After 90 s from the first under-voltage detection, if the converter shuts down for 7 times, the charger exits OTG mode by setting the EN_OTG bit to 0. If the OTG_UVP_MASK bit is low, the charger asserts an $\overline{INT}$ pulse to alert the host and the OTG_UVP_FLAG fault register gets set.

If the OTG_UVP hiccup protection is disabled by setting DIS_VOTG_UVP = 1, the converter continues running in forced PFM operation when the VBUS voltage is lower than 2.2 V. After 10 ms deglitch time, an $\overline{INT}$ pulse is asserted to alert the host if OTG_UVP_MASK is low, the OTG_UVP_STAT and OTG_UVP_FLAG fault registers get set.

7.3.13.2 Thermal Regulation and Thermal Shutdown

The device monitors its internal junction temperature (T_J) to avoid overheating and to limit the IC surface temperature. When the internal junction temperature exceeds the preset thermal regulation limit (TREG bits), the device reduces the charge current or OTG output current to maintain the junction temperature at the thermal regulation limit. A wide thermal regulation range from 60°C to 120°C allows optimization of the system thermal performance. During thermal regulation, the actual charging current is usually below the programmed value in the ICHG registers. Therefore, termination is disabled, the fast charging safety timer runs at half the clock rate, the status register TREG_STAT bit goes high, TREG_FLAG bit is set to 1, and an $\overline{INT}$ is asserted to alert host unless TREG_MASK is set to 1.

Additionally, the device has thermal shutdown to turn off the converter when the IC junction temperature exceeds the TSHUT threshold. The fault register bits TSHUT_STAT and TSHUT_FLAG are set and an $\overline{INT}$ pulse is asserted to the host, unless TSHUT_MASK is set to 1. The BATFET and the converter resumes normal operation when the IC die temperature decreases lower than TSHUT threshold by T_{SHUT_HYS}.

7.3.14 Serial Interface

The device uses I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^2C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL). Devices can be considered as masters or slaves when performing

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data transfers. A master is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with 7-bit address 0x6B, receiving control inputs from the master device like micro-controller or digital signal processor through REG00 – REG25. Register read beyond REG25 (0x25), returns 0xFF. The I^2C interface supports both standard mode (up to 100 kbits/s), and fast mode (up to 400 kbits/s). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

7.3.14.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on SCL line is LOW. One clock pulse is generated for each data bit transferred.

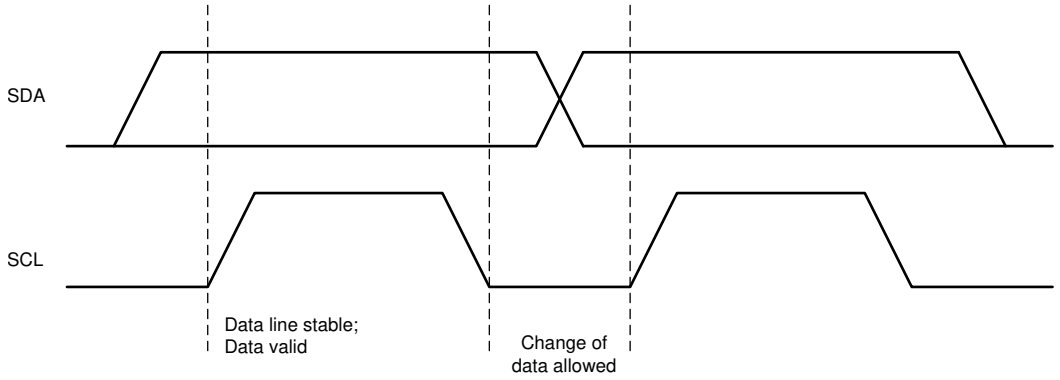

Figure 7-15. Bit Transfers on the I^2C Bus

7.3.14.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

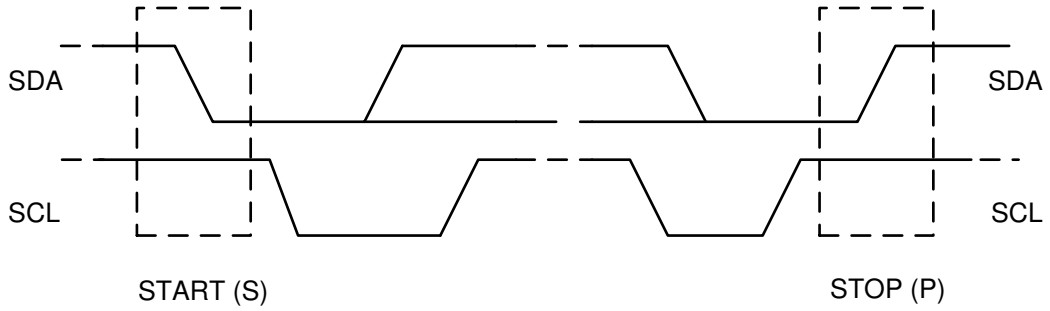

Figure 7-16. START and STOP Conditions on the I^2C Bus

7.3.14.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and releases the SCL line.

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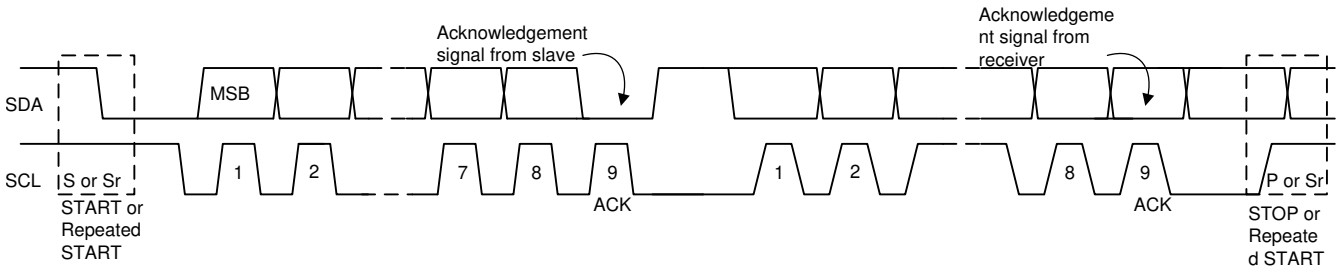

Figure 7-17. Data Transfer on the I²C Bus

7.3.14.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after each transmitted byte. The ACK bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

7.3.14.5 Slave Address and Data Direction Bit

After the START signal, a slave address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/ $\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The BQ25798 7-bit address is defined as 1101 011' (0x6B). The address bit arrangement is shown below.

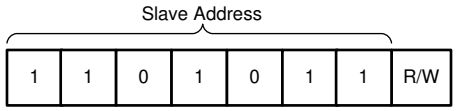

Figure 7-18. 7-Bit Addressing (0x6B)

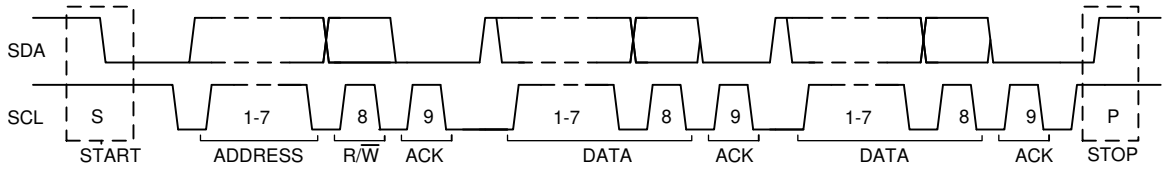

Figure 7-19. Complete Data Transfer on the I²C Bus

7.3.14.6 Single Write and Read

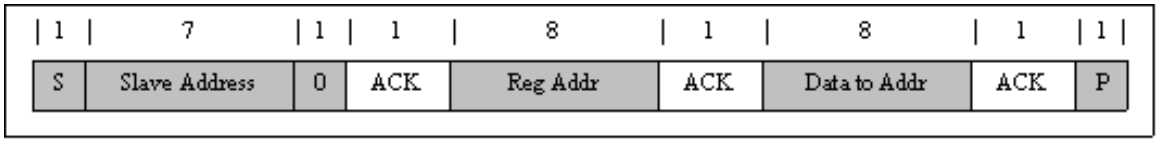

Figure 7-20. Single Write

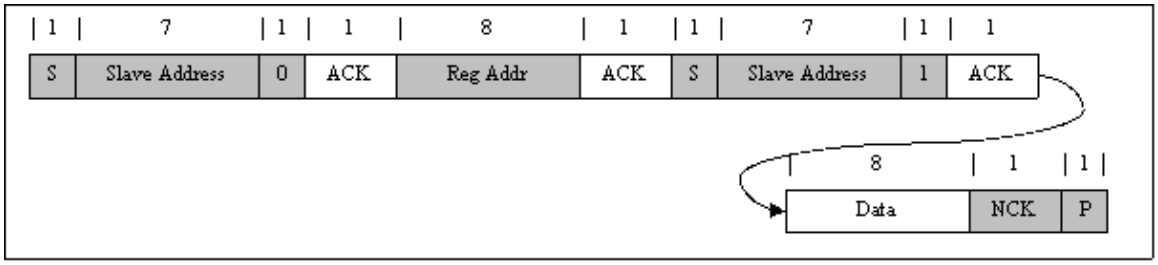

Figure 7-21. Single Read

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

7.3.14.7 Multi-Write and Multi-Read

The charger device supports multi-byte read and multi-byte write of all registers. These multi-byte operations are allowed to cross register boundaries. For instance, the entire regiser map may be read in a single operation with a 49-byte read that starts at register address 0x0.

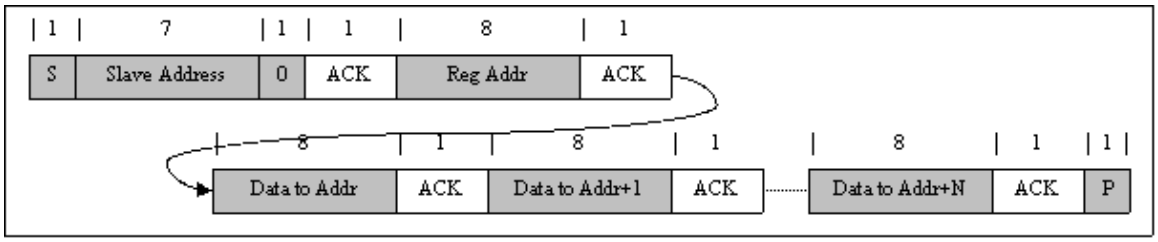

Figure 7-22. Multi-Write

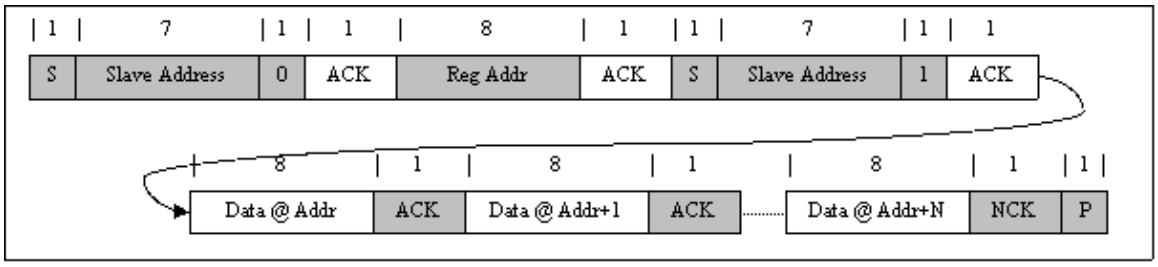

Figure 7-23. Multi-Read

7.4 Device Functional Modes

7.4.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD_STAT bit becomes HIGH, WD_FLAG is set to 1, and an $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK). The WD_FLAG bit would read as 1 upon the first read and then 0 upon subsequent reads. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 1-hour trickle charging safety timer, 2-hour pre-charging safety timer and the 12-hour fast charging safety timer. At the end of the 1-hour or 2-hour or 12-hour timer expired, the charging is stopped and the buck-boost converter continues to operate to supply system load.

A write to any I^2C register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has

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to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer is expired, the device returns to default mode and all registers are reset to default values except the ones described in Section 7.5. The watchdog timer will be reset on any write if the watchdog timer has expired. When watchdog timer expires, WD_STAT and WD_FLAG is set to 1, and an $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK).

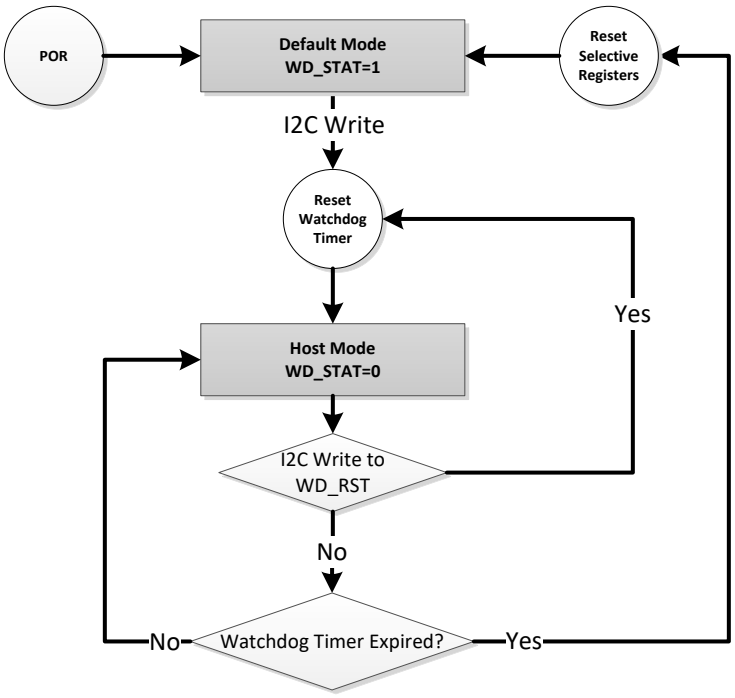

Figure 7-24. Watchdog Timer Flow Chart

7.4.2 Register Bit Reset

Beside the register reset by the watchdog timer in the default mode, the register and the timer could be reset to the default value by writing the REG_RST bit to 1. The register bits, which can be reset by the REG_RST bit, are noted in the Register Map section. After the register reset, the REG_RST bit will go back from 1 to 0 automatically.

The register reset by the REG_RST bit will not initiate the ACFET-RBFET detection, which is only done at the charger first time POR. It will not repeat the open-circuit adapter measurements for the default VINDPM setting, which in only done when an adapter is plugged in. In addition, if the charger is in the process of forced ICO, the forced open-circuit adapter measurements or the forced D+/D- detection, set the REG_RST to 1 will terminate all of these processes, because reset the register to default values will set FORCE_ICO, FORCE_INDET and FORCE_VINDPM_DET bits to 0.

7.5 Register Map

7.5.1 I2C Registers

Table 7-12 lists the I2C registers. All register offset addresses not listed in Table 7-12 should be considered as reserved locations and the register contents should not be modified.

Table 7-12. I2C Registers

Offset	Acronym	Register Name	Section
0h	REG00_Minimal_System_Voltage	Minimal System Voltage	Section 7.5.1.1
1h	REG01_Charge_Voltage_Limit	Charge Voltage Limit	Section 7.5.1.2
3h	REG03_Charge_Current_Limit	Charge Current Limit	Section 7.5.1.3
5h	REG05_Input_Voltage_Limit	Input Voltage Limit	Section 7.5.1.4
6h	REG06_Input_Current_Limit	Input Current Limit	Section 7.5.1.5
8h	REG08_Precharge_Control	Precharge Control	Section 7.5.1.6
9h	REG09_Termination_Control	Termination Control	Section 7.5.1.7
Ah	REG0A_Re-charge_Control	Re-charge Control	Section 7.5.1.8
Bh	REG0B_VOTG_regulation	VOTG regulation	Section 7.5.1.9
Dh	REG0D_IOTG_regulation	IOTG regulation	Section 7.5.1.10
Eh	REG0E_Timer_Control	Timer Control	Section 7.5.1.11
Fh	REG0F_Charger_Control_0	Charger Control 0	Section 7.5.1.12
10h	REG10_Charger_Control_1	Charger Control 1	Section 7.5.1.13
11h	REG11_Charger_Control_2	Charger Control 2	Section 7.5.1.14
12h	REG12_Charger_Control_3	Charger Control 3	Section 7.5.1.15
13h	REG13_Charger_Control_4	Charger Control 4	Section 7.5.1.16
14h	REG14_Charger_Control_5	Charger Control 5	Section 7.5.1.17
15h	REG15_MPPT_Control	MPPT Control	Section 7.5.1.18
16h	REG16_Temperature_Control	Temperature Control	Section 7.5.1.19
17h	REG17_NTC_Control_0	NTC Control 0	Section 7.5.1.20
18h	REG18_NTC_Control_1	NTC Control 1	Section 7.5.1.21
19h	REG19_ICO_Current_Limit	ICO Current Limit	Section 7.5.1.22
1Bh	REG1B_Charger_Status_0	Charger Status 0	Section 7.5.1.23
1Ch	REG1C_Charger_Status_1	Charger Status 1	Section 7.5.1.24
1Dh	REG1D_Charger_Status_2	Charger Status 2	Section 7.5.1.25
1Eh	REG1E_Charger_Status_3	Charger Status 3	Section 7.5.1.26
1Fh	REG1F_Charger_Status_4	Charger Status 4	Section 7.5.1.27
20h	REG20_FAULT_Status_0	FAULT Status 0	Section 7.5.1.28
21h	REG21_FAULT_Status_1	FAULT Status 1	Section 7.5.1.29
22h	REG22_Charger_Flag_0	Charger Flag 0	Section 7.5.1.30
23h	REG23_Charger_Flag_1	Charger Flag 1	Section 7.5.1.31
24h	REG24_Charger_Flag_2	Charger Flag 2	Section 7.5.1.32
25h	REG25_Charger_Flag_3	Charger Flag 3	Section 7.5.1.33
26h	REG26_FAULT_Flag_0	FAULT Flag 0	Section 7.5.1.34
27h	REG27_FAULT_Flag_1	FAULT Flag 1	Section 7.5.1.35
28h	REG28_Charger_Mask_0	Charger Mask 0	Section 7.5.1.36
29h	REG29_Charger_Mask_1	Charger Mask 1	Section 7.5.1.37
2Ah	REG2A_Charger_Mask_2	Charger Mask 2	Section 7.5.1.38
2Bh	REG2B_Charger_Mask_3	Charger Mask 3	Section 7.5.1.39
2Ch	REG2C_FAULT_Mask_0	FAULT Mask 0	Section 7.5.1.40
2Dh	REG2D_FAULT_Mask_1	FAULT Mask 1	Section 7.5.1.41

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Table 7-12. I2C Registers (continued)

Offset	Acronym	Register Name	Section
2Eh	REG2E_ADC_Control	ADC Control	Section 7.5.1.42
2Fh	REG2F_ADC_Function_Disable_0	ADC Function Disable 0	Section 7.5.1.43
30h	REG30_ADC_Function_Disable_1	ADC Function Disable 1	Section 7.5.1.44
31h	REG31_IBUS_ADC	IBUS ADC	Section 7.5.1.45
33h	REG33_IBAT_ADC	IBAT ADC	Section 7.5.1.46
35h	REG35_VBUS_ADC	VBUS ADC	Section 7.5.1.47
37h	REG37_VAC1_ADC	VAC1 ADC	Section 7.5.1.48
39h	REG39_VAC2_ADC	VAC2 ADC	Section 7.5.1.49
3Bh	REG3B_VBAT_ADC	VBAT ADC	Section 7.5.1.50
3Dh	REG3D_VSYS_ADC	VSYS ADC	Section 7.5.1.51
3Fh	REG3F_TS_ADC	TS ADC	Section 7.5.1.52
41h	REG41_TDIE_ADC	TDIE_ADC	Section 7.5.1.53
43h	REG43_D+_ADC	D+ ADC	Section 7.5.1.54
45h	REG45_D-_ADC	D- ADC	Section 7.5.1.55
47h	REG47_DPDM_Driver	DPDM Driver	Section 7.5.1.56
48h	REG48_Part_Information	Part Information	Section 7.5.1.57

Complex bit access types are encoded to fit into small table cells. The following table shows the codes that are used for access types in this section.

Table 7-13. I2C Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Others		
Range		The register bits are only valid in this defined range.
Clamped Low		Any write on the register lower than the minimal value of the valid range, will be ignored by the charger
Clamped High		Any write on the register higher than the maximum value of the valid range, will be ignored by the charger

ADVANCE INFORMATION

7.5.1.1 REG00_Minimal_System_Voltage Register (Offset = 0h) [reset = X]

REG00_Minimal_System_Voltage is shown in Figure 7-25 and described in Table 7-14.

Return to the Table 7-12.

Minimal System Voltage

Figure 7-25. REG00_Minimal_System_Voltage Register

7	6	5	4	3	2	1	0
RESERVED		VSYSMIN_5:0					
R/W-0h		R/W-X					

Table 7-14. REG00_Minimal_System_Voltage Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	RESERVED	R/W	0h		RESERVED
5-0	VSYSMIN_5:0	R/W	X	Reset by: REG_RST	Minimal System Voltage: During POR, the device reads the resistance tie to PROG pin, to identify the default battery cell count and determine the default power on VSYSMIN list below: 1s: 3.5V 2s: 7V 3s: 9V 4s: 12V Type : RW Range : 2500mV-16000mV Fixed Offset : 2500mV Bit Step Size : 250mV Clamped High

ADVANCE INFORMATION

7.5.1.2 REG01_Charge_Voltage_Limit Register (Offset = 1h) [reset = X]

REG01_Charge_Voltage_Limit is shown in Figure 7-26 and described in Table 7-15.

Return to the Table 7-12.

Charge Voltage Limit

Figure 7-26. REG01_Charge_Voltage_Limit Register

15	14	13	12	11	10	9	8
RESERVED					VREG_10:0		
R-0h					R/W-X		
7	6	5	4	3	2	1	0
VREG_10:0							
R/W-X							

Table 7-15. REG01_Charge_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15-11	RESERVED	R	0h		RESERVED
10-0	VREG_10:0	R/W	X	Reset by: REG_RST	Battery Voltage Limit: During POR, the device reads the resistance tie to PROG pin, to identify the default battery cell count and determine the default power-on battery voltage regulation limit: 1s: 4.2V 2s: 8.4V 3s: 12.6V 4s: 16.8V Type : RW Range : 3000mV-18800mV Fixed Offset : 0mV Bit Step Size : 10mV Clamped Low

ADVANCE INFORMATION

7.5.1.3 REG03_Charge_Current_Limit Register (Offset = 3h) [reset = X]

REG03_Charge_Current_Limit is shown in Figure 7-27 and described in Table 7-16.

Return to the Table 7-12.

Charge Current Limit

Figure 7-27. REG03_Charge_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED							ICHG_8:0
R-0h							R/W-X
7	6	5	4	3	2	1	0
ICHG_8:0							
R/W-X							

Table 7-16. REG03_Charge_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15-9	RESERVED	R	0h		RESERVED
8-0	ICHG_8:0	R/W	X	Reset by: WATCHDOG REG_RST	Charge Current Limit During POR, the device reads the resistance tie to PROG pin, to identify the default battery cell count and determine the default power-on battery charging current: 1s and 2s: 2A 3s and 4s: 1A Type : RW Range : 50mA-5000mA Fixed Offset : 0mA Bit Step Size : 10mA Clamped Low

ADVANCE INFORMATION

7.5.1.4 REG05_Input_Voltage_Limit Register (Offset = 5h) [reset = 24h]

REG05_Input_Voltage_Limit is shown in Figure 7-28 and described in Table 7-17.

Return to the Table 7-12.

Input Voltage Limit

Figure 7-28. REG05_Input_Voltage_Limit Register

7	6	5	4	3	2	1	0
VINDPM_7:0							
R/W-24h							

Table 7-17. REG05_Input_Voltage_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VINDPM_7:0	R/W	24h	Absolute VINDPM Threshold VINDPM register is reset to 3600mV upon adapter unplugged and it is set to the value based on the VBUS measurement when the adapter plugs in. It is not reset by the REG_RST and the WATCHDOG Type : RW POR: 3600mV (24h) Range : 3600mV-22000mV Fixed Offset : 0mV Bit Step Size : 100mV Clamped Low

ADVANCE INFORMATION

7.5.1.5 REG06_Input_Current_Limit Register (Offset = 6h) [reset = 12Ch]

REG06_Input_Current_Limit is shown in Figure 7-29 and described in Table 7-18.

Return to the Table 7-12.

Input Current Limit

Figure 7-29. REG06_Input_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED							IINDPM_8:0
R-0h							R/W-12Ch
7	6	5	4	3	2	1	0
IINDPM_8:0							
R/W-12Ch							

Table 7-18. REG06_Input_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15-9	RESERVED	R	0h		RESERVED
8-0	IINDPM_8:0	R/W	12Ch	Reset by: REG_RST	Based on D+/D- detection results: USB SDP = 500mA USB CDP = 1.5A USB DCP = 3.25A Adjustable High Voltage DCP = 1.5A Unknown Adapter = 3A Non-Standard Adapter = 1A/2A/2.1A/2.4A Type : RW POR: 3000mA (12Ch) Range : 100mA-3300mA Fixed Offset : 0mA Bit Step Size : 10mA Clamped Low

ADVANCE INFORMATION

7.5.1.6 REG08_Precharge_Control Register (Offset = 8h) [reset = C3h]

REG08_Precharge_Control is shown in Figure 7-30 and described in Table 7-19.

Return to the Table 7-12.

Precharge Control

Figure 7-30. REG08_Precharge_Control Register

7	6	5	4	3	2	1	0
VBAT_LOWV_1:0		IPRECHG_5:0					
R/W-3h		R/W-3h					

Table 7-19. REG08_Precharge_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	VBAT_LOWV_1:0	R/W	3h	Reset by: REG_RST	Battery voltage thresholds for the transition from precharge to fast charge, which is defined as a ratio of battery regulation limit (VREG) Type : RW POR: 11b 0h = 15%*VREG 1h = 62.2%*VREG 2h = 66.7%*VREG 3h = 71.4%*VREG
5-0	IPRECHG_5:0	R/W	3h	Reset by: WATCHDOG REG_RST	Precharge current limit Type : RW POR: 120mA (3h) Range : 40mA-2000mA Fixed Offset : 0mA Bit Step Size : 40mA Clamped Low

ADVANCE INFORMATION

7.5.1.7 REG09_Termination_Control Register (Offset = 9h) [reset = 5h]

REG09_Termination_Control is shown in Figure 7-31 and described in Table 7-20.

Return to the Table 7-12.

Termination Control

Figure 7-31. REG09_Termination_Control Register

7	6	5	4	3	2	1	0
RESERVED	REG_RST	RESERVED	ITERM_4:0				
R-0h	R/W-0h	R-0h	R/W-5h				

Table 7-20. REG09_Termination_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		RESERVED
6	REG_RST	R/W	0h		Reset registers to default values and reset timer Type : RW POR: 0b 0h = Not reset 1h = Reset
5	RESERVED	R	0h		RESERVED
4-0	ITERM_4:0	R/W	5h	Reset by: WATCHDOG REG_RST	Termination current Type : RW POR: 200mA (5h) Range : 40mA-1000mA Fixed Offset : 0mA Bit Step Size : 40mA Clamped Low

ADVANCE INFORMATION

7.5.1.8 REG0A_Re-charge_Control Register (Offset = Ah) [reset = X]

REG0A_Re-charge_Control is shown in Figure 7-32 and described in Table 7-21.

Return to the Table 7-12.

Re-charge Control

Figure 7-32. REG0A_Re-charge_Control Register

7	6	5	4	3	2	1	0
CELL_1:0		TRECHG_1:0		VRECHG_3:0			
R/W-X		R/W-2h		R/W-3h			

Table 7-21. REG0A_Re-charge_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	CELL_1:0	R/W	X		At POR, the charger reads the PROG pin resistance to determine the battery cell count and update this CELL bits accordingly. Type : RW 0h = 1s 1h = 2s 2h = 3s 3h = 4s
5-4	TRECHG_1:0	R/W	2h	Reset by: WATCHDOG REG_RST	Battery recharge deglich time Type : RW POR: 10b 0h = 64ms 1h = 256ms 2h = 1024ms (default) 3h = 2048ms
3-0	VRECHG_3:0	R/W	3h	Reset by: WATCHDOG REG_RST	Battery Recharge Threshold Offset (Below VREG) Type : RW POR: 200mV (3h) Range : 50mV-800mV Fixed Offset : 50mV Bit Step Size : 50mV

ADVANCE INFORMATION

7.5.1.9 REG0B_VOTG_regulation Register (Offset = Bh) [reset = DCh]

REG0B_VOTG_regulation is shown in Figure 7-33 and described in Table 7-22.

Return to the Table 7-12.

VOTG regulation

Figure 7-33. REG0B_VOTG_regulation Register

15	14	13	12	11	10	9	8
RESERVED					VOTG_10:0		
R-0h					R/W-DCh		
7	6	5	4	3	2	1	0
VOTG_10:0							
R/W-DCh							

Table 7-22. REG0B_VOTG_regulation Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
15-11	RESERVED	R	0h		RESERVED
10-0	VOTG_10:0	R/W	DCh	Reset by: WATCHDOG REG_RST	OTG mode regulation voltage Type : RW POR: 5000mV (DCh) Range : 2800mV-22000mV Fixed Offset : 2800mV Bit Step Size : 10mV Clamped High

ADVANCE INFORMATION

7.5.1.10 REG0D_IOTG_regulation Register (Offset = Dh) [reset = 4Bh]

REG0D_IOTG_regulation is shown in Figure 7-34 and described in Table 7-23.

Return to the Table 7-12.

IOTG regulation

Figure 7-34. REG0D_IOTG_regulation Register

7	6	5	4	3	2	1	0
PRECHG_TMR	IOTG_6:0						
R/W-0h	R/W-4Bh						

Table 7-23. REG0D_IOTG_regulation Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	PRECHG_TMR	R/W	0h	Reset by: WATCHDOG REG_RST	Pre-charge safety timer setting Type : RW POR: 0b 0h = 2 hrs (default) 1h = 0.5 hrs
6-0	IOTG_6:0	R/W	4Bh	Reset by: WATCHDOG REG_RST	OTG current limit Type : RW POR: 3000mA (4Bh) Range : 120mA-3320mA Fixed Offset : 0mA Bit Step Size : 40mA Clamped Low

7.5.1.11 REG0E_Timer_Control Register (Offset = Eh) [reset = 3Dh]

REG0E_Timer_Control is shown in Figure 7-35 and described in Table 7-24.

Return to the Table 7-12.

Timer Control

Figure 7-35. REG0E_Timer_Control Register

7	6	5	4	3	2	1	0
TOPOFF_TMR_1:0		EN_TRICHG_TMR	EN_PRECHG_TMR	EN_CHG_TMR	CHG_TMR_1:0		TMR2X_EN
R/W-0h		R/W-1h	R/W-1h	R/W-1h	R/W-2h		R/W-1h

Table 7-24. REG0E_Timer_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	TOPOFF_TMR_1:0	R/W	0h	Reset by: WATCHDOG REG_RST	Top-off timer control Type : RW POR: 00b 0h = Disabled (default) 1h = 15 mins 2h = 30 mins 3h = 45 mins
5	EN_TRICHG_TMR	R/W	1h	Reset by: WATCHDOG REG_RST	Enable trickle charge timer (fixed as 1hr) Type : RW POR: 1b 0h = Disabled 1h = Enabled (default)
4	EN_PRECHG_TMR	R/W	1h	Reset by: WATCHDOG REG_RST	Enable pre-charge timer Type : RW POR: 1b 0h = Disabled 1h = Enabled (default)
3	EN_CHG_TMR	R/W	1h	Reset by: WATCHDOG REG_RST	Enable fast charge timer Type : RW POR: 1b 0h = Disabled 1h = Enabled (default)
2-1	CHG_TMR_1:0	R/W	2h	Reset by: WATCHDOG REG_RST	Fast charge timer setting Type : RW POR: 10b 0h = 5 hrs 1h = 8 hrs 2h = 12 hrs (default) 3h = 24 hrs
0	TMR2X_EN	R/W	1h	Reset by: WATCHDOG REG_RST	TMR2X_EN Type : RW POR: 1b 0h = Trickle charge, pre-charge and fast charge timer NOT slowed by 2X during input DPM or thermal regulation. 1h = Trickle charge, pre-charge and fast charge timer slowed by 2X during input DPM or thermal regulation (default)

ADVANCE INFORMATION

7.5.1.12 REG0F_Charger_Control_0 Register (Offset = Fh) [reset = A2h]

REG0F_Charger_Control_0 is shown in Figure 7-36 and described in Table 7-25.

Return to the Table 7-12.

Charger Control 0

Figure 7-36. REG0F_Charger_Control_0 Register

7	6	5	4	3	2	1	0
EN_AUTO_IBATDIS	FORCE_IBATDIS	EN_CHG	EN_ICO	FORCE_ICO	EN_HIZ	EN_TERM	RESERVED
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R-0h

Table 7-25. REG0F_Charger_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_AUTO_IBATDIS	R/W	1h	Reset by: REG_RST	Enable the auto battery discharging during the battery OVP fault Type : RW POR: 1b 0h = The charger will NOT apply a discharging current on BAT during battery OVP 1h = The charger will apply a discharging current on BAT during battery OVP
6	FORCE_IBATDIS	R/W	0h	Reset by: REG_RST	Force a battery discharging current Type : RW POR: 0b 0h = IDLE (default) 1h = Force the charger to apply a discharging current on BAT regardless the battery OVP status
5	EN_CHG	R/W	1h	Reset by: WATCHDOG REG_RST	Charger Enable Configuration Type : RW POR: 1b 0h = Charge Disable 1h = Charge Enable (default)
4	EN_ICO	R/W	0h	Reset by: REG_RST	Input Current Optimizer (ICO) Enable Type : RW POR: 0b 0h = Disable ICO (default) 1h = Enable ICO
3	FORCE_ICO	R/W	0h	Reset by: WATCHDOG REG_RST	Force start input current optimizer (ICO) Note: This bit can only be set and returns 0 after ICO starts. This bit only valid when EN_ICO = 1 Type : RW POR: 0b 0h = Do NOT force ICO (Default) 1h = Force ICO start
2	EN_HIZ	R/W	0h	Reset by: REG_RST	Enable HIZ mode. This bit will be also reset to 0, when the adapter is plugged in at VBUS. Type : RW POR: 0b 0h = Disable (default) 1h = Enable
1	EN_TERM	R/W	1h	Reset by: WATCHDOG REG_RST	Enable termination Type : RW POR: 1b 0h = Disable 1h = Enable (default)
0	RESERVED	R	0h		Reserved

ADVANCE INFORMATION

7.5.1.13 REG10_Charger_Control_1 Register (Offset = 10h) [reset = 85h]

REG10_Charger_Control_1 is shown in Figure 7-37 and described in Table 7-26.

Return to the Table 7-12.

Charger Control 1

Figure 7-37. REG10_Charger_Control_1 Register

7	6	5	4	3	2	1	0
RESERVED		VAC_OVP_1:0		WD_RST	WATCHDOG_2:0		
R-0h		R/W-3h		R/W-0h	R/W-5h		

Table 7-26. REG10_Charger_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	RESERVED	R	0h		Reserved
5-4	VAC_OVP_1:0	R/W	0h	Reset by: REG_RST	VAC_OVP thresholds Type : RW POR: 00b 0h = 26V (default) 1h = 18V 2h = 12V 3h = 7V
3	WD_RST	R/W	0h	Reset by: WATCHDOG REG_RST	I2C watch dog timer reset Type : RW POR: 0b 0h = Normal (default) 1h = Reset (this bit goes back to 0 after timer resets)
2-0	WATCHDOG_2:0	R/W	5h	Reset by: REG_RST	Watchdog timer settings Type : RW POR: 101b 0h = Disable 1h = 0.5s 2h = 1s 3h = 2s 4h = 20s 5h = 40s (default) 6h = 80s 7h = 160s

ADVANCE INFORMATION

7.5.1.14 REG11_Charger_Control_2 Register (Offset = 11h) [reset = 40h]

REG11_Charger_Control_2 is shown in Figure 7-38 and described in Table 7-27.

Return to the Table 7-12.

Charger Control 2

Figure 7-38. REG11_Charger_Control_2 Register

7	6	5	4	3	2	1	0
FORCE_INDET	AUTO_INDET_EN	EN_12V	EN_9V	HVDCP_EN	SDRV_CTRL_1:0		SDRV_DLY
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

Table 7-27. REG11_Charger_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	FORCE_INDET	R/W	0h	Reset by: WATCHDOG REG_RST	Force D+/D- detection Type : RW POR: 0b 0h = Do NOT force D+/D- detection (default) 1h = Force D+/D- algorithm, when D+/D- detection is done, this bit will be reset to 0
6	AUTO_INDET_EN	R/W	1h	Reset by: WATCHDOG REG_RST	Automatic D+/D- Detection Enable Type : RW POR: 1b 0h = Disable D+/D- detection when VBUS is plugged-in 1h = Enable D+/D- detection when VBUS is plugged-in (default)
5	EN_12V	R/W	0h	Reset by: REG_RST	EN_12V HVDC Type : RW POR: 0b 0h = Disable 12V mode in HVDCP (default) 1h = Enable 12V mode in HVDCP
4	EN_9V	R/W	0h	Reset by: REG_RST	EN_9V HVDC Type : RW POR: 0b 0h = Disable 9V mode in HVDCP (default) 1h = Enable 9V mode in HVDCP
3	HVDCP_EN	R/W	0h	Reset by: REG_RST	High voltage DCP enable. Type : RW POR: 0b 0h = Disable HVDCP handshake (default) 1h = Enable HVDCP handshake
2-1	SDRV_CTRL_1:0	R/W	0h	Reset by: REG_RST	SFET control The external ship FET control logic to force the device enter different modes. Type : RW POR: 00b 0h = IDLE (default) 1h = Shutdown Mode 2h = Ship Mode 3h = System Power Reset
0	SDRV_DLY	R/W	0h	Reset by: REG_RST	Delay time added to the taking action in bit [2:1] of the SFET control Type : RW POR: 0b 0h = Add 10s delay time (default) 1h = Do NOT add 10s delay time

ADVANCE INFORMATION

7.5.1.15 REG12_Charger_Control_3 Register (Offset = 12h) [reset = 0h]

REG12_Charger_Control_3 is shown in Figure 7-39 and described in Table 7-28.

Return to the Table 7-12.

Charger Control 3

Figure 7-39. REG12_Charger_Control_3 Register

7	6	5	4	3	2	1	0
DIS_ACDRV	EN_OTG	PFM_OTG_DIS	PFM_FWD_DIS	WKUP_DLY	DIS_LDO	DIS_OTG_OOA	DIS_FWD_OOA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-28. REG12_Charger_Control_3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	DIS_ACDRV	R/W	0h		When this bit is set, the charger will force both EN_ACDRV1=0 and EN_ACDRV2=0 Type : RW POR: 0b
6	EN_OTG	R/W	0h	Reset by: WATCHDOG REG_RST	OTG mode control Type : RW POR: 0b 0h = OTG Disable (default) 1h = OTG Enable
5	PFM_OTG_DIS	R/W	0h	Reset by: WATCHDOG REG_RST	Disable PFM in OTG mode Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
4	PFM_FWD_DIS	R/W	0h	Reset by: REG_RST	Disable PFM in forward mode Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
3	WKUP_DLY	R/W	0h	Reset by: REG_RST	When wake up the device from ship mode, how much time (t_{SM_EXIT}) is required to pull low the $\overline{QON}$ pin. Type : RW POR: 0b 0h = 1s (Default) 1h = 15ms
2	DIS_LDO	R/W	0h	Reset by: WATCHDOG REG_RST	Disable BATFET LDO mode in pre-charge stage. Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
1	DIS_OTG_OOA	R/W	0h	Reset by: WATCHDOG REG_RST	Disable OOA in OTG mode Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
0	DIS_FWD_OOA	R/W	0h	Reset by: REG_RST	Disable OOA in forward mode Type : RW POR: 0b 0h = Enable (Default) 1h = Disable

ADVANCE INFORMATION

7.5.1.16 REG13_Charger_Control_4 Register (Offset = 13h) [reset = X]

REG13_Charger_Control_4 is shown in Figure 7-40 and described in Table 7-29.

Return to the Table 7-12.

Charger Control 4

Figure 7-40. REG13_Charger_Control_4 Register

7	6	5	4	3	2	1	0
EN_ACDRV2	EN_ACDRV1	PWM_FREQ	DIS_STAT	DIS_VSYS_SHORT	DIS_VOTG_UVP	FORCE_VINDPM_DET	EN_IBUS_OCP
R/W-0h	R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h

Table 7-29. REG13_Charger_Control_4 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	EN_ACDRV2	R/W	0h		External ACFET2-RBFET2 gate driver control At POR, if the charger detects that there is no ACFET2-RBFET2 populated, this bit will be locked at 0 Type : RW POR: 0b 0h = turn off (default) 1h = turn on
6	EN_ACDRV1	R/W	0h		External ACFET1-RBFET1 gate driver control At POR, if the charger detects that there is no ACFET1-RBFET1 populated, this bit will be locked at 0 Type : RW POR: 0b 0h = turn off (default) 1h = turn on
5	PWM_FREQ	R/W	X		Switching frequency selection, this bit POR default value is based on the PROG pin strapping. Type : RW 0h = 1.5 MHz 1h = 750 kHz
4	DIS_STAT	R/W	0h	Reset by: WATCHDOG REG_RST	Disable the STAT pin output Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
3	DIS_VSYS_SHORT	R/W	0h	Reset by: REG_RST	Disable forward mode VSYS short hiccup protection. Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
2	DIS_VOTG_UVP	R/W	0h	Reset by: REG_RST	Disable OTG mode VOTG UVP hiccup protection. Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
1	FORCE_VINDPM_DET	R/W	0h	Reset by: REG_RST	Force VINDPM detection Note: only when VBAT>VSYSMIN, this bit can be set to 1. Once the VINDPM auto detection is done, this bits returns to 0. Type : RW POR: 0b 0h = Do NOT force VINDPM detection (default) 1h = Force the converter stop switching, and ADC measures the VBUS voltage without input current, then the charger updates the VINDPM register accordingly.

Table 7-29. REG13_Charger_Control_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
0	EN_IBUS_OCP	R/W	1h	Reset by: REG_RST	Enable IBUS_OCP in forward mode Type : RW POR: 1b 0h = Disable 1h = Enable (default)

7.5.1.17 REG14_Charger_Control_5 Register (Offset = 14h) [reset = 16h]

REG14_Charger_Control_5 is shown in Figure 7-41 and described in Table 7-30.

Return to the Table 7-12.

Charger Control 5

Figure 7-41. REG14_Charger_Control_5 Register

7	6	5	4	3	2	1	0
SFET_PRESENT	RESERVED	EN_IBAT	IBAT_REG_1:0		EN_IINDPM	EN_EXTILIM	EN_BATOC
R/W-0h	R-0h	R/W-0h	R/W-2h		R/W-1h	R/W-1h	R/W-0h

Table 7-30. REG14_Charger_Control_5 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	SFET_PRESENT	R/W	0h		The user has to set this bit based on whether a ship FET is populated or not. The POR default value is 0, which means the charger does not support all the features associated with the ship FET. The register bits list below all are locked at 0. EN_BATOC=0 FORCE_SFET_OFF=0 SDRV_CTRL=00 When this bit is set to 1, the register bits list above become programmable, and the charger can support the features associated with the ship FET Type : RW POR: 0b 0h = No ship FET populated 1h = Ship FET populated
6	RESERVED	R	0h		Reserved
5	EN_IBAT	R/W	0h	Reset by: WATCHDOG REG_RST	IBAT current sensing enable Type : RW POR: 0b 0h = Disable the IBAT sensing at battery only condition (default) 1h = Enable the IBAT sensing at battery only condition
4-3	IBAT_REG_1:0	R/W	2h	Reset by: WATCHDOG REG_RST	Battery discharging current regulation in OTG mode Type : RW POR: 10b 0h = 3A 1h = 4A 2h = 5A (default) 3h = Disable
2	EN_IINDPM	R/W	1h	Reset by: WATCHDOG REG_RST	Enable the internal IINDPM register input current regulation Type : RW POR: 1b 0h = Disable 1h = Enable (default)
1	EN_EXTILIM	R/W	1h	Reset by: REG_RST	Enable the external ILIM_HIZ pin input current regulation Type : RW POR: 1b 0h = Disable 1h = Enable (default)
0	EN_BATOC	R/W	0h	Reset by: WATCHDOG REG_RST	Enable the battery discharging current OCP Type : RW POR: 0b 0h = Disable (default) 1h = Enable

ADVANCE INFORMATION

7.5.1.18 REG15_MPPT_Control Register (Offset = 15h) [reset = AAh]

REG15_MPPT_Control is shown in Figure 7-42 and described in Table 7-31.

Return to the Table 7-12.

MPPT Control

Figure 7-42. REG15_MPPT_Control Register

7	6	5	4	3	2	1	0
VOC_PCT_2:0			VOC_DLY_1:0		VOC_RATE_1:0		EN_MPPT
R/W-5h			R/W-1h		R/W-1h		R/W-0h

Table 7-31. REG15_MPPT_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-5	VOC_PCT_2:0	R/W	5h	Reset by: REG_RST	To set the VINDPM as a percentage of the VBUS open circuit voltage when the VOC measurement is done. Type : RW POR: 101b 0h = 0.5625 1h = 0.625 2h = 0.6875 3h = 0.75 4h = 0.8125 5h = 0.875 (default) 6h = 0.9375 7h = 1
4-3	VOC_DLY_1:0	R/W	1h	Reset by: REG_RST	After the converter stops switching, the time delay before the VOC is measured. Type : RW POR: 01b 0h = 50ms 1h = 300ms (default) 2h = 2s 3h = 5s
2-1	VOC_RATE_1:0	R/W	1h	Reset by: REG_RST	The time interval two VBUS open circuit voltage measurements. Type : RW POR: 01b 0h = 30s 1h = 2mins (default) 2h = 10mins 3h = 30mins
0	EN_MPPT	R/W	0h	Reset by: REG_RST	Enable the MPPT to measure the VBUS open circuit voltage. Type : RW POR: 0b 0h = Disable (default) 1h = Enable

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7.5.1.19 REG16_Temperature_Control Register (Offset = 16h) [reset = C0h]

REG16_Temperature_Control is shown in Figure 7-43 and described in Table 7-32.

Return to the Table 7-12.

Temperature Control

Figure 7-43. REG16_Temperature_Control Register

7	6	5	4	3	2	1	0
TREG_1:0		TSHUT_1:0		VBUS_PD_EN	VAC1_PD_EN	VAC2_PD_EN	RESERVED
R/W-3h		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R-0h

Table 7-32. REG16_Temperature_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	TREG_1:0	R/W	3h	Reset by: WATCHDOG REG_RST	Thermal regulation thresholds. Type : RW POR: 11b 0h = 60°C 1h = 80°C 2h = 100°C 3h = 120°C (default)
5-4	TSHUT_1:0	R/W	0h	Reset by: WATCHDOG REG_RST	Thermal shutdown thresholds. Type : RW POR: 00b 0h = 150°C (default) 1h = 130°C 2h = 120°C 3h = 85°C
3	VBUS_PD_EN	R/W	0h	Reset by: REG_RST	Enable VBUS pull down resistor (6k Ohm) Type : RW POR: 0b 0h = Disable (default) 1h = Enable
2	VAC1_PD_EN	R/W	0h	Reset by: REG_RST	Enable VAC1 pull down resistor Type : RW POR: 0b 0h = Disable (default) 1h = Enable
1	VAC2_PD_EN	R/W	0h	Reset by: REG_RST	Enable VAC2 pull down resistor Type : RW POR: 0b 0h = Disable (default) 1h = Enable
0	RESERVED	R	0h		Reserved

ADVANCE INFORMATION

7.5.1.20 REG17_NTC_Control_0 Register (Offset = 17h) [reset = 7Ah]

REG17_NTC_Control_0 is shown in Figure 7-44 and described in Table 7-33.

Return to the Table 7-12.

NTC Control 0

Figure 7-44. REG17_NTC_Control_0 Register

7	6	5	4	3	2	1	0
JEITA_VSET_2:0			JEITA_ISETH_1:0		JEITA_ISETC_1:0		RESERVED
R/W-3h			R/W-3h		R/W-1h		R-0h

Table 7-33. REG17_NTC_Control_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-5	JEITA_VSET_2:0	R/W	3h	Reset by: WATCHDOG REG_RST	JEITA high temperature range (TWARN – THOT) charge voltage setting Type : RW POR: 011b 0h = Charge Suspend 1h = Set VREG to VREG-800mV 2h = Set VREG to VREG-600mV 3h = Set VREG to VREG-400mV (default) 4h = Set VREG to VREG-300mV 5h = Set VREG to VREG-200mV 6h = Set VREG to VREG-100mV 7h = VREG unchanged
4-3	JEITA_ISETH_1:0	R/W	3h	Reset by: WATCHDOG REG_RST	JEITA high temperature range (TWARN – THOT) charge current setting Type : RW POR: 11b 0h = Charge Suspend 1h = Set ICHG to 20%* ICHG 2h = Set ICHG to 40%* ICHG 3h = ICHG unchanged (default)
2-1	JEITA_ISETC_1:0	R/W	1h	Reset by: WATCHDOG REG_RST	JEITA low temperature range (TCOLD – TCOOL) charge current setting Type : RW POR: 01b 0h = Charge Suspend 1h = Set ICHG to 20%* ICHG (default) 2h = Set ICHG to 40%* ICHG 3h = ICHG unchanged
0	RESERVED	R	0h		Reserved

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7.5.1.21 REG18_NTC_Control_1 Register (Offset = 18h) [reset = 54h]

REG18_NTC_Control_1 is shown in Figure 7-45 and described in Table 7-34.

Return to the Table 7-12.

NTC Control 1

Figure 7-45. REG18_NTC_Control_1 Register

7	6	5	4	3	2	1	0
TS_COOL_1:0		TS_WARM_1:0		BHOT_1:0		BCOLD	TS_IGNORE
R/W-1h		R/W-1h		R/W-1h		R/W-0h	R/W-0h

Table 7-34. REG18_NTC_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-6	TS_COOL_1:0	R/W	1h	Reset by: WATCHDOG REG_RST	JEITA VT2 comparator voltage rising thresholds as a percentage of REGN. The corresponding temperature in the brackets is achieved when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ. Type : RW POR: 01b 0h = 71.1% (5°C) 1h = 68.4% (default) (10°C) 2h = 65.5% (15°C) 3h = 62.4% (20°C)
5-4	TS_WARM_1:0	R/W	1h	Reset by: WATCHDOG REG_RST	JEITA VT3 comparator voltage falling thresholds as a percentage of REGN. The corresponding temperature in the brackets is achieved when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ. Type : RW POR: 01b 0h = 48.4% (40°C) 1h = 44.8% (default) (45°C) 2h = 41.2% (50°C) 3h = 37.7% (55°C)
3-2	BHOT_1:0	R/W	1h	Reset by: WATCHDOG REG_RST	OTG mode TS HOT temperature threshold Type : RW POR: 01b 0h = 55°C 1h = 60°C (default) 2h = 65°C 3h = Disable
1	BCOLD	R/W	0h	Reset by: WATCHDOG REG_RST	OTG mode TS COLD temperature threshold Type : RW POR: 0b 0h = -10°C (default) 1h = -20°C
0	TS_IGNORE	R/W	0h	Reset by: WATCHDOG REG_RST	Ignore the TS feedback, the charger considers the TS is always good to allow the charging and OTG modes, all the four TS status bits always stay at 0000 to report the normal condition. Type : RW POR: 0b 0h = NOT ignore (Default) 1h = Ignore

7.5.1.22 REG19_ICO_Current_Limit Register (Offset = 19h) [reset = 0h]

REG19_ICO_Current_Limit is shown in Figure 7-46 and described in Table 7-35.

Return to the Table 7-12.

ICO Current Limit

Figure 7-46. REG19_ICO_Current_Limit Register

15	14	13	12	11	10	9	8
RESERVED							ICO_ILIM_8:0
R-0h							R-0h
7	6	5	4	3	2	1	0
ICO_ILIM_8:0							
R-0h							

Table 7-35. REG19_ICO_Current_Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	RESERVED
8-0	ICO_ILIM_8:0	R	0h	Input Current Limit obtained from ICO or ILIM_HIZ pin setting Type : R POR: 0mA (0h) Range : 100mA-3300mA Fixed Offset : 0mA Bit Step Size : 10mA Clamped Low

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7.5.1.23 REG1B_Charger_Status_0 Register (Offset = 1Bh) [reset = 0h]

REG1B_Charger_Status_0 is shown in Figure 7-47 and described in Table 7-36.

Return to the Table 7-12.

Charger Status 0

Figure 7-47. REG1B_Charger_Status_0 Register

7	6	5	4	3	2	1	0
IINDPM_STAT	VINDPM_STAT	WD_STAT	POORSRC_STAT	PG_STAT	AC2_PRESENT_STAT	AC1_PRESENT_STAT	VBUS_PRESENT_STAT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-36. REG1B_Charger_Status_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IINDPM_STAT	R	0h	IINDPM status (forward mode) or IOTG status (OTG mode) Type : R POR: 0b 0h = Normal 1h = In IINDPM regulation or IOTG regulation
6	VINDPM_STAT	R	0h	VINDPM status (forward mode) or VOTG status (OTG mode) Type : R POR: 0b 0h = Normal 1h = In VINDPM regulation or VOTG regualtion
5	WD_STAT	R	0h	I2C watch dog timer status Type : R POR: 0b 0h = Normal 1h = WD timer expired
4	POORSRC_STAT	R	0h	Poor source detection status Type : R POR: 0b 0h = Normal 1h = Weak adaptor detected
3	PG_STAT	R	0h	Power Good Status Type : R POR: 0b 0h = NOT in power good status 1h = Power good
2	AC2_PRESENT_STAT	R	0h	VAC2 insert status Type : R POR: 0b 0h = VAC2 NOT present 1h = VAC2 present (above present threshold)
1	AC1_PRESENT_STAT	R	0h	VAC1 insert status Type : R POR: 0b 0h = VAC1 NOT present 1h = VAC1 present (above present threshold)

Table 7-36. REG1B_Charger_Status_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	VBUS_PRESENT_STAT	R	0h	VBUS present status Type : R POR: 0b 0h = VBUS NOT present 1h = VBUS present (above present threshold)

7.5.1.24 REG1C_Charger_Status_1 Register (Offset = 1Ch) [reset = 0h]

REG1C_Charger_Status_1 is shown in Figure 7-48 and described in Table 7-37.

Return to the Table 7-12.

Charger Status 1

Figure 7-48. REG1C_Charger_Status_1 Register

7	6	5	4	3	2	1	0
CHG_STAT_2:0			VBUS_STAT_3:0				BC1.2_DONE_STAT
R-0h			R-0h				R-0h

Table 7-37. REG1C_Charger_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	CHG_STAT_2:0	R	0h	Charge Status bits Type : R POR: 000b 0h = Not Charging 1h = Trickle Charge 2h = Pre-charge 3h = Fast charge (CC mode) 4h = Taper Charge (CV mode) 5h = Reserved 6h = Top-off Timer Active Charging 7h = Charge Termination Done
4-1	VBUS_STAT_3:0	R	0h	VBUS status bits 0h: No Input or BHOT or BCOLD in OTG mode 1h: USB SDP (500mA) 2h: USB CDP (1.5A) 3h: USB DCP (3.25A) 4h: Adjustable High Voltage DCP (HVDCP) (1.5A) 5h: Unknown adaptor (3A) 6h: Non-Standard Adapter (1A/2A/2.1A/2.4A) 7h: In OTG mode 8h: Not qualified adaptor 9h: Reserved Ah: Reserved Bh: Device directly powered from VBUS Ch: Reserved Dh: Reserved Eh: Reserved Fh: Reserved Type : R POR: 0h
0	BC1.2_DONE_STAT	R	0h	BC1.2 status bit Type : R POR: 0b 0h = BC1.2 or non-standard detection NOT complete 1h = BC1.2 or non-standard detection complete

7.5.1.25 REG1D_Charger_Status_2 Register (Offset = 1Dh) [reset = 0h]

REG1D_Charger_Status_2 is shown in Figure 7-49 and described in Table 7-38.

Return to the Table 7-12.

Charger Status 2

Figure 7-49. REG1D_Charger_Status_2 Register

7	6	5	4	3	2	1	0
ICO_STAT_1:0		RESERVED			TREG_STAT	DPDM_STAT	VBAT_PRESENT_STAT
R-0h		R-0h			R-0h	R-0h	R-0h

Table 7-38. REG1D_Charger_Status_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ICO_STAT_1:0	R	0h	Input Current Optimizer (ICO) status Type : R POR: 00b 0h = ICO disabled 1h = ICO optimization in progress 2h = Maximum input current detected 3h = Reserved
5-3	RESERVED	R	0h	RESERVED
2	TREG_STAT	R	0h	IC thermal regulation status Type : R POR: 0b 0h = Normal 1h = Device in thermal regulation
1	DPDM_STAT	R	0h	D+/D- detection status bits Type : R POR: 0b 0h = The D+/D- detection is NOT started yet, or the detection is done 1h = The D+/D- detection is ongoing
0	VBAT_PRESENT_STAT	R	0h	Battery present status (V_{BAT} > V_{BAT_UVLOZ}) Type : R POR: 0b 0h = V_{BAT} NOT present 1h = V_{BAT} present

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7.5.1.26 REG1E_Charger_Status_3 Register (Offset = 1Eh) [reset = 0h]

REG1E_Charger_Status_3 is shown in Figure 7-50 and described in Table 7-39.

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Charger Status 3

Figure 7-50. REG1E_Charger_Status_3 Register

7	6	5	4	3	2	1	0
ACRB2_STAT	ACRB1_STAT	ADC_DONE_STAT	VSYS_STAT	CHG_TMR_STAT	TRICHG_TMR_STAT	PRECHG_TMR_STAT	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-39. REG1E_Charger_Status_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ACRB2_STAT	R	0h	The ACFET2-RBFET2 status Type : R POR: 0b 0h = ACFET2-RBFET2 is NOT placed 1h = ACFET2-RBFET2 is placed
6	ACRB1_STAT	R	0h	The ACFET1-RBFET1 status Type : R POR: 0b 0h = ACFET1-RBFET1 is NOT placed 1h = ACFET1-RBFET1 is placed
5	ADC_DONE_STAT	R	0h	ADC Conversion Status (in one-shot mode only) Type : R POR: 0b 0h = Conversion NOT complete 1h = Conversion complete
4	VSYS_STAT	R	0h	VSYS Regulation Status (forward mode) Type : R POR: 0b 0h = Not in VSYSMIN regulation (V_{BAT} > V_{SYSMIN}) 1h = In VSYSMIN regulation (V_{BAT} < V_{SYSMIN})
3	CHG_TMR_STAT	R	0h	Fast charge timer status Type : R POR: 0b 0h = Normal 1h = Safety timer expired
2	TRICHG_TMR_STAT	R	0h	Trickle charge timer status Type : R POR: 0b 0h = Normal 1h = Safety timer expired
1	PRECHG_TMR_STAT	R	0h	Pre-charge timer status Type : R POR: 0b 0h = Normal 1h = Safety timer expired
0	RESERVED	R	0h	RESERVED

7.5.1.27 REG1F_Charger_Status_4 Register (Offset = 1Fh) [reset = 0h]

REG1F_Charger_Status_4 is shown in Figure 7-51 and described in Table 7-40.

Return to the Table 7-12.

Charger Status 4

Figure 7-51. REG1F_Charger_Status_4 Register

7	6	5	4	3	2	1	0
RESERVED			VBATOTG_LOW_STAT	TS_COLD_STAT	TS_COOL_STAT	TS_WARM_STAT	TS_HOT_STAT
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-40. REG1F_Charger_Status_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	RESERVED
4	VBATOTG_LOW_STAT	R	0h	The battery voltage is too low to enable OTG mode. Type : R POR: 0b 0h = The battery voltage is high enough to enable the OTG operation 1h = The battery volage is too low to enable the OTG operation
3	TS_COLD_STAT	R	0h	The TS temperature is in the cold range, lower than T1. Type : R POR: 0b 0h = TS status is NOT in cold range 1h = TS status is in cold range
2	TS_COOL_STAT	R	0h	The TS temperature is in the cool range, between T1 and T2. Type : R POR: 0b 0h = TS status is NOT in cool range 1h = TS status is in cool range
1	TS_WARM_STAT	R	0h	The TS temperature is in the warm range, between T3 and T5. Type : R POR: 0b 0h = TS status is NOT in warm range 1h = TS status is in warm range
0	TS_HOT_STAT	R	0h	The TS temperature is in the hot range, higher than T5. Type : R POR: 0b 0h = TS status is NOT in hot range 1h = TS status is in hot range

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7.5.1.28 REG20_FAULT_Status_0 Register (Offset = 20h) [reset = 0h]

REG20_FAULT_Status_0 is shown in Figure 7-52 and described in Table 7-41.

Return to the Table 7-12.

FAULT Status 0

Figure 7-52. REG20_FAULT_Status_0 Register

7	6	5	4	3	2	1	0
IBAT_REG_STAT	VBUS_OVP_STAT	VBAT_OVP_STAT	IBUS_OCP_STAT	IBAT_OCP_STAT	CONV_OCP_STAT	VAC2_OVP_STAT	VAC1_OVP_STAT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-41. REG20_FAULT_Status_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IBAT_REG_STAT	R	0h	IBAT regulation status Type : R POR: 0b 0h = Normal 1h = Device in battery discharging current regulation
6	VBUS_OVP_STAT	R	0h	VBUS over-voltage status Type : R POR: 0b 0h = Normal 1h = Device in over voltage protection
5	VBAT_OVP_STAT	R	0h	VBAT over-voltage status Type : R POR: 0b 0h = Normal 1h = Device in over voltage protection
4	IBUS_OCP_STAT	R	0h	IBUS over-current status Type : R POR: 0b 0h = Normal 1h = Device in over current protection
3	IBAT_OCP_STAT	R	0h	IBAT over-current status Type : R POR: 0b 0h = Normal 1h = Device in over current protection
2	CONV_OCP_STAT	R	0h	Converter over current status Type : R POR: 0b 0h = Normal 1h = Converter in over current protection
1	VAC2_OVP_STAT	R	0h	VAC2 over-voltage status Type : R POR: 0b 0h = Normal 1h = Device in over voltage protection

Table 7-41. REG20_FAULT_Status_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	VAC1_OVP_STAT	R	0h	VAC1 over-voltage status Type : R POR: 0b 0h = Normal 1h = Device in over voltage protection

7.5.1.29 REG21_FAULT_Status_1 Register (Offset = 21h) [reset = 0h]

REG21_FAULT_Status_1 is shown in Figure 7-53 and described in Table 7-42.

Return to the Table 7-12.

FAULT Status 1

Figure 7-53. REG21_FAULT_Status_1 Register

7	6	5	4	3	2	1	0
VSYS_SHORT_STAT	VSYS_OVP_STAT	OTG_OVP_STAT	OTG_UVP_STAT	RESERVED	TSHUT_STAT	RESERVED	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	

Table 7-42. REG21_FAULT_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VSYS_SHORT_STAT	R	0h	VSYS short circuit status Type : R POR: 0b 0h = Normal 1h = Device in SYS short circuit protection
6	VSYS_OVP_STAT	R	0h	VSYS over-voltage status Type : R POR: 0b 0h = Normal 1h = Device in SYS over-voltage protection
5	OTG_OVP_STAT	R	0h	OTG over voltage status Type : R POR: 0b 0h = Normal 1h = Device in OTG over-voltage
4	OTG_UVP_STAT	R	0h	OTG under voltage status. Type : R POR: 0b 0h = Normal 1h = Device in OTG under voltage
3	RESERVED	R	0h	RESERVED
2	TSHUT_STAT	R	0h	IC temperature shutdown status Type : R POR: 0b 0h = Normal 1h = Device in thermal shutdown protection
1-0	RESERVED	R	0h	RESERVED

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7.5.1.30 REG22_Charger_Flag_0 Register (Offset = 22h) [reset = 0h]

REG22_Charger_Flag_0 is shown in Figure 7-54 and described in Table 7-43.

Return to the Table 7-12.

Charger Flag 0

Figure 7-54. REG22_Charger_Flag_0 Register

7	6	5	4	3	2	1	0
IINDPM_FLAG	VINDPM_FLAG	WD_FLAG	POORSRC_FLAG	PG_FLAG	AC2_PRESENT_FLAG	AC1_PRESENT_FLAG	VBUS_PRESENT_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-43. REG22_Charger_Flag_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IINDPM_FLAG	R	0h	IINDPM / IOTG flag Type : R POR: 0b 0h = Normal 1h = IINDPM / IOTG signal rising edge detected
6	VINDPM_FLAG	R	0h	VINDPM / VOTG Flag Type : R POR: 0b 0h = Normal 1h = VINDPM / VOTG regulation signal rising edge detected
5	WD_FLAG	R	0h	I2C watchdog timer flag Type : R POR: 0b 0h = Normal 1h = WD timer signal rising edge detected
4	POORSRC_FLAG	R	0h	Poor source detection flag Type : R POR: 0b 0h = Normal 1h = Poor source status rising edge detected
3	PG_FLAG	R	0h	Power good flag Type : R POR: 0b 0h = Normal 1h = Any change in PG_STAT even (adapter good qualification or adapter good going away)
2	AC2_PRESENT_FLAG	R	0h	VAC2 present flag Type : R POR: 0b 0h = Normal 1h = VAC2 present status changed
1	AC1_PRESENT_FLAG	R	0h	VAC1 present flag Type : R POR: 0b 0h = Normal 1h = VAC1 present status changed

Table 7-43. REG22_Charger_Flag_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	VBUS_PRESENT_FLAG	R	0h	VBUS present flag Type : R POR: 0b 0h = Normal 1h = VBUS present status changed

7.5.1.31 REG23_Charger_Flag_1 Register (Offset = 23h) [reset = 0h]

REG23_Charger_Flag_1 is shown in Figure 7-55 and described in Table 7-44.

Return to the Table 7-12.

Charger Flag 1

Figure 7-55. REG23_Charger_Flag_1 Register

7	6	5	4	3	2	1	0
CHG_FLAG	ICO_FLAG	RESERVED	VBUS_FLAG	RESERVED	TREG_FLAG	VBAT_PRESENT_FLAG	BC1.2_DONE_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-44. REG23_Charger_Flag_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CHG_FLAG	R	0h	Charge status flag Type : R POR: 0b 0h = Normal 1h = Charge status changed
6	ICO_FLAG	R	0h	ICO status flag Type : R POR: 0b 0h = Normal 1h = ICO status changed
5	RESERVED	R	0h	RESERVED
4	VBUS_FLAG	R	0h	VBUS status flag Type : R POR: 0b 0h = Normal 1h = VBUS status changed
3	RESERVED	R	0h	RESERVED
2	TREG_FLAG	R	0h	IC thermal regulation flag Type : R POR: 0b 0h = Normal 1h = TREG signal rising threshold detected
1	VBAT_PRESENT_FLAG	R	0h	VBAT present flag Type : R POR: 0b 0h = Normal 1h = VBAT present status changed
0	BC1.2_DONE_FLAG	R	0h	BC1.2 status Flag Type : R POR: 0b 0h = Normal 1h = BC1.2 detection status changed

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7.5.1.32 REG24_Charger_Flag_2 Register (Offset = 24h) [reset = 0h]

REG24_Charger_Flag_2 is shown in Figure 7-56 and described in Table 7-45.

Return to the Table 7-12.

Charger Flag 2

Figure 7-56. REG24_Charger_Flag_2 Register

7	6	5	4	3	2	1	0
RESERVED	DPDM_DONE_FLAG	ADC_DONE_FLAG	VSYS_FLAG	CHG_TMR_FLAG	TRICHG_TMR_FLAG	PRECHG_TMR_FLAG	TOPOFF_TMR_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-45. REG24_Charger_Flag_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	RESERVED
6	DPDM_DONE_FLAG	R	0h	D+/D- detection is done flag. Type : R POR: 0b 0h = D+/D- detection is NOT started or still ongoing 1h = D+/D- detection is completed
5	ADC_DONE_FLAG	R	0h	ADC conversion flag (only in one-shot mode) Type : R POR: 0b 0h = Conversion NOT completed 1h = Conversion completed
4	VSYS_FLAG	R	0h	VSYSMIN regulation flag Type : R POR: 0b 0h = Normal 1h = Entered or existed VSYSMIN regulation
3	CHG_TMR_FLAG	R	0h	Fast charge timer flag Type : R POR: 0b 0h = Normal 1h = Fast charge timer expired rising edge detected
2	TRICHG_TMR_FLAG	R	0h	Trickle charge timer flag Type : R POR: 0b 0h = Normal 1h = Trickle charger timer expired rising edge detected
1	PRECHG_TMR_FLAG	R	0h	Pre-charge timer flag Type : R POR: 0b 0h = Normal 1h = Pre-charge timer expired rising edge detected
0	TOPOFF_TMR_FLAG	R	0h	Top off timer flag Type : R POR: 0b 0h = Normal 1h = Top off timer expired rising edge detected

7.5.1.33 REG25_Charger_Flag_3 Register (Offset = 25h) [reset = 0h]

REG25_Charger_Flag_3 is shown in Figure 7-57 and described in Table 7-46.

Return to the Table 7-12.

Charger Flag 3

Figure 7-57. REG25_Charger_Flag_3 Register

7	6	5	4	3	2	1	0
RESERVED			VBATOTG_LOW_FLAG	TS_COLD_FLAG	TS_COOL_FLAG	TS_WARM_FLAG	TS_HOT_FLAG
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-46. REG25_Charger_Flag_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	RESERVED
4	VBATOTG_LOW_FLAG	R	0h	VBAT too low to enable OTG flag Type : R POR: 0b 0h = Normal 1h = VBAT falls below the threshold to enable the OTG mode
3	TS_COLD_FLAG	R	0h	TS cold temperature flag Type : R POR: 0b 0h = Normal 1h = TS across cold temperature (T1) is detected
2	TS_COOL_FLAG	R	0h	TS cool temperature flag Type : R POR: 0b 0h = Normal 1h = TS across cool temperature (T2) is detected
1	TS_WARM_FLAG	R	0h	TS warm temperature flag Type : R POR: 0b 0h = Normal 1h = TS across warm temperature (T3) is detected
0	TS_HOT_FLAG	R	0h	TS hot temperature flag Type : R POR: 0b 0h = Normal 1h = TS across hot temperature (T5) is detected

7.5.1.34 REG26_FAULT_Flag_0 Register (Offset = 26h) [reset = 0h]

REG26_FAULT_Flag_0 is shown in Figure 7-58 and described in Table 7-47.

Return to the Table 7-12.

FAULT Flag 0

Figure 7-58. REG26_FAULT_Flag_0 Register

7	6	5	4	3	2	1	0
IBAT_REG_FLAG	VBUS_OVP_FLAG	VBAT_OVP_FLAG	IBUS_OCP_FLAG	IBAT_OCP_FLAG	CONV_OCP_FLAG	VAC2_OVP_FLAG	VAC1_OVP_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-47. REG26_FAULT_Flag_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IBAT_REG_FLAG	R	0h	IBAT regulation flag Type : R POR: 0b 0h = Normal 1h = Enter or exit IBAT regulation
6	VBUS_OVP_FLAG	R	0h	VBUS over-voltage flag Type : R POR: 0b 0h = Normal 1h = Enter VBUS OVP
5	VBAT_OVP_FLAG	R	0h	VBAT over-voltage flag Type : R POR: 0b 0h = Normal 1h = Enter VBAT OVP
4	IBUS_OCP_FLAG	R	0h	IBUS over-current flag Type : R POR: 0b 0h = Normal 1h = Enter IBUS OCP
3	IBAT_OCP_FLAG	R	0h	IBAT over-current flag Type : R POR: 0b 0h = Normal 1h = Enter discharged OCP
2	CONV_OCP_FLAG	R	0h	Converter over-current flag Type : R POR: 0b 0h = Normal 1h = Enter converter OCP
1	VAC2_OVP_FLAG	R	0h	VAC2 over-voltage flag Type : R POR: 0b 0h = Normal 1h = Enter VAC2 OVP

Table 7-47. REG26_FAULT_Flag_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	VAC1_OVP_FLAG	R	0h	VAC1 over-voltage flag Type : R POR: 0b 0h = Normal 1h = Enter VAC1 OVP

7.5.1.35 REG27_FAULT_Flag_1 Register (Offset = 27h) [reset = 0h]

REG27_FAULT_Flag_1 is shown in Figure 7-59 and described in Table 7-48.

Return to the Table 7-12.

FAULT Flag 1

Figure 7-59. REG27_FAULT_Flag_1 Register

7	6	5	4	3	2	1	0
VSYS_SHORT_FLAG	VSYS_OVP_FLAG	OTG_OVP_FLAG	OTG_UVP_FLAG	RESERVED	TSHUT_FLAG	RESERVED	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	

Table 7-48. REG27_FAULT_Flag_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VSYS_SHORT_FLAG	R	0h	VSYS short circuit flag Type : R POR: 0b 0h = Normal 1h = Stop switching due to system short
6	VSYS_OVP_FLAG	R	0h	VSYS over-voltage flag Type : R POR: 0b 0h = Normal 1h = Stop switching due to system over-voltage
5	OTG_OVP_FLAG	R	0h	OTG over-voltage flag Type : R POR: 0b 0h = Normal 1h = Stop OTG due to VBUS over voltage
4	OTG_UVP_FLAG	R	0h	OTG under-voltage flag Type : R POR: 0b 0h = Normal 1h = Stop OTG due to VBUS under-voltage
3	RESERVED	R	0h	RESERVED
2	TSHUT_FLAG	R	0h	IC thermal shutdown flag Type : R POR: 0b 0h = Normal 1h = TS shutdown signal rising threshold detected
1-0	RESERVED	R	0h	RESERVED

7.5.1.36 REG28_Charger_Mask_0 Register (Offset = 28h) [reset = 0h]

REG28_Charger_Mask_0 is shown in Figure 7-60 and described in Table 7-49.

Return to the Table 7-12.

Charger Mask 0

Figure 7-60. REG28_Charger_Mask_0 Register

7	6	5	4	3	2	1	0
IINDPM_MASK	VINDPM_MASK	WD_MASK	POORSRC_MASK	PG_MASK	AC2_PRESENT_MASK	AC1_PRESENT_MASK	VBUS_PRESENT_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-49. REG28_Charger_Mask_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	IINDPM_MASK	R/W	0h	Reset by: REG_RST	IINDPM / IOTG mask flag Type : RW POR: 0b 0h = Enter IINDPM / IOTG does produce INT pulse 1h = Enter IINDPM / IOTG does NOT produce INT pulse
6	VINDPM_MASK	R/W	0h	Reset by: REG_RST	VINDPM / VOTG mask flag Type : RW POR: 0b 0h = Enter VINDPM / VOTG does produce INT pulse 1h = Enter VINDPM / VOTG does NOT produce INT pulse
5	WD_MASK	R/W	0h	Reset by: REG_RST	I2C watch dog timer mask flag Type : RW POR: 0b 0h = I2C watch dog timer expired does produce INT pulse 1h = I2C watch dog timer expired does NOT produce INT pulse
4	POORSRC_MASK	R/W	0h	Reset by: REG_RST	Poor source detection mask flag Type : RW POR: 0b 0h = Poor source detected does produce INT 1h = Poor source detected does NOT produce INT
3	PG_MASK	R/W	0h	Reset by: REG_RST	Power Good mask flag Type : RW POR: 0b 0h = PG toggle does produce INT 1h = PG toggle does NOT produce INT
2	AC2_PRESENT_MASK	R/W	0h	Reset by: REG_RST	VAC2 present mask flag Type : RW POR: 0b 0h = VAC2 present status change does produce INT 1h = VAC2 present status change does NOT produce INT
1	AC1_PRESENT_MASK	R/W	0h	Reset by: REG_RST	VAC1 present mask flag Type : RW POR: 0b 0h = VAC1 present status change does produce INT 1h = VAC1 present status change does NOT produce INT

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Table 7-49. REG28_Charger_Mask_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Notes	Description
0	VBUS_PRESENT_MASK	R/W	0h	Reset by: REG_RST	VBUS present mask flag Type : RW POR: 0b 0h = VBUS present status change does produce INT 1h = VBUS present status change does NOT produce INT

7.5.1.37 REG29_Charger_Mask_1 Register (Offset = 29h) [reset = 0h]

REG29_Charger_Mask_1 is shown in Figure 7-61 and described in Table 7-50.

Return to the Table 7-12.

Charger Mask 1

Figure 7-61. REG29_Charger_Mask_1 Register

7	6	5	4	3	2	1	0
CHG_MASK	ICO_MASK	RESERVED	VBUS_MASK	RESERVED	TREG_MASK	VBAT_PRESENT_MASK	BC1.2_DONE_MASK
R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-50. REG29_Charger_Mask_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	CHG_MASK	R/W	0h	Reset by: REG_RST	Charge status mask flag Type : RW POR: 0b 0h = Charging status change does produce INT 1h = Charging status change does NOT produce INT
6	ICO_MASK	R/W	0h	Reset by: REG_RST	ICO status mask flag Type : RW POR: 0b 0h = ICO status change does produce INT 1h = ICO status change does NOT produce INT
5	RESERVED	R	0h		RESERVED
4	VBUS_MASK	R/W	0h	Reset by: REG_RST	VBUS status mask flag Type : RW POR: 0b 0h = VBUS status change does produce INT 1h = VBUS status change does NOT produce INT
3	RESERVED	R	0h		RESERVED
2	TREG_MASK	R/W	0h	Reset by: REG_RST	IC thermal regulation mask flag Type : RW POR: 0b 0h = entering TREG does produce INT 1h = entering TREG does NOT produce INT
1	VBAT_PRESENT_MASK	R/W	0h	Reset by: REG_RST	VBAT present mask flag Type : RW POR: 0b 0h = VBAT present status change does produce INT 1h = VBAT present status change does NOT produce INT
0	BC1.2_DONE_MASK	R/W	0h	Reset by: REG_RST	BC1.2 status mask flag Type : RW POR: 0b 0h = BC1.2 status change does produce INT 1h = BC1.2 status change does NOT produce INT

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7.5.1.38 REG2A_Charger_Mask_2 Register (Offset = 2Ah) [reset = 0h]

REG2A_Charger_Mask_2 is shown in Figure 7-62 and described in Table 7-51.

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Charger Mask 2

Figure 7-62. REG2A_Charger_Mask_2 Register

7	6	5	4	3	2	1	0
RESERVED	DPDM_DONE_MASK	ADC_DONE_MASK	VSYS_MASK	CHG_TMR_MASK	TRICHG_TMR_MASK	PRECHG_TMR_MASK	TOPOFF_TMR_MASK
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-51. REG2A_Charger_Mask_2 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	RESERVED	R	0h		RESERVED
6	DPDM_DONE_MASK	R/W	0h	Reset by: REG_RST	D+/D- detection is done mask flag Type : RW POR: 0b 0h = D+/D- detection done does produce INT pulse 1h = D+/D- detection done does NOT produce INT pulse
5	ADC_DONE_MASK	R/W	0h	Reset by: REG_RST	ADC conversion mask flag (only in one-shot mode) Type : RW POR: 0b 0h = ADC conversion done does produce INT pulse 1h = ADC conversion done does NOT produce INT pulse
4	VSYS_MASK	R/W	0h	Reset by: REG_RST	VSYS min regulation mask flag Type : RW POR: 0b 0h = enter or exit VSYSMIN regulation does produce INT pulse 1h = enter or exit VSYSMIN regulation does NOT produce INT pulse
3	CHG_TMR_MASK	R/W	0h	Reset by: REG_RST	Fast charge timer mask flag Type : RW POR: 0b 0h = Fast charge timer expire does produce INT 1h = Fast charge timer expire does NOT produce INT
2	TRICHG_TMR_MASK	R/W	0h	Reset by: REG_RST	Trickle charge timer mask flag Type : RW POR: 0b 0h = Trickle charge timer expire does produce INT 1h = Trickle charge timer expire does NOT produce INT
1	PRECHG_TMR_MASK	R/W	0h	Reset by: REG_RST	Pre-charge timer mask flag Type : RW POR: 0b 0h = Pre-charge timer expire does produce INT 1h = Pre-charge timer expire does NOT produce INT
0	TOPOFF_TMR_MASK	R/W	0h	Reset by: REG_RST	Top off timer mask flag Type : RW POR: 0b 0h = Top off timer expire does produce INT 1h = Top off timer expire does NOT produce INT

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7.5.1.39 REG2B_Charger_Mask_3 Register (Offset = 2Bh) [reset = 0h]

REG2B_Charger_Mask_3 is shown in Figure 7-63 and described in Table 7-52.

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Charger Mask 3

Figure 7-63. REG2B_Charger_Mask_3 Register

7	6	5	4	3	2	1	0
RESERVED			VBATOTG_LOW_MASK	TS_COLD_MASK	TS_COOL_MASK	TS_WARM_MASK	TS_HOT_MASK
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-52. REG2B_Charger_Mask_3 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7-5	RESERVED	R	0h		RESERVED
4	VBATOTG_LOW_MASK	R/W	0h	Reset by: WATCHDOG REG_RST	VBAT too low to enable OTG mask Type : RW POR: 0b 0h = VBAT falling below the threshold to enable the OTG mode, does produce INT 1h = VBAT falling below the threshold to enable the OTG mode, does NOT produce INT
3	TS_COLD_MASK	R/W	0h	Reset by: WATCHDOG REG_RST	TS cold temperature interrupt mask Type : RW POR: 0b 0h = TS across cold temperature (T1) does produce INT 1h = TS across cold temperature (T1) does NOT produce INT
2	TS_COOL_MASK	R/W	0h	Reset by: WATCHDOG REG_RST	TS cool temperature interrupt mask Type : RW POR: 0b 0h = TS across cool temperature (T2) does produce INT 1h = TS across cool temperature (T2) does NOT produce INT
1	TS_WARM_MASK	R/W	0h	Reset by: WATCHDOG REG_RST	TS warm temperature interrupt mask Type : RW POR: 0b 0h = TS across warm temperature (T3) does produce INT 1h = TS across warm temperature (T3) does NOT produce INT
0	TS_HOT_MASK	R/W	0h	Reset by: WATCHDOG REG_RST	TS hot temperature interrupt mask Type : RW POR: 0b 0h = TS across hot temperature (T5) does produce INT 1h = TS across hot temperature (T5) does NOT produce INT

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7.5.1.40 REG2C_FAULT_Mask_0 Register (Offset = 2Ch) [reset = 0h]

REG2C_FAULT_Mask_0 is shown in Figure 7-64 and described in Table 7-53.

Return to the Table 7-12.

FAULT Mask 0

Figure 7-64. REG2C_FAULT_Mask_0 Register

7	6	5	4	3	2	1	0
IBAT_REG_MASK	VBUS_OVP_MASK	VBAT_OVP_MASK	IBUS_OCP_MASK	IBAT_OCP_MASK	CONV_OCP_MASK	VAC2_OVP_MASK	VAC1_OVP_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-53. REG2C_FAULT_Mask_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	IBAT_REG_MASK	R/W	0h	Reset by: REG_RST	IBAT regulation mask flag Type : RW POR: 0b 0h = enter or exit IBAT regulation does produce INT 1h = enter or exit IBAT regulation does NOT produce INT
6	VBUS_OVP_MASK	R/W	0h	Reset by: REG_RST	VBUS over-voltage mask flag Type : RW POR: 0b 0h = entering VBUS OVP does produce INT 1h = entering VBUS OVP does NOT produce INT
5	VBAT_OVP_MASK	R/W	0h	Reset by: REG_RST	VBAT over-voltage mask flag Type : RW POR: 0b 0h = entering VBAT OVP does produce INT 1h = entering VBAT OVP does NOT produce INT
4	IBUS_OCP_MASK	R/W	0h	Reset by: REG_RST	IBUS over-current mask flag Type : RW POR: 0b 0h = IBUS OCP fault does produce INT 1h = IBUS OCP fault does NOT produce INT
3	IBAT_OCP_MASK	R/W	0h	Reset by: REG_RST	IBAT over-current mask flag Type : RW POR: 0b 0h = IBAT OCP fault does produce INT 1h = IBAT OCP fault does NOT produce INT
2	CONV_OCP_MASK	R/W	0h	Reset by: REG_RST	Converter over-current mask flag Type : RW POR: 0b 0h = Converter OCP fault does produce INT 1h = Converter OCP fault does NOT produce INT
1	VAC2_OVP_MASK	R/W	0h	Reset by: REG_RST	VAC2 over-voltage mask flag Type : RW POR: 0b 0h = entering VAC2 OVP does produce INT 1h = entering VAC2 OVP does NOT produce INT
0	VAC1_OVP_MASK	R/W	0h	Reset by: REG_RST	VAC1 over-voltage mask flag Type : RW POR: 0b 0h = entering VAC1 OVP does produce INT 1h = entering VAC1 OVP does NOT produce INT

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7.5.1.41 REG2D_FAULT_Mask_1 Register (Offset = 2Dh) [reset = 0h]

REG2D_FAULT_Mask_1 is shown in Figure 7-65 and described in Table 7-54.

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FAULT Mask 1

Figure 7-65. REG2D_FAULT_Mask_1 Register

7	6	5	4	3	2	1	0
VSYS_SHORT_MASK	VSYS_OVP_MASK	OTG_OVP_MASK	OTG_UVP_MASK	RESERVED	TSHUT_MASK	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	

Table 7-54. REG2D_FAULT_Mask_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	VSYS_SHORT_MASK	R/W	0h	Reset by: REG_RST	VSYS short circuit mask flag Type : RW POR: 0b 0h = System short fault does produce INT 1h = System short fault does NOT produce INT
6	VSYS_OVP_MASK	R/W	0h	Reset by: REG_RST	VSYS over-voltage mask flag Type : RW POR: 0b 0h = System over-voltage fault does produce INT 1h = System over-voltage fault does NOT produce INT
5	OTG_OVP_MASK	R/W	0h	Reset by: REG_RST	OTG over-voltage mask flag Type : RW POR: 0b 0h = OTG VBUS over-voltage fault does produce INT 1h = OTG VBUS over-voltage fault does NOT produce INT
4	OTG_UVP_MASK	R/W	0h	Reset by: REG_RST	OTG under-voltage mask flag Type : RW POR: 0b 0h = OTG VBUS under voltage fault does produce INT 1h = OTG VBUS under voltage fault does NOT produce INT
3	RESERVED	R/W	0h		RESERVED
2	TSHUT_MASK	R/W	0h	Reset by: REG_RST	IC thermal shutdown mask flag Type : RW POR: 0b 0h = TSHUT does produce INT 1h = TSHUT does NOT produce INT
1-0	RESERVED	R	0h		RESERVED

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7.5.1.42 REG2E_ADC_Control Register (Offset = 2Eh) [reset = 30h]

REG2E_ADC_Control is shown in Figure 7-66 and described in Table 7-55.

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ADC Control

Figure 7-66. REG2E_ADC_Control Register

7	6	5	4	3	2	1	0
ADC_EN	ADC_RATE	ADC_SAMPLE_1:0		ADC_AVG	ADC_AVG_INIT	RESERVED	
R/W-0h	R/W-0h	R/W-3h		R/W-0h	R/W-0h	R/W-0h	

Table 7-55. REG2E_ADC_Control Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	ADC_EN	R/W	0h	Reset by: WATCHDOG REG_RST	ADC Control Type : RW POR: 0b 0h = Disable 1h = Enable
6	ADC_RATE	R/W	0h	Reset by: REG_RST	ADC conversion rate control Type : RW POR: 0b 0h = Continuous conversion 1h = One shot conversion
5-4	ADC_SAMPLE_1:0	R/W	3h	Reset by: REG_RST	ADC sample speed Type : RW POR: 11b 0h = 15 bit effective resolution 1h = 14 bit effective resolution 2h = 13 bit effective resolution 3h = 12 bit effective resolution
3	ADC_AVG	R/W	0h	Reset by: REG_RST	ADC average control Type : RW POR: 0b 0h = Single value 1h = Running average
2	ADC_AVG_INIT	R/W	0h	Reset by: REG_RST	ADC average initial value control Type : RW POR: 0b 0h = Start average using the existing register value 1h = Start average using a new ADC conversion
1-0	RESERVED	R/W	0h		RESERVED

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7.5.1.43 REG2F_ADC_Function_Disable_0 Register (Offset = 2Fh) [reset = 0h]

REG2F_ADC_Function_Disable_0 is shown in Figure 7-67 and described in Table 7-56.

Return to the Table 7-12.

ADC Function Disable 0

Figure 7-67. REG2F_ADC_Function_Disable_0 Register

7	6	5	4	3	2	1	0
IBUS_ADC_DIS	IBAT_ADC_DIS	VBUS_ADC_DIS	VBAT_ADC_DIS	VSYS_ADC_DIS	TS_ADC_DIS	TDIE_ADC_DIS	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

Table 7-56. REG2F_ADC_Function_Disable_0 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	IBUS_ADC_DIS	R/W	0h	Reset by: REG_RST	IBUS ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
6	IBAT_ADC_DIS	R/W	0h	Reset by: REG_RST	IBAT ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
5	VBUS_ADC_DIS	R/W	0h	Reset by: REG_RST	VBUS ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
4	VBAT_ADC_DIS	R/W	0h	Reset by: REG_RST	VBAT ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
3	VSYS_ADC_DIS	R/W	0h	Reset by: REG_RST	VSYS ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
2	TS_ADC_DIS	R/W	0h	Reset by: REG_RST	TS ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
1	TDIE_ADC_DIS	R/W	0h	Reset by: REG_RST	TDIE ADC control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
0	RESERVED	R	0h		RESERVED

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7.5.1.44 REG30_ADC_Function_Disable_1 Register (Offset = 30h) [reset = 0h]

REG30_ADC_Function_Disable_1 is shown in Figure 7-68 and described in Table 7-57.

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ADC Function Disable 1

Figure 7-68. REG30_ADC_Function_Disable_1 Register

7	6	5	4	3	2	1	0
DP_ADC_DIS	DM_ADC_DIS	VAC2_ADC_DIS	VAC1_ADC_DIS	RESERVED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			

Table 7-57. REG30_ADC_Function_Disable_1 Register Field Descriptions

Bit	Field	Type	Reset	Notes	Description
7	DP_ADC_DIS	R/W	0h	Reset by: REG_RST	D+ ADC Control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
6	DM_ADC_DIS	R/W	0h	Reset by: REG_RST	D- ADC Control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
5	VAC2_ADC_DIS	R/W	0h	Reset by: REG_RST	VAC2 ADC Control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
4	VAC1_ADC_DIS	R/W	0h	Reset by: REG_RST	VAC1 ADC Control Type : RW POR: 0b 0h = Enable (Default) 1h = Disable
3-0	RESERVED	R	0h		RESERVED

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7.5.1.45 REG31_IBUS_ADC Register (Offset = 31h) [reset = 0h]

REG31_IBUS_ADC is shown in Figure 7-69 and described in Table 7-58.

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IBUS ADC

Figure 7-69. REG31_IBUS_ADC Register

15	14	13	12	11	10	9	8
IBUS_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
IBUS_ADC_15:0							
R-0h							

Table 7-58. REG31_IBUS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	IBUS_ADC_15:0	R	0h	IBUS ADC reading Reported in 2 's Complement. When the current is flowing from VBUS to PMID, IBUS ADC reports positive value, and when the current is flowing from PMID to VBUS, IBUS ADC reports negative value. Type : R POR: 0mA (0h) Range : 0mA-5000mA Fixed Offset : 0mA Bit Step Size : 1mA

ADVANCE INFORMATION

7.5.1.46 REG33_IBAT_ADC Register (Offset = 33h) [reset = 0h]

REG33_IBAT_ADC is shown in Figure 7-70 and described in Table 7-59.

Return to the Table 7-12.

IBAT ADC

Figure 7-70. REG33_IBAT_ADC Register

15	14	13	12	11	10	9	8
IBAT_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
IBAT_ADC_15:0							
R-0h							

Table 7-59. REG33_IBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	IBAT_ADC_15:0	R	0h	IBAT ADC reading Reported in 2 's Complement. The IBAT ADC reports positive value for the battery charging current, and negative value for the battery discharging current. Type : R POR: 0mA (0h) Range : 0mA-8000mA Fixed Offset : 0mA Bit Step Size : 1mA

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7.5.1.47 REG35_VBUS_ADC Register (Offset = 35h) [reset = 0h]

REG35_VBUS_ADC is shown in Figure 7-71 and described in Table 7-60.

Return to the Table 7-12.

VBUS ADC

Figure 7-71. REG35_VBUS_ADC Register

15	14	13	12	11	10	9	8
VBUS_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
VBUS_ADC_15:0							
R-0h							

Table 7-60. REG35_VBUS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VBUS_ADC_15:0	R	0h	VBUS ADC reading Reported in 2 's Complement. Type : R POR: 0mV (0h) Range : 0mV-30000mV Fixed Offset : 0mV Bit Step Size : 1mV

7.5.1.48 REG37_VAC1_ADC Register (Offset = 37h) [reset = 0h]

REG37_VAC1_ADC is shown in Figure 7-72 and described in Table 7-61.

Return to the Table 7-12.

VAC1 ADC

Figure 7-72. REG37_VAC1_ADC Register

15	14	13	12	11	10	9	8
VAC1_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
VAC1_ADC_15:0							
R-0h							

Table 7-61. REG37_VAC1_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VAC1_ADC_15:0	R	0h	VAC1 ADC reading Reported in 2 's Complement. Type : R POR: 0mV (0h) Range : 0mV-30000mV Fixed Offset : 0mV Bit Step Size : 1mV

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7.5.1.49 REG39_VAC2_ADC Register (Offset = 39h) [reset = 0h]

REG39_VAC2_ADC is shown in Figure 7-73 and described in Table 7-62.

Return to the Table 7-12.

VAC2 ADC

Figure 7-73. REG39_VAC2_ADC Register

15	14	13	12	11	10	9	8
VAC2_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
VAC2_ADC_15:0							
R-0h							

Table 7-62. REG39_VAC2_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VAC2_ADC_15:0	R	0h	VAC2 ADC reading Reported in 2 's Complement. Type : R POR: 0mV (0h) Range : 0mV-30000mV Fixed Offset : 0mV Bit Step Size : 1mV

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7.5.1.50 REG3B_VBAT_ADC Register (Offset = 3Bh) [reset = 0h]

REG3B_VBAT_ADC is shown in Figure 7-74 and described in Table 7-63.

Return to the Table 7-12.

VBAT ADC

Figure 7-74. REG3B_VBAT_ADC Register

15	14	13	12	11	10	9	8
VBAT_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
VBAT_ADC_15:0							
R-0h							

Table 7-63. REG3B_VBAT_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VBAT_ADC_15:0	R	0h	The battery remote sensing voltage (VBATP) ADC reading Reported in 2 's Complement. Type : R POR: 0mV (0h) Range : 0mV-20000mV Fixed Offset : 0mV Bit Step Size : 1mV

ADVANCE INFORMATION

7.5.1.51 REG3D_VSYS_ADC Register (Offset = 3Dh) [reset = 0h]

REG3D_VSYS_ADC is shown in Figure 7-75 and described in Table 7-64.

Return to the Table 7-12.

VSYS ADC

Figure 7-75. REG3D_VSYS_ADC Register

15	14	13	12	11	10	9	8
VSYS_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
VSYS_ADC_15:0							
R-0h							

Table 7-64. REG3D_VSYS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VSYS_ADC_15:0	R	0h	VSYS ADC reading Reported in 2 's Complement. Type : R POR: 0mV (0h) Range : 0mV-24000mV Fixed Offset : 0mV Bit Step Size : 1mV

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7.5.1.52 REG3F_TS_ADC Register (Offset = 3Fh) [reset = 0h]

REG3F_TS_ADC is shown in Figure 7-76 and described in Table 7-65.

Return to the Table 7-12.

TS ADC

Figure 7-76. REG3F_TS_ADC Register

15	14	13	12	11	10	9	8
TS_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
TS_ADC_15:0							
R-0h							

Table 7-65. REG3F_TS_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TS_ADC_15:0	R	0h	TS ADC reading Type : R POR: 0% (0h) Range : 0%-99.9023% Fixed Offset : 0% Bit Step Size : 0.0976563%

7.5.1.53 REG41_TDIE_ADC Register (Offset = 41h) [reset = 0h]

REG41_TDIE_ADC is shown in Figure 7-77 and described in Table 7-66.

Return to the Table 7-12.

TDIE_ADC

Figure 7-77. REG41_TDIE_ADC Register

15	14	13	12	11	10	9	8
TDIE_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
TDIE_ADC_15:0							
R-0h							

Table 7-66. REG41_TDIE_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TDIE_ADC_15:0	R	0h	TDIE ADC reading Reported in 2 's Complement. Type : R POR: 0°C (0h) Range : -40°C-150°C Fixed Offset : 0°C Bit Step Size : 0.5°C

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7.5.1.54 REG43_D+_ADC Register (Offset = 43h) [reset = 0h]

REG43_D+_ADC is shown in Figure 7-78 and described in Table 7-67.

Return to the Table 7-12.

D+ ADC

Figure 7-78. REG43_D+_ADC Register

15	14	13	12	11	10	9	8
D+_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
D+_ADC_15:0							
R-0h							

Table 7-67. REG43_D+_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	D+_ADC_15:0	R	0h	D+ ADC reading Type : R POR: 0mV (0h) Range : 0mV-3600mV Fixed Offset : 0mV Bit Step Size : 1mV

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7.5.1.55 REG45_D-_ADC Register (Offset = 45h) [reset = 0h]

REG45_D-_ADC is shown in Figure 7-79 and described in Table 7-68.

Return to the Table 7-12.

D- ADC

Figure 7-79. REG45_D-_ADC Register

15	14	13	12	11	10	9	8
D-_ADC_15:0							
R-0h							
7	6	5	4	3	2	1	0
D-_ADC_15:0							
R-0h							

Table 7-68. REG45_D-_ADC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	D-_ADC_15:0	R	0h	D- ADC reading Type : R POR: 0mV (0h) Range : 0mV-3600mV Fixed Offset : 0mV Bit Step Size : 1mV

7.5.1.56 REG47_DPDM_Driver Register (Offset = 47h) [reset = 0h]

REG47_DPDM_Driver is shown in Figure 7-80 and described in Table 7-69.

Return to the Table 7-12.

DPDM Driver

Figure 7-80. REG47_DPDM_Driver Register

7	6	5	4	3	2	1	0
DPLUS_DAC_2:0			DMINUS_DAC_2:0			RESERVED	
R/W-0h			R/W-0h			R/W-0h	

Table 7-69. REG47_DPDM_Driver Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	DPLUS_DAC_2:0	R/W	0h	D+ Output Driver Type : RW POR: 000b 0h = HIZ 1h = 0 2h = 0.6V 3h = 1.2V 4h = 2.0V 5h = 2.7V 6h = 3.3V 7h = D+/D- Short
4-2	DMINUS_DAC_2:0	R/W	0h	D- Output Driver Type : RW POR: 000b 0h = HIZ 1h = 0 2h = 0.6V 3h = 1.2V 4h = 2.0V 5h = 2.7V 6h = 3.3V 7h = reserved
1-0	RESERVED	R/W	0h	RESERVED

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7.5.1.57 REG48_Part_Information Register (Offset = 48h) [reset = 0h]

REG48_Part_Information is shown in Figure 7-81 and described in Table 7-70.

Return to the Table 7-12.

Part Information

Figure 7-81. REG48_Part_Information Register

7	6	5	4	3	2	1	0
RESERVED		PN_2:0			DEV_REV_2:0		
R-0h		R-0h			R-0h		

Table 7-70. REG48_Part_Information Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-3	PN_2:0	R	1h	Device Part number 000 = BQ25792 001 = BQ25798 All other options are reserved.
2-0	DEV_REV_2:0	R	3h	Device Revision 001 = BQ25792 010 = BQ25796 011 = BQ25798 100 = BQ25672 All other options are reserved.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A typical application consists of the device configured as an I^2C controlled power path management device and a multi-cell battery charger for Li-Ion and Li-polymer batteries. It integrates the four switching MOSFETs (Q_1 to Q_4) for the buck-boost converter, and the battery FET (BATFET) between system and battery. The device also integrates the input current sensing and charging current sensing circuitries, the bootstrap diode for the high-side gate driving and the dual-input power mux for the power sources selection.

The charger's MPPT algorithm allows a simple but efficient interface between the charger and a small photovoltaic panel. The power mux may optionally be used to add a secondary charging port such as a barrel jack or USB input.

8.2 Typical Application

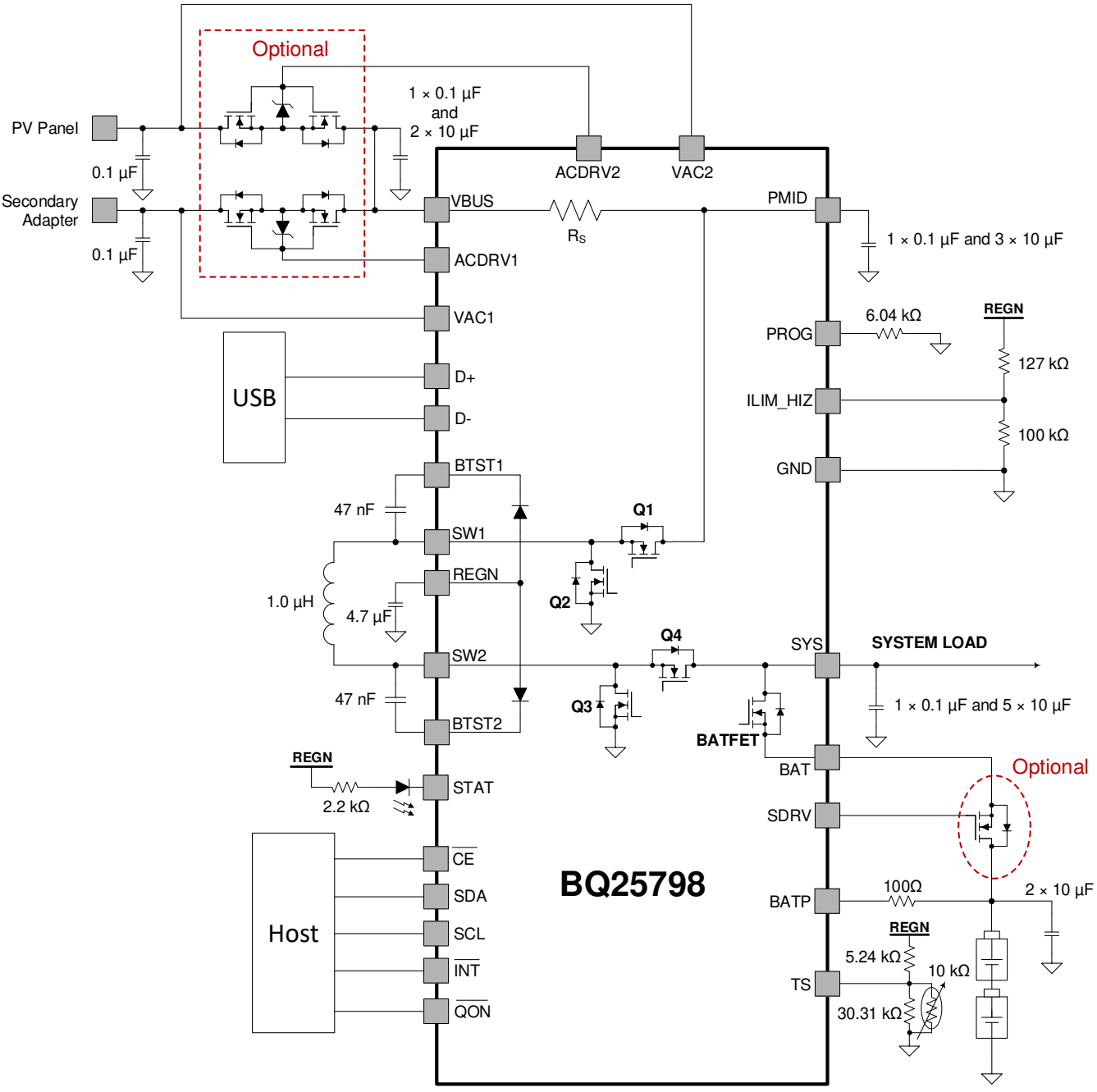

Figure 8-1. BQ25798 Application Diagram with Two Input Sources and Ship FET

ADVANCE INFORMATION

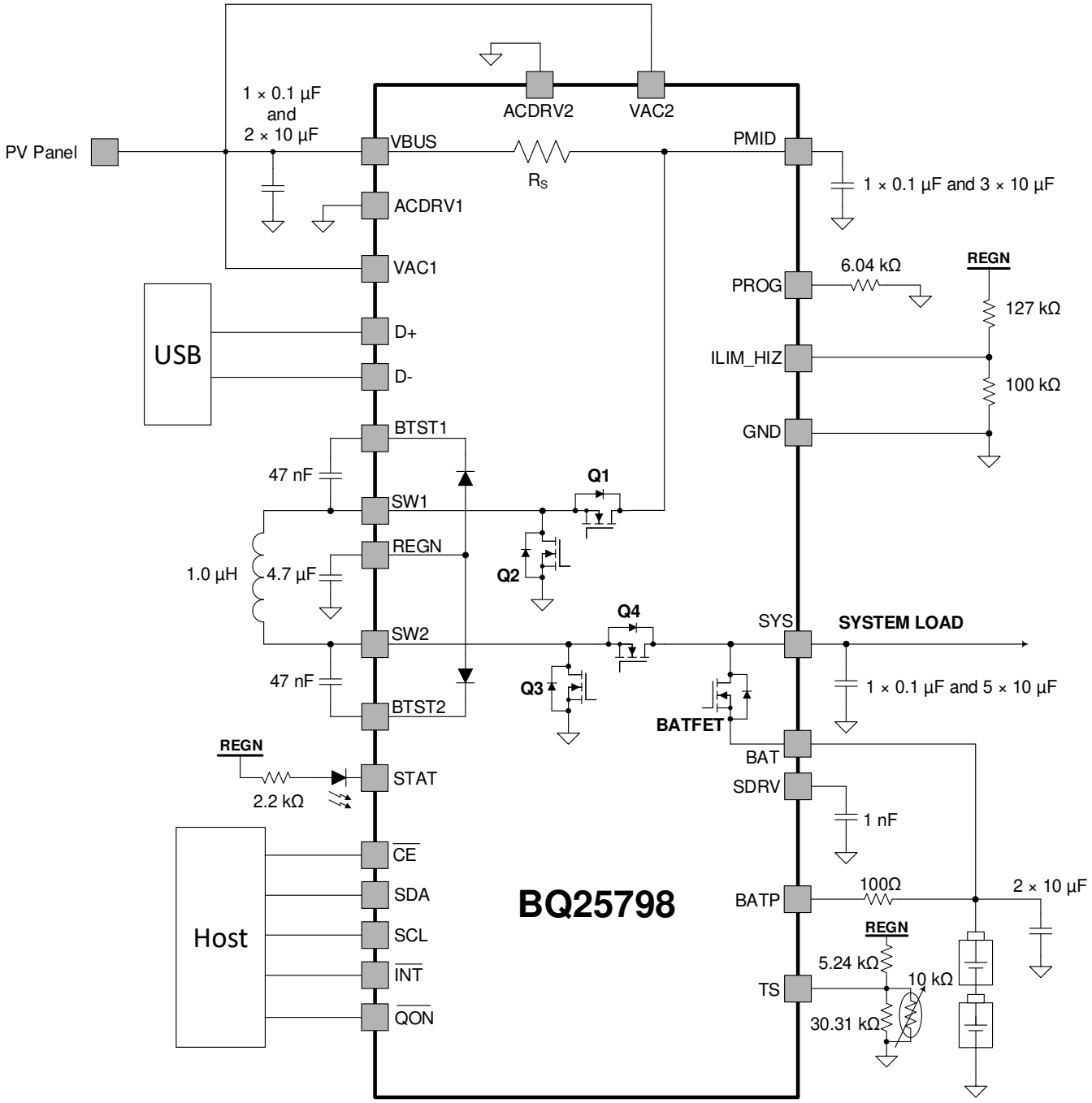

Figure 8-2. BQ25798 Application Diagram with Single Input Source and No Ship FET

8.2.1 Design Requirements

For this design example, use the parameters shown in the table below.

Table 8-1. Design Parameters

PARAMETER	VALUE
PV panel voltage	V_{OC} = 21.5, V_{MPP} = 17.5
Secondary adapter voltage range	5 V to 20 V
Input current limit (IINDPM[8:0])	3.0 A
Fast charge current limit (ICHG[8:0])	3.0 A
Battery regulation voltage (VREG[10:0])	8.4 V

8.2.2 Detailed Design Procedure

8.2.2.1 PV Panel Selection

BQ25798 has a 3.6 to 24V wide input voltage range, allowing it to interface with 6V, 9V and 12V photovoltaic panels. Two critical parameters of the PV panel are the open circuit voltage, V_{OC}, and the maximum power point voltage, V_{MPP}. The open-circuit voltage should not exceed the 24V recommended operating condition of VIN1 or VIN2. BQ25798 has a small-PV maximum power point tracking algorithm (see Section 7.3.6.3) to simplify the interface to the solar panel while maintaining high effiiency.

The ratio of maximum power point voltage to open circuit voltage can change over differing conditions such as temperature and irradiance, but the ratio of V_{MPP} / V_{OC} as provided in the PV panel manufacturer's datasheet provides a good estimate to use when configuraing VOC_PCT. For a panel with V_{OC} = 21.5 and V_{MPP} = 17.5, the calculated maximum power point ratio is 17.5 / 21.5 = 81.4%. A setting of VOC_PCT = 4 (81.25%) is a good starting configuration for this panel. Users may wish to characterize their PV panel's operation over their specific application conditions of temperature, irradiance, humidity and other parameters in order to adjust this setting if necessary.

8.2.2.2 Inductor Selection

The device has 1.5 MHz switching frequency to allow the use of small inductor (1μH) and capacitor values. It also provide the 750kHz switching frequency to achieve higher efficiency for the applications which have enough design space to accommodate the larger inductor (2.2 μH) and capacitors. Please note that the 1.5 MHz switching frequency only works with the 1μH inductor and the 750 kHz switching frequency only works with the 2.2μH inductor.

Because the converter might be either operated in the buck mode or the boost mode, so the inductor current is equal to either the charging current or the input current. The inductor saturation current should be higher than the larger value of the input current (I_{IN}) or the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq MAX\left[\left(I_{IN} + \frac{I_{RIPPLE}}{2}\right), \left(I_{CHG} + \frac{I_{RIPPLE}}{2}\right)\right] \quad (4)$$

The inductor ripple current (I_{RIPPLE}) depends on the input voltage (V_{BUS}), the output voltage (V_{SYS}), the switching frequency (F_{SW}) and the inductance (L). The inductor current ripples for buck mode and boost mode are calculated with equations (4) and (5), respectively:

$$I_{RIPPLE\_BUCK} = \frac{V_{SYS} \times (V_{BUS} - V_{SYS})}{V_{BUS} \times F_{SW} \times L} \quad (5)$$

$$I_{RIPPLE\_BOOST} = \frac{V_{BUS} \times (V_{SYS} - V_{BUS})}{V_{SYS} \times F_{SW} \times L} \quad (6)$$

The inductor current ripple in the buck mode is usually larger than that in the boost mode, since the voltage-second applied on the inductor is larger. The maximum inductor current ripple in the buck mode happens in the

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vicinity of D = V_{SYS} / V_{BUS} = 0.5. The SYS voltage is approximately 8V for the 2s battery configuration, so the worst case for the inductor ripples is with the 15V or 20V input voltage.

8.2.2.3 Input (VBUS / PMID) Capacitor

In the buck mode operation, the input current is discontinuous, which dominates the input RMS ripple current and input voltage ripple. The input capacitors should have enough ripple current rating to absorb the input AC current and have large enough capacitance to maintain the small input voltage ripple. For the buck mode operation, the input RMS ripple current is calculated by the equation (6) and the input voltage ripple is calculated by the equation (7), where D = V_{SYS} / V_{BUS}.

$$I_{CIN\_BUCK} = I_{CHG} \times \sqrt{D \times (1 - D)} \tag{7}$$

$$\Delta V_{IN\_BUCK} = \frac{D \times (1 - D) \times I_{CHG}}{C_{IN} \times F_{SW}} \tag{8}$$

The worst case input RMS ripple current and input voltage ripple both occur at 0.5 duty cycle condition. The SYS voltage is approximately 8V for the 2s battery configuration, so the worst case is when 15V to 20V VBUS condition. Low ESR ceramic capacitor such as X7R or X5R is preferred for the input decoupling capacitor and should be placed close to the PMID and GND pins of the IC. The voltage rating of the capacitor must be higher than the normal input voltage level. The capacitor with 25V or higher voltage rating is preferred for up to 20V input voltage. 1*0.1 µF + 3*10 µF ceramic capacitors are suggested for up to 3.3-A input current limit to support the converter in forward mode.

8.2.2.4 Output (VSYS) Capacitor

In the boost mode operation, the output current is discontinuous, which dominates the output RMS ripple current and output voltage ripple. The output capacitors should have enough ripple current rating to absorb the output AC current and have large enough capacitance to maintain the small output voltage ripple. For the boost mode operation, the output RMS ripple current is calculated by the equation (8) and the output voltage ripple is calculated by the equation (9), where D = (1 - V_{BUS} / V_{SYS}).

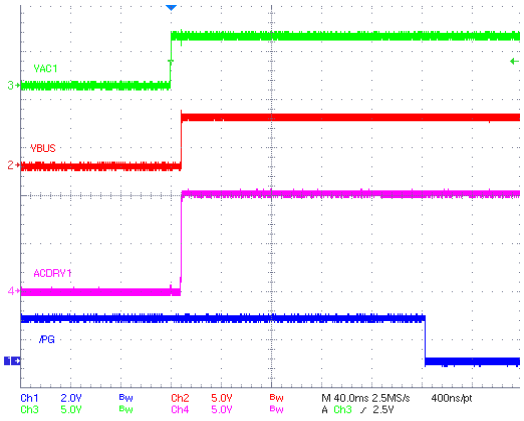
$$I_{COUT\_BOOST} = I_{CHG} \times \sqrt{\frac{D}{(1 - D)}} \tag{9}$$

$$\Delta V_{OUT\_BOOST} = \frac{I_{CHG} \times D}{C_{OUT} \times F_{SW}} \tag{10}$$

The worst case output RMS ripple current and output voltage ripple both occur at the lowest VBUS input voltage. The SYS voltage is approximately 8V for the 2s battery configuration, so the worst case is 5V VBUS condition. Low ESR ceramic capacitor such as X7R or X5R is preferred for the output decoupling capacitor and should be placed close to the SYS and GND pins of the IC. The voltage rating of the capacitor must be higher than the normal input voltage level. The capacitor with 16V or higher voltage rating is preferred for the 2s battery configuration. 1*0.1 µF + 5*10 µF capacitors are suggested for up to 5A charging current.

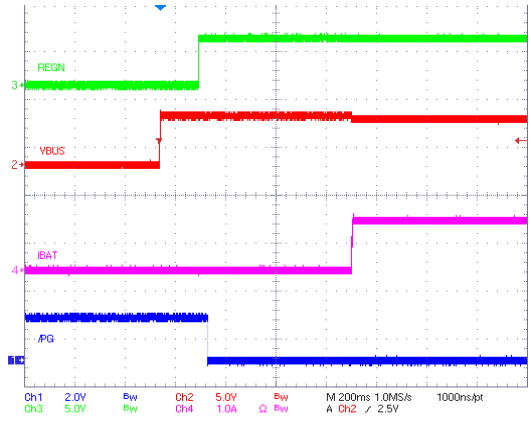
8.2.3 Application Curves

C_{VBUS} = 2*10µF, C_{PMID}= 3*10µF, C_{SYS} = 5*10µF, C_{BAT} = 2*10µF, L1 = 1µH (SPM6530T-1R0M120), Fsw = 1.5MHz.



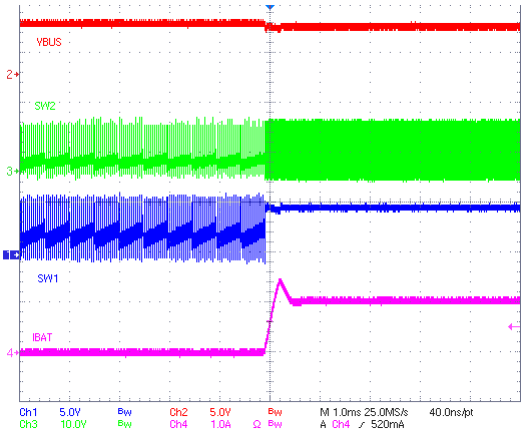
VAC1 = VBUS = 5V VBAT = 8V

Figure 8-3. ACFET1-RBFET1 Turns on at Power Up



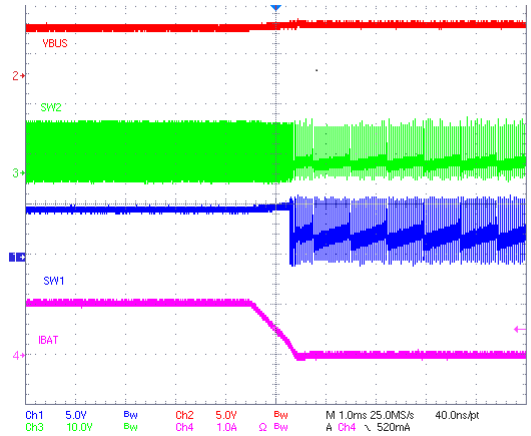
VAC1 = VBUS = 5V VBAT = 8V

Figure 8-4. Power Up from VAC1 with Charge Enabled



VBUS = 5V VBAT = 8V ICHG = 1A

Figure 8-5. Charge Enable



VBUS = 5V VBAT = 8V ICHG = 1A

Figure 8-6. Charge Disable

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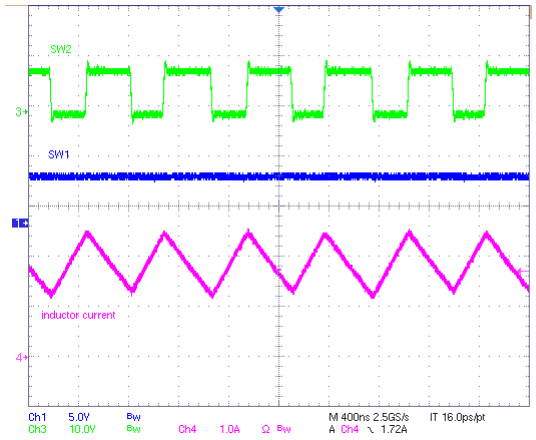
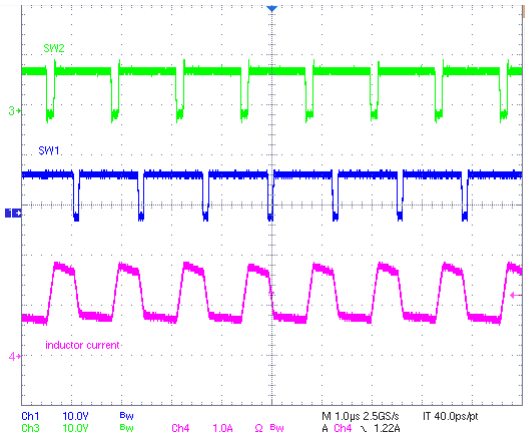


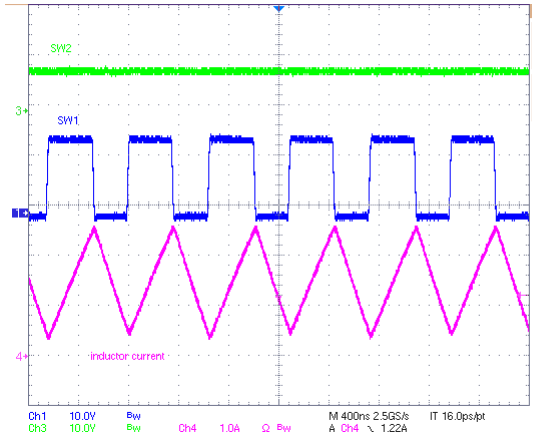
VBUS = 5V VBAT = 8V ICHG = 1A

Figure 8-7. Boost Charging Mode PWM Operation



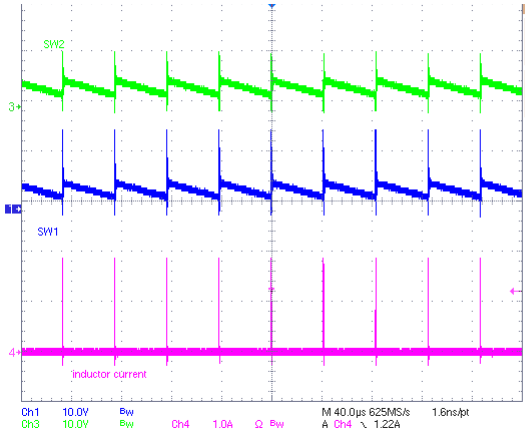
VBUS = 8V VBAT = 8V ICHG = 1A

Figure 8-8. Buck-Boost Charging Mode PWM Operation



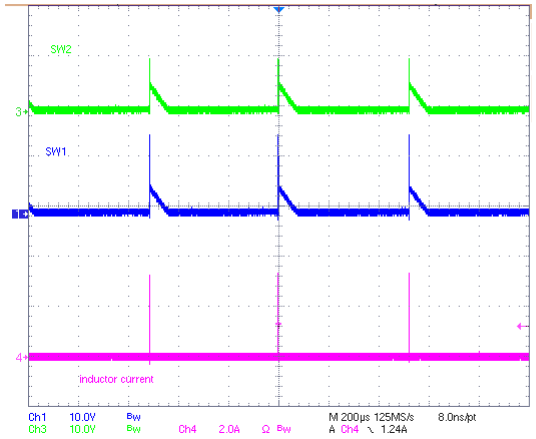
VBUS = 15V VBAT = 8V ICHG = 1.5A

Figure 8-9. Buck Charging Mode PWM Operation



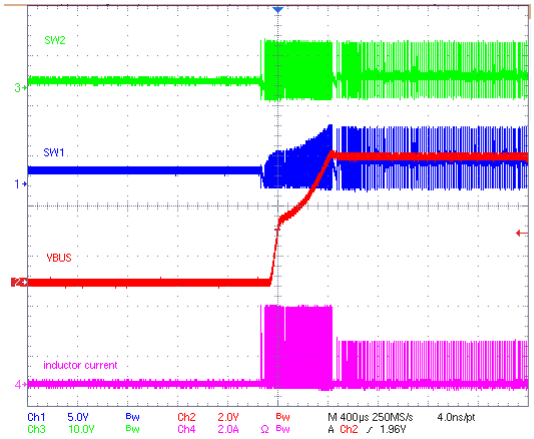
VBUS = 15V VBAT = 8V ICHG = 0A

Figure 8-10. Buck Mode PFM with OOA



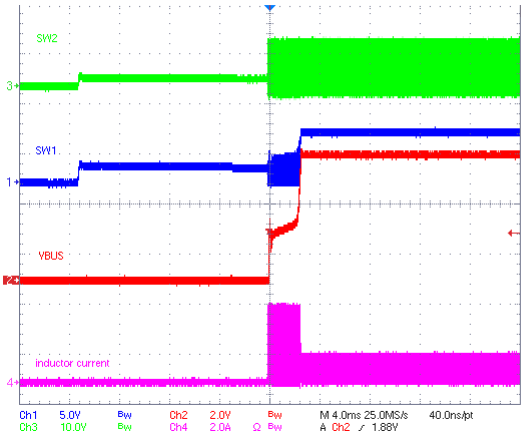
VBUS = 15V VBAT = 8V ICHG = 0A

Figure 8-11. Buck Mode PFM without OOA



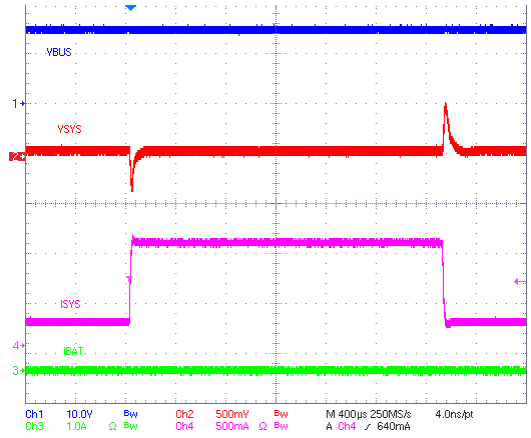
VBAT = 8V VOTG = 5V IBUS = 0A

Figure 8-12. OTG Startup at No Load



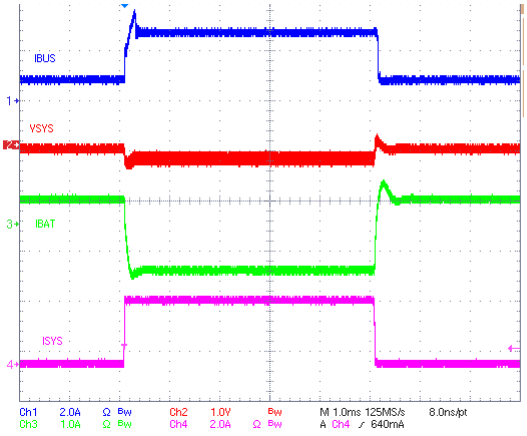
VBAT = 8V VOTG = 5V IBUS = 500mA

Figure 8-13. OTG Startup at 500-mA Load



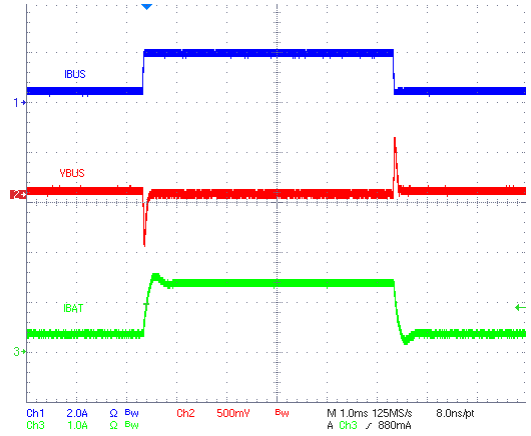
VBUS = 15V VBAT = 8V Charge disabled

Figure 8-14. VSYS Load Transient Response



VBUS = 5V VBAT = 8V Charge enabled

Figure 8-15. IINDPM Transient Response



VBAT = 8V VOTG = 5V

Figure 8-16. VOTG Load Transient Response

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9 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.6 V and 24 V input with recommended >500mA current rating connected to VBUS or a 1s to 4s Li-Ion battery with voltage higher than V_{BAT_UVLO} connected to BAT. The source current rating needs to be at least 3A for the buck-boost converter of the charger to provide maximum output power to SYS.

The charger does not support the testing condition when the battery connection is floating. The BAT pin has to be connected to a real battery or some devices which can emulate the battery, like the battery emulator or bulk capacitors. When the BAT pin is floating, please disable charge by setting EN_CHG to 0 or pulling low the $\overline{CE}$ pin. Otherwise, the voltage overshoot at SYS might trigger the SYSOVP protection periodically.

10 Layout

10.1 Layout Guidelines

The switching nodes rising and falling times should be minimized for minimum switching loss. Proper layout of the components to minimize the high frequency current path loops (shown in the figure below) is important to prevent the electrical and magnetic field radiation and the high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place the SYS output capacitors as close to SYS and GND as possible. Place a 0.1 µF small size (such as 0402 or 0201) capacitor closer than the other 10 µF capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
2. Place the PMID input capacitors as close to PMID and GND as possible. Place a 0.1 µF small size (such as 0402 or 0201) capacitor closer than the other 10 µF capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
3. Place the VBUS input capacitors as close to VBUS and GND as possible. Place a 0.1 µF small size (such as 0402 or 0201) capacitor closer than the other 10 µF capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. The connection from SYS/PMID/VBUS to the 0.1 µF has to be routed on the top layer of the PCB, the returning back to GND also has to be in the top layer. Keep the whole routing loop as small as possible.
5. Place the inductor input terminal to SW1 and the inductor output terminal to SW2 as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the inductor current. Minimize parasitic capacitance from this area to any other trace or plane.
6. Place the BAT capacitors close to BAT and GND, place the VBUS capacitors close to VBUS and GND.
7. The REGN decoupling capacitor and the bootstrap capacitors should be placed next to the IC and make trace connection as short as possible.
8. Ensure that there are sufficient thermal vias directly under the power MOSFETs, connecting to copper on other layers.
9. Via size and number should be enough for a given current path.
10. Route BATP away from switching nodes such as SW1 and SW2.

Refer to the EVM design and more information in the *BQ25792EVM, BQ25795EVM, BQ25796EVM and BQ25798EVM (BMS034) Evaluation Module* for the recommended component placement with trace and via locations.

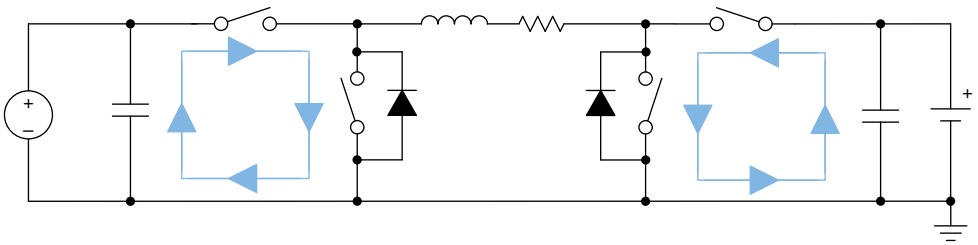

Figure 10-1. Converter High Frequency Current Path

ADVANCE INFORMATION

10.2 Layout Example

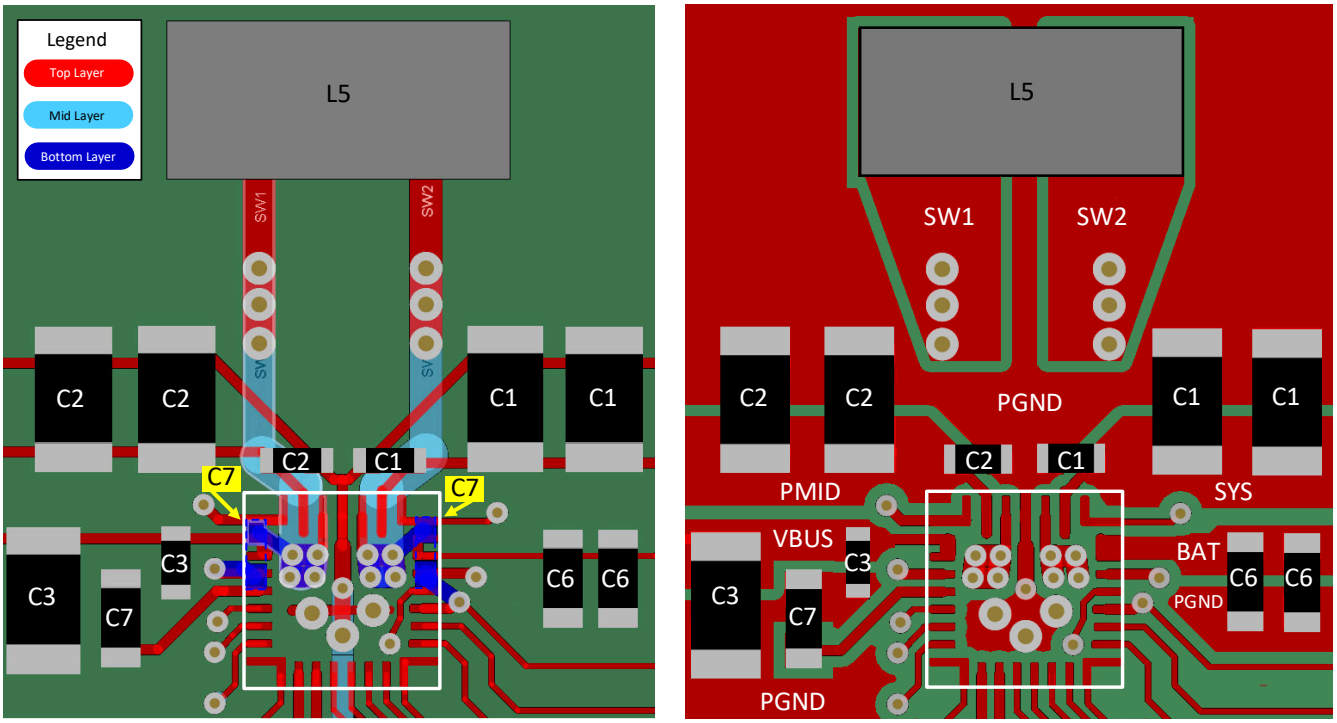

Figure 10-2. PCB Layout Example (Top Layer Copper Pours Removed on Left, Shown on Right)

Figure 10-2 shows the recommended placement and routing of external components. The components are labelled with "R," "C" or "L" to indicate resistor, capacitor or inductor and a number that corresponds to the numbered list in Section 10.1. Since the layout guidelines are listed in priority order, this number also provides a priority for component placement.

The placement of C1 and C2 0.1 µF PMID and SYS capacitors is critical for noise filtering. They should be placed on the same layer as the BQ25798, as close to the IC as possible. This will generally require that the traces to connect SW1 and SW2 to the inductor are routed on a different layer.

The SW1 and SW2 pins are routed to vias placed under the IC and then back out on an inner PCB layer. This supports the tightest placement of C1 and C2 capctiors as described above. These vias are also used to route to the C7 BTST1 and BTST2 capactiors on the bottom layer as shown.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *BQ25792EVM, BQ25795EVM, BQ25796EVM and BQ25798EVM (BMS034) Evaluation Module*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
BQ25798RQMR	N/A	VQFN-HR	RQM	29	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25798
BQ25798RQMT	N/A	VQFN-HR	RQM	29	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25798

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

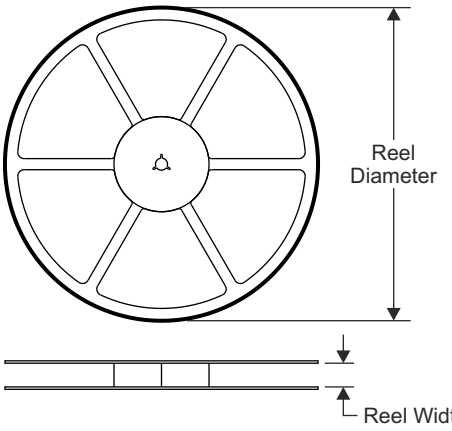
(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

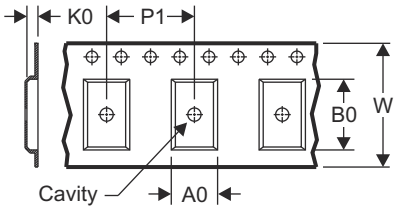
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

12.1.2 Tape and Reel Information

REEL DIMENSIONS

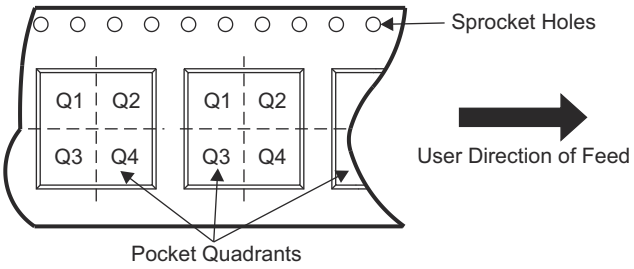


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

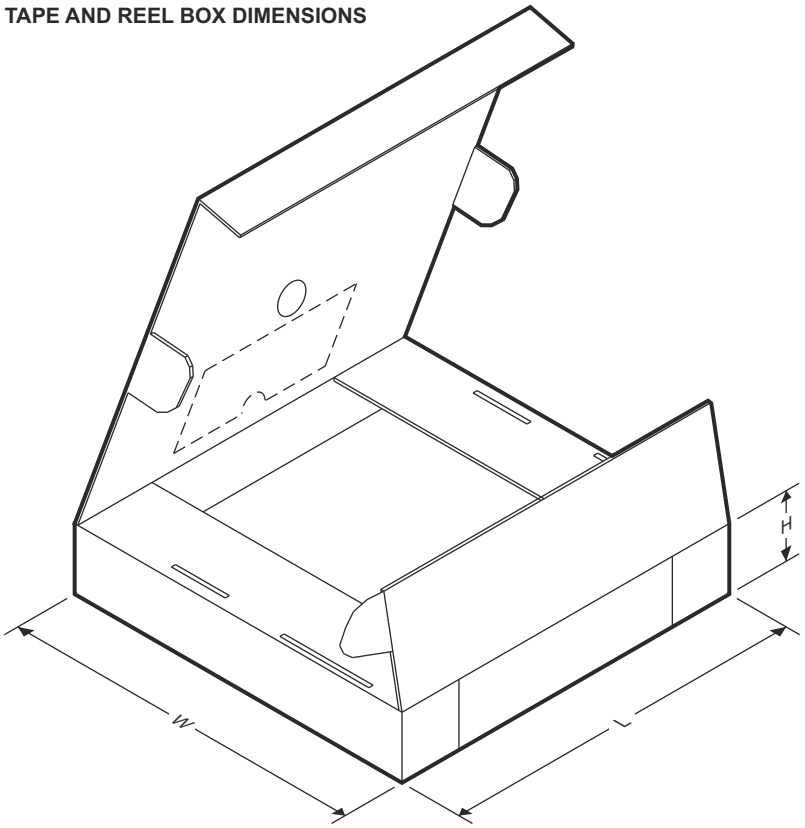


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25798RQMR	VQFN-HR	RQM	29	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25798RQMT	VQFN-HR	RQM	29	250	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS

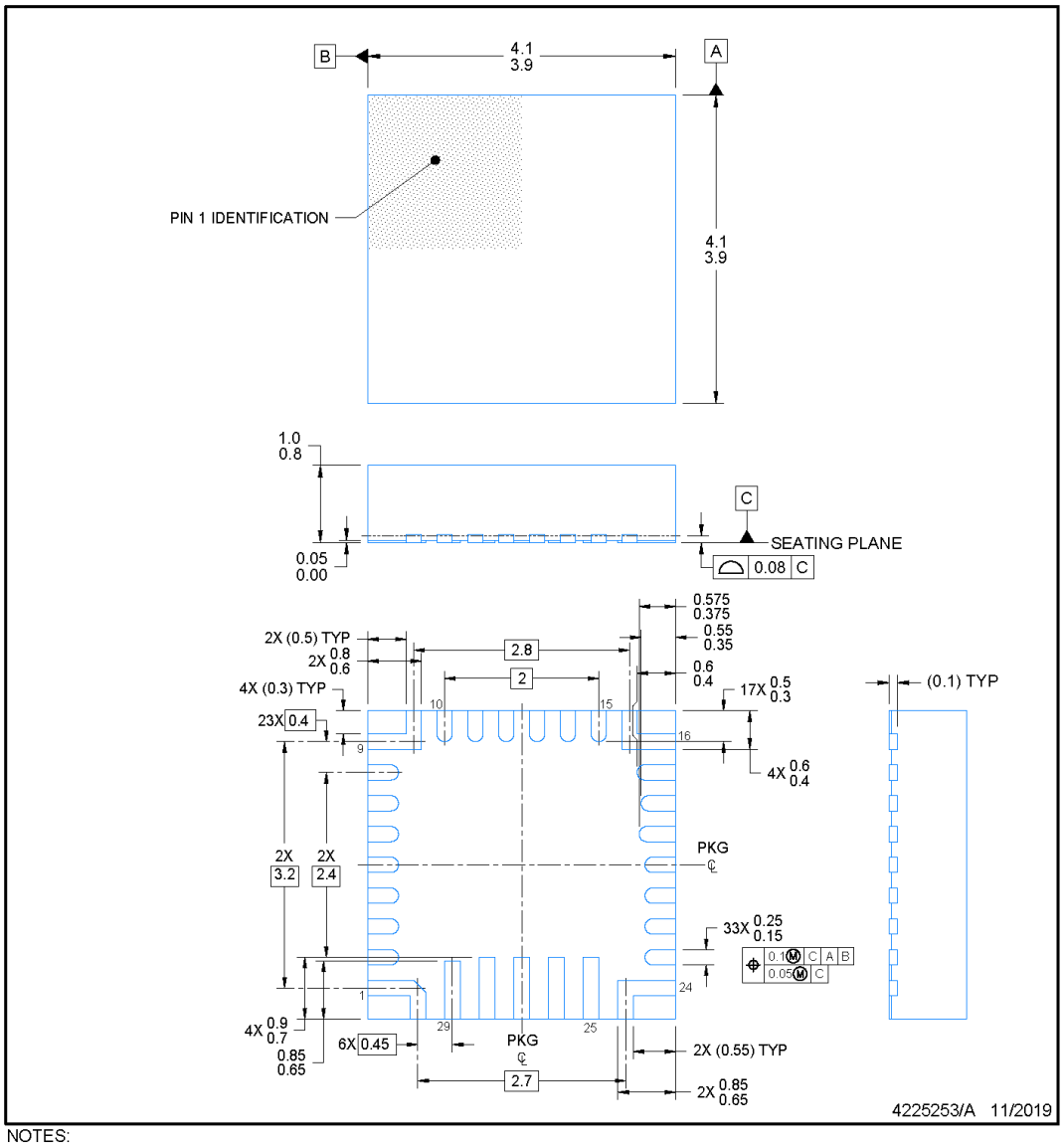


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25798RQMR	VQFN-HR	RQM	29	3000	367.0	367.0	35.0
BQ25798RQMT	VQFN-HR	RQM	29	250	367.0	367.0	35.0

PACKAGE OUTLINE

RQM0029A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

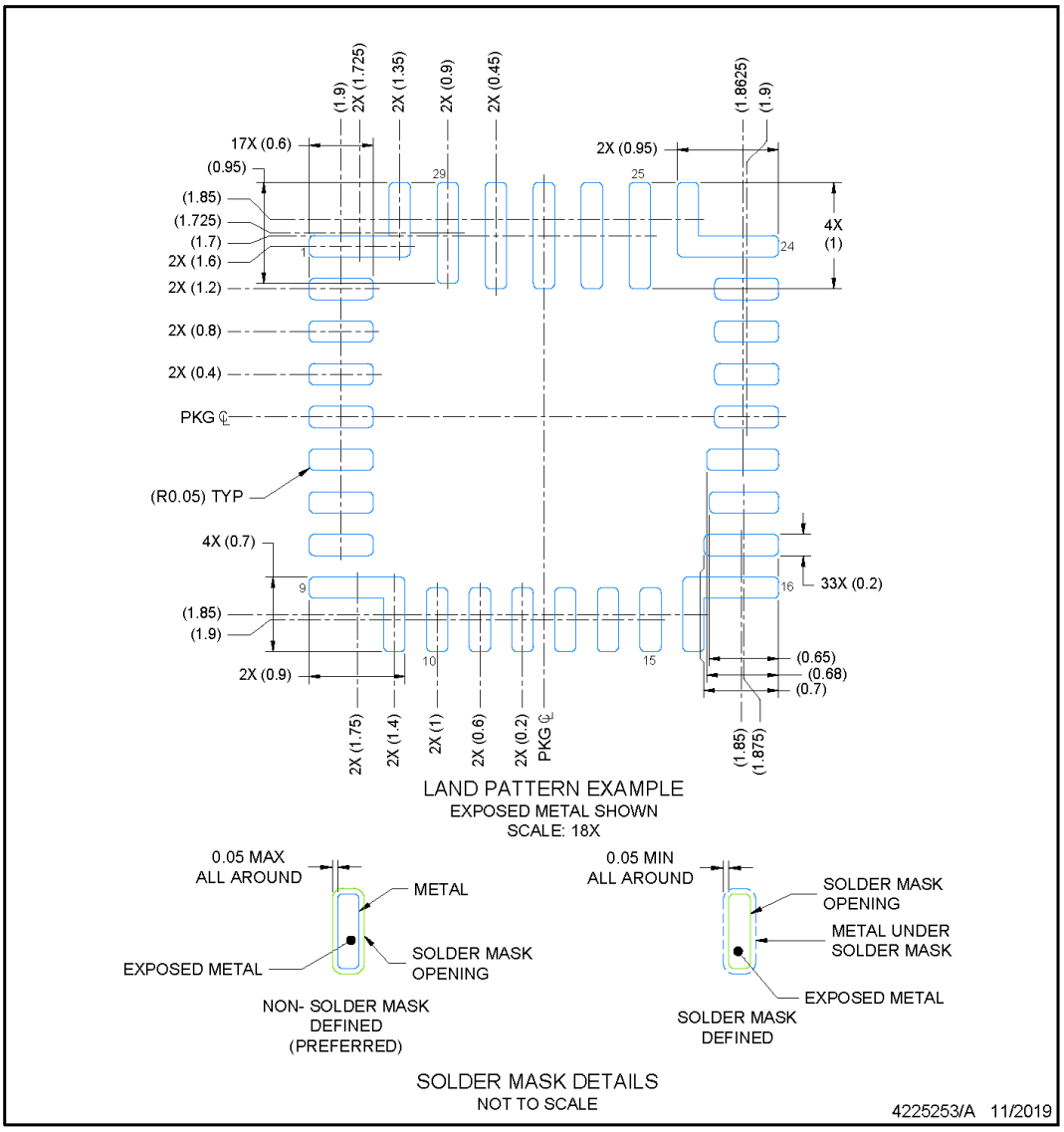
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RQM0029A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



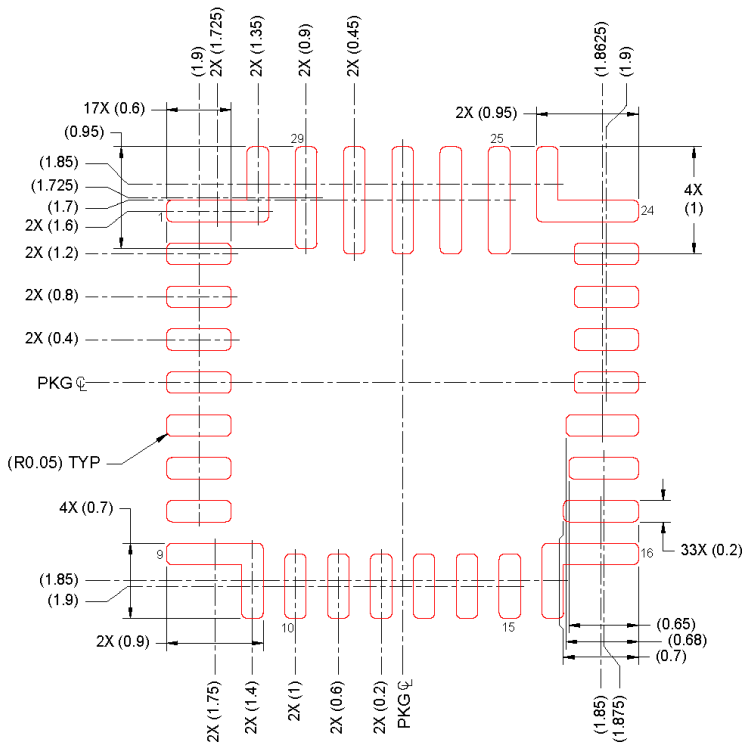
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

RQM0029A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
SCALE: 18X

4225253/A 11/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

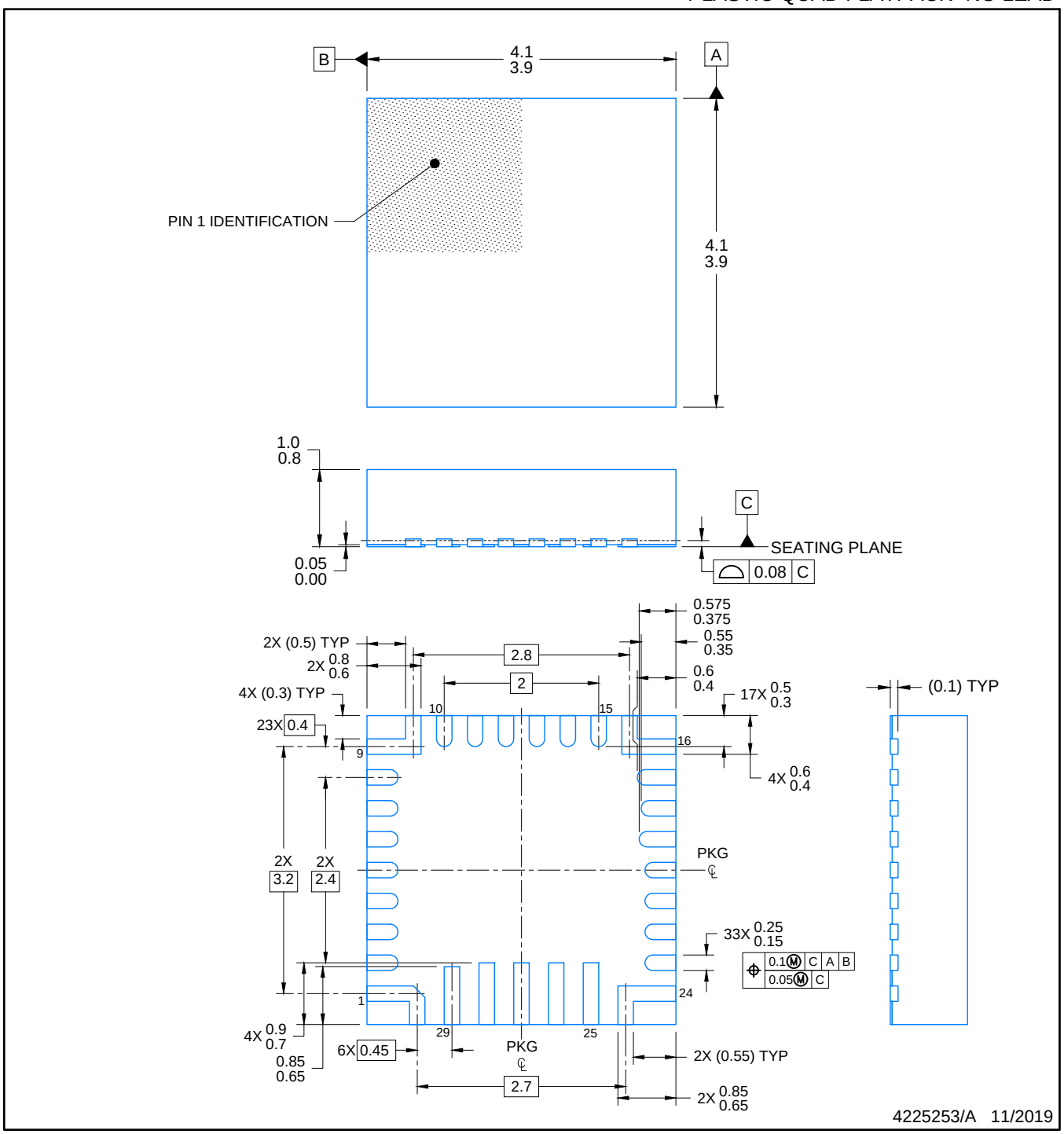
ADVANCE INFORMATION

PACKAGE OUTLINE

RQM0029A

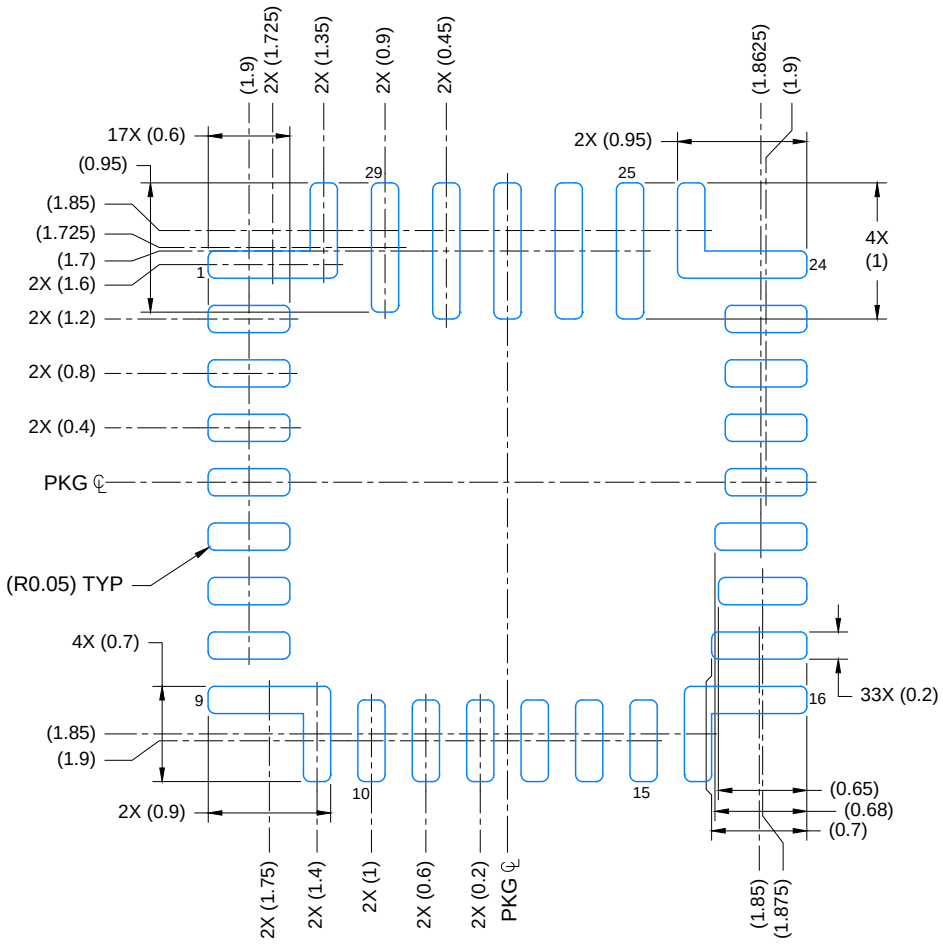
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

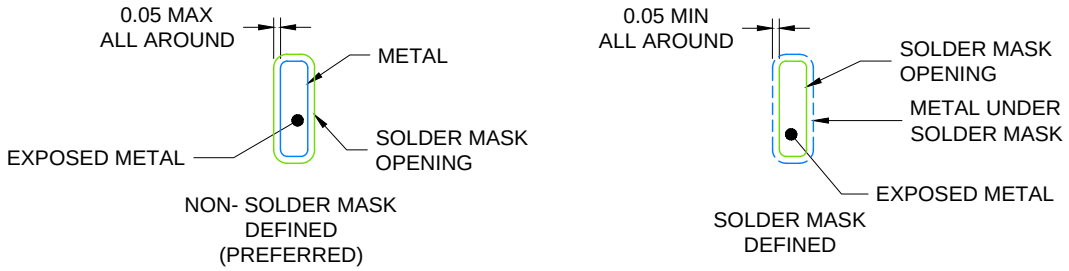
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 18X



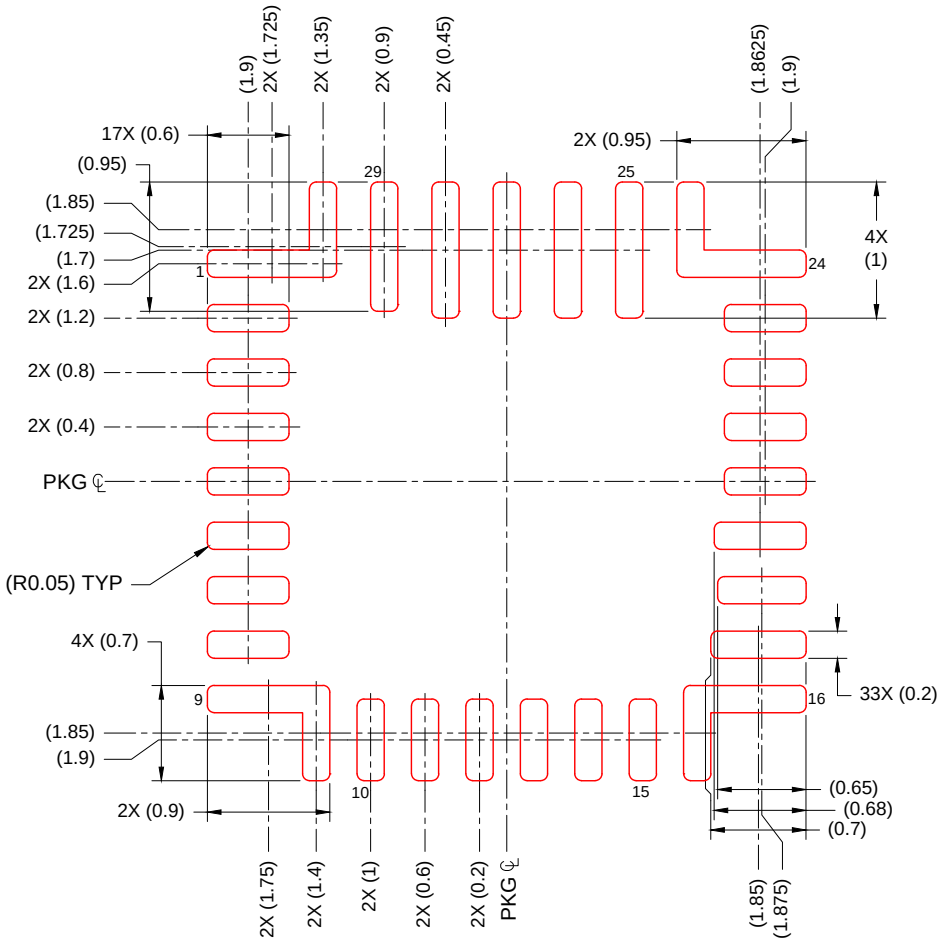
SOLDER MASK DETAILS

NOT TO SCALE

4225253/A 11/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
SCALE: 18X

4225253/A 11/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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