User's Guide

BQ25792EVM, BQ25796EVM, and BQ25798EVM (BMS034) Evaluation Module

ABSTRACT

This user's guide describes the characteristics, operation, and functionality of the BQ25792, BQ25796, and BQ25798 Evaluation Module (EVM). It will also describe the equipment, test setup, and software required to operate the EVM. A complete schematic diagram, printed-circuit board (PCB) layouts, and bill of materials (BOM) are also included in this document.

Throughout this user's guide, the abbreviations and terms *EVM, BQ2579XEVM, BMS034,* and *evaluation module* are synonymous with the BQ25792, BQ25796, and BQ25798 EVM. Note that the BQ25796 and BQ25798 EVMs are not yet available for order.

WARNING

Hot surface! Contact may cause burns. Do not touch!

Some components may reach high temperatures >55°C when the board is powered on. The user must not touch the board at any point during operation or immediately after operating, as high temperatures may be present.

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1 Introduction

The BQ25792, BQ25796, and BQ25798 (BQ25792/6/8) is an integrated switched-mode buck-boost battery charge management device in QFN package. It is intended to charge 1- to 4-series cell Li-ion and Li-polymer batteries. The charger features a narrow VDC architecture (NVDC) which allows the system to be regulated to a minimum value even if the battery is completely discharged. Additionally, the BQ25792/6/8 supports input source detection through D+ and D- which is compatible with USB2.0, USB3.0 power delivery, non-standard adapters, and high voltage adapters. With dual input source selection, USB OTG support, and an integrated 16-bit multi-channel analog-to-digital converter (ADC), the BQ25792/6/8 is a complete charging solution.

1.1 EVM Features

The BQ25792/6/8EVM is a complete module for evaluating the BQ25792/6/8 charger IC in the QFN package. Key features of this EVM include:

- Synchronous Switch Mode Buck-Boost Charger for 1s-4s Battery Configuration for 5-A Charging with 10-mA Resolution
- Support for 3.6-V to 24-V Wide Range of Input Sources USB Auto-Detect, USB PD and Wireless Input
- Dual Input Source Selector to Drive Bi-Directional Blocking NFETs
- Power up USB Port from Battery (USB OTG) with 2.8-V to 22-V OTG Output Voltage with 10-mV Resolution
- Low Battery Quiescent Current < 1 µA in Shutdown Mode
- BQ25796 has backup mode feature. BQ25798 has MPPT feature.

The device data sheet, listed in Table 1-1, provides detailed features and operation.

Table 1-1. Device Data Sheet

Device	Data Sheet
BQ25792	SLUSDG1
BQ25796	SLUSDV3
BQ25798	SLUSDV2

1.2 I/O Descriptions

Table 1-2 table lists the BQ25792/6/8EVM board connections and ports.

Table 1-2. EVM Connections

Connector, Port		Description
J1	VIN1	Positive rail of the priority input adapter or power supply
	GND	Ground
J2	VIN2	Positive rail of the secondary input adapter or power supply
	GND	Ground
J3	SYSTEM	Positive rail of the charger system output voltage, typically connected to the system load
	GND	Ground
J4	VPMID	Positive rail of the charger output voltage for reverse mode (OTG). This output also shares the rail with VBUS in forward mode
	GND	Ground
J5	BATTERY	Positive rail of the charger battery input
	SNS_BATP	Input connected to the positive terminal of the battery for remote battery voltage measurement
	GND	Ground
J6	USB port	USB Micro B port used for input source type detection and handshaking. Connected to either VIN1 or VIN2
J7	EXTERNAL THERMISTOR	Input connected to an external battery temperature sensing thermistor
	GND	Ground
J8	Communication port	I^2C communication port for use with the EV2300/2400 Interface Board
J9	Communication port	I^2C communication port for use with the USB2ANY Interface Adapter (for future use)

Table 1-3 lists the shunt installations available on the EVM, and their respective descriptions.

Table 1-3. EVM Shunt and Switch Installation

Shunt	Description	BQ25792/6/8 Setting
JP1	ACDRV1 pin connection to control ACFET1-RBFET1. Connect this to _acdrv1 net (labeled VAC1 FET) when utilizing the input protection MOSFETs. Connect this to GND when input protection MOSFETs are not used or bypassed	ACDRV1 to VAC1 FETs (short pins 1 to 2)
JP2	ACDRV2 pin connection to control ACFET2-RBFET2. Connect this to _acdrv2 net (labeled VAC2 FET) when utilizing the input protection MOSFETs. Connect this to GND when input protection MOSFETs are not used or bypassed	ACDRV2 to VAC2 FETs (short pins 1 to 2)
JP3	VIN1/VAC1 to VBUS bypass connection. Connect this when the input protection MOSFET feature is not desired. This connects the input source on VIN1 to VBUS.	Not Installed
JP4	VIN2/VAC2 to VBUS bypass connection. Connect this when the input protection MOSFET feature is not desired. This connects the input source on VIN2 to VBUS.	Not Installed
JP5	BAT to BATTERY bypass connection. Connect this when the ship and shutdown mode features are not desired and JP8 pins 1 and 2 are shorted.	Not Installed
JP6	USB Micro B input D– connection to charger D- pin. Connect this when the input source detection and handshake features are desired.	Installed
JP7	USB port J6 positive rail to charger VBUS selection. Use shunt to select either VIN1/VAC1 or VIN2/VAC2 as the connection for the USB port.	USB_VIN to VAC1
JP8	SDRV pin connection to control SFET. Short pins 1 to 2 of JP8 and install shunt across JP5 when ship and shutdown mode features are not desired. Short pins 2 to 3 of JP8 and remove shunt from JP5 when ship and shutdown mode features are desired.	Short pins 2 to 3
JP9	BATP pin connection. BATP is always connected to J5 pin 2 for remote battery sense. If remote sense is not used, short pin 1 to J5 pin 1 (BATTERY) for the charger constant voltage sensing to occur at the connector pin Short pin 2 to pin 3 (BAT pin) for the charger constant voltage sensing to occur on the PCB board. Do not leave BATP pin floating.	Short pin 1 to J5 pin 1 (BATTERY)
JP10	Charger D+ and D- pin short connection. Connect this to simulate a DCP type adapter for the input source detection and handshake feature. Remove in order to use the charger's D+/D- detection feature.	Installed

Table 1-3. EVM Shunt and Switch Installation (continued)

Shunt	Description	BQ25792/6/8 Setting
JP11	USB Micro B input D+ connection to charger D+ pin. Connect this when the input source detection and handshake features are desired.	Installed
JP12	REGN to TS resistor divider network connection. This must remain connected.	Installed
JP13	ILIM_HIZ pin setting for 500 mA. Connect to set the external input current limit setting to 500mA	Not Installed
JP14	ILIM_HIZ pin setting for 1.5 A. Connect to set the external input current limit setting to 500mA	Installed
JP15	Thermistor COOL temperature setting. Connect jumper to simulate charger entering TCOOL (T1-T2) temperature region.	Not Installed
JP16	Thermistor COLD temperature setting. Connect jumper to simulate charger entering TCOLD (<T1) temperature region.	Not Installed
JP17	$\overline{CE}$ pin connection to ground to enable charging. When removed, $\overline{CE}$ pin will pull up to disable charge	Installed
JP18	Thermistor NORMAL temperature setting. Connect jumper to simulate charger entering TNORMAL (T2-T3) temperature region. Keep connected when testing other thermistor temperature settings (JP17 - TCOOL, JP18 - TCOLD, JP21 - TWARM, JP22 - THOT). Remove this jumper whenever using an externally connected thermistor.	Installed
JP19	Thermistor WARM temperature setting. Connect jumper to simulate charger entering TWARM (T3-T5) temperature region.	Not Installed
JP20	Thermistor HOT temperature setting. Connect jumper to simulate charger entering THOT (>T5) temperature region.	Not Installed
JP21	ILIM_HIZ pin setting for HIZ mode. Connect to enter the charger high impedance (HIZ) mode to disable the converter	Not Installed
JP22	PROG pin setting for 1S, 1.5 MHz. Connect to configure charger default setting to 1S charge regulation voltage, 2 A charging current, and 1.5 MHz switching frequency	Not Installed
JP23	PROG pin setting for 1S, 750 kHz. Connect to configure charger default setting to 1S charge regulation voltage, 2 A charging current, and 750 kHz switching frequency	Not Installed
JP24	PROG pin setting for 2S, 1.5 MHz. Connect to configure charger default setting to 2S charge regulation voltage, 2 A charging current, and 1.5 MHz switching frequency	Installed
JP25	PROG pin setting for 2S, 750 kHz. Connect to configure charger default setting to 2S charge regulation voltage, 2 A charging current, and 750 kHz switching frequency	Not Installed
JP26	PROG pin setting for 3S, 1.5 MHz. Connect to configure charger default setting to 3S charge regulation voltage, 1 A charging current, and 1.5 MHz switching frequency	Not Installed
JP27	PROG pin setting for 3S, 750 kHz. Connect to configure charger default setting to 3S charge regulation voltage, 1 A charging current, and 750 kHz switching frequency	Not Installed
JP28	PROG pin setting for 4S, 1.5 MHz. Connect to configure charger default setting to 4S charge regulation voltage, 1 A charging current, and 1.5 MHz switching frequency	Not Installed
JP29	PROG pin setting for 4S, 750 kHz. Connect to configure charger default setting to 4S charge regulation voltage, 1 A charging current, and 750 kHz switching frequency	Not Installed
JP30	Input connection for onboard PULLUP rail LDO. Connect to power onboard 3.3V pullup rail. LDO input will be connected via diode-OR between VBUS and BAT	Installed
JP31	EV2400 internal pullup to PULLUP connection. Connect to use EV2400 internal 3.3 V pullup to drive the EVM PULLUP rail [1]	Not Installed
JP32	STAT pin LED indicator connection. This indicates the current charger Status	Installed
JP33	USB2ANY internal pullup to PULLUP connection. Connect to use the USB2ANY internal 3.3 V pullup to drive the EVM PULLUP rail	Not Installed
S1	$\overline{QON}$ control switch. Press to either exit Ship Mode or reset the System Power	Default Off

[1] EV2400 internal 3.3V pullup rail is not active by default. Requires modification to the internal circuit of the EV2400.

1.3 Recommended Operating Conditions

Table 1-4. Recommended Operating Conditions

	Description	MIN	TYP	MAX	Unit
V(VINx) at J1 or J2	Power supply voltage to the external blocking FETs which allow power to VBUS pin	3.6		24	V
I(INx) into J1 or J2	Power supply current, which can be limited by charger's input current limit feature (IINDPM)	0.01		3.3	A
V(BATTERY) voltage at J5	Battery voltage supported for pre charge	2.2	3.8(1S), 7.6(2S), 11.4(3S), 15.2V(4S)	18.8	V
I(BATTERY) out of/into J5	Battery charge current	0.01	2 (1S, 2S), 1(3S, 4S)	5	A
V(SYS) at J3	System voltage regulation range	3.2		19	V
I(SYS) out of J3	System load current	0		5	A

2 Test Setup and Results

2.1 Equipment

This section includes a list of supplies required to perform tests on the BQ25790EVM.

1. **Power Supplies for VBUS pin:** Power Supply #1 (PS1): A power supply capable of supplying up to 24 V at 3 A is required.
2. **Battery Simulator for BAT pin:** Load #1 (4-Quadrant Supply): A "Kepco" Load, BOP, 20-5M, DC 0 to ±20 V, 0 to ±6 A (or higher) or a Keithley 2450 3-A sourcemeter. When using both, a 1000-µF or higher, low ESR, 25-V rated or higher connected at the EVM battery and ground terminals is recommended.
   Alternative Option: A 0–20 V/0–5 A, > 60-W DC electronic load set in a constant voltage loading mode in parallel with a second power supply can be used. The second power supply is set to a voltage slightly below the electronic load's constant voltage setting. When enabled, the charger's charge current then replaces the current provided the second power supply.
3. **System load simulator for SYS pin:**Load #2(Electronic load set to constant resistance or Resistive Load): 10 Ω, 5 W (or higher)
4. **Meters:** (6x) "Fluke 75" multimeters, (equivalent or better).
   Alternative Option: (4x) equivalent voltage meters and (2x) equivalent current meters. The current meters must be capable of measuring at least 5 A. If used in series between the PS#1, Load#1 or Load#2, the meters should be set for manual not auto ranging. Current meters add significant series resistance which affects charger performance.
5. **Computer:** A computer with at least one USB port and a USB cable. A valid internet connection is required when using the GUI Composer application.
6. **PC Communication Interface:**EV2300/2400 USB-Based PC Interface Board (when using Battery Management Studio).

2.2 Equipment Setup

Use the following list to set up the EVM testing equipment. Refer to Figure 2-1 for the test setup connections to the EVM:

1. Review the EVM connections in Table 1-2.
2. Set PS#1 for 5.0-V, 3-A current limit and then turn off the supply. Connect PS#1 to J1 (VIN1 and PGND).
3. Connect a voltage meter across TP23 (VBUS) and TP44 (PGND) to measure the input voltage as seen from the VBUS pins of the charger.
4. Connect a voltage meter across TP1 and TP2 (I_VAC1_SENSE) to measure the input current into the VBUS pins through the VIN1 path. Alternatively, you may connect a current meter between PS1 and J1.
5. Set Load #1 to constant voltage mode, capable of sinking (for example, compliance) at least 3 A, and output to 5.0 V, and then disable load. Connect Load #1 to J5 (BATTERY and PGND).
6. Connect a voltage meter across TP29 (BAT) and TP46 (PGND) to measure the battery voltage as seen from the BAT pins of the charger.

7. Connect a voltage meter across TP19 and TP20 (I_BAT_SENSE) to measure the battery charge current out of and discharge current into BAT pins. Alternatively, you may connect a current meter between Load #1 and J5.
8. Connect a voltage meter across TP28 (SYS) and TP45 (PGND) to measure the system voltage as seen from the SYS pins of the charger.
9. Install shunts as shown in Table 1-3.

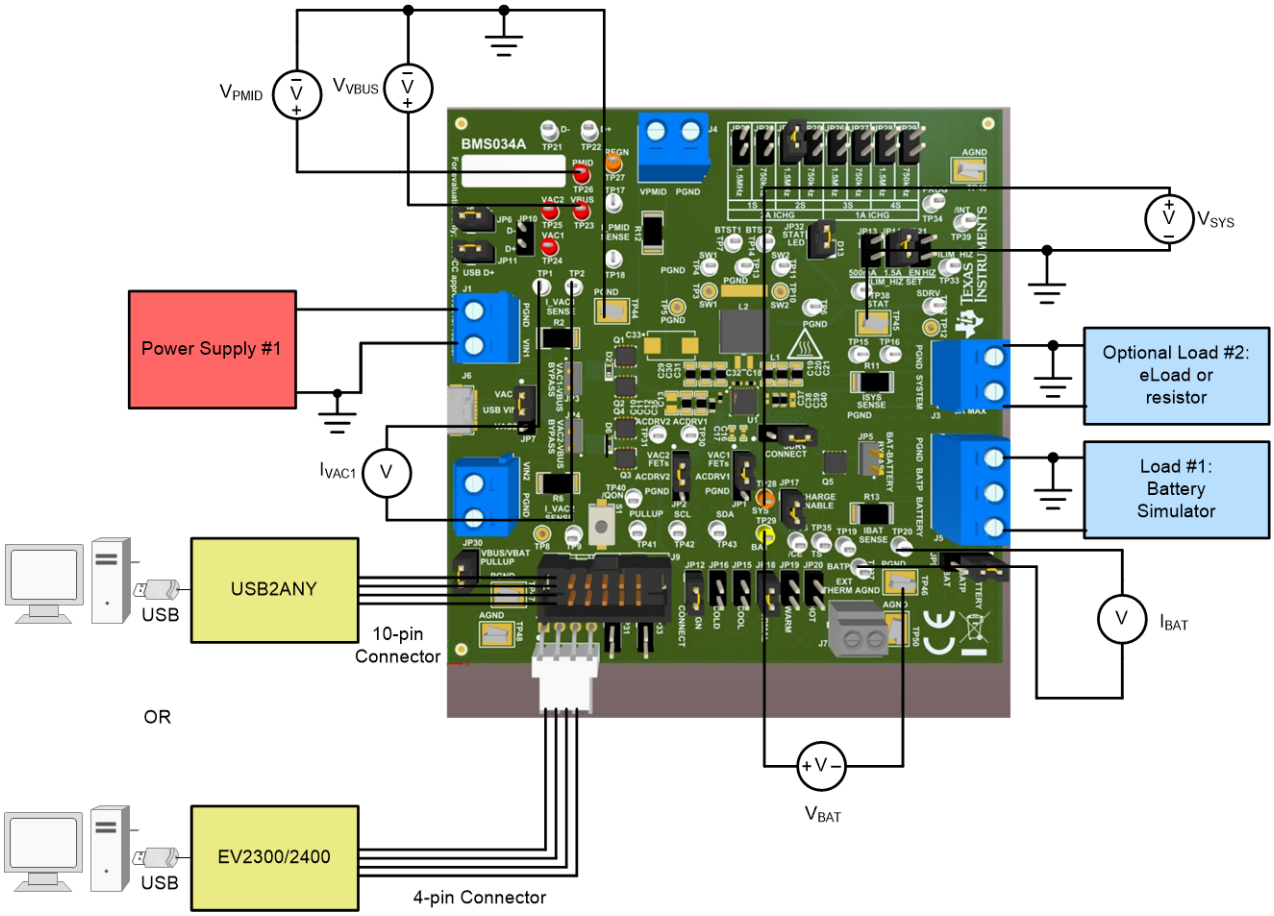


Figure 2-1. Equipment Test Setup for Testing Battery Charging

2.3 Software Setup

2.3.1 BQSTUDIO using EV2400

Download the latest version of BQSTUDIOTEST. Double click the *Battery Management Studio* installation file and follow the installation steps. The software supports Microsoft® Windows® XP, 7, and 10 operating systems. Launch BQSTUDIO and select *Charger*. If the EVM configuration file for BQSTUDIO does not appear in the Charger, close BQSTUDIO and either download the .BQZ file from the EVM product folder at www.ti.com or request the file via e2e.ti.com. The file must be saved into C:\XXX\BatteryManagementStudio\config, where XXX is the directory you selected to install BQSTUDIO.

2.3.2 TI Charger GUI for USB2ANY

Navigate to the TI-CHARGER-GUI tool folder. Once at the tool page click on the "Start Evaluation" button. The browser will automatically be redirected to the TI Charger GUI landing page. From the landing page locate the device desired for evaluation and click "Select Device." Please note that the EVM must be powered and the USB2ANY must be connected to both the EVM and the PC for a connection be established.

2.4 Test Procedure

2.4.1 Initial Settings

Use the following steps to enable the EVM test setup.

1. Make sure Section 2.2 steps have been followed.
2. Remove the shunt on JP17 to disable charge.
3. Launch the BQSTUDIO software and select Charger then BQ25792EVM, if not already done.
4. Turn on PS1 and Load #1:
   - **Measure ➡** $V_{SYS-PGND}$ (TP28 and TP45) = 8.55 V ±0.2 V

2.4.2 Communication Verification

Use the following steps for communications verification:

1. In Battery Management Studio, select "READ REGISTER" at the top of the page. "Device ACK OK" should appear at the top of the page.

Note

If the device is not communicating and does not ACK, verify that Section 2.2 and Section 2.4.1 steps have been followed. Verify the voltage across TP41 (PULLUP) and TP49 (AGND) is approximately 3.3 V.

2. Select **Field View** in the top right of the screen. Note there are two tabs, one for 8-bit registers and one for 16-bit registers. In the 8-bit tab, there are sections for chip, charger and OTG single-bit and multi-bit registers. In the 16-bit tab are the charger and OTG multi-bit registers for setting voltages and currents. In addition, the ADC registers are on the 16-bit tab.
3. Prepare the charge mode charger register settings in the following way if not already set there by default:
   - On the **8-bit Registers tab** in the *Chip Config Multi-bit Registers* section
     - REG10b[2:0] = 000 to disable watchdog time
   - On the**8-bit Registers tab** in the *Chip Config Single-bit Registers* section
     - REG14b[7] = 1 to tell the charger that the ShipFET is present
   - On the **8-bit Registers tab** in the *Charger Multi-bit Registers* section
     - REG08b[5:0] = 000110 to set the pre-charge current regulation limit to 240 mA.
     - REG05b[7:0] = 00101000 to set the input voltage regulation limit (VINDPM) to 4000 mV.
   - On the**16-bit Registers tab** in the *Charger Multi-bit Registers* section
     - REG00b[5:0] = 001110 to set the minimum system voltage to 7000 mV.
     - REG01b[10:0] = 00111000010 to set the maximum constant voltage (CV) charging regulation limit to 8400 mV.
     - REG03b[8:0] = 001100100 to set the maximum constant current (CC) charging regulation limit to 500 mA.
     - REG06b[8:0] = 100101100 to set the input current regulation limit (IINDPM) to 3000 mA.

2.4.3 Charge Mode Verification

Use the following steps for charge mode verification, including pre-charge, CC and CV phases for boost operation:

1. PS1 and Load #1 should be on from Section 2.4.1. In the EVM GUI, it is generally recommended to read REG22-REG27 (or READ ALL REGISTERS) one time in order to show all the interrupts (from status changes, automated routine completion, faults) that occurred since the last read. Reading those registers a second clears the interrupts. After reading the registers,
   - **Verify ➡** REG1B reports all Normal, meaning no DPM loops active and no WD timer fault (bits 7-4), VAC1 Present (bit2), VBUS Present (bit 0) and Power Good (bit 3)
2. Reinstall the shunt on jumper J17 to enable charge
   - **Verify ➡** STAT LED (D13) is lit
3. Take measurements as follows, noting that you may have to adjust the output of the load to accommodate for voltage drop across the leads from the load to the EVM:

- **Measure** ➡ $V_{VBUS-PGND}$ (TP23 and TP44) = 5.0 V ±0.2 V
- **Measure** ➡ $V_{BAT-PGND}$ (TP29 and TP46) = 5.0 V ±0.2 V
- **Measure** ➡ I_{BAT_SENSE} (voltage across 0.01 ohm resistor between TP19 and TP20) = 240 mA ±60 mA
- **Click READ ALL REGISTERS and Verify** ➡ REG1Cb[7:5] reports pre charge

4. Increase Load #1 regulation voltage to 8.0 V and take measurements as follows, noting that you may have to adjust the output of the load to accommodate for voltage drop across the leads from the load to the EVM:
   - **Measure** ➡ $V_{VBUS-PGND}$ (TP23 and TP44) = 5.0 V ±0.2 V
   - **Measure** ➡ $V_{BAT-PGND}$ (TP29 and TP46) = 8.0 V ±0.1 V
   - **Measure** ➡ I_{BAT_SENSE} (voltage across 0.01-Ω resistor between TP19 and TP20) = 500 mA ±50 mA
   - **Measure** ➡ I_{VAC1_SENSE} (voltage across 0.01-Ω resistor between TP1 and TP2) = 900 mA ±60 mA
   - **Click READ ALL REGISTERS and Verify** ➡ REG1Cb[7:5] reports fast charge
5. Increase Load #1 regulation voltage to 8.4 V and take measurements as follows:
   - **Measure** ➡ $V_{BAT-PGND}$ (TP29 and TP46) = 8.4 V ±0.04 V
   - **Measure** ➡ I_{BAT_SENSE} (voltage across 0.01-Ω resistor between TP19 and TP20) = 0 mA ±10 mA
   - **Click READ ALL REGISTERS and Verify** ➡ REG1Cb[7:5] reports termination
6. Helpful hints when changing voltages and register settings from those above during charge mode:
   - If increasing charge current or adding a load at SYS J3 terminal, you will likely need to disable the EN_ILIM bit using 8-bit register tab/Charger Single-bit Registers/REG14b[1] and increase the IINDPM register setting in 16-bit register tab/Charger Multi-bit Registers/REG06b[8:0].
   - If increasing the input voltage above 8 V for the charger to enter buck mode, you will need to increase the VAC_OVP from 7 V default using 8-bit register tab/Charger Multi-bit Registers/REG10b[5:4].
   - The battery configuration is set at startup using the PROG pin (Jumpers JP24 to JP31). The battery configuration can also be changed using 16-bit register tab/Charger Multi-bit Registers/REG0Ab[7:6]. Note that the SYSMIN and charge current charge with cell configuration.
   - The status, fault and interrupt bits report are helpful debug tools.

2.4.4 OTG Mode Verification

Use the following steps for OTG mode verification for boost operation:

1. Power up then turn off Load#2 output. Set to CR = 12 V/0.5 A = 24 Ω. Disconnect PS1 from J1 and attach Load#2 to J1 (VIN1 and GND).
2. Increase Load #1 regulation voltage to 8.0 V and take measurements as follows:
   - **Measure** ➡ $V_{BAT-PGND}$ (TP29 and TP46) = 8.0 V ±0.1 V
3. Prepare the OTG mode charger register settings in the following way:
   - On the **8-bit Registers tab** in the *Chip Config Multi-bit Registers* section
     - REG0Fb[5] = 0 to disable charge mode
     - REG12b[6] = 1 to enable OTG mode
     - REG13b[6] = 1 to enable ACDR1 FETs
   - On the **8-bit Registers tab** in the *OTG Multi-bit Registers* section
     - REG0Bb[10:0] = 01110011000 to set the OTG mode regulation voltage to 12000 mV.
   - On the **8-bit Registers tab** in the *OTG Multi-bit Registers* section
     - REG0Db[6:0] = 0011001 to set the OTG mode current limit to 1000 mA.
4. Take measurements as follows:
   - **Measure** ➡ $V_{VBUS-PGND}$ (TP23 and TP44) = 12.0 V ±0.2 V
   - **Measure** ➡ $V_{AC1-PGND}$ (TP24 and TP44) = 12.0 V ±0.2 V. Note that the PCB silk screen for VAC1 and VAC2 are reversed.
   - **Click READ ALL REGISTERS**
     - **Verify** ➡ REG1Bb[6] reports VINDPM or OTG
     - **Verify** ➡ REG1Cb[4:1] reports VBUS Status as Normal OTG
5. Turn on Load#2 output set to constant resistance (CR) of 24 Ω.
6. Take measurements as follows:
   - **Measure** ➡ $V_{AC1-PGND}$ (TP23 and TP44) = 12.0 V ±0.2 V

- **Measure ➡** $I_{AC1\text{-}SENSE}$ (TP1 and TP2) = 500 mA ±0.10 A

7. Lower the Load#2 to constant resistance (CR) to 10 Ω.
8. Take measurements as follows to confirm OTG current limit function:
   - **Measure ➡** $V_{AC1\text{-}PGND}$ (TP23 and TP44) < 12.0 V ±0.2 V
   - **Measure ➡** $I_{AC1\text{-}SENSE}$ (TP1 and TP2) = 1000 mA ±0.10 A
   - **Click READ ALL REGISTERS and Verify ➡** REG1Bb[7] reports IINDPM
9. Hints for further OTG testing:
   - Enabling OTG mode is a two-step process, first enable OTG and then turn on the appropriate AC drive FETs.

3 PCB Layout Guidelines

Careful placement of components is critical in order for the charger to meet specifications. The items below are listed in order of placement priority.

1. Place high frequency decoupling capacitors for PMID and SYS (C3 and C18 on the EVM) as close possible to their respective pins and ground pin on the same layer as the charger IC (in other words, no vias) in order to have the smallest current loop.
2. Place bulk capacitors for PMID and SYS as close possible to their respective pins and the charger's ground pin on the same layer as the charger IC on the same layer as the charger IC (in other words, no vias).
3. Place the REGN capacitor (C35) to ground and BTST capacitors (C6 and C8) to SW as close as possible to their respective pins only using vias for 1 side of each component if necessary.
4. Place high frequency decoupling capacitors for VBUS and BAT pins as close as possible to their respective pins. Use at least 2 vias per capacitor terminal if required.
5. Place bulk capacitors for VBUS and BAT pins as close as possible to their respective pins. Use at least 2 vias per capacitor terminal if required.
6. Place the inductor close to SW1 and SW2 pins. It is acceptable to use multiple vias to make these connections as the vias are only adding small amounts of inductance and resistance to an inductor.
7. While this EVM has analog ground (AGND) and power ground (PGND) planes that connect close to the charge GND pin, two grounds not required. Resistors and capacitors used for setting sensitive nodes (for example, ILIM, TS) can use one common ground plane but with their ground terminals connected away from high current ground return paths containing switching noise.

Note that this EVM has test points and jumpers requiring traces out to the PCB edges. Routing these traces required some PCB layout compromises for less critical components than those listed in the first six items above.

4 Board Layout, Schematic and Bill of Materials

4.1 BMS034 Board Layout

Figure 4-1 through Figure 4-4 illustrate the schematic for the BQ25792/6/8EVM

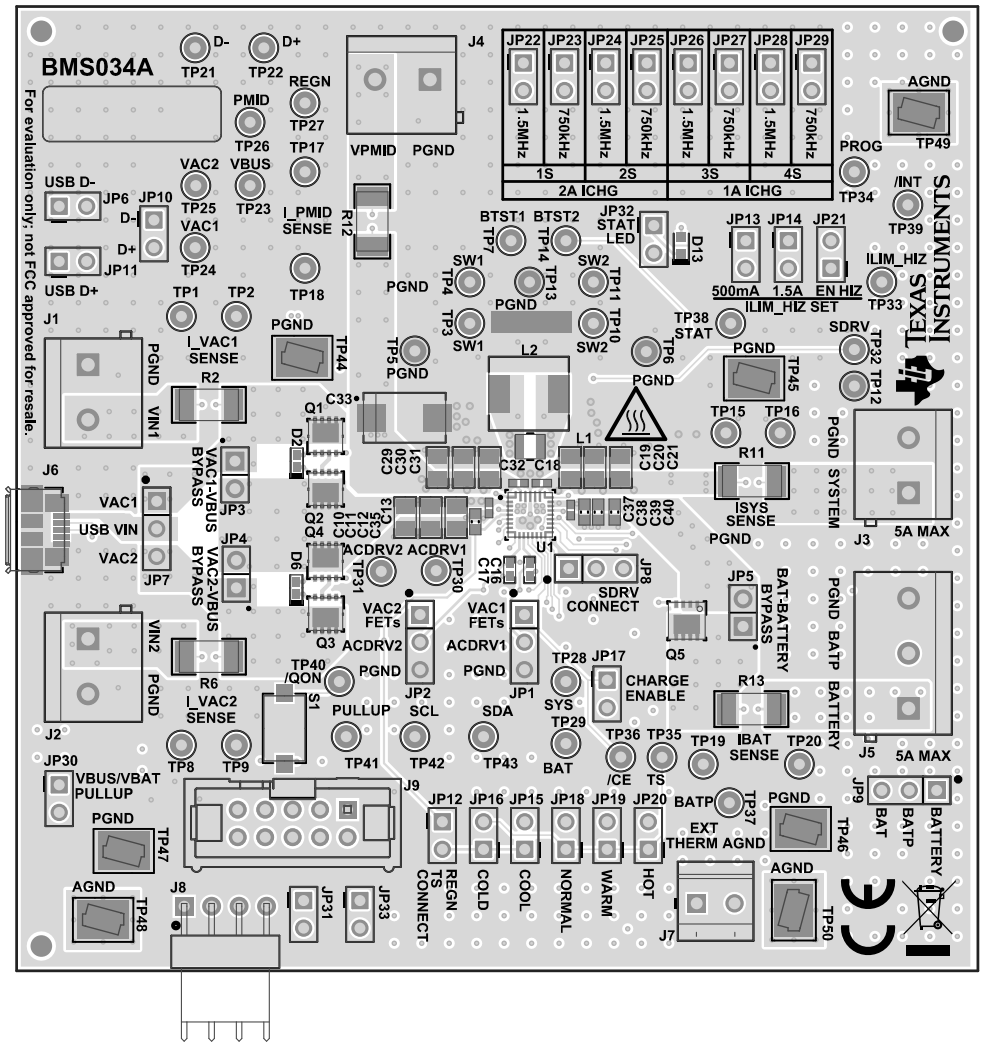


Figure 4-1. BMS034E2/A Top Layer

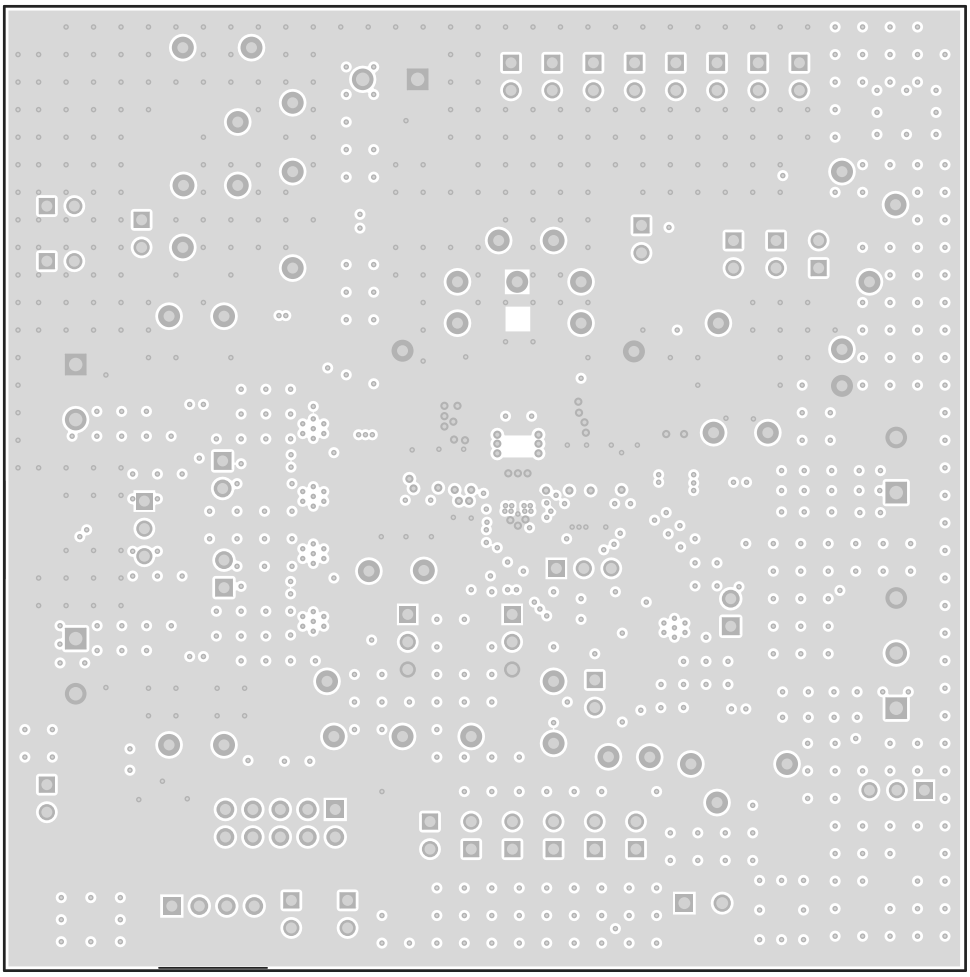


Figure 4-2. BMS034E2/A Signal Layer 1

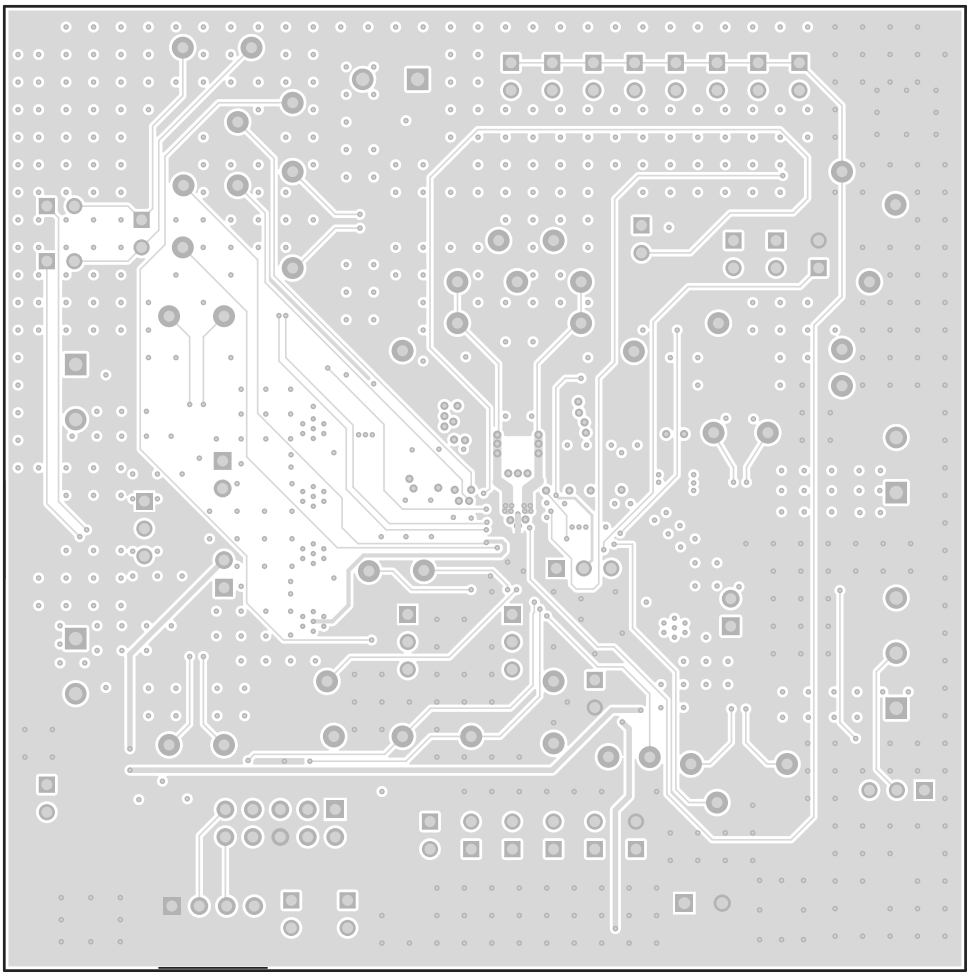


Figure 4-3. BMS034E2/A Signal Layer 2

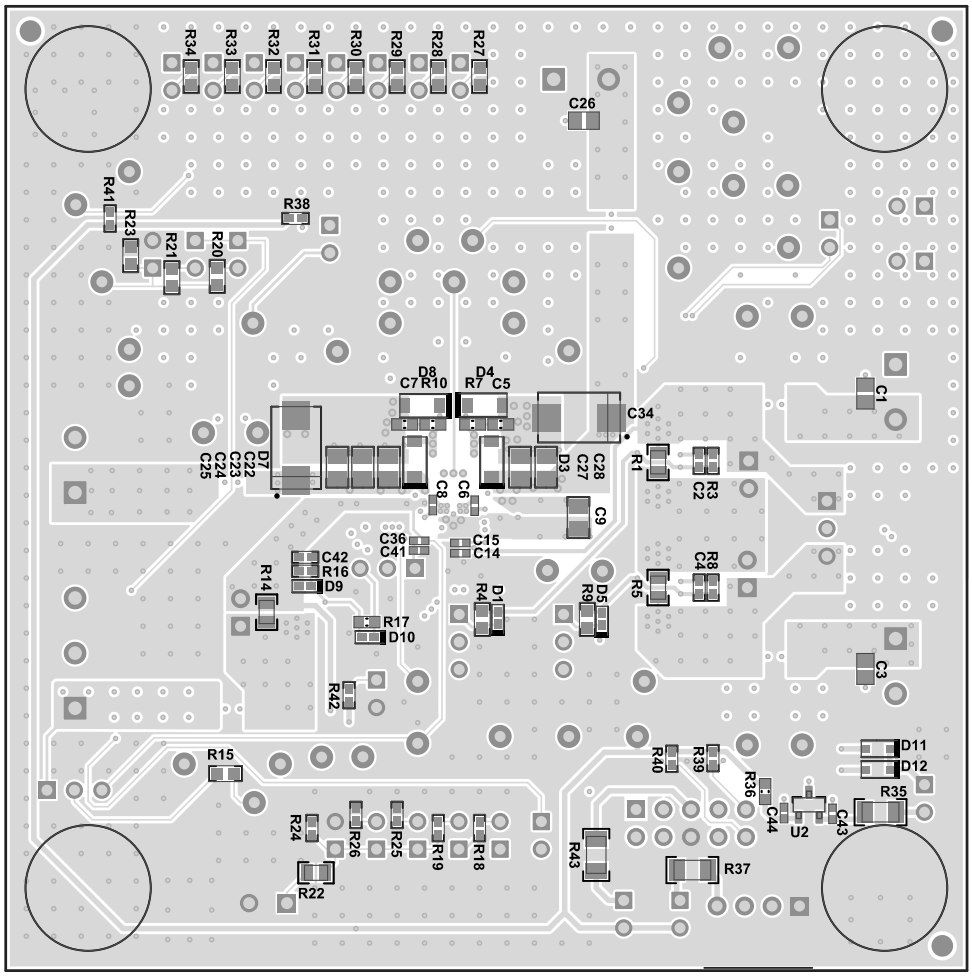
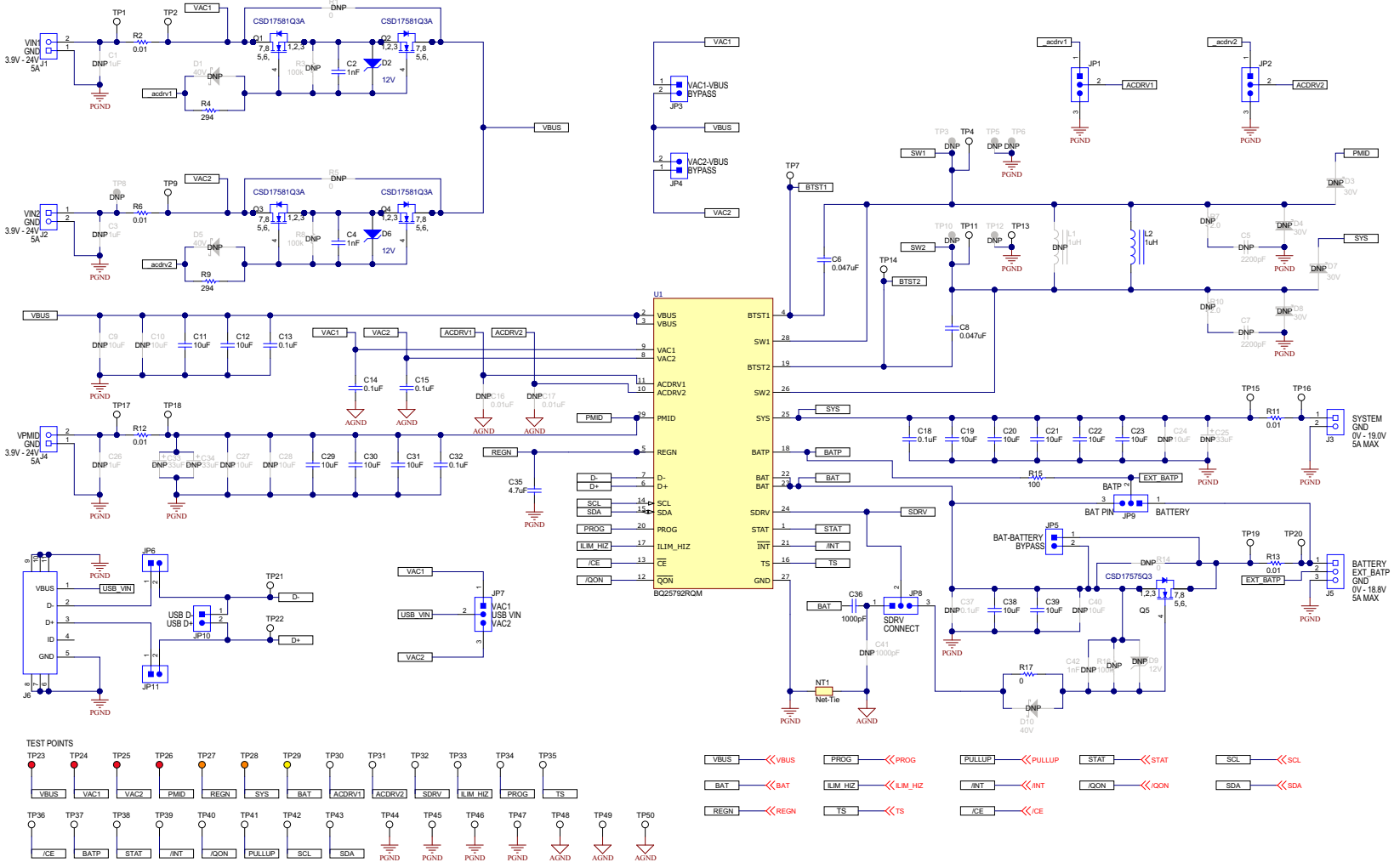


Figure 4-4. BMS034E2/A Bottom Layer

4.2 BQ2579XEVM (BMS034) Schematics

Figure 4-5, Figure 4-6, and Figure 4-7 illustrate the schematics for the BQ2579XEVM



Note

BQ25798 instead of BQ25792 IC is installed on BQ25798EVM.

Figure 4-5. BQ25792EVM (BMS034A-001) and BQ25798EVM (BMS034A-003) Schematic Page 1

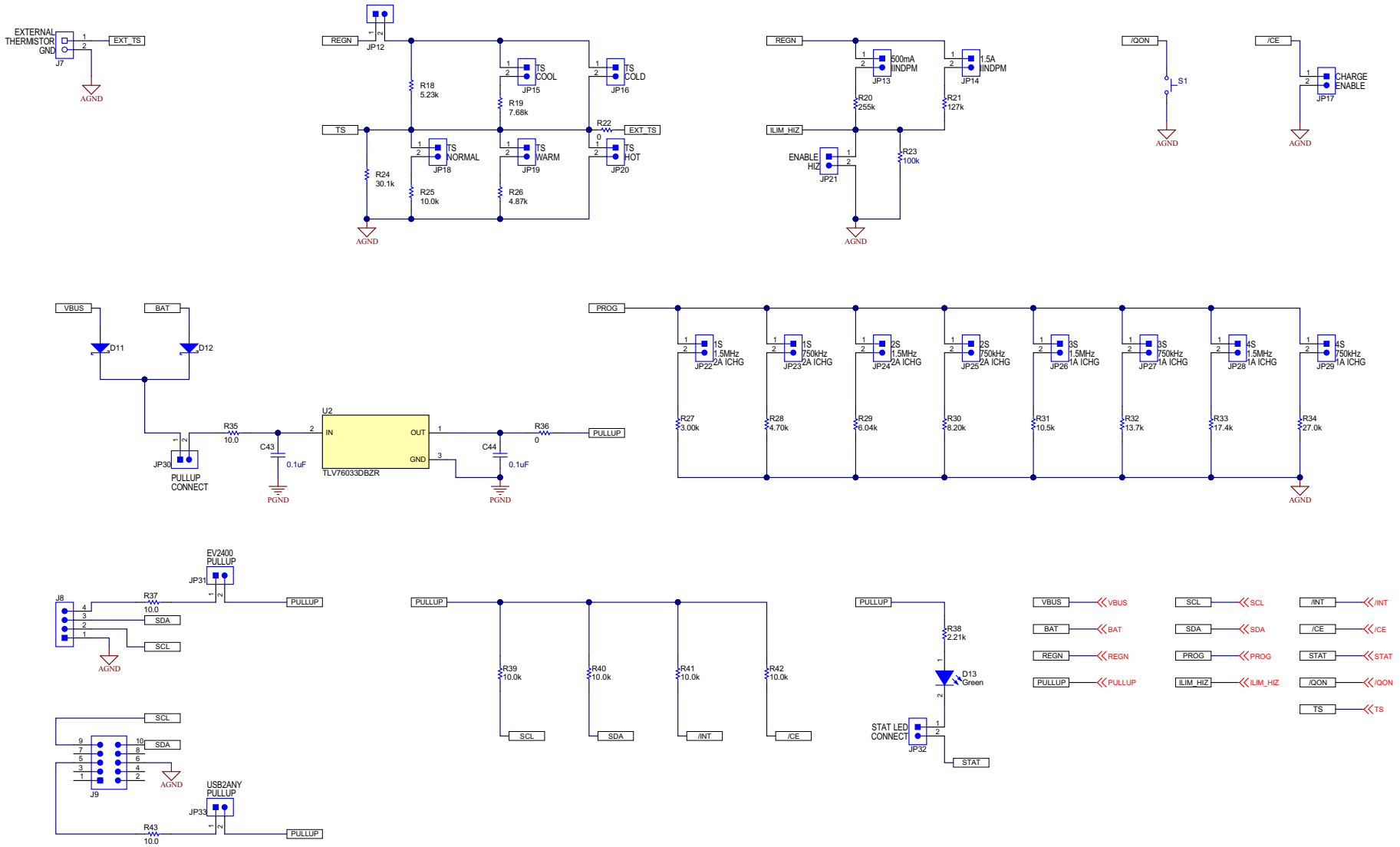


Figure 4-6. BQ25792EVM (BMS034A-001), BQ25796EVM (BMS034A-002) and BQ25798EVM (BMS034A-003) Schematic Page 2

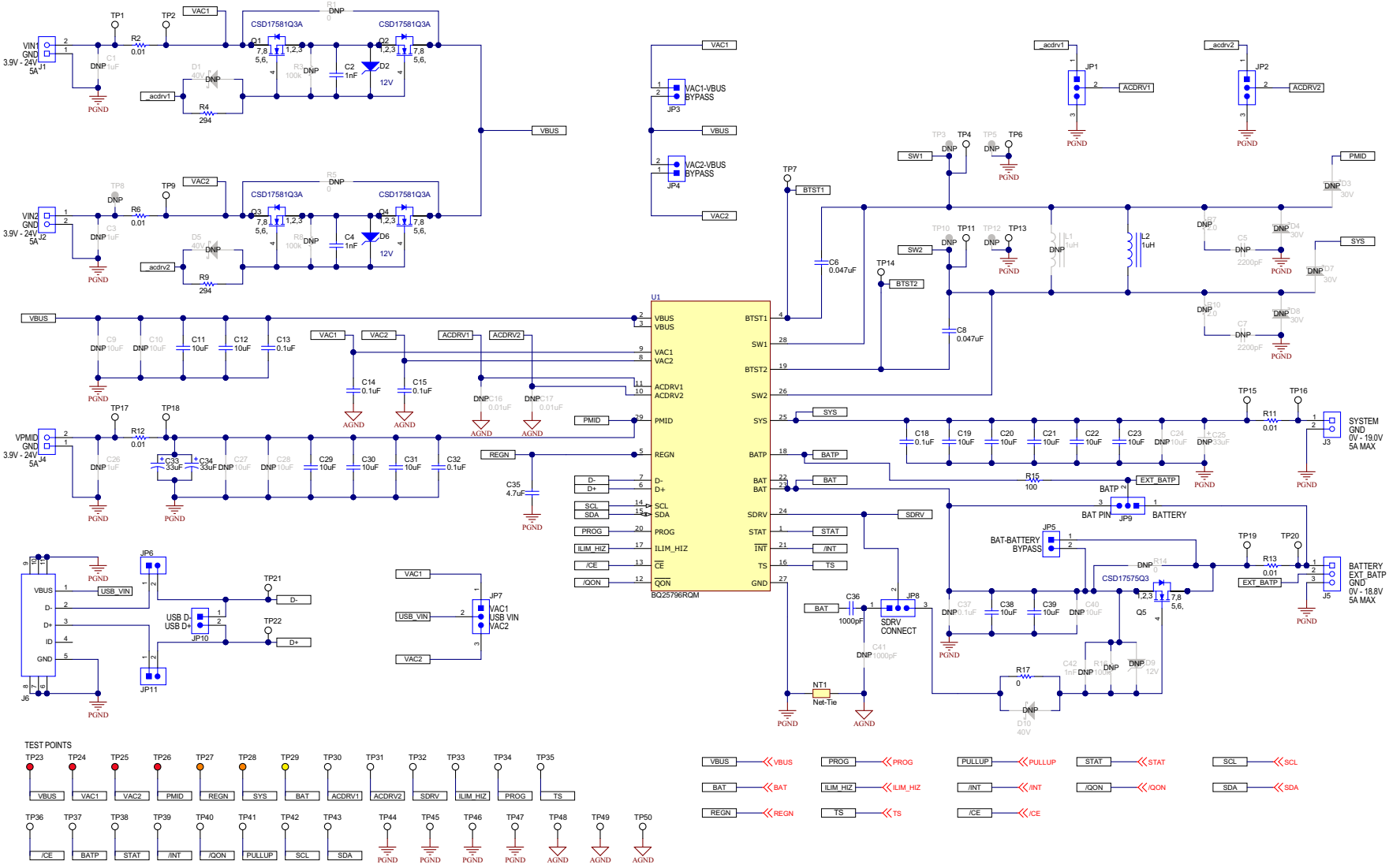


Figure 4-7. BQ25796EVM (BMS034A-002) Schematic Page 1

4.3 Bill of Materials

Table 4-1 lists the BQ2579XEVM bill of materials.

Table 4-1. BQ2579XEVM Bill of Materials

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
C2, C4	2	1000pF	CAP, CERM, 1000 pF, 50 V, ±1%, C0G/NP0, 0402	0402	GRM1555C1H102FA01D	MuRata
C6, C8	2	0.047uF	CAP, CERM, 0.047 uF, 25 V, ±10%, X7R, 0402	0402	GRM155R71E473KA88D	MuRata
C11, C12, C19, C20, C21, C22, C23, C29, C30, C31	10	10uF	CAP, CERM, 10 uF, 25 V, ±10%, X5R, 0805	0805	C2012X5R1E106K125AB	TDK
C13, C14, C15, C18, C32	5	0.1uF	CAP, CERM, 0.1 uF, 50 V,±10%, X7R, 0402	0402	C1005X7R1H104K050BE	TDK
C33, C34 **(BQ25796EVM only)**	2	33uF	CAP, TA, 33 uF, 35 V, ±20%, 0.065 ohm, SMD	7343-31	T521D336M035ATE065	Kemet
C35	1	4.7uF	CAP, CERM, 4.7 uF, 16 V, ±10%, X5R, 0603	0603	GRM188R61C475KAAJD	MuRata
C36	1	1000pF	CAP, CERM, 1000 pF, 50 V, ±5%, C0G/NP0, 0402	0402	GRM1555C1H102JA01D	MuRata
C38, C39	2	10uF	CAP, CERM, 10 uF, 25 V, ±20%, X5R, 0603	0603	GRT188R61E106ME13D	MuRata
C43, C44	2	0.1uF	CAP, CERM, 0.1 uF, 25 V, ±10%, X5R, 0402	0402	GRM155R61E104KA87D	MuRata
D2, D6	2	12V	Diode, Zener, 12 V, 300 mW, SOD-523	SOD-523	BZT52C12T-7	Diodes Inc.
D11, D12	2	30V	Diode, Schottky, 30 V, 0.2 A, SOD-323	SOD-323	BAT54HT1G	ON Semiconductor
D13	1	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT	Lite-On
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J3, J4	4		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
J5	1		Terminal Block, 5.08 mm, 3x1, Brass, TH	3x1 5.08 mm Terminal Block	ED120/3DS	On-Shore Technology
J6	1		Connector, Receptacle, Micro-USB Type B, R/A, Bottom Mount SMT	7.5x2.45x5mm	47346-0001	Molex
J7	1		Terminal Block, 3.5 mm, 2x1, Tin, TH	Terminal Block, 3.5 mm, 2x1, TH	0393570002	Molex
J8	1		Header (friction lock), 100mil, 4x1, R/A, TH	4x1 R/A Header	0022053041	Molex
J9	1		Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH	5x2 Shrouded header	N2510-6002-RB	3M
JP1, JP2, JP7, JP8, JP9	5		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions
JP3, JP4, JP5	3		Header, 100mil, 2x1, Gold, TH	Header, 100mil, 2x1, TH	HTSW-102-07-G-S	Samtec
JP6, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP20, JP21, JP22, JP23, JP24, JP25, JP26, JP27, JP28, JP29, JP30, JP31, JP32, JP33	25		Header, 100mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions
L2	1	1uH	Inductor, Shielded, Ferrite, 1 uH, 11.1 A, 0.0078 ohm, SMD	SMD 7.1x3.0x6.5mm	SPM6530T-1R0M120	TDK
Q1, Q2, Q3, Q4	4	30V	MOSFET, N-CH, 30 V, 60 A, DNH0008A (VSONP-8)	DNH0008A	CSD17581Q3A	Texas Instruments
Q5	1	30V	MOSFET, N-CH, 30 V, 60 A, DQG0008A (VSON-CLIP-8)	DQG0008A	CSD17575Q3	Texas Instruments
R2, R6, R11, R12, R13	5	0.01	RES, 0.01, 1%, 1 W, 2010	2010	WSL2010R0100FEA18	Vishay-Dale
R4, R9	2	294	RES, 294, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603294RFKEA	Vishay-Dale

Table 4-1. BQ2579XEVM Bill of Materials (continued)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
R15	1	100	RES, 100, 1%, 0.1 W, 0603	0603	RC0603FR-07100RL	Yageo
R17, R36	2	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R18	1	5.23k	RES, 5.23 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04025K23FKED	Vishay-Dale
R19	1	7.68k	RES, 7.68 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04027K68FKED	Vishay-Dale
R20	1	255k	RES, 255 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603255KFKEA	Vishay-Dale
R21	1	127k	RES, 127 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603127KFKEA	Vishay-Dale
R22	1	0	RES, 0, 1%, 0.5 W, 0805	0805	5106	Keystone
R23	1	100k	RES, 100 k, 1%, 0.1 W, 0603	0603	RC0603FR-07100KL	Yageo
R24	1	30.1k	RES, 30.1 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040230K1FKED	Vishay-Dale
R25, R39, R40, R41, R42	5	10.0k	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040210K0FKED	Vishay-Dale
R26	1	4.87k	RES, 4.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K87FKED	Vishay-Dale
R27	1	3.57k	RES, 3.57 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06033K57FKEA	Vishay-Dale
R28	1	4.75k	RES, 4.75 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06034K75FKEA	Vishay-Dale
R29	1	6.20k	RES, 6.20 k, 1%, 0.1 W, 0603	0603	RC0603FR-076K2L	Yageo
R30	1	8.20k	RES, 8.20 k, 1%, 0.1 W, 0603	0603	RC0603FR-078K2L	Yageo
R31	1	10.5k	RES, 10.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K5FKEA	Vishay-Dale
R32	1	14.0k	RES, 14.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060314K0FKEA	Vishay-Dale
R33	1	18.0k	RES, 18.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF1802V	Panasonic
R34	1	27.0k	RES, 27.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF2702V	Panasonic
R35, R37, R43	3	10.0	RES, 10.0, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	ERJ-8ENF10R0V	Panasonic
R38	1	2.21k	RES, 2.21 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K21FKED	Vishay-Dale
S1	1		Switch, Normally open, 2.3N force, 200k operations, SMD	KSR	KSR221GLFS	C&K Components
SH-JP1, SH-JP2, SH-JP6, SH-JP7, SH-JP8, SH-JP9, SH-JP11, SH-JP12, SH-JP14, SH-JP17, SH-JP18, SH-JP24, SH-JP30, SH-JP32	14	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP4, TP6, TP7, TP9, TP11, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40, TP41, TP42, TP43	31		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
TP23, TP24, TP25, TP26	4		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP27, TP28	2		Test Point, Miniature, Orange, TH	Orange Miniature Testpoint	5003	Keystone
TP29	1		Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
TP44, TP45, TP46, TP47, TP48, TP49, TP50	7		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone
U1	1		BQ2579x HotRod	VQFN-HR29	BQ25792RQM	Texas Instruments

Table 4-1. BQ2579XEVM Bill of Materials (continued)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
U2	1		100-mA, 30-V, Fixed-Output, Linear-Voltage Regulator, DBZ0003A (SOT-23-3)	DBZ0003A	TLV76033DBZR	Texas Instruments
C1, C3, C26	0	1uF	CAP, CERM, 1 uF, 25 V, ±10%, X7R, 0805	0805	GRM219R71E105KA88D	MuRata
C5, C7	0	2200pF	CAP, CERM, 2200 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H222JA01D	MuRata
C9, C10, C24, C27, C28	0	10uF	CAP, CERM, 10 uF, 25 V, ±10%, X5R, 0805	0805	C2012X5R1E106K125AB	TDK
C16, C17	0	0.01uF	CAP, CERM, 0.01 uF, 50 V, ±5%, X7R, 0402	0402	C0402C103J5RACTU	Kemet
C25	0	33uF	CAP, TA, 33 uF, 35 V, ±20%, 0.065 ohm, SMD	7343-31	T521D336M035ATE065	Kemet
C37	0	0.1uF	CAP, CERM, 0.1 uF, 50 V,±10%, X7R, 0402	0402	C1005X7R1H104K050BE	TDK
C40	0	10uF	CAP, CERM, 10 uF, 25 V, ±20%, X5R, 0603	0603	GRT188R61E106ME13D	MuRata
C41	0	1000pF	CAP, CERM, 1000 pF, 50 V, ±5%, C0G/NP0, 0402	0402	GRM1555C1H102JA01D	MuRata
C42	0	1000pF	CAP, CERM, 1000 pF, 50 V, ±1%, C0G/NP0, 0402	0402	GRM1555C1H102FA01D	MuRata
D1, D5, D10	0	40V	Diode, Schottky, 40 V, 0.38 A, SOD-523	SOD-523	ZLLS350TA	Diodes Inc.
D3, D4, D7, D8	0	30V	Diode, Schottky, 30 V, 1 A, SOD-123	SOD-123	MBR130T1G	Diodes Inc.
D9	0	12V	Diode, Zener, 12 V, 300 mW, SOD-523	SOD-523	BZT52C12T-7	Diodes Inc.
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
L1	0	1uH	Inductor, 1 uH, 3.2 A, 0.028 ohm, SMD	2.5x2mm	MPIM252010F1R0M-LF	Microgate
R1, R5, R14	0	0	RES, 0, 1%, 0.5 W, 0805	0805	5106	Keystone
R3, R8, R16	0	100k	RES, 100 k, 1%, 0.0625 W, 0402	0402	RC0402FR-07100KL	Yageo America
R7, R10	0	2.0	RES, 2.0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06032R00JNEA	Vishay-Dale
SH-JP3, SH-JP4, SH-JP5, SH-JP10, SH-JP13, SH-JP15, SH-JP16, SH-JP19, SH-JP20, SH-JP21, SH-JP22, SH-JP23, SH-JP25, SH-JP26, SH-JP27, SH-JP28, SH-JP29, SH-JP31, SH-JP33	0	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP3, TP5, TP8, TP10, TP12	0		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2020) to Revision B (December 2020) **Page**

- Added BQ25796 and BQ25798 features and data sheet literature numbers..... 2
- Updated description for JP1, JP2, JP5, JP8, and JP9 shunts..... 3
- Deleted EVM revision E2 text. Added BQ25796 schematic and reference to BQ25798 schematic. 15
- Updated existing BOM to include BQ25796EVM components..... 18

Changes from Revision * (June 2020) to Revision A (September 2020) **Page**

- Deleted BQ25795EVM..... 2
- Deleted BQ25795. 2
- Deleted BQ25795EVM from text and table.....2
- Deleted BQ25795EVM..... 3
- Updated *Equipment Test Setup for Testing Battery Charging* image..... 5
- Updated *BMS034E2/A Top Layer* image..... 11
- Changed BMS034E1 to BMS034E2/A.....11
- Updated both schematic images..... 15
- Updated from BMS034E1 to BMS034E2/A..... 15
- Updated C37, D3 and D7 to non-populated 18
- Added D3, D4, D7 and D8 to MBR130T1G..... 18

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