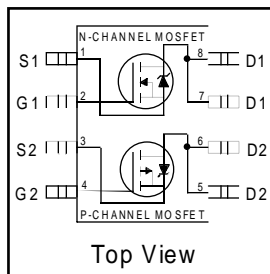


- Generation V Technology
- Ultra Low On-Resistance
- Dual N and P Channel MOSFET
- Surface Mount
- Fully Avalanche Rated

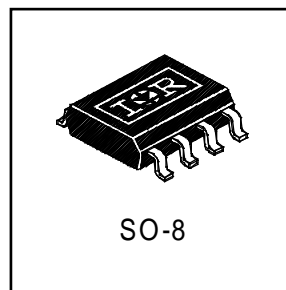
Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques.



	N-Ch	P-Ch
V_{DS}	30V	-30V
$R_{DS(on)}$	0.029 Ω	0.058 Ω



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

		Symbol	Maximum		Units
			N-Channel	P-Channel	
Drain-Source Voltage		V _{DS}	30	-30	V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current⑤	T _A = 25°C	I _D	6.5	-4.9	A
	T _A = 70°C		5.2	-3.9	
Pulsed Drain Current		I _{DM}	30	-30	
Continuous Source Current (Diode Conduction)		I _S	2.5	-2.5	
Maximum Power Dissipation ⑤	T _A = 25°C	P _D	2.0		W
	T _A = 70°C		1.3		
Single Pulse Avalanche Energy		E _{AS}	82	140	mJ
Avalanche Current		I _{AR}	4.0	-2.8	A
Repetitive Avalanche Energy		E _{AR}	0.20		mJ
Peak Diode Recovery dv/dt ②		dv/dt	5.0	-5.0	V/ ns
Junction and Storage Temperature Range		T _J , T _{STG}	-55 to + 150 °C		

Thermal Resistance Ratings

Parameter	Symbol	Limit	Units
Maximum Junction-to-Ambient ⑤	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
		P-Ch	-30	—	—		$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.022	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
		P-Ch	—	0.022	—		Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	0.023	0.029	Ω	$V_{GS} = 10V, I_D = 5.8A$ ④
			—	0.032	0.046		$V_{GS} = 4.5V, I_D = 4.7A$ ④
		P-Ch	—	0.042	0.058		$V_{GS} = -10V, I_D = -4.9A$ ④
			—	0.076	0.098		$V_{GS} = -4.5V, I_D = -3.6A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		P-Ch	-1.0	—	—		$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	N-Ch	—	14	—	S	$V_{DS} = 15V, I_D = 5.8A$ ④
		P-Ch	—	7.7	—		$V_{DS} = -15V, I_D = -4.9A$ ④
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		P-Ch	—	—	-1.0		$V_{DS} = -24V, V_{GS} = 0V$
		N-Ch	—	—	25		$V_{DS} = 24V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
		P-Ch	—	—	-25		$V_{DS} = -24V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	± 100	nA	$V_{GS} = \pm 20V$
Q_g	Total Gate Charge	N-Ch	—	22	33		N-Channel $I_D = 5.8A, V_{DS} = 15V, V_{GS} = 10V$ ④
		P-Ch	—	23	34		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	2.6	3.9	nC	
		P-Ch	—	3.8	5.7		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	6.4	9.6		P-Channel $I_D = -4.9A, V_{DS} = -15V, V_{GS} = -10V$
		P-Ch	—	5.9	8.9		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	8.1	12		N-Channel $V_{DD} = 15V, I_D = 1.0A, R_G = 6.0\Omega, R_D = 15\Omega$ ④
		P-Ch	—	13	19		
t_r	Rise Time	N-Ch	—	8.9	13		
		P-Ch	—	13	20		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	26	39	ns	
		P-Ch	—	34	51		
t_f	Fall Time	N-Ch	—	17	26		P-Channel $V_{DD} = -15V, I_D = -1.0A, R_G = 6.0\Omega, R_D = 15\Omega$
		P-Ch	—	32	48		
C_{iss}	Input Capacitance	N-Ch	—	650	—	pF	N-Channel $V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$
		P-Ch	—	710	—		
C_{oss}	Output Capacitance	N-Ch	—	320	—		P-Channel $V_{GS} = 0V, V_{DS} = -25V, f = 1.0\text{MHz}$
		P-Ch	—	380	—		
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	130	—		
		P-Ch	—	180	—		

Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	2.5	A	
		P-Ch	—	—	-2.5		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	30		
		P-Ch	—	—	-30		
V_{SD}	Diode Forward Voltage	N-Ch	—	0.78	1.0	V	$T_J = 25^\circ\text{C}, I_S = 1.7A, V_{GS} = 0V$ ③
		P-Ch	—	-0.78	-1.0		$T_J = 25^\circ\text{C}, I_S = -1.7A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	N-Ch	—	45	68	ns	N-Channel $T_J = 25^\circ\text{C}, I_F = 1.7A, di/dt = 100A/\mu s$ ④
		P-Ch	—	44	66		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	58	87	nC	
		P-Ch	—	42	63		

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 22)
- ② N-Channel $I_{SD} \leq 4.0A, di/dt \leq 74A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
P-Channel $I_{SD} \leq -2.8A, di/dt \leq 150A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ③ N-Channel Starting $T_J = 25^\circ\text{C}, L = 10\text{mH}, R_G = 25\Omega, I_{AS} = 4.0A$. (See Figure 12)
P-Channel Starting $T_J = 25^\circ\text{C}, L = 35\text{mH}, R_G = 25\Omega, I_{AS} = -2.8A$.
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

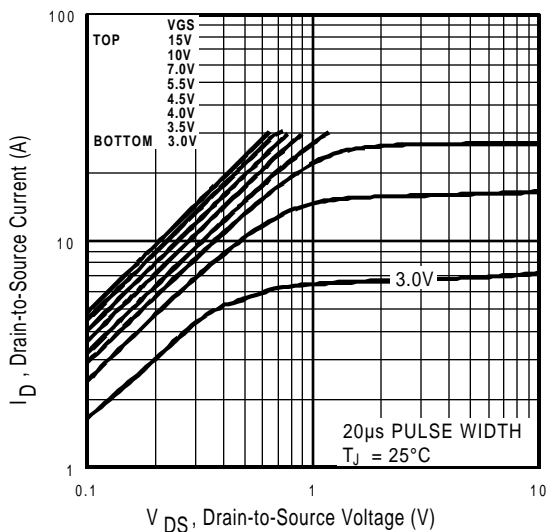


Fig 1. Typical Output Characteristics

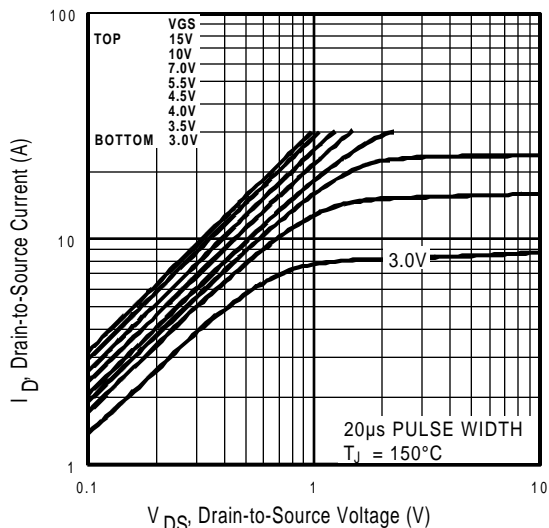


Fig 2. Typical Output Characteristics

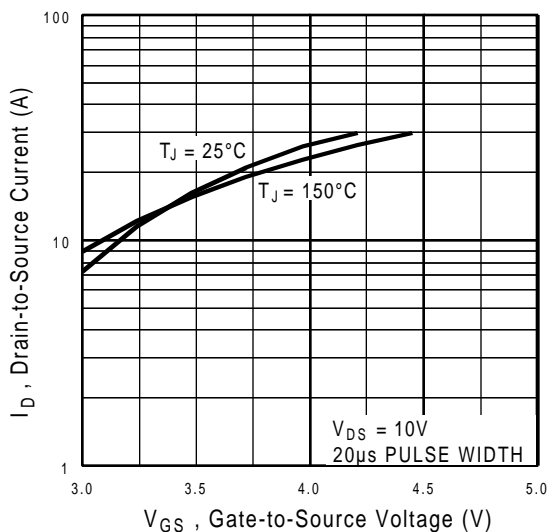


Fig 3. Typical Transfer Characteristics

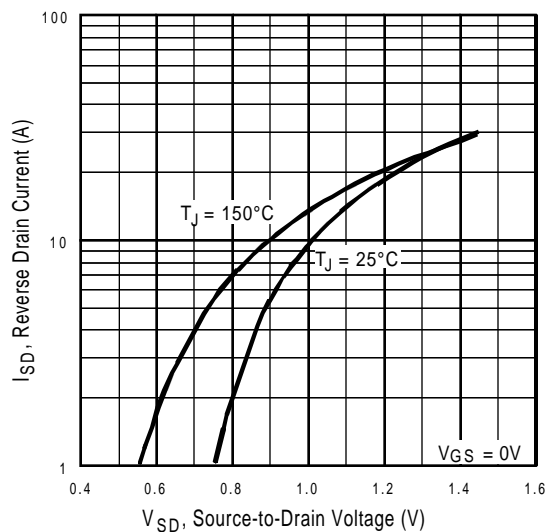


Fig 4. Typical Source-Drain Diode Forward Voltage

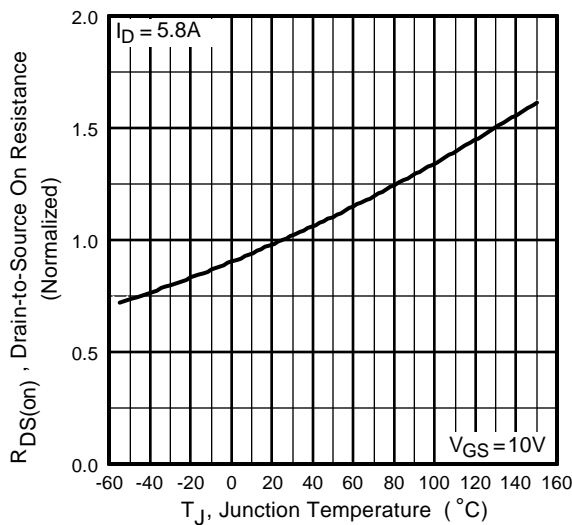


Fig 5. Normalized On-Resistance Vs. Temperature

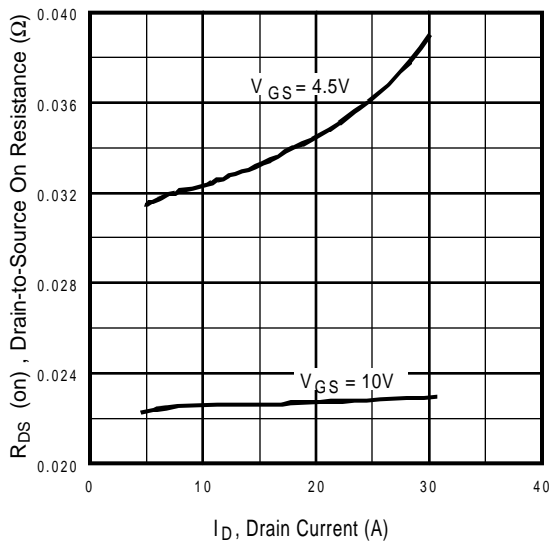


Fig 6. Typical On-Resistance Vs. Drain Current

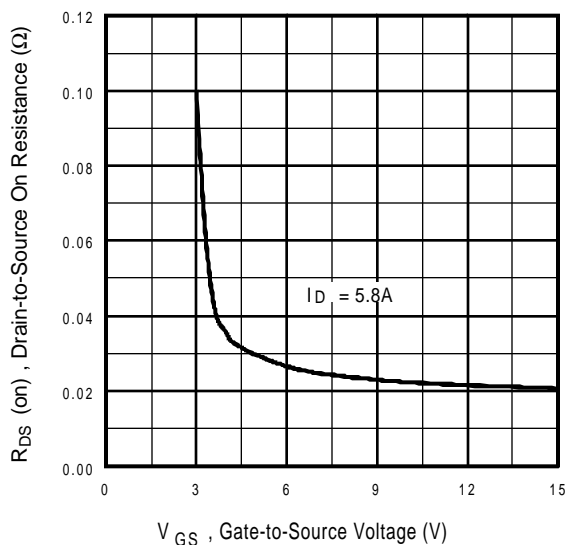


Fig 7. Typical On-Resistance Vs. Gate Voltage

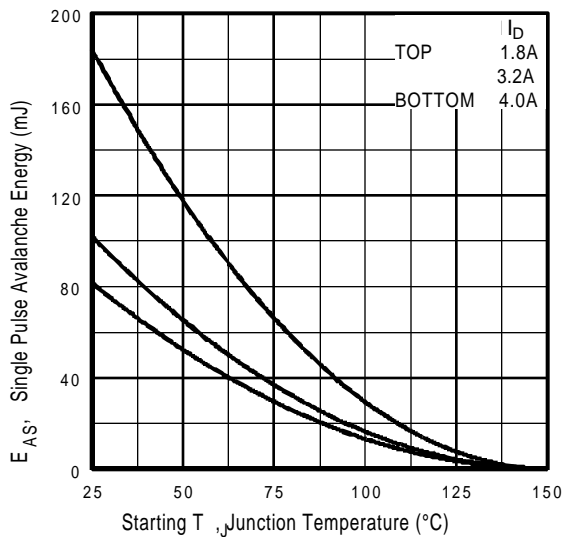


Fig 8. Maximum Avalanche Energy Vs. Drain Current

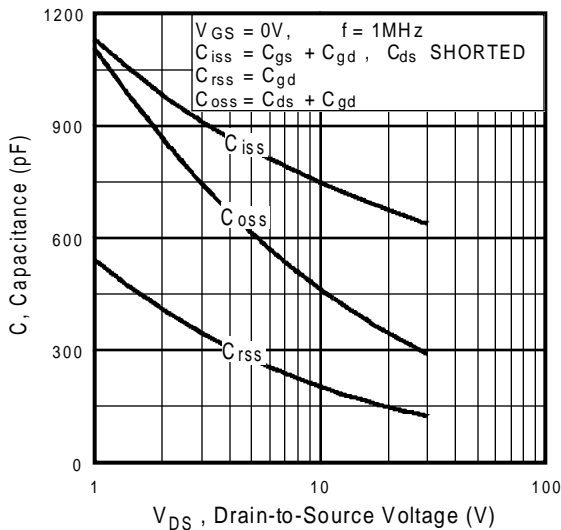


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

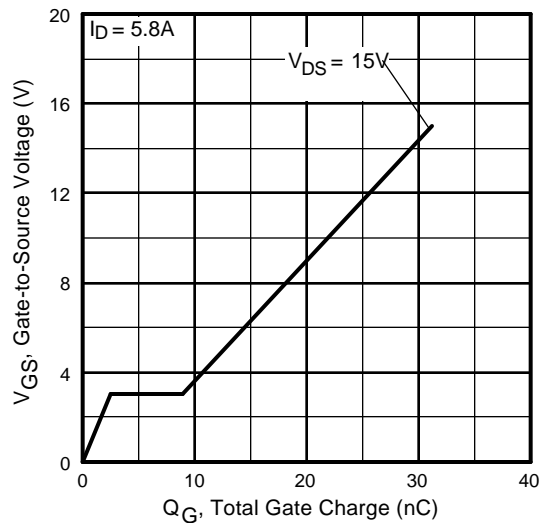


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

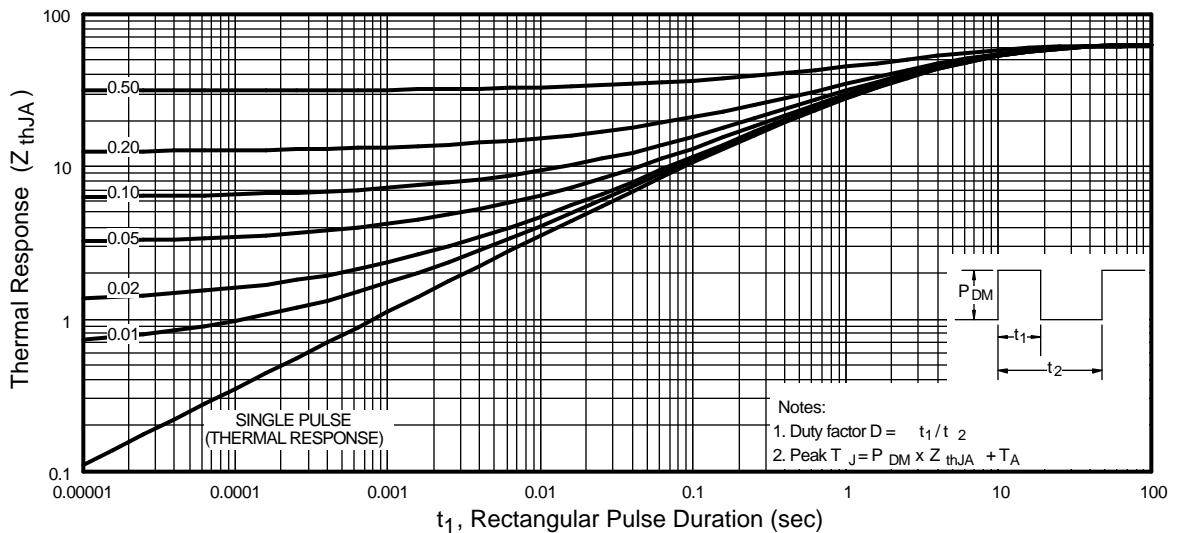
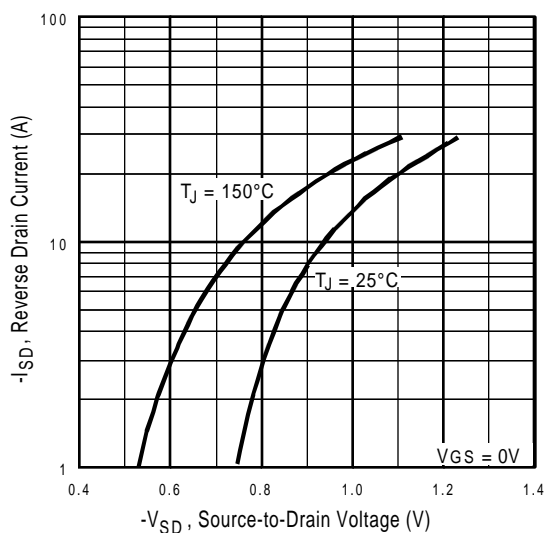
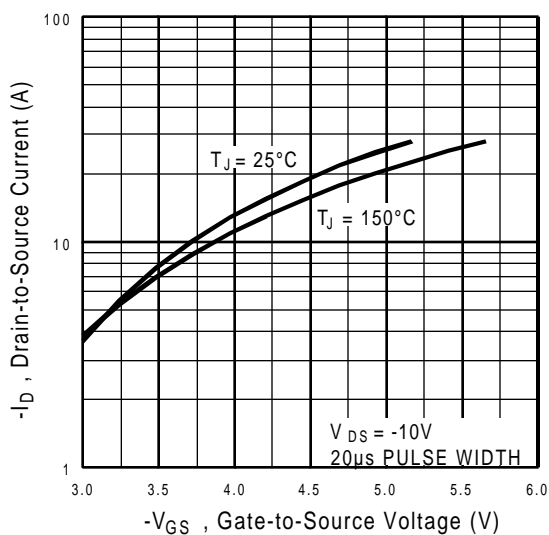
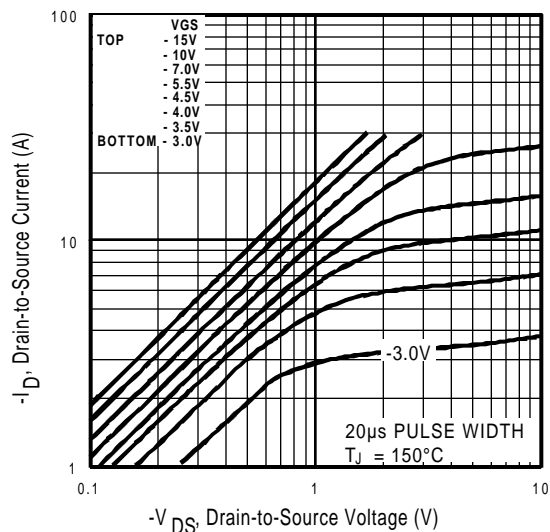
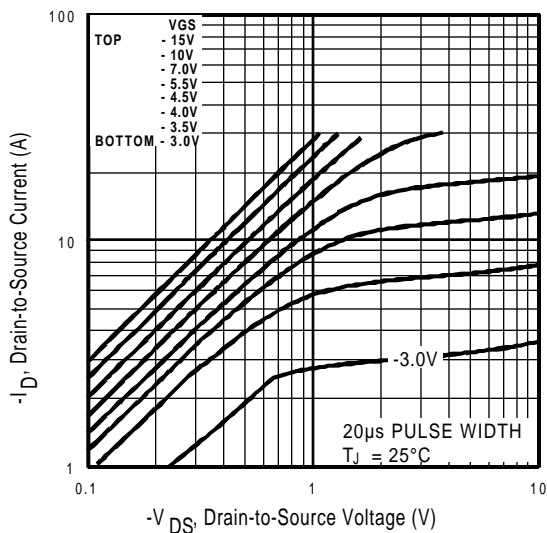


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



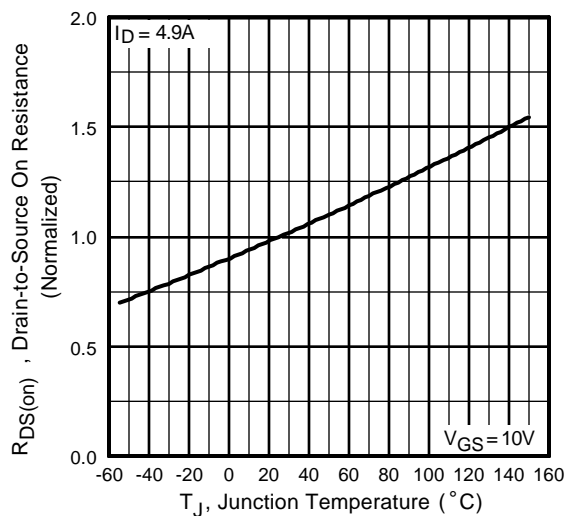


Fig 16. Normalized On-Resistance Vs. Temperature

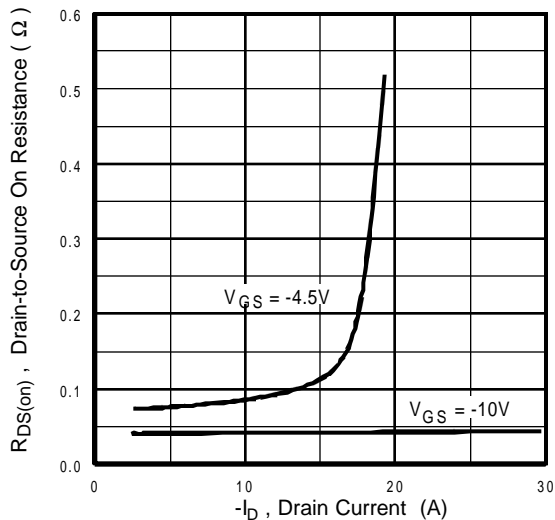


Fig 17. Typical On-Resistance Vs. Drain Current

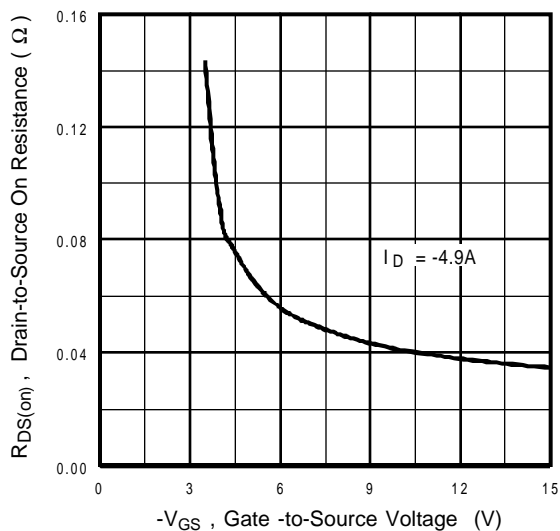


Fig 18. Typical On-Resistance Vs. Gate Voltage

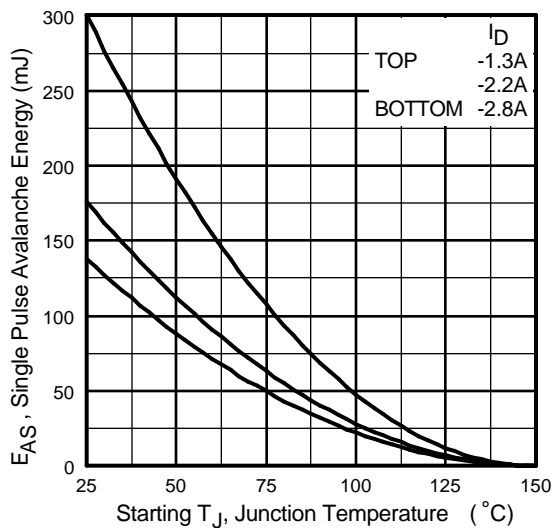


Fig 19. Maximum Avalanche Energy Vs. Drain Current

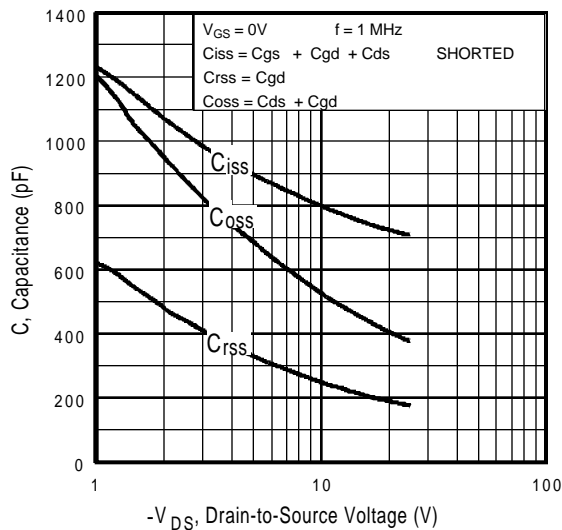


Fig 20. Typical Capacitance Vs. Drain-to-Source Voltage

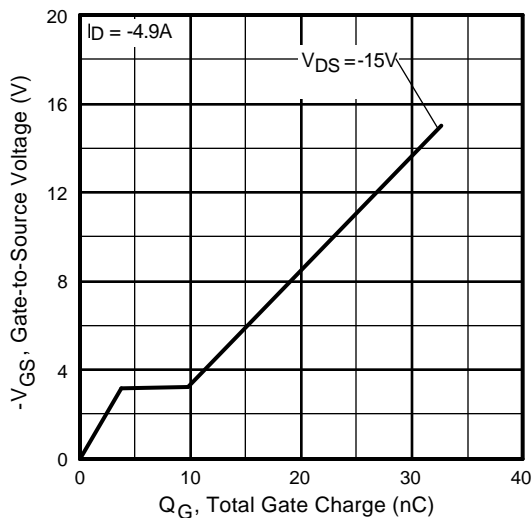


Fig 21. Typical Gate Charge Vs. Gate-to-Source Voltage

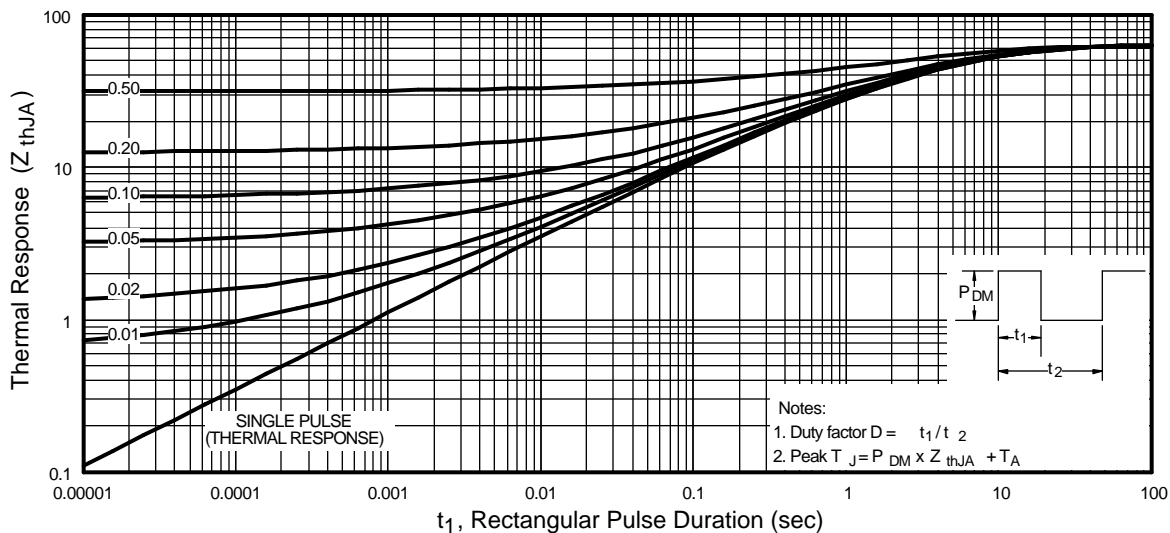
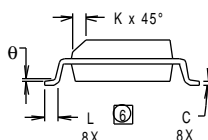
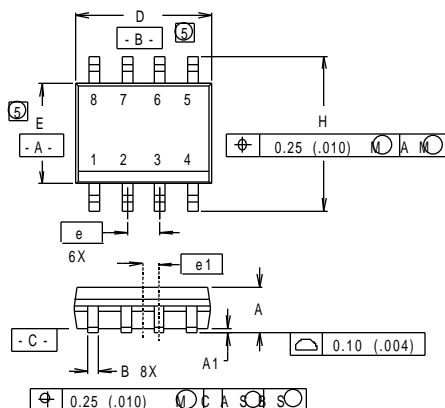


Fig 22. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

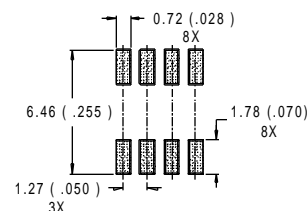
Package Outline

SO8 Outline



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	0.16	.050	0.41	1.27
θ	0°	8°	0°	8°

RECOMMENDED FOOTPRINT



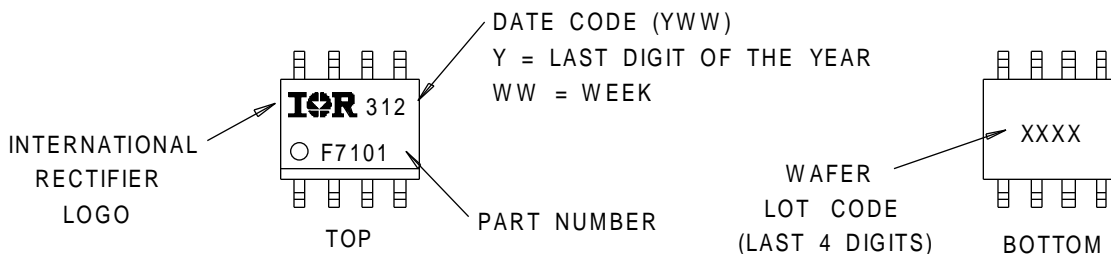
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS
MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).
- ⑥ DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..

Part Marking Information

SO8

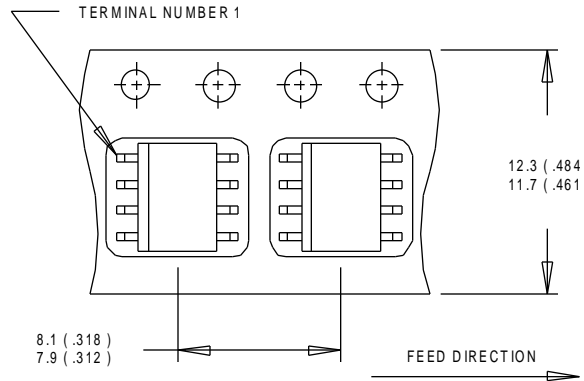
EXAMPLE : THIS IS AN IRF7101



Tape & Reel Information

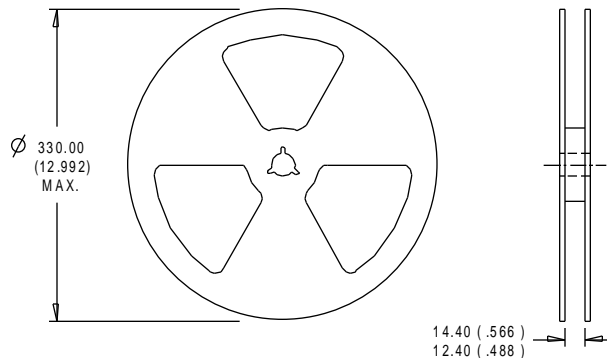
S08

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

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IR Rectifier

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Data and specifications subject to change without notice.

9/97