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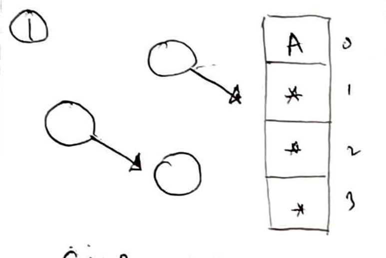
2)(a) So we have been given a 4-way set associative cache that uses pseudo-LRU block replacement policy.

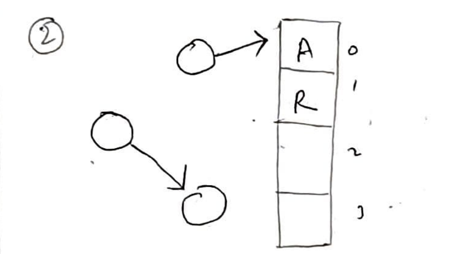
The 13 block nos. (excluding #, $ and @ are as follows):-

A, R, S, R, B, A, D, C, S, A, S, B, E

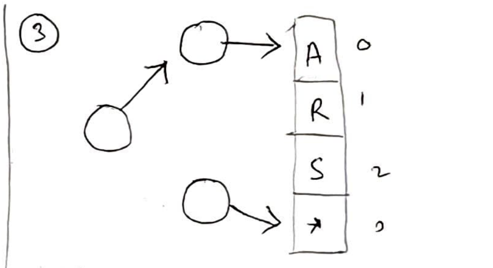
Let us draw the ~~LRU~~ pseudo-LRU tree:-

① 

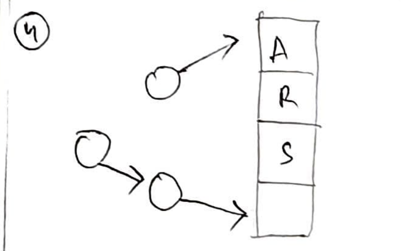
CMP-MISS (A)

② 

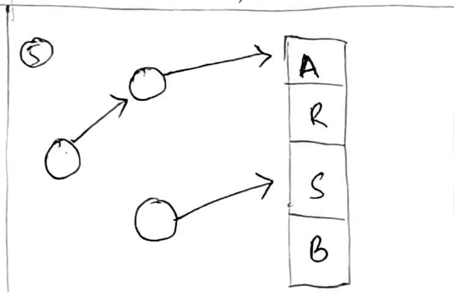
CMP-MISS (R)

③ 

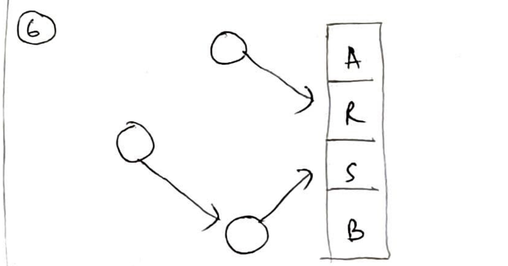
CMP-MISS (S)

④ 

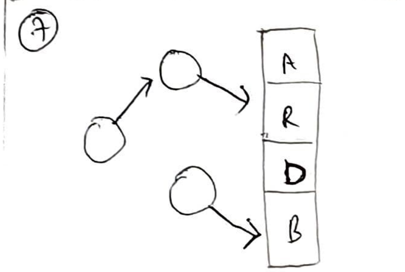
HIT (R)

⑤ 

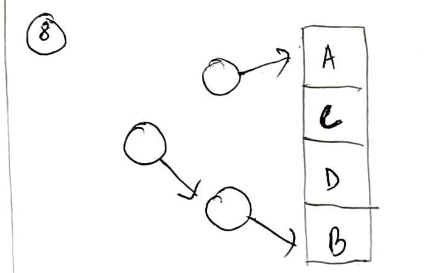
CMP-MISS (B)

⑥ 

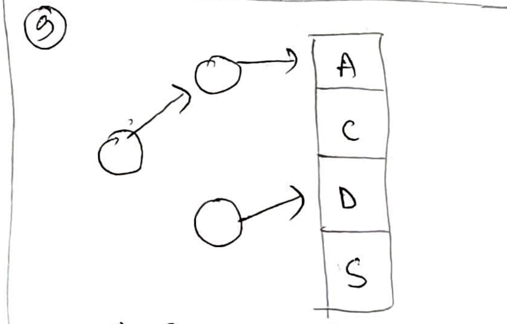
HIT (A)

⑦ 

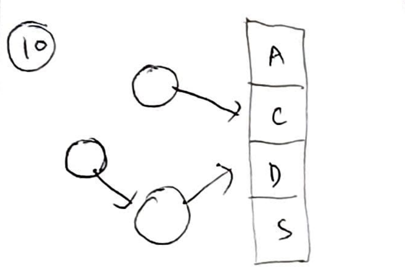
CMP-MISS (D)

⑧ 

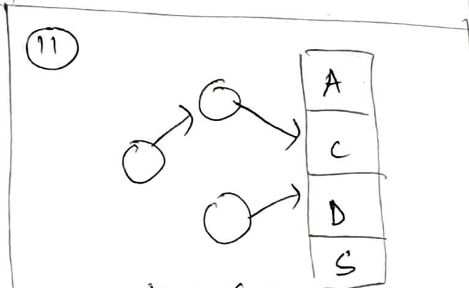
CMP-MISS (C)

⑨ 

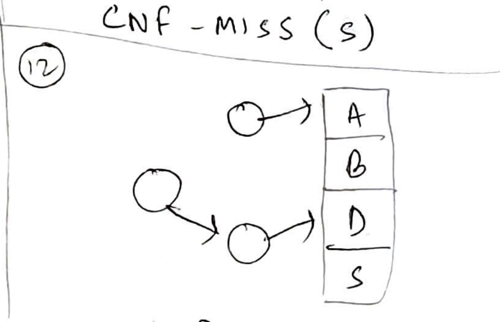
CNF-MISS (S)

⑩ 

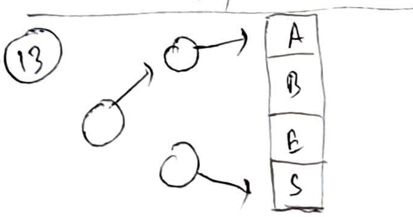
HIT (A)

⑪ 

HIT (S)

⑫ 

CNF-MISS (B)

⑬ 

CMP-MISS (E)

So, no. of compulsory miss (CMP-MISS) = 7

no. of conflict miss (CNF-MISS) = 2

So $\boxed{\text{golden-ratio of set } n = \frac{7}{2} = 3.5}$

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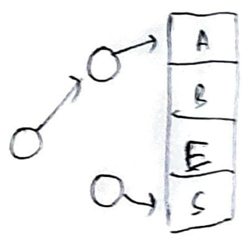
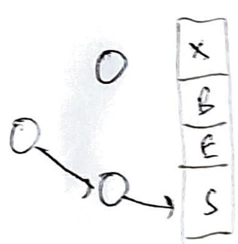
2) (contd.) Let us observe the latest condition (state) of the pseudo-LRU
(b) after processing A, R, S, R, B, A, D, C, S, A, S, B, E, #, $.



Now it has been said that '#' resulted in a CNF-miss.
Also, '@' resulted in replacement of block 'S'
Now we have to give all possible values of # and $ s.t access to '$' is a hit.

Now # can have values: {R, D, C} (as they have occurred earlier).
s.t # results in CNF-M
Now let's say # has one of these values; then state of LRU tree is



where $X = \{R, D, C\}$.
We can clearly see that S be replaced by '@' iff it is a miss.

Since $ is a hit it is one among these sets. (A is pseudo-lru-victim)
$\$ = \{C, B, E, S\}$ if # is 'C'
$= \{D, B, E, S\}$ if # is 'D'
$= \{R, B, E, S\}$ if # is 'R'

- Now since # is a hit @ has to be in the complement set of state after # (i.e same as $). So @ will be one of {A, D, R} if # is 'C' and {A, C, R} is # is 'D' and {A, C, D} if # is 'R'.

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3) In this question we have been asked to fill up the time of issue, execution, MEM-access, CDB write and commit for 2 iterations of loop of code given below.

We assume that ROB size = 6; and latencies of diff. functional units as given in the question.

Iter. no.	Instruction	Issue	Execute	MEM access	CDB write	Commit
1.	LD F1, 8(R0)	1	2	3	4	5
1.	LD F2, 0(Rx)	2	3	4	5	6
1.	MUL.D F3, F2, F1	3	6 (F2 is required)	—	10	11
1.	ADD.D F5, F5, F3	4	11	—	13	14
1.	S.D F5, 0(Ry)	5	6	15	—	15
1.	SUB Ry, Ry, #8	6	7	—	8	16
1.	SUB Rx, Rx, #8	7	8	—	9	17
1.	BNEZ Rx, loop	8	10	—	11	18
2.	L.D F2, 0(Rx)	12	13	14	15	19
2.	MUL.D F3, F2, F1	15	16	—	20	21
2.	ADD.D F5, F5, F3	16	21	—	23	24
2.	S.D F5, 0(Ry)	17	18	25	—	25
2.	SUB Ry, Ry, #8	18	19	—	21 (since at 20 CDB collision)	26
2.	SUB Rx, Rx, #8	19	21	—	22	27
2.	BNEZ Rx, loop	20	23	—	24	28

(The columns op1 and op2 are included in next page)

Here instead of 20, we have CDB write at CC 21 because of clash of 2 CDB write at same time.

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(3.) Now the columns <u>operand 1</u> and <u>operand 2</u> would look as follows; in order :-

1.

Iter no	operand 1	operand 2
1.	Imm	RF
2.	Imm	RF
3.	CDB	CDB
4.	RF	ROB
5.	RF	~~ROB~~ RF

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4) So we have been asked to consider two different cache organizations X and Y.

X :- 16 KB IC, and 16 KB D.C.

Miss rate of IC = ~~0.064~~, 0.0064 and miss rate of DC = 0.0647

Now AMAT = HT + (Miss rate) × (Miss Penalty).

Now we need to calculate the avg. miss rate of (X).

So miss rate of (X) = (0.0064 + 0.33 × 0.0647)

= 0.0277

Now lets calculate the AMAT for both X and Y.

$$(AMAT)_X = HT + (MR_X \times MP)$$

$$= 1 + (0.0277 \times 50) = 2.385 \text{ cc}$$

$$(AMAT)_Y = HT + (MR_Y \times MP)$$

$$= 1 + (0.0199 \times 50) = 1.995 \text{ cc}$$

So organization Y is better than X.