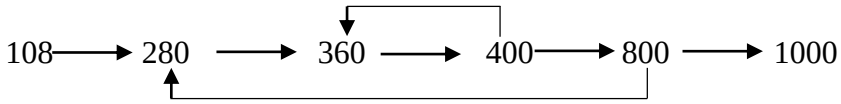
IIT Guwahati - Department of Computer Science & Engineering

CS 223- Computer Organization & Architecture –Quiz 3 (10.04.2021)

Submission Link:
https://forms.office.com/Pages/ResponsePage.aspx?id=jacKheGUxkuc84wRtTBwHANSILeDKUNOi1YB2VJD6t1UNTE0MFpTNTBJRDlZMEo2STI5MEVETTBENy4u

Answer all the questions. Mark the correct question number. Show calculations and diagrams wherever necessary. Q1 carries 10 marks, Q2 and Q3 carry 8 marks each and Q4 carries 4 marks. [Max: 30 marks, Duration 90 minutes]

1. The memory of a computer is byte-addressable, and the word length is 8 bits. A program consists of a pair of nested loops; a small inner loop (executed 20 times for each outer loop iteration) inside a larger outer loop (executed 10 times). The general structure of the program is given in the figure below. The decimal memory addresses shown delineate the location of the two loops and the beginning and end of the total program. All memory locations in the various sections of the program addresses, 108-279, 280-359, 360-400, 401-800, 801-1000 contain instructions to be executed in straight-line sequencing. Instructions at addresses 400 and 800 are conditional jumps. The program is to be run on a computer that has an instruction cache of 1 KB capacity, organized in the direct-mapped manner with a block size of 16 B. The miss penalty in the instruction cache is 80*x* clock cycles, where *x* is the hit time of the cache. Assume the cache is initially empty, Compute the miss-rate of the cache and the total time needed for instruction fetching in the execution of the entire program.



2. Consider a 4-way set associative cache that uses pseudo LRU block replacement policy. Assume all the cache blocks are initially empty and filling up of empty blocks in a given cache set happens from way-0 to way-3. Consider the following 13 block numbers (excluding #, $, and @) all mapped to set n given in the order of arrival. A, R, S, R, B, A, D, C, S, A, S, B, E, #, $, @.

(a) Find the golden miss ratio of set n, if it is defined as the ratio of compulsory miss to conflict miss in the above sequence of 13 block requests.

(b) Consider the 14^{th}, 15^{th} and 16^{th} requests #, $, and @, respectively given above mapped to set n. If access to # resulted in a conflict miss, and access to @ resulted in replacement of block 'S', give the set of all possible values that # and $ can have such that request to $ is a hit.

3. Consider a dynamically scheduled single-issue pipeline with speculation using a branch predictor that always predicts the branch as taken. ROB has a capacity of 6 entry. The pipeline has one floating point unit, one memory unit (L.D /S.D), and one integer unit. Branch is also scheduled in the integer unit and branch outcome is written to CDB to initiate committing in ROB. The floating-point unit takes 4 cycles for multiplication and 2 cycles for addition and they are fully pipelined with normal operand forwarding. Even though the floating-point unit is capable of doing two operations, it can initiate only one operation in a given clock cycle. The integer unit takes 1 cycle and supports full operand forwarding.

Memory access of a load operation is done in the immediate cycle after address computation. Stores access memory only upon commit. Assume you have enough reservation station entries. At most one CDB write can happen in a cycle.

```
        L.D     F1, 8 (R0)
loop:   L.D     F2, 0 (Rx)
        MUL.D   F3, F2, F1
        ADD.D   F5, F5, F3
        S.D     F5, 0 (Ry)
        SUB     Ry, Ry, #8
        SUB     Rx, Rx, #8
        BNEZ    Rx,  loop
```

Fill up the location of operand, time of issue, execution, MEM access, CDB write and commit for 2 iterations of the loop for the code given above. *(Use the following table format)*

Iter No	Instruction	Operand 1	Operand 2	Issue	Execute	MEM Access	CDB Write	Commit
1	L.D F1, 8 (R0)	Imm	RF	1	2	3	4	5
1	L.D F2, 0 (Rx)	Imm	RF	2	3	4	5	6
1	MUL.D F3, F2, F1	CDB	CDB	3				

4. Consider two different cache organizations X and Y that can be attached to a processor. X has 16KB Instruction cache (IC) and 16KB Data cache (DC). Y has 32KB Unified cache (UC) with a single port. Miss rates of IC and DC are 0.64% and 6.47% respectively. Aggregate miss rate of UC is 1.99%. Assume that an application has 33% of data access operations. Hit time is 1 cycle and miss penalty is 50 cycles. By calculating AMAT, decide which organization is better for this application? As a further upgrade, lets us consider another organization Z wherein the UC is a dual ported cache, but requires 1.2 cycle hit time. Is Z better? Support your answer.