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**TERM PROJECT**

**A) Overview of the design with states**

The states are defined with parameter, and they were each given a number as a representative.

(IDLE =0, BUSY =1, REJECTED=2, RINGING =3, CALLER =4, COST =5)

Other than current state and next state, three additional registers were defined that were to be utilized in the following steps.

Following this, an always block was created to apply counter required states where counter keeps the track of clock cycles. After that, a second always block was used to define current state-next state relation. This was followed by the third always block which shows the state connections and how transitions happen according to the input values. Lastly a long always block was put in use to set output values sentMsg and statusMsg in the time frame of each state.

**B) Simulation results**

These are simulation results of first test file that was uploaded to sucourse+. (the one with “term project” input)

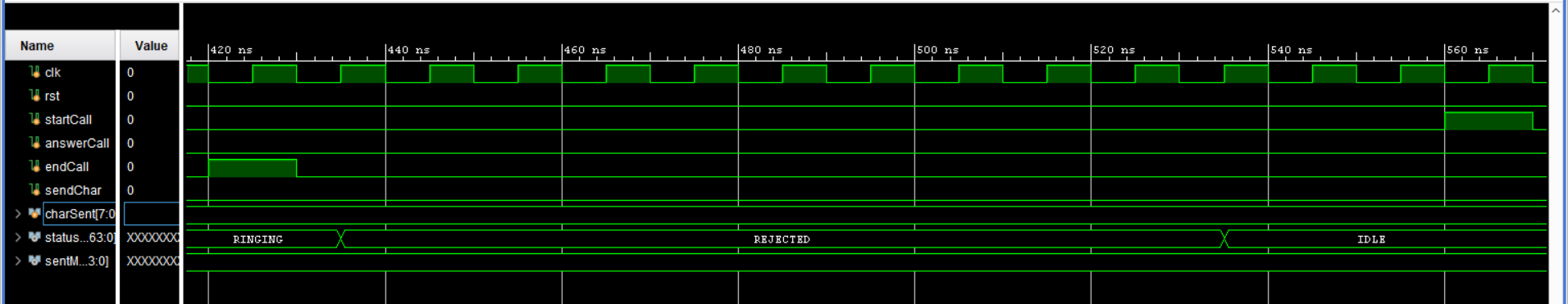


metin, ekran, ekran görüntüsü içeren bir resim

Açıklama otomatik olarak oluşturuldu

metin, ekran, ekran görüntüsü içeren bir resim

Açıklama otomatik olarak oluşturuldu

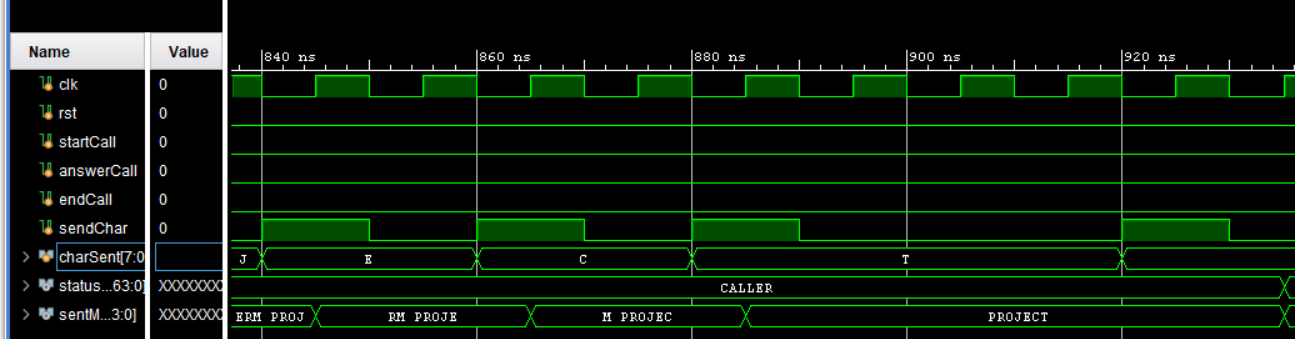


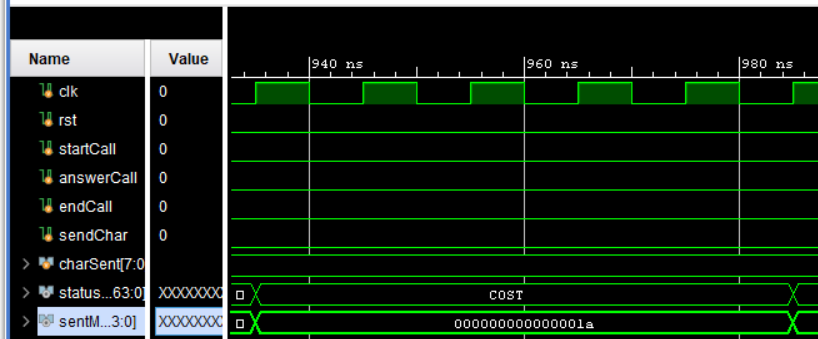
metin, ekran, iç mekan içeren bir resim

Açıklama otomatik olarak oluşturuldu

metin, yeşil, ekran, ekran görüntüsü içeren bir resim

Açıklama otomatik olarak oluşturuldu





(in the last screenshot, sentMsg radix was switched to hexadecimal from ASCII, the simulation was later followed by idle state until 1500ns which was set by me)

**C) Synthesis Results**

tablo içeren bir resim

Açıklama otomatik olarak oluşturuldu