Eric Krause

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Education

M.S., Computer Engineering **GPA: 3.86/4.00**
Portland State University, Portland Oregon – Expected Graduation: 12/2013 *2011-Current*

Post-Bac, Electrical/Computer Engineering **GPA: 3.88/4.00**
Portland State University, Portland Oregon *2010-2012*

B.A., Environmental Studies **GPA: 3.80/4.00**
University of Oregon, Eugene Oregon *2005-2009*

Relevant Coursework

- Microprocessor Design
- Superscalar Processor System Architecture
- Parallel Computing Architecture
- SoC Design with FPGAs
- Embedded Systems with FPGAs
- Embedded Software Programming

Technical Skills

- **Proficient Languages:** Verilog, C, Assembly (ARM, z80, MIPS, PicoBlaze)
- **Familiar Languages:** C++, SystemVerilog, Python, Bash, Java (for Android Development)
- **Hardware:** RTL design and debug, digital design and SoC/embedded system design and debug with FPGAs. Experience using test equipment in a laboratory setting to verify and debug digital designs.
- **Software:** Experience with Mac/Windows/Linux. Professional experience with Xilinx Toolchain (ISE, Lab Tools, EDK, SDK). Limited experience with GNU tools (Make, GCC) and VCS (git).

Experience

IEEE Computer Engineering Tutor – Portland State University – *Portland, Oregon* *9/2012 - Current*
- Instructed students on a variety Computer Engineering topics, including programming and digital design.
- Adapted teaching strategies the unique background and abilities level of each student.

Platform Deployment Tech Volunteer – Free Geek – *Portland, Oregon* *9/2013 - Current*
- Assembled and repaired desktops, workstations, and servers.
- Tested and debugged hardware peripherals for reuse or recycling.
- Administrated installation of Linux OS and other software.

Data Center Group Intern – Intel Corporation – *Hillsboro, Oregon* *3/2011 - 9/2013*
- Wrote RTL and testbenches for an FPGA-based DDR3 Memory Error Injector (MEI) interposer.
- Developed automated testing CLI utilities in Python to simplify testing of MEI on Intel server platforms.
- Optimized existing FPGA RTL designs to improve timing and enhance features as per customer needs.
- Tested memory error injection functionality of MEI and memory error detection on Intel server platforms.
- Received professional award for identifying, debugging and repairing a critical functionality in a key product.

Microarchitecture Researcher – Portland State University – *Portland, Oregon* *3/2013*
- Implemented simulation of branch predictor, branch target buffer as a term project for Comp. Architecture.
- Designed N-way associative cache, Return Address Stack, and Fully-Associative cache structures in C++ .
- Evaluated performance of many design iterations using instruction traces from an unknown processor.

Embedded Systems Engineer – Portland State University – *Portland, Oregon* *12/2012*
- Designed, assembled, and programmed an autonomous, color-seeking robot controlled by an FPGA SoC.
- Implemented computer vision, environmental awareness, and behavioral control using Verilog and ASM.

Honors

Member and Organizer – Etta Kappa Nu (HKN) – *IEEE Honors Society* *12/2012 - Current*
- Planed and organized events to promote HKN at Portland State University.

Scholarship Recipient – Ford Family Foundation – *Academic Scholarship* *8/2005 and 8/2012*
- Inducted into Ford Family Foundation Scholarship program in 2005 for leadership and academic excellence.
- Awarded additional Graduate Scholarship in 2012 following academic success of undergraduate work.