Eric Krause

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Objective

Seeking full-time engineering position in the fields of Computer Architecture and/or Embedded Systems

Education

M.S., Computer Engineering **GPA: 3.86/4.00**
Portland State University *2011-2013*

Post-Bac, Electrical/Computer Engineering **GPA: 3.88/4.00**
Portland State University *2010-2012*

B.A., Environmental Studies **GPA: 3.80/4.00**
University of Oregon *2005-2009*

Technical Skills

Proficient Languages: Verilog, C, Assembly (ARM, z80, MIPS, PicoBlaze)

Familiar Languages: C++, SystemVerilog, Python, Bash Script, LaTeX, AHK, Java (for Android Development)

Hardware: RTL design and debug, digital design and SoC/embedded system design and debug with FPGAs. Comfortable using test equipment in a laboratory setting to verify and debug digital designs.

Software: Relatively OS agnostic; equal experience with Mac/Windows/Linux. Professional experience with Xilinx Toolchain (ISE, Lab Tools, EDK, SDK). Limited experience with GNU tools (Make, GCC) and VCS (git).

Academic Projects

- **FPGA-Based Color-Tracking Robot (Verilog, PicoBlaze)** http://tinyurl.com/color-fpga-bot
  I worked with a partner to design and built an autonomous color-seeking robot for the final project in an SoC with FPGAs course. The robot was controlled with a combination of custom Verilog code and a Picoblaze soft-core microcontroller instantiated inside the FPGA on a Spartan-6E development board. This robot used a CMUCam4 camera for vision and several proximity sensors for environmental awareness. It could be trained to any color, which it would then seek out and follow. In a classwide competition, this design was awarded 1^{st} place for best term project by the instructors.
- **Branch Predictor/BTB simulation (C)** https://github.com/rattboi/flanders_ece486
  I worked with a partner to develop a branch predictor and branch target buffer simulation as a final project in a Computer Architecture course. Our algorithm was tested against numerous traces from an unknown processor and obtained the 3^{rd} best performance in the class.
- **Microprocessor Cache Simulation (Verilog)** https://github.com/ekrause/0xBEEFA55
  I developed a split-level L1 cache simulator with a small team for the final project of a Microprocessor Design course. It read in a text file of sample trace data, and displayed cache hit/miss statistics at completion of the trace. We were later contacted by the professor and our source code was incorporated into the course material.

Honors, Awards, and Volunteering

- **Etta Kappa Nu (HKN)** http://web.cecs.pdx.edu/~eta/
  IEEE Honors Society. Limited to top 25% of Department.
- **Golden Key International Honour Society** https://www.goldenkey.org/
  Member since 2008.
- **Ford Family Foundation Scholarships: Undergraduate/Graduate** http://www.tfff.org/
  I was one of fewer than 100 Scholars in Oregon to be inducted into the prestigious Ford Family Family Foundation program in 2005. In 2012, I was awarded the Ford Family Foundation Graduate scholarship, following my academic success at University of Oregon (B.A.) and my Portland State University (Post-Bac).
- **Intel Internal Recognition** http://db.tt/0nqPo3Yf
  During my first engineering internship, I was recognized for my "excellent creative and technical abilities", after identifying, debugging and repairing a critical functionality in our key product in 2013.

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Honors, Awards, and Volunteering (Continued)

- **IEEE ECE Tutor** `http://www.pdx.edu/ece/tutoring-resources`
  I am an IEEE Tutor for lower-level ECE courses, specializing in digital logic, programming, and digital design.
- **FreeGeek Volunteer** `http://www.freegeek.org/`
  I am a regular volunteer at FreeGeek, a Portland nonprofit dedicated to the mission of recycling technology and providing affordable access to computers.

Work History

Intel Corporation
2011-2013: *Technology Solutions Enabling Intern*
- Testing/Verification/Development of FPGA-based Memory Error Injector (MEI)
- Design and development of many CLI utilities for testing, automation, and customer use.
- Development of new features in RTL.
- Optimization of existing design and synthesis of new modules
- Design of testbenches for verification of features implemented in future revisions

Umpqua Bank
2010-2011: *Financial Services Representative*
- Business development, community presentations.
- Loan applications, sales, and financial transactions.

Oregon Community Credit Union
2009-2010: *Sales Associate*
- Loan applications, audits (security, policy, cash verification), and financial transactions.

References

Isaac Itotia	Technology Solutions Enabling (Intel)	`isaac.itotia@intel.com`	(651) 278-5309
Mark Faust	Professor (Portland State University)	`faustm@pdx.edu`	(503) 725-5412
Roy Kravitz	Professor/Director (Portland State University)	`roy.kravitz@ece.pdx.edu`	(503) 913-1678