

Analog Engineer's

Circuit Cookbook: Amplifiers



TEXAS INSTRUMENTS

Introduction

The *Analog Engineer's Circuit Cookbook: Amplifiers* provides amplifier subcircuit ideas that you can quickly adapt to meet your specific system needs. Each circuit is presented as a “definition by example.” It includes step-by-step instructions, like a recipe, with formulas enabling you to adapt the circuit to meet your design goals. Additionally, all circuits are verified with SPICE simulations.

We've provided at least one recommended amplifier for each circuit, but you can swap it with another amplifier if you've found one that's a better fit for your design. You can search our portfolio at ti.com/amplifiers.

Our circuits require a basic understanding of amplifier concepts. If you're new to amplifier design, we highly recommend completing our [TI Precision Labs \(TIPL\) training series](#). TIPL includes courses on introductory topics, such as device architectures, as well as advanced, application-specific problem-solving, using both theory and practical knowledge. Check out our curriculum for operational amplifiers (op amps), analog-to-digital converters (ADCs) and more at ti.com/precisionlabs.

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Analog Engineer's Circuit

Integrator Circuit

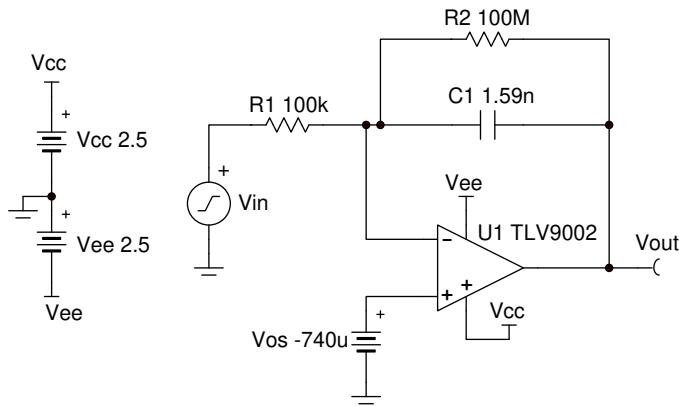


Design Goals

Input			Output		Supply	
f _{Min}	f _{0dB}	f _{Max}	V _{oMin}	V _{oMax}	V _{cc}	V _{ee}
100 Hz	1 kHz	100 kHz	-2.45 V	2.45 V	2.5 V	-2.5 V

Design Description

The integrator circuit outputs the integral of the input signal over a frequency range based on the circuit time constant and the bandwidth of the amplifier. The input signal is applied to the inverting input so the output is inverted relative to the polarity of the input signal. The ideal integrator circuit will saturate to the supply rails depending on the polarity of the input offset voltage and requires the addition of a feedback resistor, R₂, to provide a stable DC operating point. The feedback resistor limits the lower frequency range over which the integration function is performed. This circuit is most commonly used as part of a larger feedback/servo loop which provides the DC feedback path, thus removing the requirement for a feedback resistor.



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Design Notes

1. Use as large of a value as practical for the feedback resistor.
2. Select a CMOS op amp to minimize the errors from the input bias current.
3. The gain bandwidth product (GBP) of the amplifier will set the upper frequency range of the integrator function. The effectiveness of the integration function is usually reduced starting about one decade away from the amplifier bandwidth.
4. An adjustable reference needs to be connected to the non-inverting input of the op amp to cancel the input offset voltage or the large DC noise gain will cause the circuit to saturate. Op amps with very low offset voltage may not require this.

Design Steps

The ideal circuit transfer function is given below.

$$V_{\text{out}} = -\frac{1}{R_1 \times C_1} \int_0^t V_{\text{in}}(t) dt$$

1. Set R_1 to a standard value.

$$R_1 = 100\text{k}\Omega$$

2. Calculate C_1 to set the unity-gain integration frequency.

$$C_1 = \frac{1}{2 \times \pi \times R_1 \times f_{0\text{dB}}} = \frac{1}{2 \times \pi \times 100\text{k}\Omega \times 1 \text{ kHz}} = 1.59\text{nF}$$

3. Calculate R_2 to set the lower cutoff frequency a decade less than the minimum operating frequency.

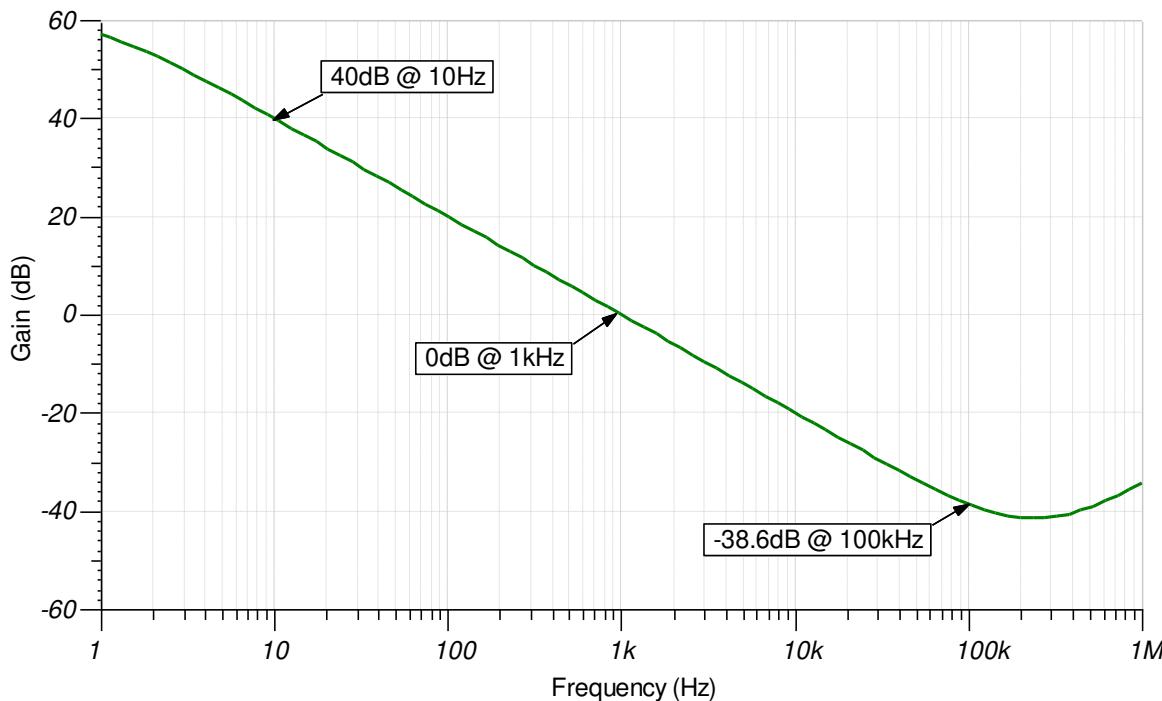
$$R_2 \geq \frac{10}{2 \times \pi \times C_1 \times f_{\text{Min}}} \geq \frac{10}{2 \times \pi \times 1.59\text{nF} \times 10\text{Hz}} \geq 100\text{M}\Omega$$

4. Select an amplifier with a gain bandwidth at least 10 times the desired maximum operating frequency.

$$\text{GBP} \geq 10 \times f_{\text{Max}} \geq 10 \times 100\text{kHz} \geq 1 \text{ MHz}$$

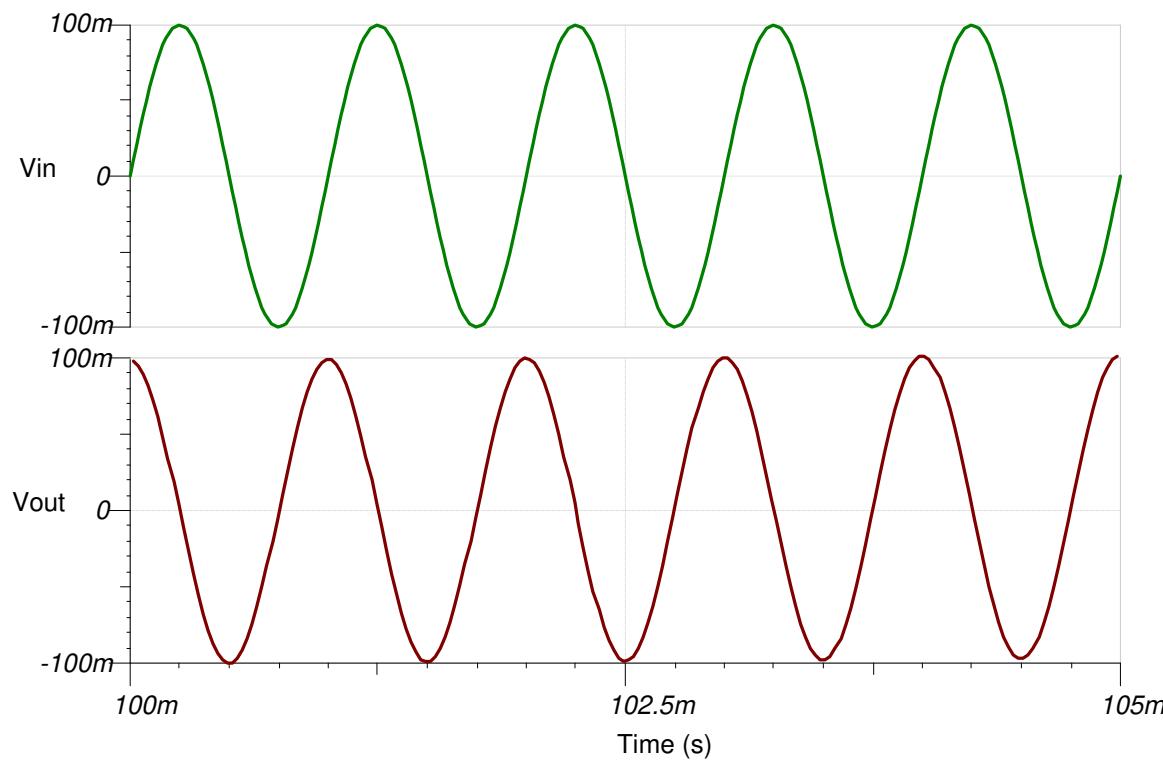
Design Simulations

AC Simulation Results

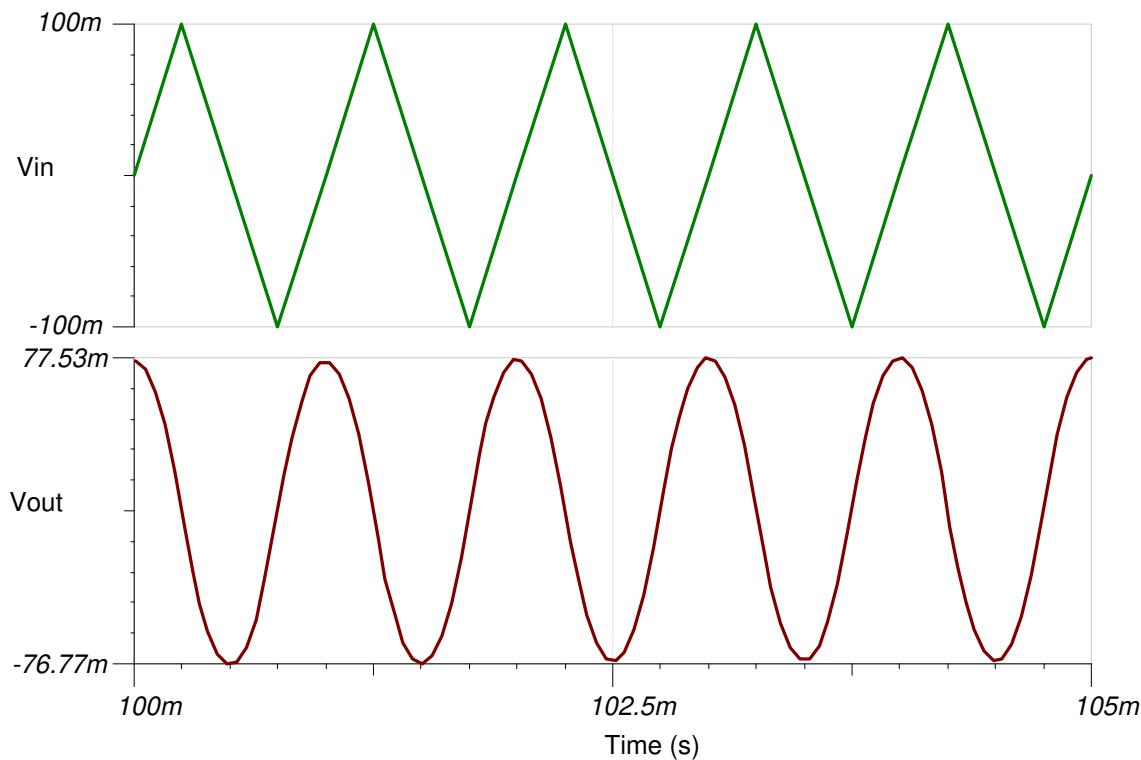


Transient Simulation Results

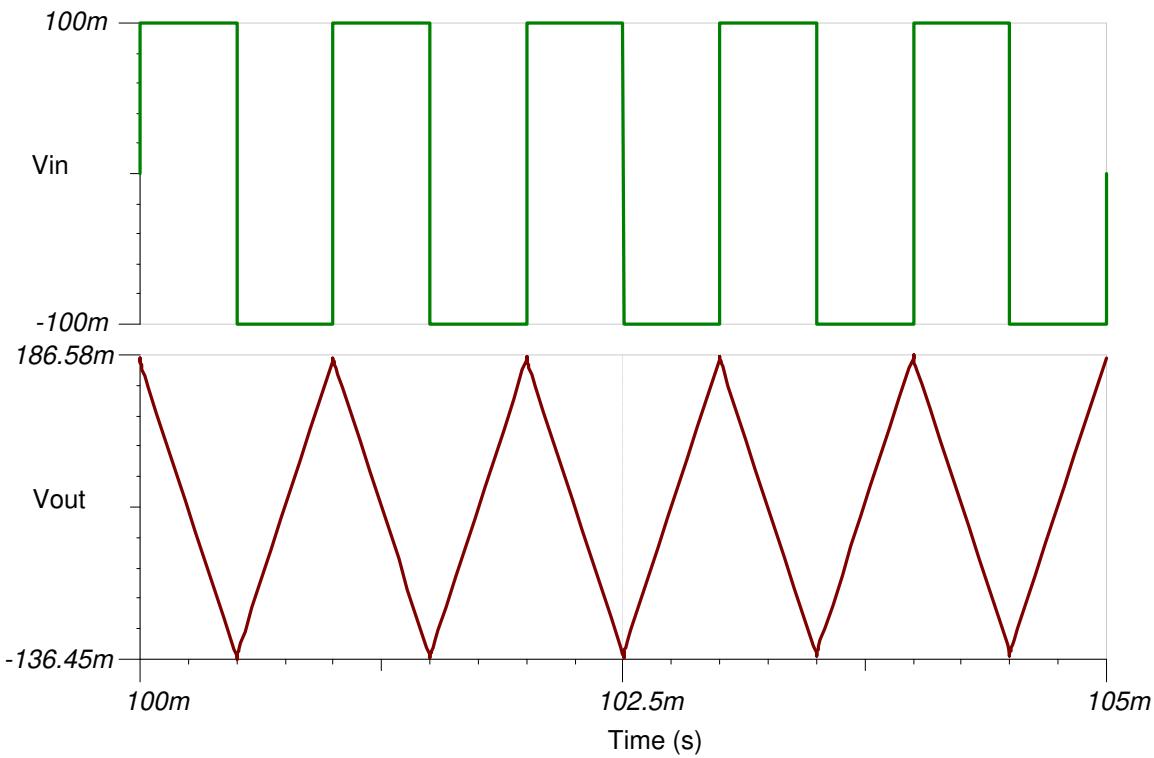
A 1 kHz sine wave input yields a 1 kHz cosine output.



A 1 kHz triangle wave input yields a 1 kHz sine wave output.



A 1 kHz square wave input yields a 1 kHz triangle wave output.



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC496](#).

See [TIPD191](#).

Design Featured Op Amp

TLV9002	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.4 mV
I_q	0.06 mA
I_b	5 pA
UGBW	1 MHz
SR	2 V/ μ s
#Channels	1, 2, and 4
TLV9002	

Design Alternate Op Amp

OPA376	
V_{cc}	2.2 V to 5.5 V
V_{inCM}	(V_{ee} -0.1 V) to (V_{cc} -1.3 V)
V_{out}	Rail-to-rail
V_{os}	0.005 mV
I_q	0.76 mA
I_b	0.2 pA
UGBW	5.5 MHz
SR	2 V/ μ s
#Channels	1, 2, and 4
OPA376	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 22, 2018 to January 31, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.....1

Analog Engineer's Circuit

Buffer (Follower) Circuit

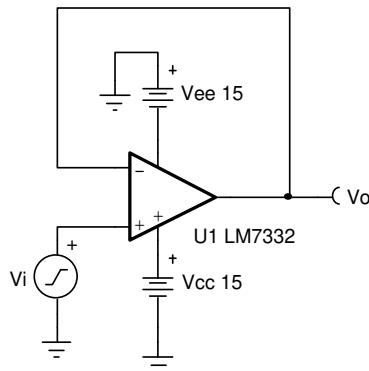


Design Goals

Input		Output		Freq.	Supply	
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	f	V_{cc}	V_{ee}
-10 V	10 V	-10 V	10 V	100 kHz	15 V	-15 V

Design Description

This design is used to buffer signals by presenting a high input impedance and a low output impedance. This circuit is commonly used to drive low-impedance loads, analog-to-digital converters (ADC) and buffer reference voltages. The output voltage of this circuit is equal to the input voltage.



Design Notes

1. Use the op-amp linear output operating range, which is usually specified under the A_{OL} test conditions.
2. The small-signal bandwidth is determined by the unity-gain bandwidth of the amplifier.
3. Check the maximum output voltage swing versus frequency graph in the data sheet to minimize slew-induced distortion.
4. The common mode voltage is equal to the input signal.
5. Do not place capacitive loads directly on the output that are greater than the values recommended in the data sheet.
6. High output current amplifiers may be required if driving low impedance loads.
7. For more information on op-amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth, see the *Design References* section.

Design Steps

The transfer function for this circuit follows:

$$V_o = V_i$$

1. Verify that the amplifier can achieve the desired output swing using the supply voltages provided. Use the output swing stated in the A_{OL} test conditions. The output swing range of the amplifier must be greater than the output swing required for the design.

$$-14V \leq V_o \leq 14V$$

- The output swing of the LM7332 using ± 15 V supplies is greater than the required output swing of the design. Therefore, this requirement is met.
 - Review the Output Voltage versus Output Current curves in the product data sheet to verify the desired output voltage can be achieved for the desired output current.
2. Verify the input common mode voltage of the amplifier will not be violated using the supply voltage provided. The input common mode voltage range of the amplifier must be greater than the input signal voltage range.

$$-15.1 \text{ V} \leq V_{icm} \leq 15.1 \text{ V}$$

- The input common-mode range of the LM7332 using ± 15 V supplies is greater than the required input common-mode range of the design. Therefore, this requirement is met.
3. Calculate the minimum slew rate required to minimize slew-induced distortion.

$$SR > 2 \times \pi \times V_p \times f = 2 \times \pi \times 10V \times 100\text{kHz} = 6.28\text{V}/\mu\text{s}$$

- The slew rate of the LM7332 is $15.2 \text{ V}/\mu\text{s}$. Therefore, this requirement is met.
4. Verify the device will have sufficient bandwidth for the desired output signal frequency.

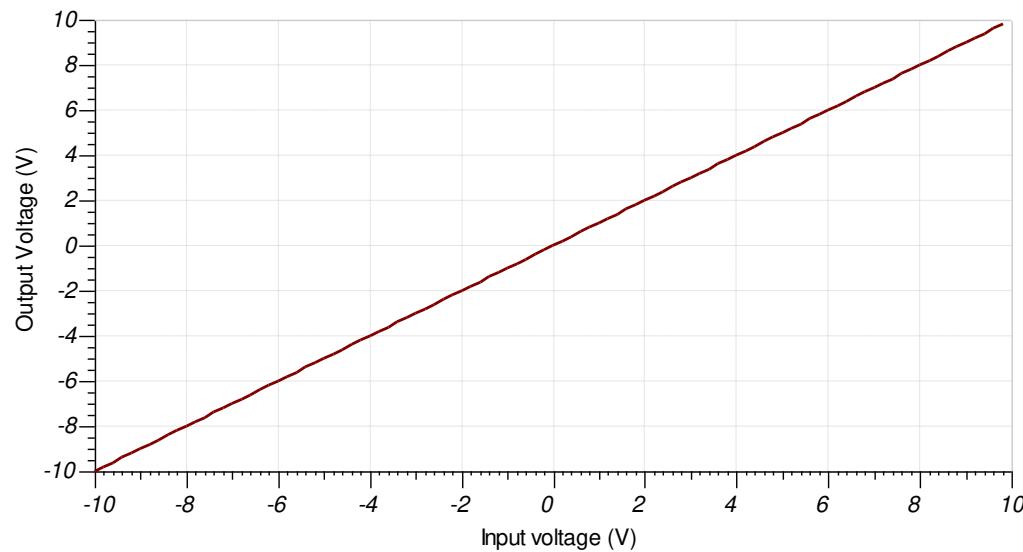
$$f_{signal} < f_{unity}$$

$$100\text{kHz} < 7.5\text{MHz}$$

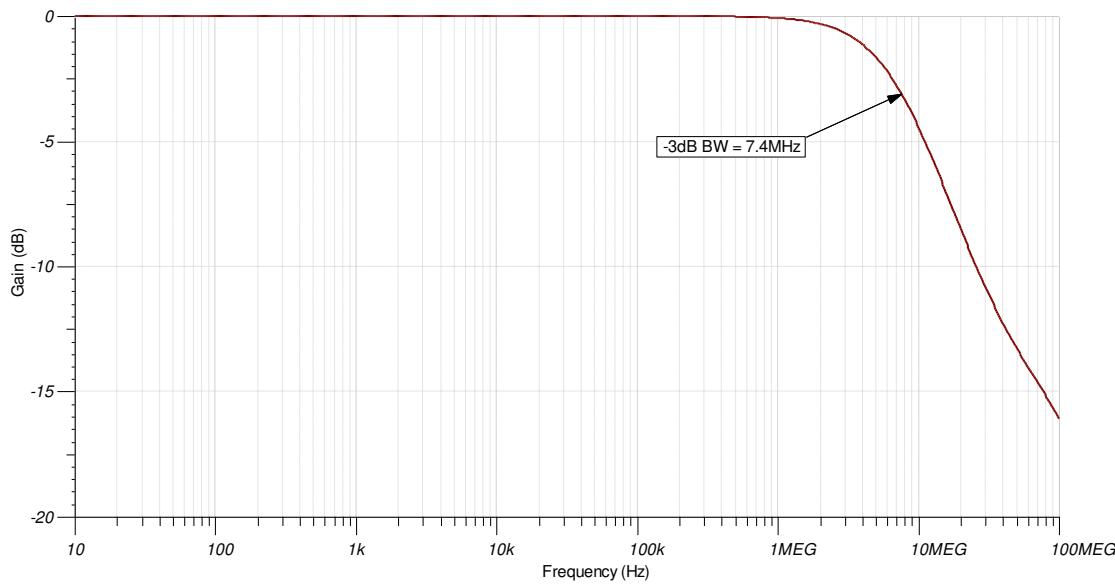
- The desired output signal frequency is less than the unity-gain bandwidth of the LM7332. Therefore, this requirement is met.

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See the [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

For more information, see the [Capacitive Load Drive Verified Reference Design Using an Isolation Resistor](#) TI Design.

See the circuit SPICE simulation file [SBOC491](#).

For more information on many op amp topics including common-mode range, output swing, bandwidth, slew rate, and how to drive an ADC, see [TI Precision Labs](#).

Design Featured Op Amp

LM7332	
V_{ss}	2.5 V to 32 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1.6 mV
I_q	2 mA
I_b	1 μ A
UGBW	7.5 MHz (± 5 V supply)
SR	15.2 V/ μ s
#Channels	2
LM7332	

Design Alternate Op Amp

OPA192	
V_{ss}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 μ V
I_q	1 mA
I_b	5 pA
UGBW	10 MHz
SR	20 V/ μ s
#Channels	1, 2, and 4
OPA192	

The following device is for battery-operated or power-conscious designs outside of the original design goals described earlier, where lowering the total system power is desired.

LPV511	
V_{ss}	2.7 V to 12 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.2 mV
I_q	1.2 μ A
I_b	0.8 nA
UGBW	27 KHz
SR	7.5 V/ms
#Channels	1
LPV511	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 22, 2018 to January 14, 2019	Page
Downscale title. Added LPV511 table in the <i>Design Alternate Op Amp</i> section.....	1

Analog Engineer's Circuit

Differentiator Circuit

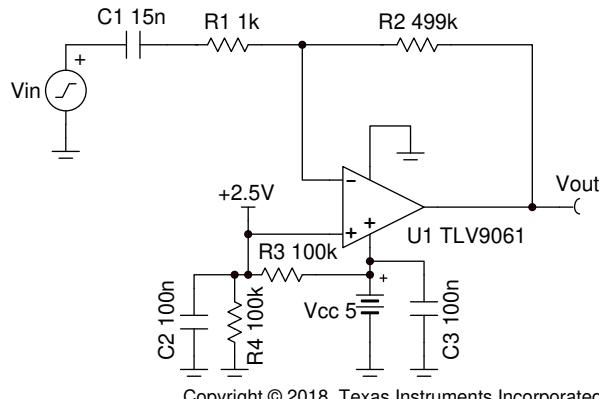


Design Goals

Input		Output		Supply		
f _{Min}	f _{Max}	V _{oMin}	V _{oMax}	V _{cc}	V _{ee}	V _{ref}
100Hz	2.5kHz	0.1V	4.9V	5V	0V	2.5V

Design Description

The differentiator circuit outputs the derivative of the input signal over a frequency range based on the circuit time constant and the bandwidth of the amplifier. The input signal is applied to the inverting input so the output is inverted relative to the polarity of the input signal. The ideal differentiator circuit is fundamentally unstable and requires the addition of an input resistor, a feedback capacitor, or both, to be stable. The components required for stability limit the bandwidth over which the differentiator function is performed.



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Design Notes

1. Select a large resistance for R₂ to keep the value of C₁ reasonable.
2. A capacitor can be added in parallel with R₂ to filter the high-frequency noise of the circuit. The capacitor will limit the effectiveness of the differentiator function starting about half a decade (approximately 3.5 times) away from the filter cutoff frequency.
3. A reference voltage can be applied to the non-inverting input to set the DC output voltage which allows the circuit to work single-supply. The reference voltage can be derived from a voltage divider.
4. Operate within the linear output voltage swing (see AOL specification) to minimize non-linearity errors.

Design Steps

The ideal circuit transfer function is given below.

$$V_{out} = -R_2 \times C_1 \times \frac{d V_{in}(t)}{d t}$$

1. Set R_2 to a large standard value.

$$R_2 = 499\text{k}\Omega$$

2. Set the minimum differentiation frequency at least half a decade below the minimum operating frequency.

$$C_1 \geq \frac{3.5}{2 \times \pi \times R_2 \times f_{min}} \geq \frac{3.5}{2 \times \pi \times 499\text{k}\Omega \times 100\text{Hz}} \geq 11.1 \text{ nF} \approx 15\text{nF} \quad (\text{Standard Value})$$

3. Set the upper cutoff frequency at least half a decade above the maximum operating frequency.

$$R_1 \leq \frac{1}{3.5 \times 2 \times \pi \times C_1 \times f_{Max}} \leq \frac{1}{7 \times \pi \times 15\text{nF} \times 2.5\text{kHz}} \leq 1.2\text{k}\Omega \approx 1 \text{ k}\Omega \quad (\text{Standard Value})$$

4. Calculate the necessary op amp gain bandwidth product (GBP) for the circuit to be stable.

$$\text{GBP} > \frac{R_1 + R_2}{2 \times \pi \times R_1^2 \times C_1} > \frac{499\text{k}\Omega + 1 \text{ k}\Omega}{2 \times \pi \times 1 \text{ k}\Omega^2 \times 15\text{nF}} > 5.3\text{MHz}$$

- The bandwidth of the TLV9061 is 10MHz, therefore this requirement is met.
- 5. If a feedback capacitor, C_F , is added in parallel with R_2 , the equation to calculate the cutoff frequency follows.

$$f_c = \frac{1}{2 \times \pi \times R_2 \times C_F}$$

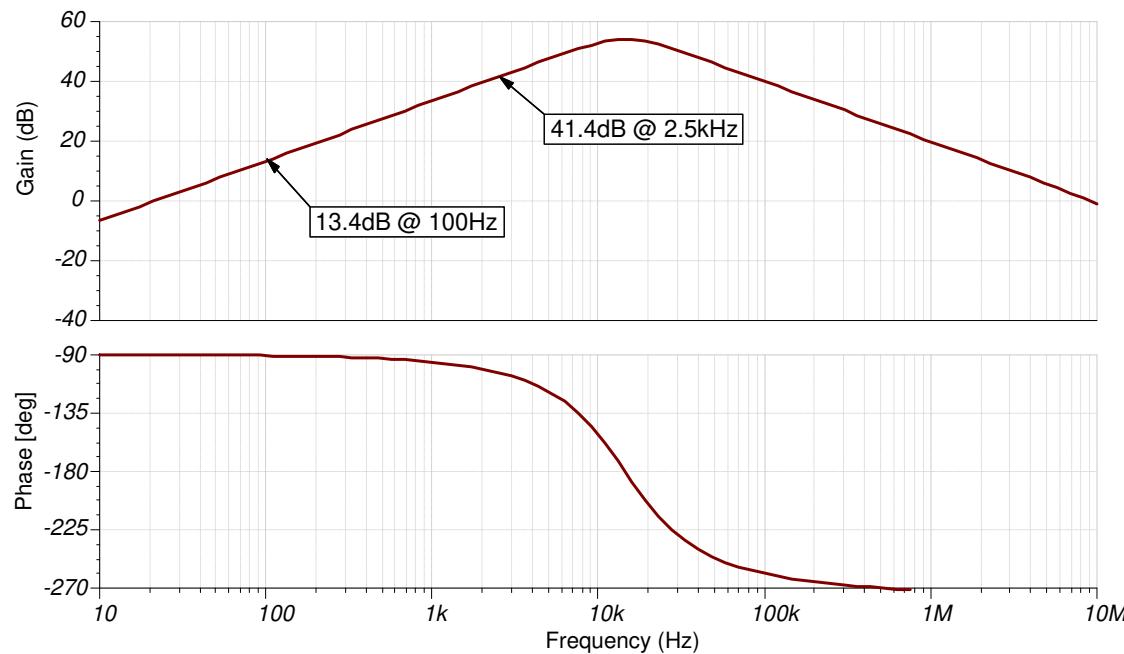
6. Calculate the resistor divider values for a 2.5-V reference voltage.

$$R_3 = \frac{V_{cc} - V_{ref}}{V_{ref}} \times R_4 = \frac{5V - 2.5V}{2.5V} \times R_4 = R_4$$

$$R_3 = R_4 = 100\text{k}\Omega \quad (\text{Standard Values})$$

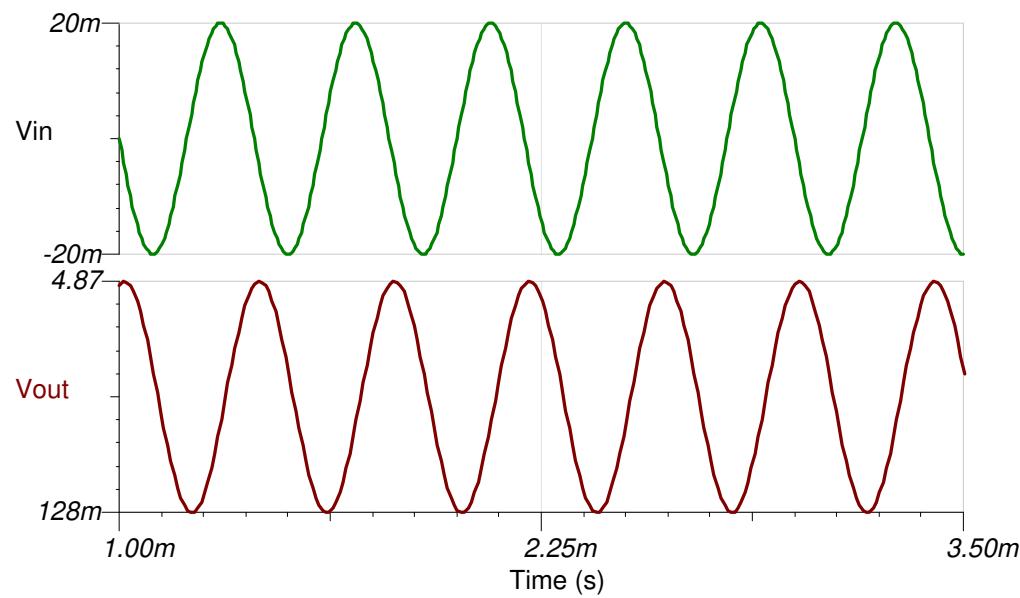
Design Simulations

AC Simulation Results

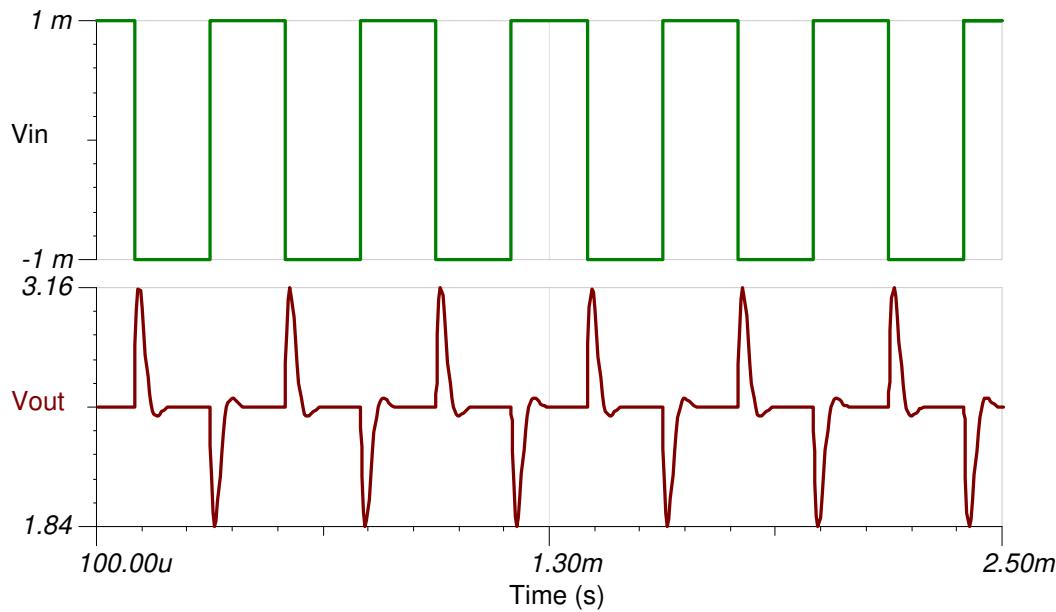


Transient Simulation Results

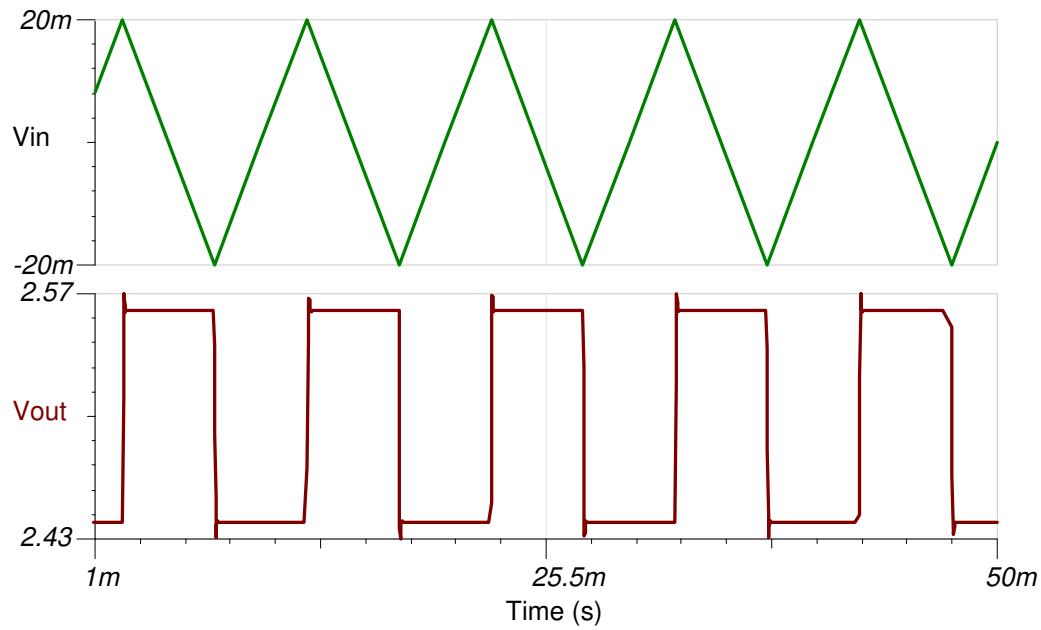
A 2.5-kHz sine wave input yields a 2.5-kHz cosine output.



A 2.5-kHz square wave input produces an impulse output.



A 100-Hz triangle wave input yields a square wave output.



Design Featured Op Amp

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC497](#).

TLV9061	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	0.538mA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/ μ s
#Channels	1, 2, 4
www.ti.com/product/tlv9061	

Design Alternate Op Amp

OPA374	
V_{cc}	2.3V to 5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1mV
I_q	0.585mA
I_b	0.5pA
UGBW	6.5MHz
SR	0.4V/ μ s
#Channels	1, 2, 4
www.ti.com/product/opa374	

Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.
B	April 2020	Changed f_{MAX} in the Design Goals from 5kHz to 2.5kHz.
C	August 2021	Updated the numbering format for tables, figures and cross-references throughout the document.

Three Op Amp Instrumentation Amplifier Circuit



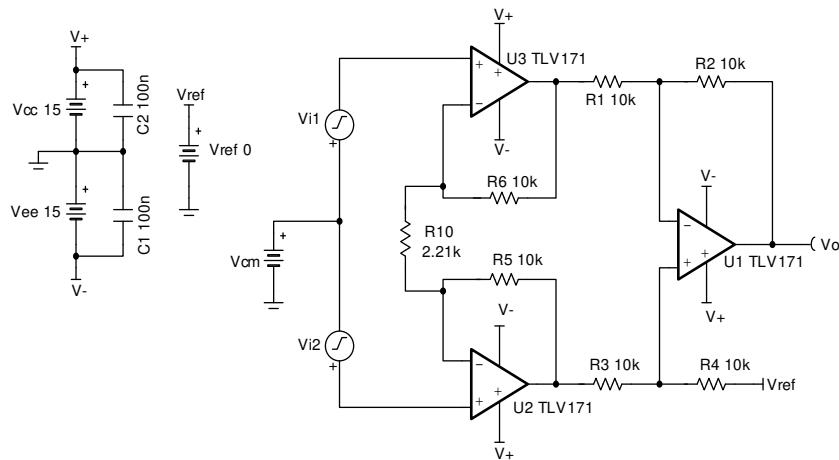
Amplifiers

Design Goals

Input V_{diff} ($V_{i2} - V_{i1}$)		Common-Mode Voltage	Output		Supply		
$V_{i \text{ diff Min}}$	$V_{i \text{ diff Max}}$	V_{cm}	$V_{o \text{Min}}$	$V_{o \text{Max}}$	V_{cc}	V_{ee}	V_{ref}
-0.5 V	+0.5 V	± 7 V	-5 V	+5 V	+15 V	-15 V	0 V

Design Description

This design uses 3 op amps to build a discrete instrumentation amplifier. The circuit converts a differential signal to a single-ended output signal. Linear operation of an instrumentation amplifier depends upon linear operation of its building block: op amps. An op amp operates linearly when the input and output signals are within the device's input common-mode and output swing ranges, respectively. The supply voltages used to power the op amps define these ranges.



Design Notes

1. Use precision resistors to achieve high DC CMRR performance
2. R_{10} sets the gain of the circuit.
3. Add an isolation resistor to the output stage to drive large capacitive loads.
4. High-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
5. Linear operation is contingent upon the input common-mode and the output swing ranges of the discrete op amps used. The linear output swing ranges are specified under the A_{ol} test conditions in the op amps data sheets.

Design Steps

- Transfer function of this circuit:

$$V_O = (V_{i2} - V_{i1}) \times G + V_{ref}$$

When $V_{ref} = 0$, the transfer function simplifies to the following equation:

$$V_O = (V_{i2} - V_{i1}) \times G$$

where

$$G = \frac{R_4}{R_3} \times \left(1 + \frac{2 \times R_5}{R_{10}} \right)$$

- Select the feedback loop resistors R_5 and R_6 :

Choose $R_5 = R_6 = 10\text{k}\Omega$ (Standard Value)

- Select R_1, R_2, R_3, R_4 . To set the Vref gain at 1 V/V and avoid degrading the instrumentation amplifier's CMRR, ratios of R_4/R_3 and R_2/R_1 must be equal.

Choose $R_1 = R_2 = R_3 = R_4 = 10\text{k}\Omega$ (Standard Value)

- Calculate R_{10} to meet the desired gain:

$$G = \frac{R_4}{R_3} \times \left(1 + \frac{2 \times R_5}{R_{10}} \right) = 10 \frac{V}{V}$$

$$R_4 = R_3 = 10\text{k}\Omega$$

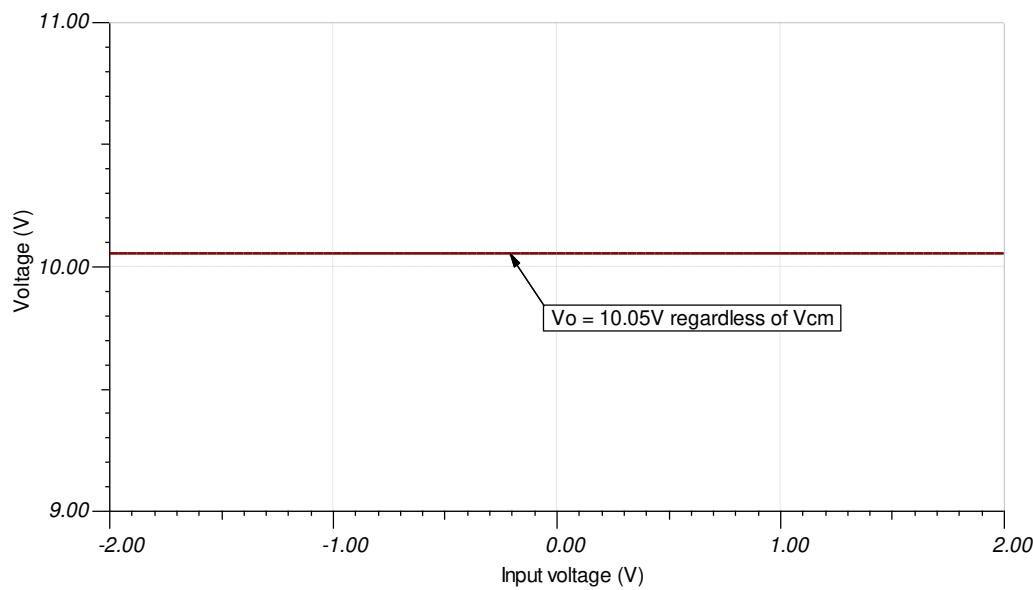
$$\rightarrow G = \left(1 + \frac{2 \times 10\text{k}\Omega}{R_{10}} \right) = 10 \frac{V}{V} \rightarrow \left(1 + \frac{20\text{k}\Omega}{R_{10}} \right) = 10 \frac{V}{V}$$

$$\frac{20\text{k}\Omega}{R_{10}} = 9 \frac{V}{V} \rightarrow R_{10} = \frac{20\text{k}\Omega}{9} = 2222.2\Omega \rightarrow R_{10} = 2.21\text{k}\Omega \text{ (Standard Value)}$$

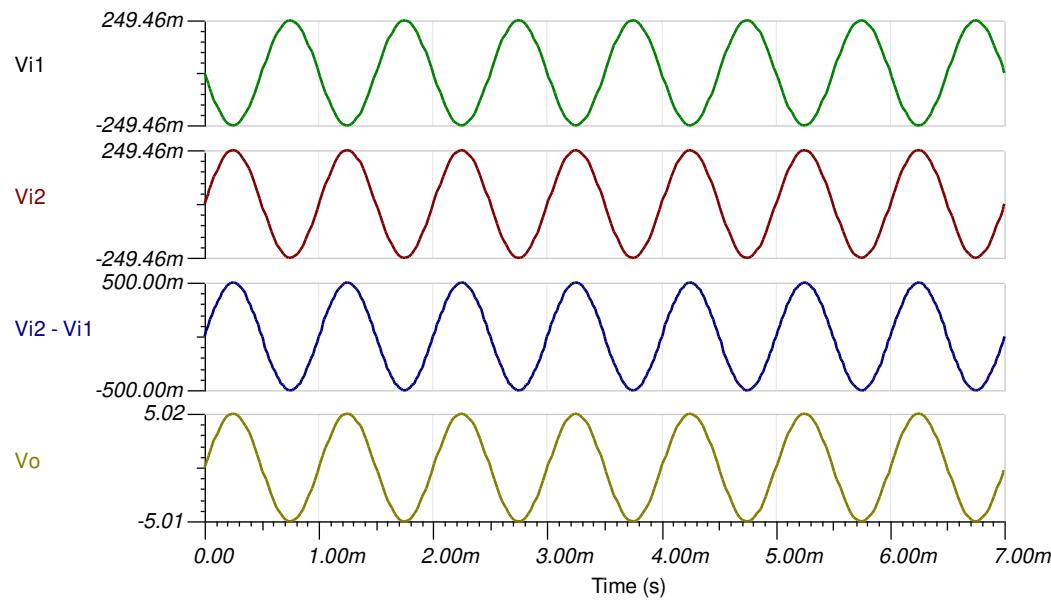
- To check the common-mode voltage range, download and install the program from reference [5]. Edit the INA_Data.txt file in the installation directory by adding the code for a 3 op amp INA whose internal amplifiers have the common-mode range, output swing, and supply voltage range as defined by the amplifier of choice (TLV172, in this case). There is no V_{be} shift in this design and the gain of the output stage difference amplifier is 1 V/V. The default supply voltage and reference voltages are $\pm 15\text{ V}$ and 0 V , respectively. Run the program and set the gain and reference voltage accordingly. The resulting V_{CM} vs. V_{OUT} plot approximates the linear operating region of the discrete INA.

Design Simulations

DC Simulation Results



Transient Simulation Results



References:

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOMAU8](#)
3. [TI Precision Labs](#)
4. [Instrumentation Amplifier \$V_{CM}\$ vs. \$V_{OUT}\$ Plots](#)
5. [Common-mode Range Calculator for Instrumentation Amplifiers](#)

Design Featured Op Amp

TLV171	
V_{ss}	4.5 V to 36 V
V_{inCM}	$(V-) - 0.1 \text{ V} < V_{in} < (V+) - 2 \text{ V}$
V_{out}	Rail-to-rail
V_{os}	0.25 mV
I_q	475 μA
I_b	8 pA
UGBW	3 MHz
SR	1.5 V/ μs
#Channels	1,2, and 4
TLV171	

Design Alternate Op Amp

	OPA172	OPA192
V_{ss}	4.5 V to 36 V	4.5 V to 36 V
V_{inCM}	$(V-) - 0.1 \text{ V} < V_{in} < (V+) - 2 \text{ V}$	$V_{ee} - 0.1 \text{ V} < V_{cc} + 0.1 \text{ V}$
V_{out}	Rail-to-rail	Rail-to-rail
V_{os}	0.2 mV	$\pm 5 \mu\text{V}$
I_q	1.6 mA	1 mA/Ch
I_b	8 pA	5 pA
UGBW	10 MHz	10 MHz
SR	10 V/ μs	20 V/ μs
#Channels	1, 2, and 4	1, 2, and 4
	OPA172	OPA192

Difference Amplifier (Subtractor) Circuit

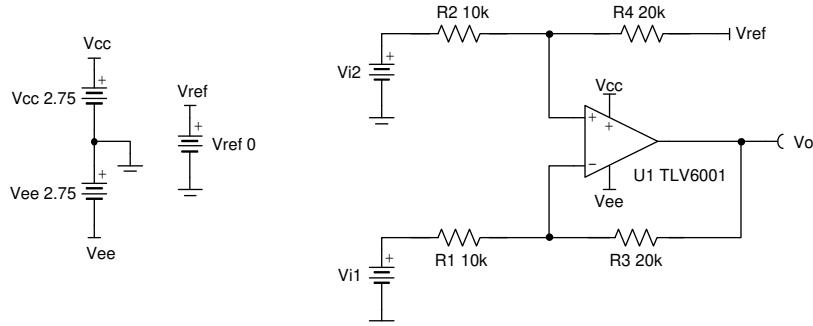


Design Goals

Input ($V_{i2}-V_{i1}$)		Output		CMRR (min)	Supply		
$V_{idiffMin}$	$V_{idiffMax}$	V_{oMin}	V_{oMax}	dB	V_{cc}	V_{ee}	V_{ref}
-1.25 V	1.25 V	-2.5 V	2.5 V	50	2.75 V	-2.75 V	0 V

Design Description

This design inputs two signals, V_{i1} and V_{i2} , and outputs their difference (subtracts). The input signals typically come from low-impedance sources because the input impedance of this circuit is determined by the resistive network. Difference amplifiers are typically used to amplify differential input signals and reject common-mode voltages. A common-mode voltage is the voltage common to both inputs. The effectiveness of the ability of a difference amplifier to reject a common-mode signal is known as common-mode rejection ratio (CMRR). The CMRR of a difference amplifier is dominated by the tolerance of the resistors.



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Design Notes

1. Use the op amp in a linear operating region. Ensure that the inputs of the op amp do not exceed the common-mode range of the device. Linear output swing is usually specified under the A_{OL} test conditions.
2. The input impedance is determined by the input resistive network. Make sure these values are large when compared to the output impedance of the sources.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitors in parallel to R_3 and R_4 . Adding capacitors in parallel with R_3 and R_4 will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the *Design References* section.

Design Steps

The complete transfer function for this circuit is shown below.

$$V_o = V_{i1} \times \left(-\frac{R_3}{R_1} \right) + V_{i2} \times \left(\frac{R_4}{R_2 + R_4} \right) \times \left(1 + \frac{R_3}{R_1} \right) + V_{ref} \times \left(\frac{R_2}{R_2 + R_4} \right) \times \left(1 + \frac{R_3}{R_1} \right)$$

If $R_1 = R_2$ and $R_3 = R_4$ the transfer function for this circuit simplifies to the following equation.

$$V_o = (V_{i2} - V_{i1}) \times \frac{R_3}{R_1} + V_{ref}$$

- Where the gain, G, is R_3/R_1 .
- 1. Determine the starting value of R_1 and R_2 . The relative size of R_1 and R_2 to the signal impedance of the source affects the gain error.

$$R_1 = R_2 = 10k\Omega$$

2. Calculate the gain required for the circuit.

$$G = \frac{V_{oMax} - V_{oMin}}{V_{idiffMax} - V_{idiffMin}} = \frac{2.5V - (-2.5V)}{1.25V - (-1.25V)} = 2\frac{V}{V} = 6.02\text{dB}$$

3. Calculate the values for R_3 and R_4 .

$$G = 2\frac{V}{V} = \frac{R_3}{R_1} \rightarrow 2 \times R_1 = R_3 = R_4 = 20k\Omega$$

4. Calculate resistor tolerance to meet the minimum common-mode rejection ratio (CMRR). For minimum (worst-case) CMRR, $\alpha = 4$. For a more probable, or typical value of CMRR, $\alpha = 0.33$.

$$\text{CMRR}_{\text{dB}} \cong 20\log_{10}\left(\frac{1+G}{\alpha \times \varepsilon}\right)$$

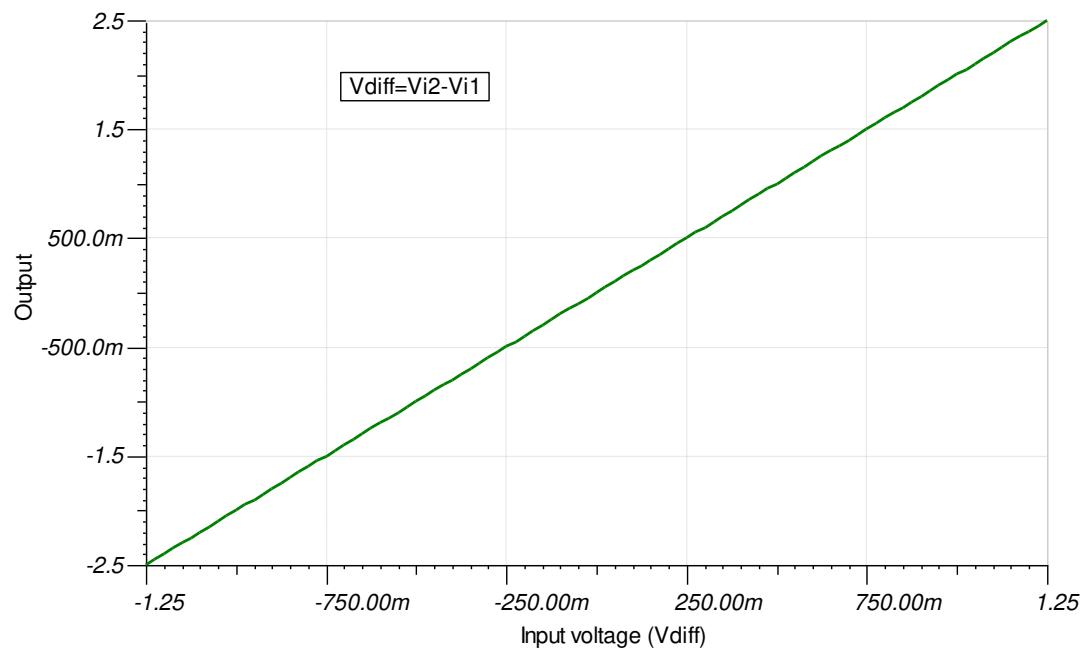
$$\varepsilon = \frac{1+G}{\alpha \times 10^{\left(\frac{\text{CMRR}_{\text{dB}}}{20}\right)}} = \frac{3}{4 \times 10^{\left(\frac{50}{20}\right)}} = 0.024 = 0.24\% \rightarrow \text{Use } 0.1\% \text{ resistors}$$

5. For quick reference, the following table compares resistor tolerance to minimum and typical CMRR values assuming $G = 1$ or $G = 2$. As shown above, as gain increases so does CMRR.

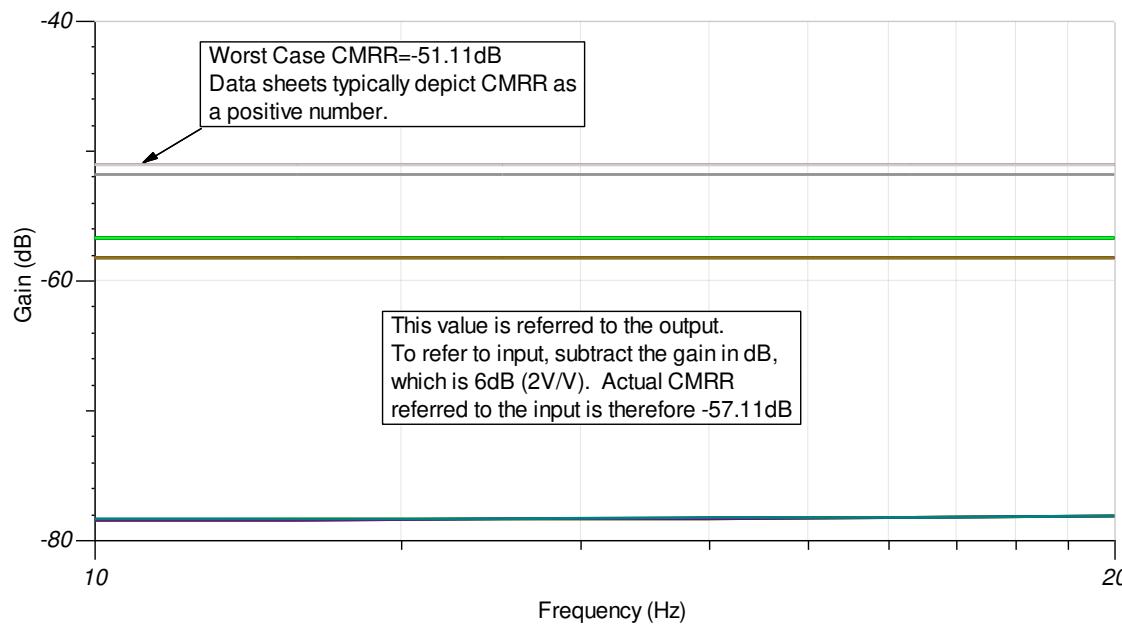
Tolerance	G=1 Minimum (dB)	G=1 Typical (dB)	G=2 Minimum (dB)	G=2 Typical (dB)
0.01% = 0.0001	74	95.6	77.5	99.2
0.1% = 0.001	54	75.6	57.5	79.2
0.5% = 0.005	40	61.6	43.5	65.2
1% = 0.01	34	55.6	37.5	59.2
5% = 0.05	20	41.6	23.5	45.2

Design Simulations

DC Simulation Results



CMRR Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC495](#).

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit [TI Precision Labs](#). For more information on difference amplifier CMRR, please read [Overlooking the obvious: the input impedance of a difference amplifier](#).

Design Featured Op Amp

TLV6001	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	750 μ V
I_q	75 μ A
I_b	1 pA
UGBW	1 MHz
SR	0.5 V/ μ s
#Channels	1, 2, and 4
TLV6001	

Design Alternate Op Amp

OPA320	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	40 μ V
I_q	1.5 mA
I_b	0.2 pA
UGBW	20 MHz
SR	10 V/ μ s
#Channels	1 and 2
OPA320	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 22, 2018 to January 31, 2019

	Page
• Downscale title. Added link to circuit cookbook landing page.....	1

Analog Engineer's Circuit Amplifiers

Inverting Amplifier Circuit

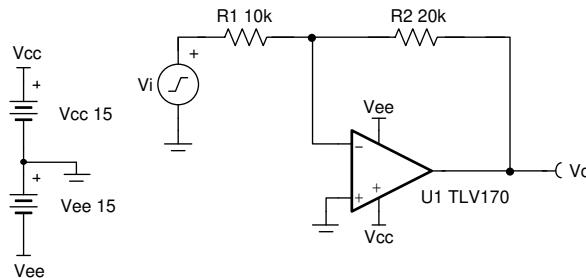


Design Goals

Input		Output		Freq.	Supply	
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	f	V_{cc}	V_{ee}
-7V	7V	-14V	14V	3kHz	15V	-15V

Design Description

This design inverts the input signal, V_i , and applies a signal gain of $-2V/V$. The input signal typically comes from a low-impedance source because the input impedance of this circuit is determined by the input resistor, R_1 . The common-mode voltage of an inverting amplifier is equal to the voltage connected to the non-inverting node, which is ground in this design.



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Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions. The common-mode voltage in this circuit does not vary with input voltage.
2. The input impedance is determined by the input resistor. Make sure this value is large when compared to the source output impedance.
3. Using high value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitor in parallel to R_2 . Adding a capacitor in parallel with R_2 improves stability of the circuit if high value resistors are used.
6. Large signal performance can be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth, see the Design References section.

Design Steps

The transfer function of this circuit follows:

$$V_o = V_i \times \left(-\frac{R_2}{R_1} \right)$$

- Determine the starting value of R_1 . The relative size of R_1 to the signal source impedance affects the gain error. Assuming the impedance from the signal source is low (for example, 100Ω), set $R_1 = 10k\Omega$ for 1% gain error.

$$R_1 = 10 \text{ k}\Omega$$

- Calculate the gain required for the circuit. Since this is an inverting amplifier, use V_{iMin} and V_{oMax} for the calculation.

$$G = \frac{V_{oMax}}{V_{iMin}} = \frac{14 \text{ V}}{-7 \text{ V}} = -2 \frac{\text{V}}{\text{V}}$$

- Calculate R_2 for a desired signal gain of -2 V/V .

$$G = -\frac{R_2}{R_1} \rightarrow R_2 = -G \times R_1 = -(-2 \frac{\text{V}}{\text{V}}) \times 10 \text{ k}\Omega = 20 \text{ k}\Omega$$

- Calculate the small signal circuit bandwidth to ensure it meets the 3-kHz requirement. Be sure to use the noise gain, or non-inverting gain, of the circuit.

$$\text{GBP}_{\text{TLV } 170} = 1.2 \text{ MHz}$$

$$\text{NG} = \left(1 + \frac{R_2}{R_1} \right) = 3 \frac{\text{V}}{\text{V}}$$

$$\text{BW} = \frac{\text{GBP}}{\text{NG}} = \frac{1.2 \text{ MHz}}{3 \text{ V/V}} = 400 \text{ kHz}$$

- Calculate the minimum slew rate required to minimize slew-induced distortion.

$$V_p = \frac{\text{SR}}{2 \times \pi \times f} \rightarrow \text{SR} > 2 \times \pi \times f \times V_p$$

$$\text{SR} > 2 \times \pi \times 3 \text{ kHz} \times 14 \text{ V} = 263.89 \frac{\text{kV}}{\text{s}} = 0.26 \frac{\text{V}}{\mu\text{s}}$$

- $\text{SR}_{\text{TLV } 170} = 0.4 \text{ V}/\mu\text{s}$, therefore, it meets this requirement.
- To avoid stability issues, ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

$$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_2 \parallel R_1)} > \frac{\text{GBP}}{\text{NG}}$$

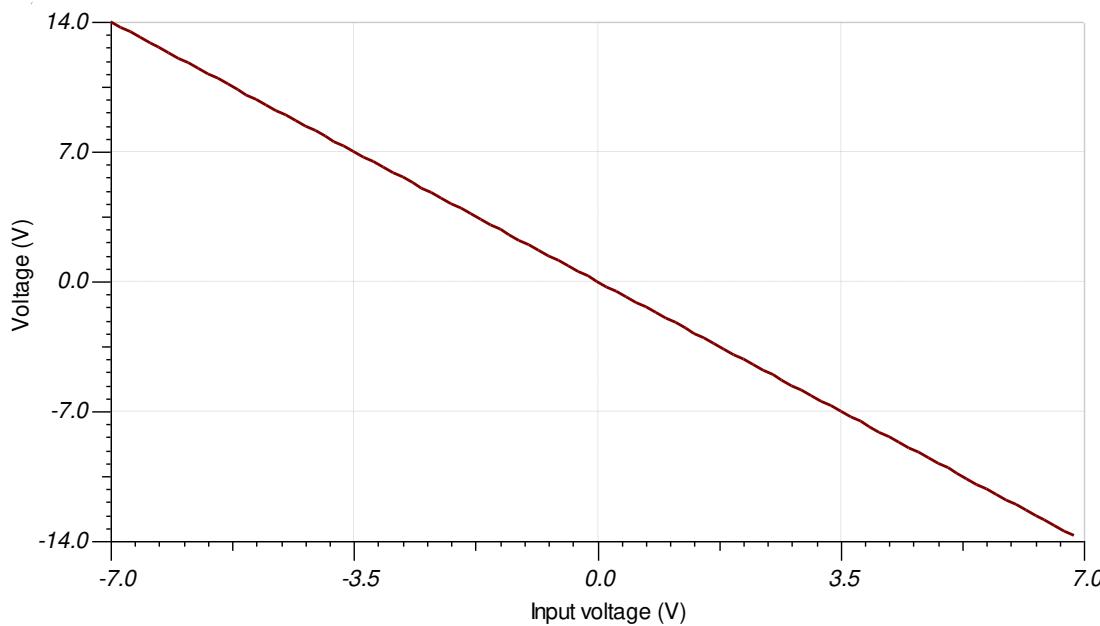
$$\frac{1}{2 \times \pi \times (3 \text{ pF} + 3 \text{ pF}) \times \frac{20 \text{ k}\Omega \times 10 \text{ k}\Omega}{20 \text{ k}\Omega + 10 \text{ k}\Omega}} > \frac{1.2 \text{ MHz}}{3 \text{ V/V}}$$

$$3.97 \text{ MHz} > 400 \text{ kHz}$$

- C_{cm} and C_{diff} are the common-mode and differential input capacitance of the TLV170, respectively.
- Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

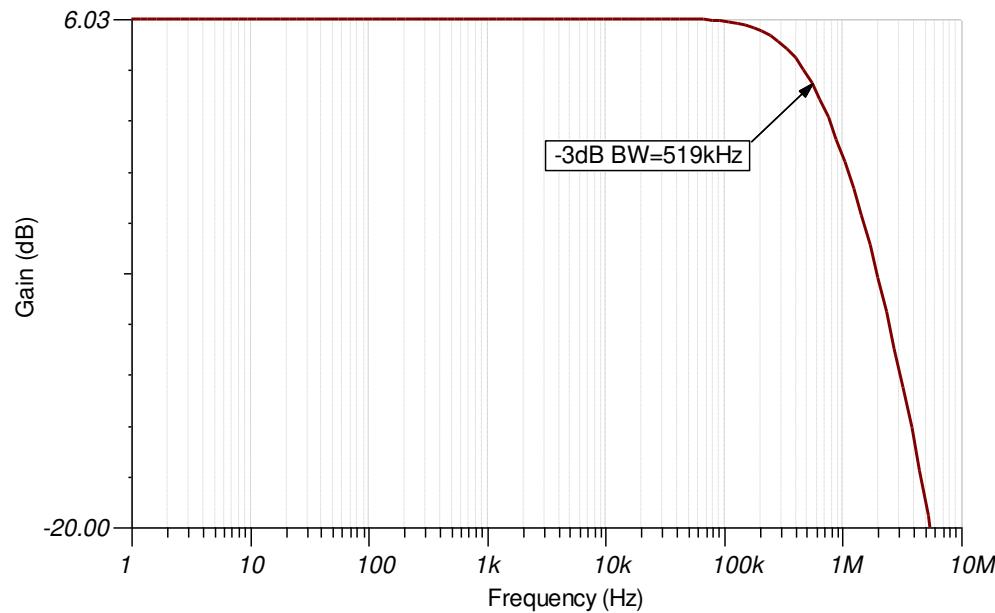
Design Simulations

DC Simulation Results



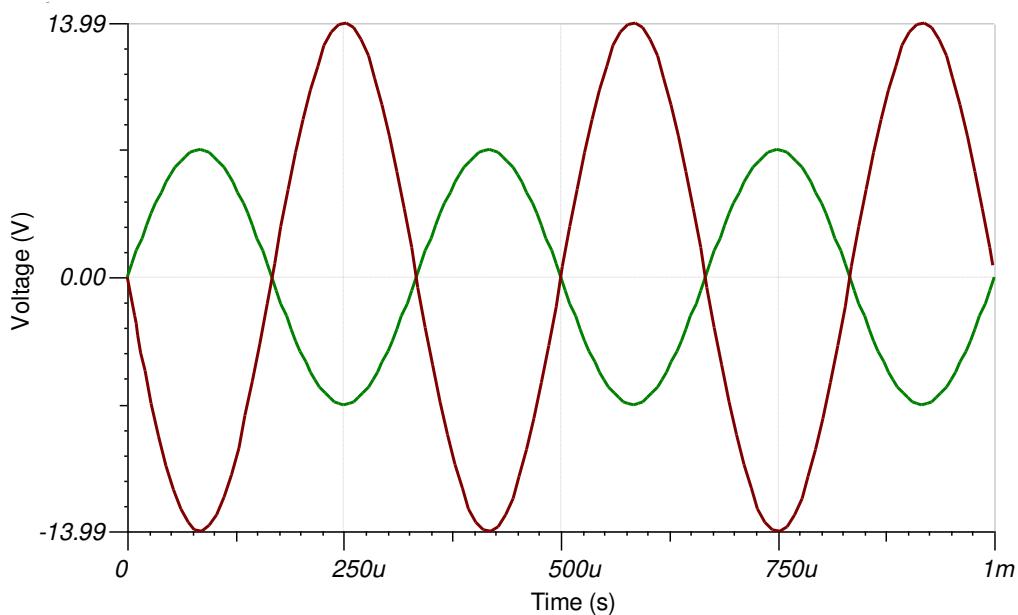
AC Simulation Results

The bandwidth of the circuit depends on the noise gain, which is 3V/V. The bandwidth is determined by looking at the -3-dB point, which is located at 3dB given a signal gain of 6dB. The simulation sufficiently correlates with the calculated value of 400kHz.



Transient Simulation Results

The output is double the magnitude of the input and inverted.



References:

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOC492](#)
3. [TI Precision Labs](#)

Design Featured Op Amp

TLV170	
V_{ss}	$\pm 18\text{ V}$ (36 V)
V_{inCM}	($V_{ee}-0.1\text{ V}$) to ($V_{cc}-2\text{ V}$)
V_{out}	Rail-to-rail
V_{os}	0.5 mV
I_q	125 μA
I_b	10 pA
UGBW	1.2 MHz
SR	0.4 V/ μs
#Channels	1, 2, 4
www.ti.com/product/tlv170	

Design Alternate Op Amp

LMV358A	
V_{ss}	2.5 V to 5.5 V
V_{inCM}	($V_{ee}-0.1\text{ V}$) to ($V_{cc}-1\text{ V}$)
V_{out}	Rail-to-rail
V_{os}	1 mV
I_q	70 μA
I_b	10 pA
UGBW	1 MHz
SR	1.7 V/ μs
#Channels	1 (LMV321A), 2 (LMV358A), 4 (LMV324A)
www.ti.com/product/lmv358A	

Revision History

Revision	Date	Change
C	December 2020	Updated result for Design Step 6.
B	March 2019	Changed LMV358 to LMV358A in the Design Alternate Op Amp section.
A	January 2019	Downstyle title. Added link to circuit cookbook landing page.

Application Note

Two op amp instrumentation amplifier circuit

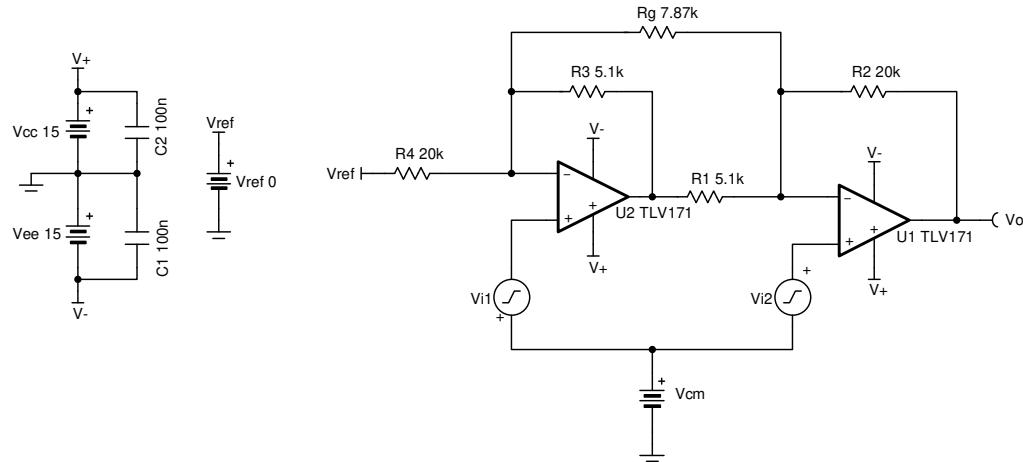


Design Goals

Input $V_{iDiff}(V_{i2} - V_{i1})$		Output		Supply		
V_{iDiff_Min}	V_{iDiff_Max}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
+/-1V	+/-2V	-10V	+10V	15V	-15V	0V
V_{cm}		Gain Range				
+/-10V		5V/V to 10V/V				

Design Description

This design amplifies the difference between V_{i1} and V_{i2} and outputs a single ended signal while rejecting the common-mode voltage. Linear operation of an instrumentation amplifier depends upon the linear operation of its primary building block: op amps. An op amp operates linearly when the input and output signals are within the device's input common-mode and output-swing ranges, respectively. The supply voltages used to power the op amps define these ranges.



Design Notes

1. R_g sets the gain of the circuit.
2. High-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
3. The ratio of R_4 and R_3 set the minimum gain when R_g is removed.
4. Ratios of R_2/R_1 and R_4/R_3 must be matched to avoid degrading the instrumentation amplifier's DC CMRR and ensuring the V_{ref} gain is 1V/V.
5. Linear operation is contingent upon the input common-mode and the output swing ranges of the discrete op amps used. The linear output swing ranges are specified under the A_{ol} test conditions in the op amps data sheets.

Design Steps

- Transfer function of this circuit.

$$V_o = V_{iDiff} \times G + V_{ref} = (V_{i2} - V_{i1}) \times G + V_{ref}$$

when $V_{ref} = 0$, the transfer function simplifies to the following equation:

$$V_o = (V_{i2} - V_{i1}) \times G$$

where G is the gain of the instrumentation amplifier and $G = 1 + \frac{R_4}{R_3} + \frac{2R_2}{R_g}$

- Select R_4 and R_3 to set the minimum gain.

$$G_{min} = 1 + \frac{R_4}{R_3} = 5 \frac{V}{V}$$

Choose $R_4 = 20k\Omega$

$$G_{min} = 1 + \frac{20k\Omega}{R_3} = 5 \frac{V}{V}$$

$$R_3 = \frac{R_4}{5 - 1} = \frac{20k\Omega}{4} = 5k\Omega \rightarrow R_3 = 5.1k\Omega \quad (\text{Standard Value})$$

- Select R_1 and R_2 . Ensure that R_1/R_2 and R_3/R_4 ratios are matched to set the gain applied to the reference voltage at 1V/V.

$$\frac{V_{o_ref}}{V_{ref}} = \left(-\frac{R_3}{R_4} \right) \times \left(-\frac{R_2}{R_1} \right) = \frac{R_3 \times R_2}{R_4 \times R_1} = 1 \frac{V}{V}$$

$$\frac{R_2}{R_1} = \frac{R_4}{R_3} \rightarrow R_1 = R_3 = 5.1k\Omega \text{ and } R_2 = R_4 = 20k\Omega \quad (\text{Standad Value})$$

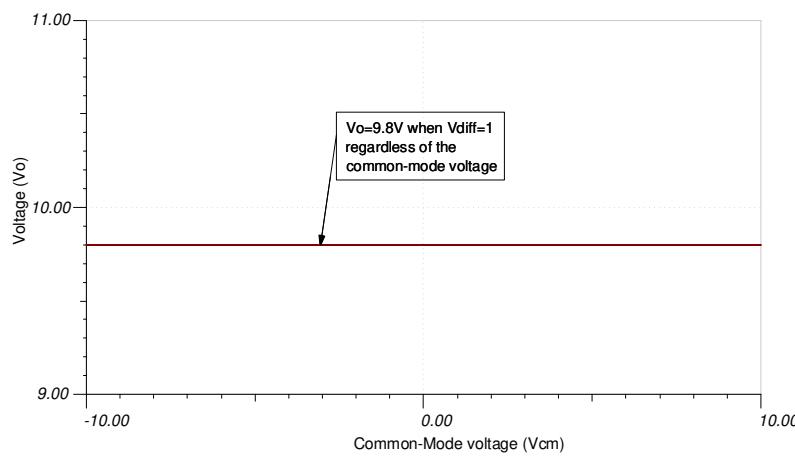
- Select R_g to meet the desired maximum gain $G = 10V/V$.

$$G = 1 + \frac{R_4}{R_3} + \frac{2R_2}{R_g} = 1 + \frac{20 k\Omega}{5.1 k\Omega} + \frac{2 \times 20 k\Omega}{R_g} = 10 V/V$$

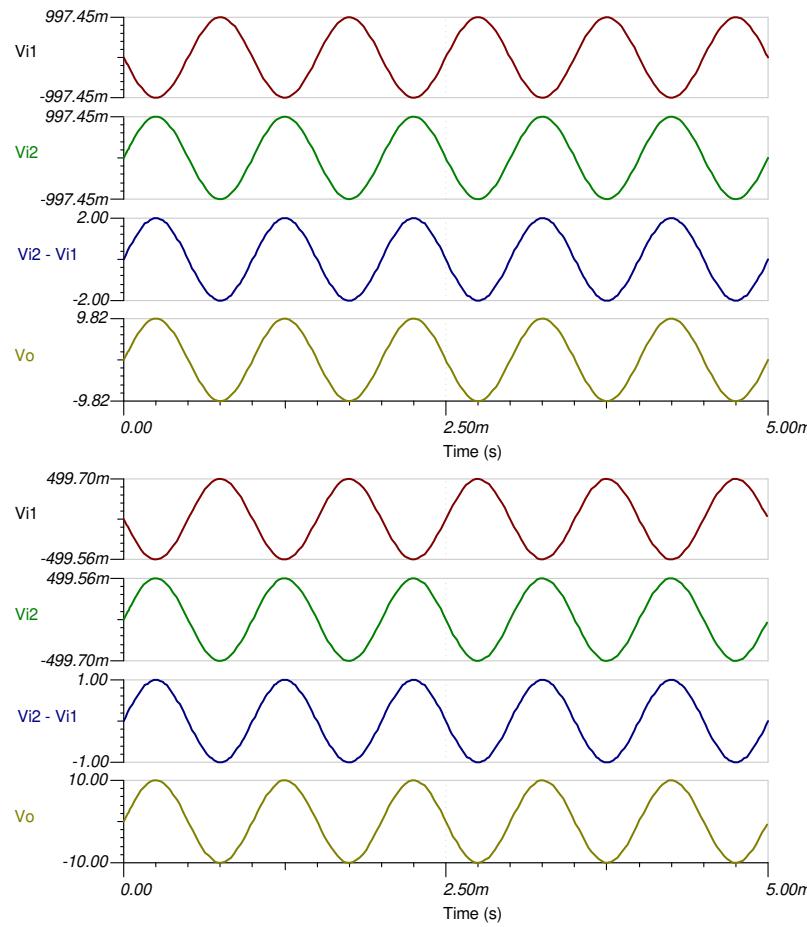
$$R_g = 8 k\Omega \rightarrow R_g = 7.87 k\Omega \quad (\text{Standard Value})$$

Design Simulations

DC Simulation Results



Transient Simulation Results



References:

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOMAU7](#)
3. [TI Precision Labs](#)
4. [V_{CM} vs. V_{OUT} plots for instrumentation amplifiers with two op amps](#)
5. [Common-mode Range Calculator for Instrumentation Amplifiers](#)

Design Featured Op Amp

TLV171	
V _{ss}	4.5V to 36V
V _{inCM}	(V _{ee} -0.1V) to (V _{cc} -2V)
V _{out}	Rail-to-rail
V _{os}	0.25mV
I _q	475µA
I _b	8pA
UGBW	3MHz
SR	1.5V/µs
#Channels	1,2,4
www.ti.com/product/tlv171	

Design Alternate Op Amp

OPA172	
V _{ss}	4.5V to 36V
V _{inCM}	(V _{ee} -0.1V) to (V _{cc} -2V)
V _{out}	Rail-to-rail
V _{os}	0.2mV
I _q	1.6mA
I _b	8pA
UGBW	10MHz
SR	10V/µs
#Channels	1,2,4
www.ti.com/product/opa172	

Analog Engineer's Circuit

Non-Inverting Amplifier Circuit

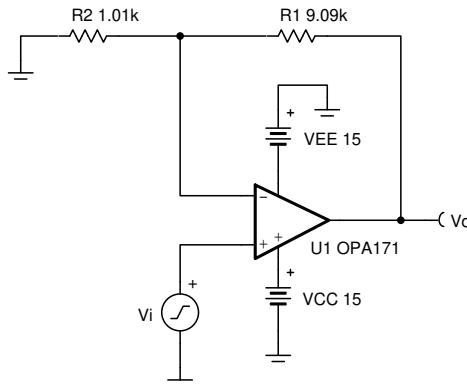


Design Goals

Input		Output		Supply	
ViMin	ViMax	VoMin	VoMax	Vcc	Vee
-1 V	1 V	-10 V	10 V	15 V	-15 V

Design Description

This design amplifies the input signal, V_i , with a signal gain of 10 V/V. The input signal may come from a high-impedance source (for example, $M\Omega$) because the input impedance of this circuit is determined by the extremely high input impedance of the op amp (for example, $G\Omega$). The common-mode voltage of a non-inverting amplifier is equal to the input signal.



Design Notes

1. Use the op amp linear output operating range, which is usually specified under the A_{OL} test conditions. The common-mode voltage is equal to the input signal.
2. The input impedance of this circuit is equal to the input impedance of the amplifier.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. The small-signal bandwidth of a non-inverting amplifier depends on the gain of the circuit and the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to R_1 . Adding a capacitor in parallel with R_1 will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the *Design References* section.

Design Steps

The transfer function for this circuit is given below.

$$V_o = V_i \times \left(1 + \frac{R_1}{R_2}\right)$$

1. Calculate the gain.

$$G = \frac{V_{o_max} - V_{o_min}}{V_{i_max} - V_{i_min}}$$

$$G = \frac{10V - (-10V)}{1V - (-1V)} = 10V/V$$

2. Calculate values for R_1 and R_2 .

$$G = 1 + \frac{R_1}{R_2}$$

Choose $R_1 = 9.09k\Omega$

$$R_2 = \frac{R_1}{G - 1} = \frac{9.09k\Omega}{(10V/V) - 1} = 1.01k\Omega$$

3. Calculate the minimum slew rate required to minimize slew-induced distortion.

$$SR > 2 \times \pi \times V_p \times f = 2 \times \pi \times 10V \times 20kHz = 1.257V/\mu s$$

- The slew rate of the OPA171 is 1.5 V/ μs , therefore it meets this requirement.
4. To maintain sufficient phase margin, ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

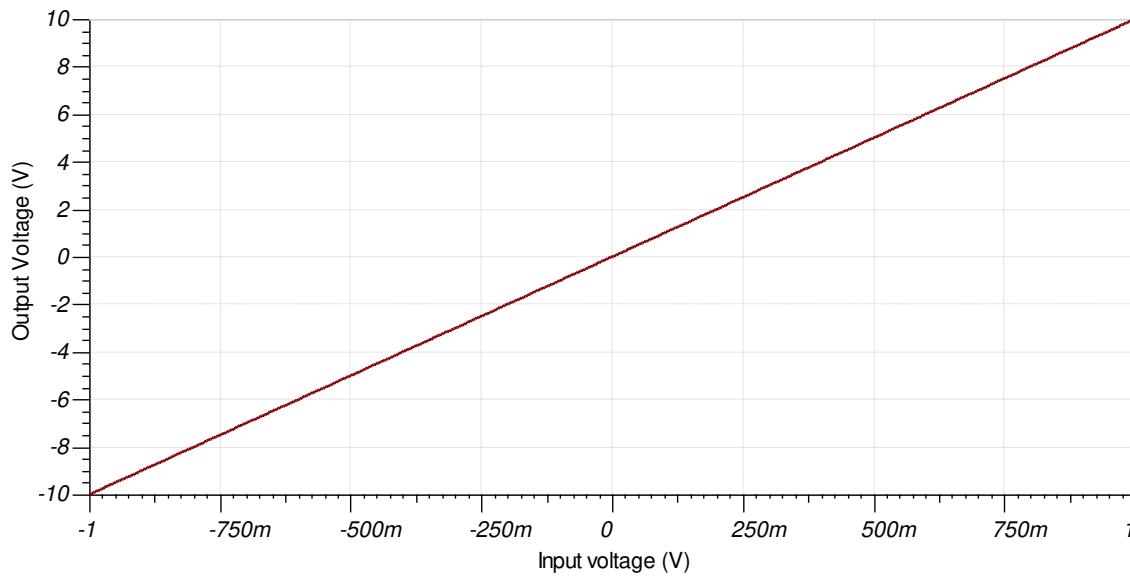
$$\frac{\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_1 \parallel R_2)}}{2 \times \pi \times (3pF + 3pF) \times \frac{1.01k\Omega \times 9.09k\Omega}{1.01k\Omega + 9.09k\Omega}} > \frac{3MHz}{10V/V}$$

$$29.18MHz > 300kHz$$

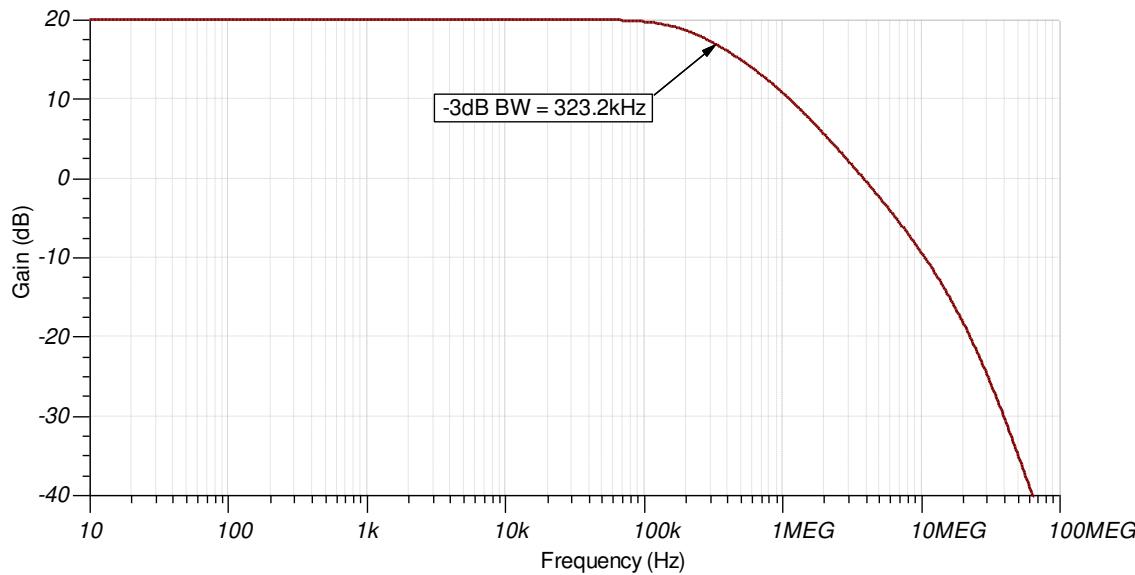
- C_{cm} and C_{diff} are the common-mode and differential input capacitances of the OPA171, respectively.
- Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC493](#).

For more information on many op amp topics including common-mode range, output swing, and bandwidth please visit [TI Precision Labs](#).

Design Featured Op Amp

OPA171	
V_{ss}	2.7 V to 36 V
V_{inCM}	(V _{ee} -0.1 V) to (V _{cc} -2 V)
V_{out}	Rail-to-rail
V_{os}	250 μ V
I_q	475 μ A
I_b	8 pA
UGBW	3 MHz
SR	1.5 V/ μ s
#Channels	1, 2, and 4
OPA171	

Design Alternate Op Amp

OPA191	
V_{ss}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 μ V
I_q	140 μ A
I_b	5 pA
UGBW	2.5 MHz
SR	7.5 V/ μ s
#Channels	1, 2, and 4
OPA191	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 22, 2018 to January 31, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.....1

Analog Engineer's Circuit Amplifiers

Inverting Summer Circuit

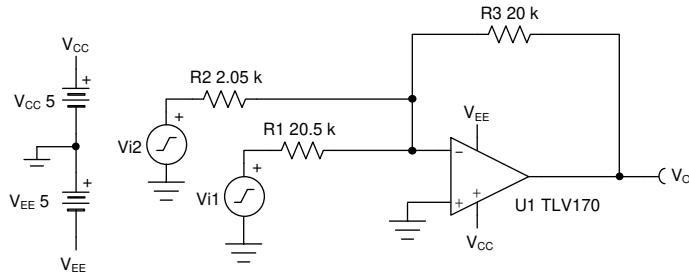


Design Goals

Input 1		Input 2		Output		Freq.	Supply	
$V_{i1\text{Min}}$	$V_{i1\text{Max}}$	$V_{i2\text{Min}}$	$V_{i2\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	f	V_{cc}	V_{ee}
-2.5V	2.5V	-250mV	250mV	-4.9V	4.9V	10kHz	5V	-5V

Design Description

This design sums (adds) and inverts two input signals, V_{i1} and V_{i2} . The input signals typically come from low-impedance sources because the input impedance of this circuit is determined by the input resistors, R_1 and R_2 . The common-mode voltage of an inverting amplifier is equal to the voltage connected to the non-inverting node, which is ground in this design.



Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions. The common-mode voltage in this circuit does not vary with input voltage.
2. The input impedance is determined by the input resistors. Make sure these values are large when compared to the output impedance of the source.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitor in parallel to R_3 . Adding a capacitor in parallel with R_3 will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the *Design References* section.

Design Steps

The transfer function for this circuit is given below.

$$V_o = V_{i1} \times \left(-\frac{R_3}{R_1} \right) + V_{i2} \times \left(-\frac{R_3}{R_2} \right)$$

1. Select a reasonable resistance value for R_3 .

$$R_3 = 20 \text{ k}\Omega$$

2. Calculate gain required for V_{i1} . For this design, half of the output swing is devoted to each input.

$$|G_{Vi1}| = \left| \frac{\frac{V_{oMax} - V_{oMin}}{2}}{V_{i1Max} - V_{i1Min}} \right| = \left| \frac{\frac{4.9 \text{ V} - (-4.9 \text{ V})}{2}}{2.5 \text{ V} - (-2.5 \text{ V})} \right| = 0.98 \frac{V}{V} = -0.175 \text{ dB}$$

3. Calculate the value of R_1 .

$$|G_{Vi1}| = \frac{R_3}{R_1} \rightarrow R_1 = \frac{R_3}{|G_{Vi1}|} = \frac{20 \text{ k}\Omega}{0.98 \frac{V}{V}} = 20.4 \text{ k}\Omega \approx 20.5 \text{ k}\Omega \text{ (Standard Value)}$$

4. Calculate gain required for V_{i2} . For this design, half of the output swing is devoted to each input.

$$|G_{Vi2}| = \left| \frac{\frac{V_{oMax} - V_{oMin}}{2}}{V_{i2Max} - V_{i2Min}} \right| = \left| \frac{\frac{4.9 \text{ V} - (-4.9 \text{ V})}{2}}{250 \text{ mV} - (-250 \text{ mV})} \right| = 9.8 \frac{V}{V} = 19.82 \text{ dB}$$

5. Calculate the value of R_2 .

$$|G_{Vi2}| = \frac{R_3}{R_2} \rightarrow R_2 = \frac{R_3}{|G_{Vi2}|} = \frac{20 \text{ k}\Omega}{9.8 \frac{V}{V}} = 2.04 \text{ k}\Omega \approx 2.05 \text{ k}\Omega \text{ (Standard Value)}$$

6. Calculate the small signal circuit bandwidth to ensure it meets the 10-kHz requirement. Be sure to use the noise gain (NG), or non-inverting gain, of the circuit. When calculating the noise gain note that R_1 and R_2 are in parallel.

$$GBP_{OPA170} = 1.2 \text{ MHz}$$

$$NG = 1 + \frac{R_3}{R_1 || R_2} = 1 + \frac{20 \text{ k}\Omega}{1.86 \text{ k}\Omega} = 11.75 \frac{V}{V} = 21.4 \text{ dB} \quad (8)$$

$$BW = \frac{GBP}{NG} = \frac{1.2 \text{ MHz}}{11.75 \frac{V}{V}} = 102 \text{ kHz} \quad (9)$$

- This requirement is met because the closed-loop bandwidth is 102kHz and the design goal is 10kHz.

7. Calculate the minimum slew rate to minimize slew-induced distortion.

$$V_p = \frac{SR}{2 \times \pi \times f} \rightarrow SR > 2 \times \pi \times f \times V_p$$

$$SR > 2 \times \pi \times 10 \text{ kHz} \times 4.9 \text{ V} = 307.87 \frac{kV}{s} = 0.31 \frac{V}{\mu s} \quad (11)$$

- $SR_{OPA170}=0.4V/\mu s$, therefore it meets this requirement.

8. To avoid stability issues ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

$$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_1 || R_2 || R_3)} > \frac{GBP}{NG}$$

$$\frac{1}{2 \times \pi \times 3 \text{ pF} \times 3 \text{ pF} \times 1.7 \text{ k}\Omega} > \frac{1.2 \text{ MHz}}{11.75 \frac{V}{V}} \quad (13)$$

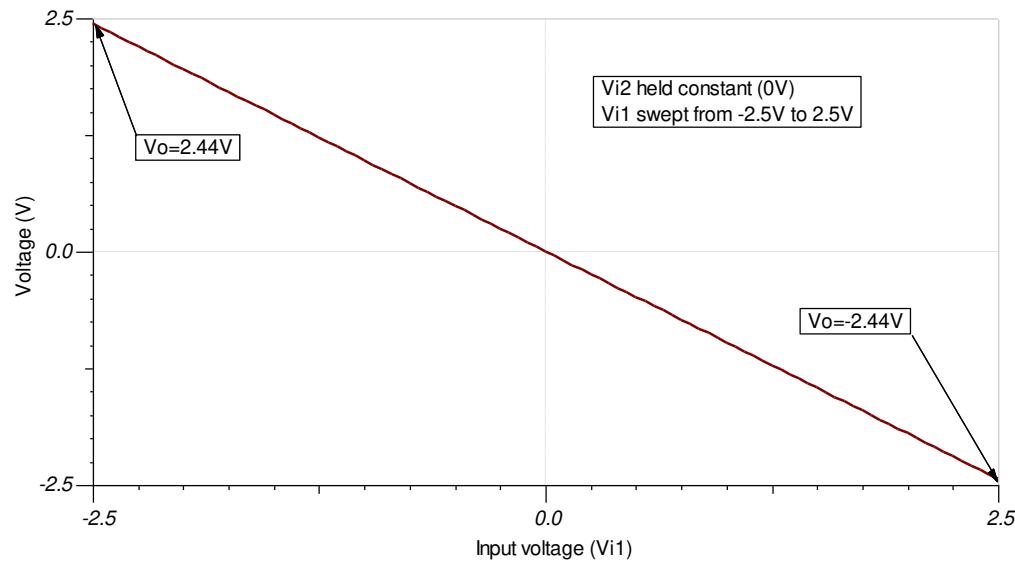
$$15.6 \text{ MHz} > 102 \text{ kHz} \quad (14)$$

- C_{cm} and C_{diff} are the common-mode and differential input capacitances.
- Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

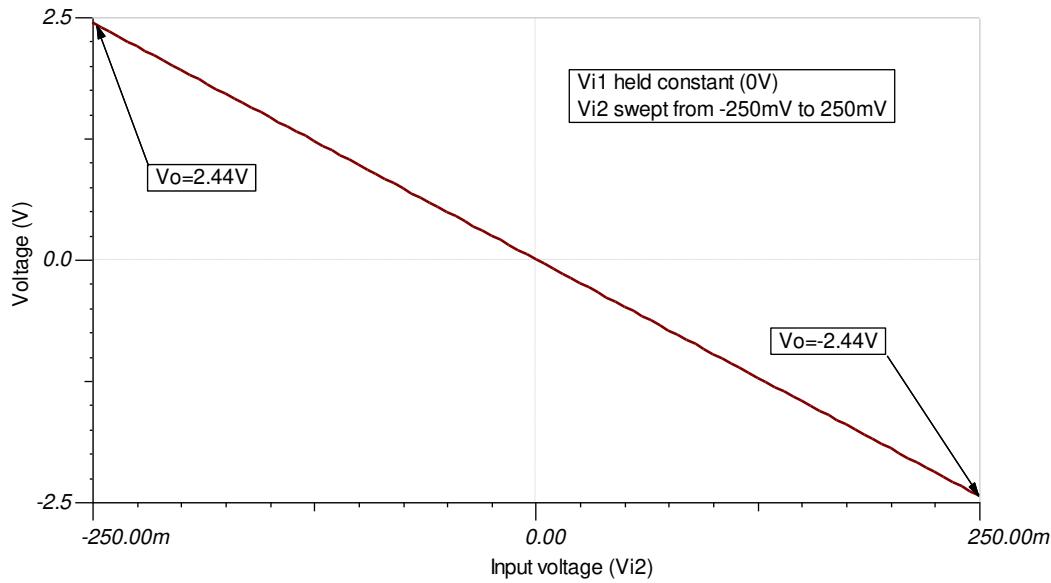
Design Simulations

DC Simulation Results

This simulation sweeps V_{i1} from $-2.5V$ to $2.5V$ while V_{i2} is held constant at $0V$. The output is inverted and ranges from $-2.44V$ to $2.44V$.

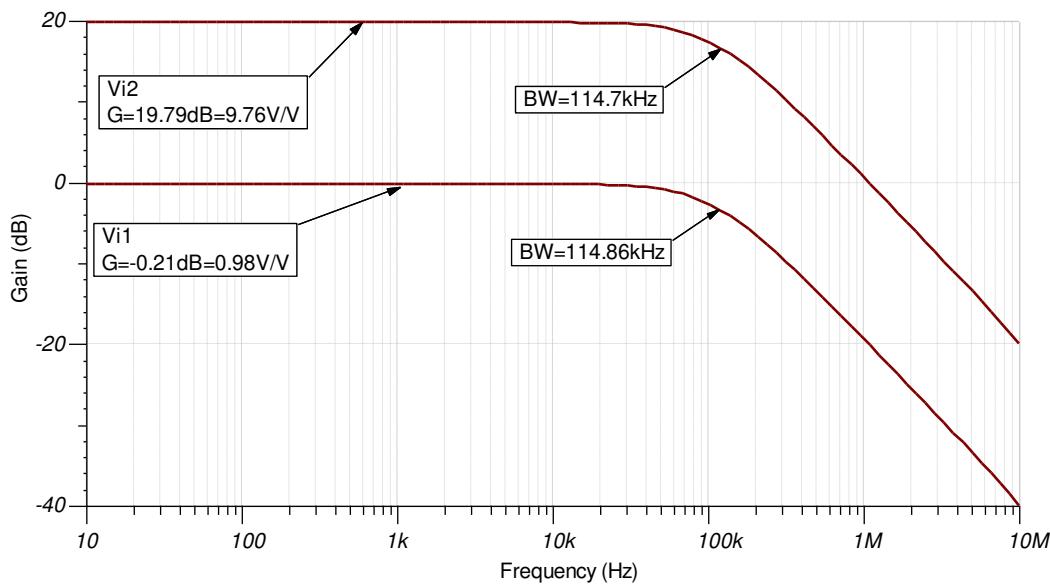


This simulation sweeps V_{i2} from $-250mV$ to $250mV$ while V_{i1} is held constant at $0V$. The output is inverted and ranges from $-2.44V$ to $2.44V$.



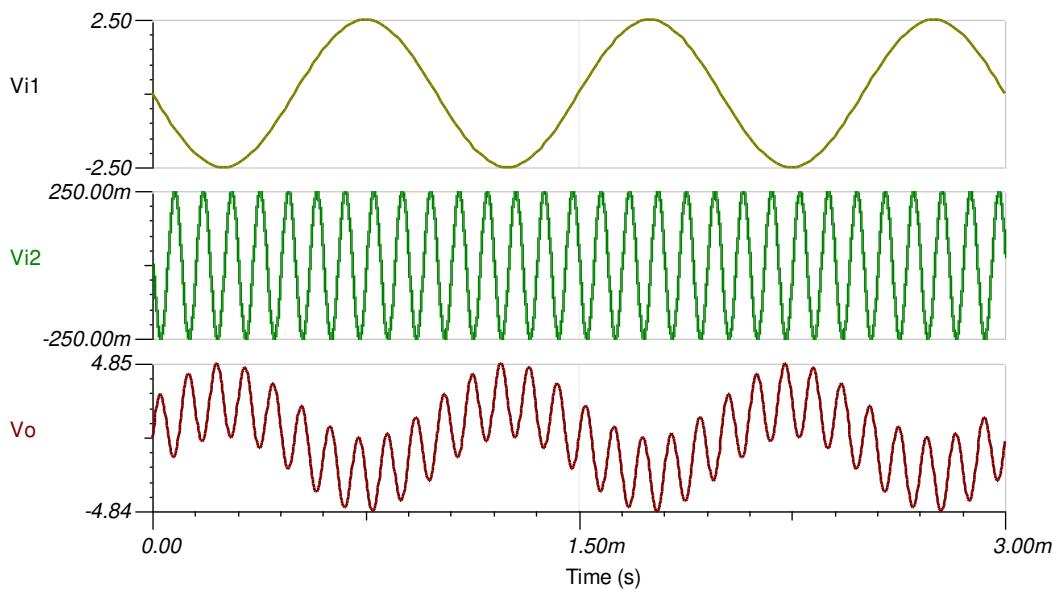
AC Simulation Results

This simulation shows the bandwidth of the circuit. Note that the bandwidth is the same for either input. This is because the bandwidth depends on the noise gain of the circuit, not the signal gain of each input. These results correlate well with the calculations.



Transient Simulation Results

This simulation shows the inversion and summing of the two input signals. V_{i1} is a 1-kHz, 5-V_{pp} sine wave and V_{i2} is a 10-kHz, 500-mV_{pp} sine wave. Since both inputs are properly amplified or attenuated, the output is within specification.



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC494](#).

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit [TI Precision Labs](#).

Design Featured Op Amp

OPA170	
V_{ss}	2.7V to 36V
V_{inCM}	(Vee-0.1V) to (Vcc-2V)
V_{out}	Rail-to-rail
V_{os}	0.25mV
I_q	110µA
I_b	8pA
UGBW	1.2MHz
SR	0.4V/µs
#Channels	1, 2, 4
www.ti.com/product/opa170	

Design Alternate Op Amp

LMC7101	
V_{ss}	2.7V to 15.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	110µV
I_q	0.8mA
I_b	1pA
UGBW	1.1MHz
SR	1.1V/µs
#Channels	1
www.ti.com/product/lmc7101	

Revision History

Revision	Date	Change
C	January 2021	Updated Formula format
B	December 2020	Updated Design Goals Table
A	January 2019	Down-style title. Updated title role to <i>Amplifiers</i> . Added link to circuit cookbook landing page.

Analog Engineer's Circuit

Transimpedance Amplifier Circuit

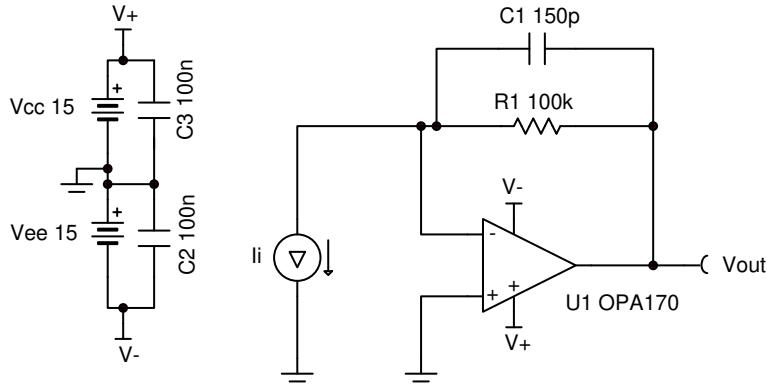


Design Goals

Input		Output		BW	Supply	
I _{iMin}	I _{iMax}	V _{oMin}	V _{oMax}	f _p	V _{cc}	V _{ee}
0 A	50 μ A	0 V	5 V	10 kHz	15 V	-15 V

Design Description

The transimpedance op amp circuit configuration converts an input current source into an output voltage. The current to voltage gain is based on the feedback resistance. The circuit is able to maintain a constant voltage bias across the input source as the input current changes which benefits many sensors.



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Design Notes

1. Use a JFET or CMOS input op amp with low bias current to reduce DC errors.
2. A bias voltage can be added to the non-inverting input to set the output voltage for 0 A input currents.
3. Operate within the linear output voltage swing (see A_{ol} specification) to minimize non-linearity errors.

Design Steps

1. Select the gain resistor.

$$R_1 = \frac{V_{oMax} - V_{oMin}}{I_{iMax}} = \frac{5V - 0V}{50\mu A} = 100k\Omega$$

2. Select the feedback capacitor to meet the circuit bandwidth.

$$C_1 \leq \frac{1}{2 \times \pi \times R_1 \times f_p}$$

$$C_1 \leq \frac{1}{2 \times \pi \times 100k\Omega \times 10kHz} \leq 159pF \approx 150pF \text{ (Standard Value)}$$

3. Calculate the necessary op amp gain bandwidth (GBW) for the circuit to be stable.

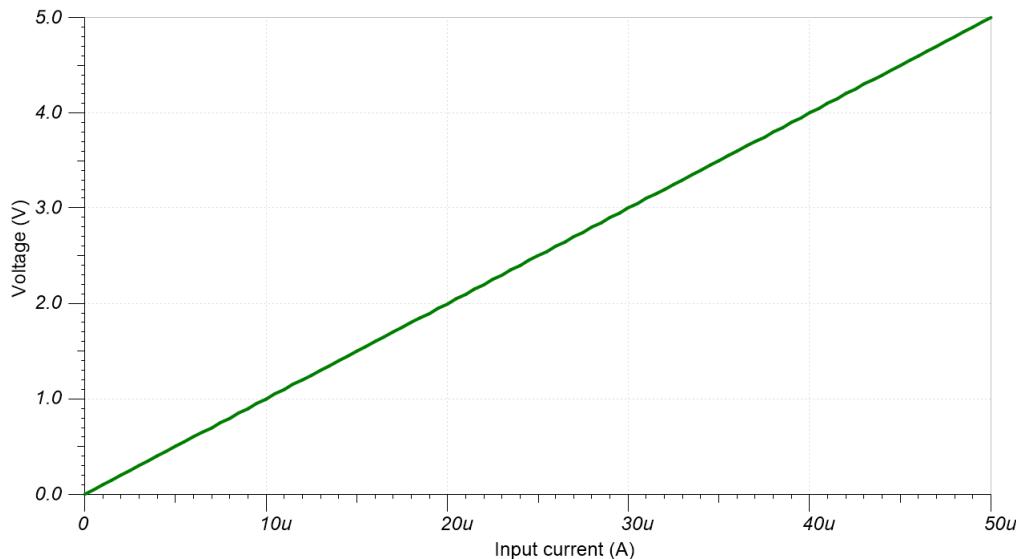
$$\text{GBW} > \frac{C_i + C_1}{2 \times \pi \times R_1 \times C_1^2} > \frac{6pF + 150pF}{2 \times \pi \times 100k\Omega \times (150pF)^2} > 11.03kHz$$

where $C_i = C_s + C_d + C_{cm} = 0pF + 3pF + 3pF = 6pF$ given

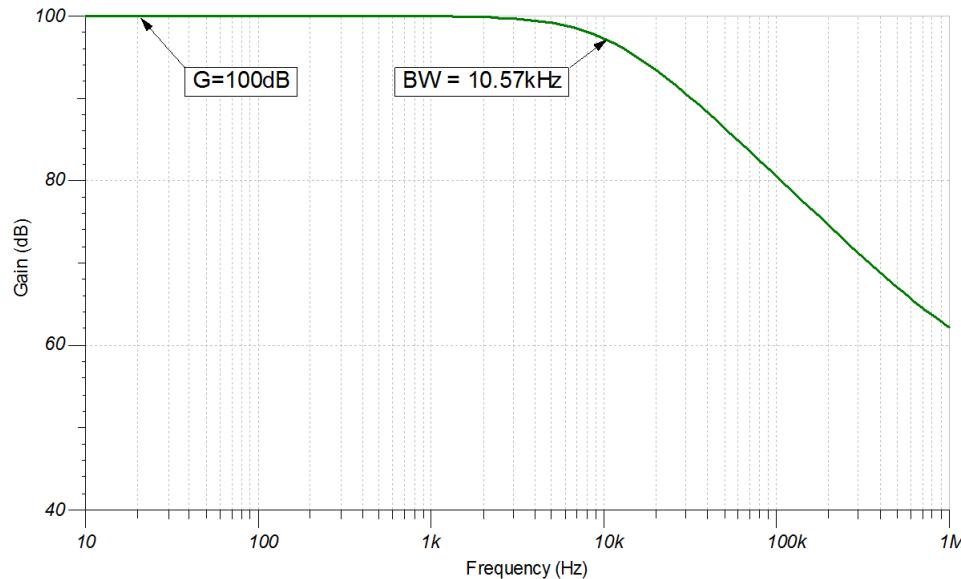
- C_s : Input source capacitance
- C_d : Differential input capacitance of the amplifier
- C_{cm} : Common-mode input capacitance of the inverting input

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC501](#).

See [TIPD176](#).

Design Featured Op Amp

OPA170	
V_{cc}	2.7 V to 36 V
V_{inCM}	($V_{ee} - 0.1$ V) to ($V_{cc} - 2$ V)
V_{out}	Rail-to-rail
V_{os}	0.25 mV
I_q	0.11 mA
I_b	8 pA
UGBW	1.2 MHz
SR	0.4 V/ μ s
#Channels	1, 2, and 4
OPA170	

Design Alternate Op Amp

OPA1671	
V_{cc}	1.7 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	($V_{ee} + 10$ mV) to ($V_{cc} - 10$ mV) at 275 μ A
V_{os}	250 μ V
I_q	940 μ A
I_b	1 pA
UGBW	12 MHz
SR	5 V/ μ s
#Channels	1
OPA1671	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 1, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Updated *Design Alternate Op Amp* table with OPA1671. Added link to circuit cookbook landing page..... [1](#)

High-Side Current-Sensing Circuit Design

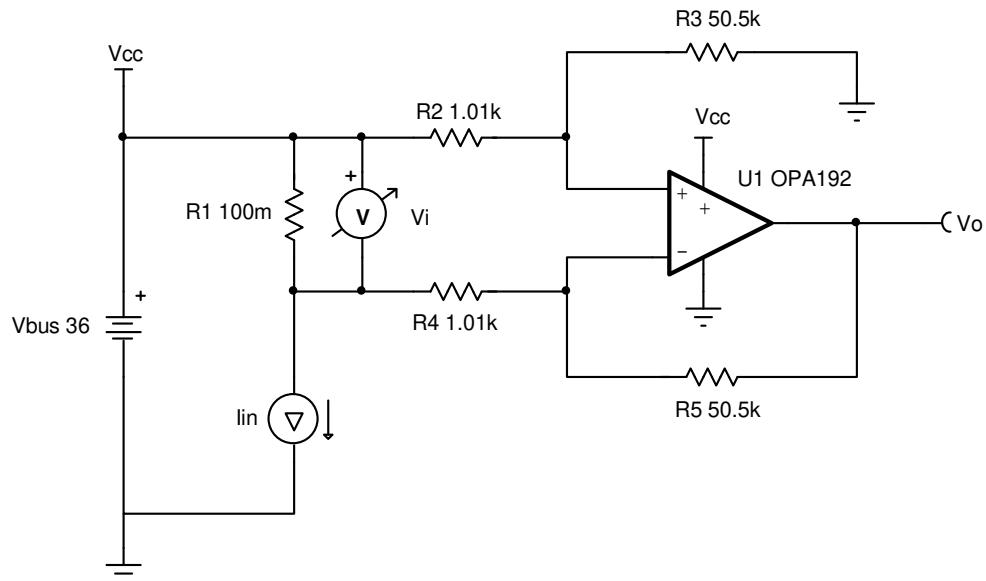


Design Goals

Input		Output		Supply	
I _{iMin}	I _{iMax}	V _{oMin}	V _{oMax}	V _{cc}	V _{ee}
50 mA	1 A	0.25 V	5 V	36 V	0 V

Design Description

This single-supply, high-side, low-cost current sensing solution detects load current between 50 mA and 1 A and converts it to an output voltage from 0.25 V to 5 V. High-side sensing allows for the system to identify ground shorts and does not create a ground disturbance on the load.



Design Notes

1. DC common mode rejection ratio (CMRR) performance is dependent on the matching of the gain setting resistors, R₂-R₅.
2. Increasing the shunt resistor increases power dissipation.
3. Ensure that the common-mode voltage is within the linear input operating region of the amplifier. The common mode voltage is set by the resistor divider formed by R₂, R₃, and the bus voltage. Depending on the common-mode voltage determined by the resistor divider a rail-to-rail input (RRI) amplifier may not be required for this application.
4. An op amp that does not have a common-mode voltage range that extends to V_{cc} may be used in low-gain or an attenuating configuration.
5. A capacitor placed in parallel with the feedback resistor will limit bandwidth, improve stability, and help reduce noise.
6. Use the op amp in a linear output operating region. Linear output swing is usually specified under the A_{OL} test conditions.

Design Steps

1. The full transfer function of the circuit is provided below.

$$V_o = I_{in} \times R_1 \times \frac{R_5}{R_4}$$

Given $R_2 = R_4$ and $R_3 = R_5$

2. Calculate the maximum shunt resistance. Set the maximum voltage across the shunt to 100 mV.

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{100mV}{1A} = 100m\Omega$$

3. Calculate the gain to set the maximum output swing range.

$$\text{Gain} = \frac{V_{oMax} - V_{oMin}}{(I_{iMax} - I_{iMin}) \times R_1} = \frac{5V - 0.25V}{(1A - 0.05A) \times 100m\Omega} = 50 \frac{V}{V}$$

4. Calculate the gain setting resistors to set the gain calculated in step 3.

Choose $R_2 = R_4 = 1.01k \Omega$ (Standard value)

$$R_3 = R_5 = R_2 \times \text{Gain} = 1.01k \Omega \times 50 \frac{V}{V} = 50.5k \Omega \text{ (Standard value)}$$

5. Calculate the common-mode voltage of the amplifier to ensure linear operation.

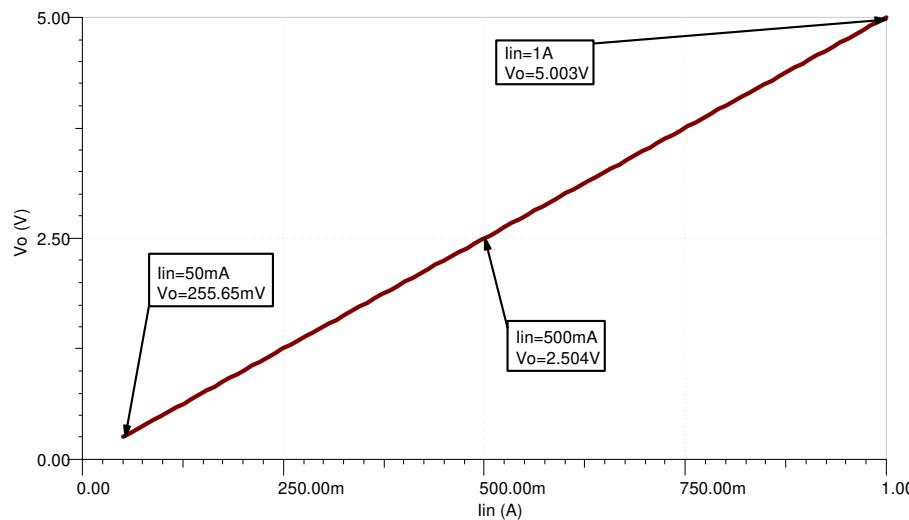
$$V_{cm} = V_{CC} \times \frac{R_3}{R_2 + R_3} = 36V \times \frac{50.5k}{1.01k + 50.5k} = 35.294 V$$

6. The upper cutoff frequency (f_H) is set by the non-inverting gain (noise gain) of the circuit and the gain bandwidth (GBW) of the op amp.

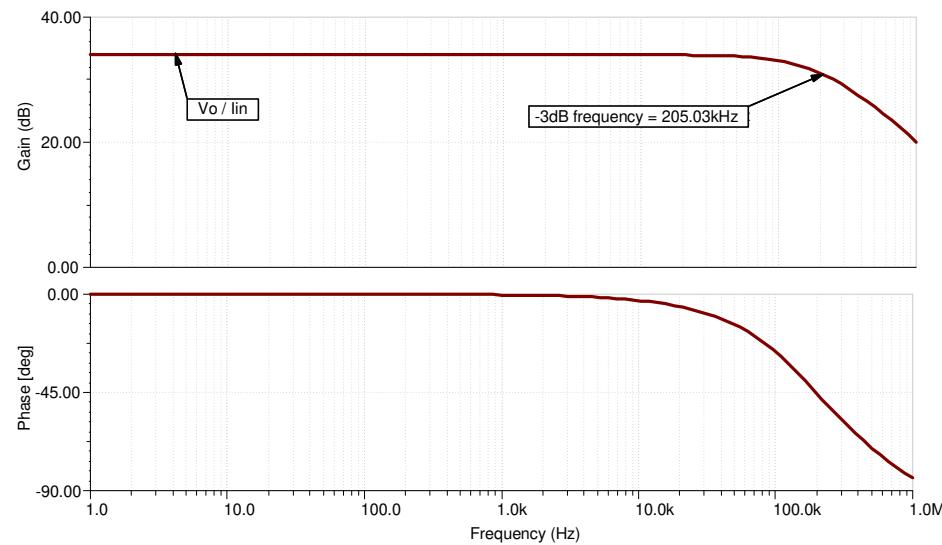
$$f_H = \frac{\text{GBW}}{\text{Noise Gain}} = \frac{10\text{MHz}}{51 \frac{V}{V}} = 196.1 \text{ kHz}$$

Design Simulations

DC Simulation Results



AC Simulation Results



References:

1. [Analog Engineer's Circuit Cookbooks](#)
2. SPICE Simulation File [SBOMAV4](#)
3. [TI Precision Labs](#)

Design Featured Op Amp

OPA192	
V_{cc}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 μ V
I_q	1 mA
I_b	5 pA
UGBW	10 MHz
SR	20 V/ μ s
#Channels	1, 2, and 4
OPA192	

Design Alternate Op Amp

OPA2990	
V_{cc}	2.7 V to 40 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	250 μ V
I_q	120 μ A
I_b	10 pA
UGBW	1.25 MHz
SR	5V/ μ s
#Channels	2
OPA2990	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from December 30, 2018 to February 13, 2019
Page

- Downstyle title. Added *Design Alternate Op Amp* table..... **1**

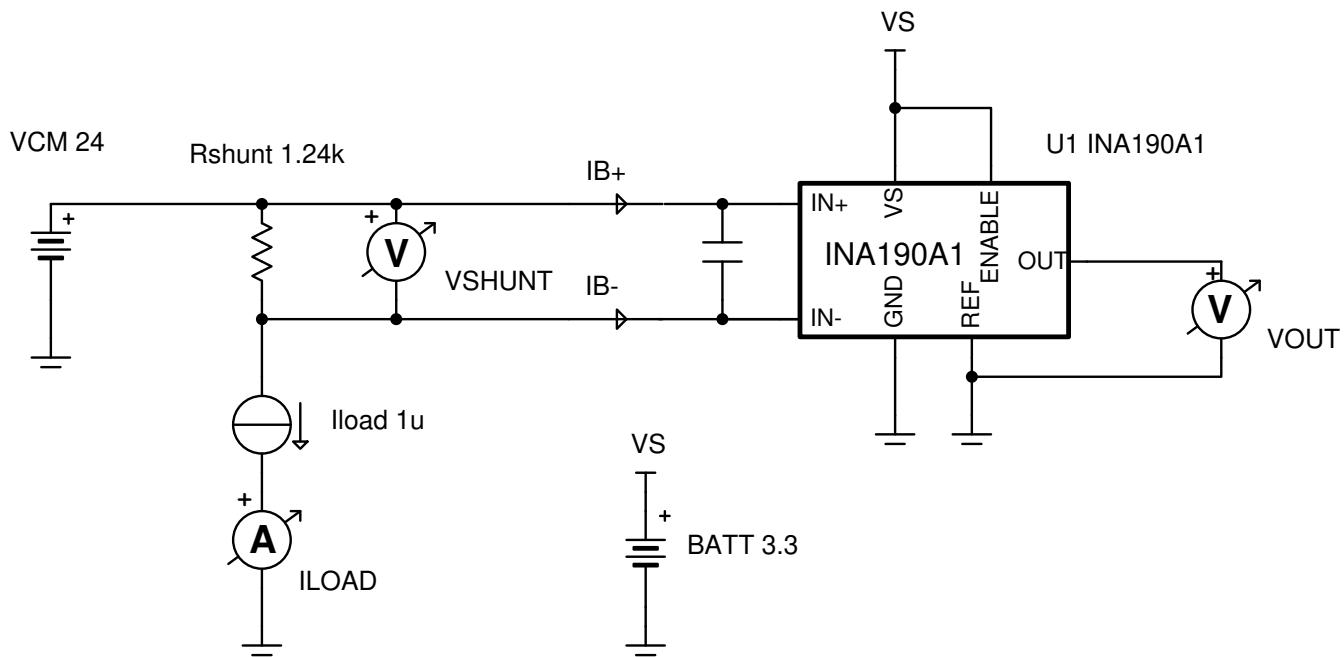
Low (Microamp), High-Side, Current-Sensing Circuit with Current-Sensing Amplifier at High Voltage and Overtemperature



Input			Output		Supply			Temperature	
I _{load} Min	I _{load} Max	V _{CM}	V _{OUT} Min	V _{OUT} Max	I _Q Max	V _{ss}	V _{ee}	Low	High
1 μ A	104 μ A	-0.1 V \leq V _{CM} \leq 40 V	31.0 mV at 1 μ A	3.224 V at 104 μ A	65 μ A	3.3 V	GND (0 V)	0°C	85°C

Design Description

This circuit demonstrates how to use a current sense amplifier to accurately and robustly measure small micro-amp currents and maximize dynamic range. The following error analysis can be applied to many current sense amplifiers. This design relies on using a precision, low input-bias current sense amplifier and analyzing the dynamic error due to input bias currents on large shunt resistors.



Design Notes

1. The [Getting Started with Current Sense Amplifiers](#) video series introduces implementation, error sources, and advanced topic for using current sense amplifiers.
2. Choose a precision 0.1% shunt resistor to limit gain error at higher currents.
3. Choose a low input-bias current (high input-impedance) amplifier such as the [INA190](#).
4. Ensure VCM is within the operating VCM range of INA190: -0.1 V to 40 V.
5. Error significantly reduces if DC offsets are calibrated out with one-point calibration or if device operates under the same conditions as the [INA190 Low-Supply, High-Accuracy, Low- and High-Side Current-Shunt Monitor With Picoamp Bias Current and Enable](#) data sheet specifies ($V_{VS} = 1.8$ V, $V_{CM} = 12$ V, $V_{REF} = 0.9$ V, $T_A = 25^\circ\text{C}$). A two-point calibration can be done to eliminate gain error.
6. It is recommended to add ≥ 1 nF input differential capacitor to INA190 inputs when working with large shunt resistors and DC currents.
7. Follow best practices for layout according to the data sheet: decoupling capacitor close to VS pin, routing the input traces for IN+ and IN- as a differential pair, and so forth.

Design Steps

1. Given the design requirements, ensure the shunt resistor achieves a maximum total error of 3.51% at 1 μA load current. Assume all offset and gain errors are negative. Note that error due to input bias current (I_{IB}) is a function of the V_{SHUNT} and input differential impedance (R_{DIFF}) where $R_{DIFF} = I_{IB+}/V_{DIFF}$. Since I_{IB-} starts around +500 pA and decreases as V_{SHUNT} increases, this generates a negative input offset error. See the *IB+ and IB- vs Differential Input Voltage* plot in the data sheet.

$$T_{MIN} = 0^\circ\text{C}; T_{MAX} = 85^\circ\text{C}$$

$$I_{LOAD_MINIMUM} = 1\mu\text{A}$$

$$R_{SHUNT} = 1240\Omega, 0.1\%$$

$$V_{VS} = 3.3\text{V}; V_{CM} = 24\text{V}; V_{REF} = \text{GND} = 0\text{V}$$

$$V_{OSI_MAX} = -15\mu\text{V}$$

$$V_{OS_CMRR_MAX} = |12\text{V} - V_{CM}| \cdot 10^{\frac{-CMRR_{MIN}}{20\text{dB}}} = 12\text{V} \cdot 10^{\frac{-132\text{dB}}{20\text{dB}}} = -3.01\mu\text{V}$$

$$V_{OS_PSRR_MAX} = |1.8\text{V} - V_{VS}| \cdot PSRR_{MAX} = 3.2\text{V} \cdot 5\mu\text{V/V} = -7.5\mu\text{V}$$

$$V_{OS_RVRR_MAX} = |0.9\text{V} - V_{REF}| \cdot RVRR_{MAX} = 0.9\text{V} \cdot 10\mu\text{V/V} = -9\mu\text{V}$$

$$V_{OS_Drift_MAX} = |25^\circ\text{C} - T_{MAX}| \cdot \left(\frac{dV_{OS}}{dT}\right)_{MAX} = 60^\circ\text{C} \cdot 80\text{nV/C} = -4.8\mu\text{V}$$

$$V_{OS_IB_MAX} = \text{func}\{V_{SHUNT}\} = R_{SHUNT} \cdot \left[\frac{-V_{SHUNT}}{R_{DIFF}} + I_{IB_Typ} \right] = 1240\Omega \cdot \left[\frac{-1.24\text{mV}}{2.3\text{M}\Omega} + 0.5\text{nA} \right] = -48.5\text{nV}$$

$$V_{OS_MAX} = V_{OSI_MAX} + V_{OS_CMRR_MAX} + V_{OS_PSRR_MAX} + V_{OS_RVRR_MAX} + V_{OS_Drift_MAX} + V_{OS_IB_MAX}$$

$$V_{OS_MAX} = -39.4\mu\text{V}$$

$$R_{shunt_tolerance} = -0.1\% \quad 0.001$$

$$GE_{25\text{C_MAX}} = -0.3\% \quad -0.003$$

$$GE_{Drift_MAX} = -7\text{ppm/C} \cdot (85^\circ\text{C} - 25^\circ\text{C}) \cdot 10^{-6} = -0.00042$$

$$\text{Gain}_{MAX} = 25 \cdot (1 + GE_{25\text{C_MAX}} + GE_{Drift_MAX}) = 25 \cdot (0.99758) = 24.940\text{V/V}$$

$$V_{OUT_MIN_1\mu\text{A}} = [V_{OS_MAX} + I_{LOAD} \cdot R_{SHUNT} \cdot (1 + R_{shunt_tolerance})] \cdot \text{Gain}_{MAX} = 29.9\text{mV}$$

$$V_{OUT_IDEAL_1\mu\text{A}} = [I_{LOAD_MINIMUM} \cdot R_{SHUNT}] \cdot \text{Gain} = 31.0\text{mV}$$

$$\text{Error} = 100 \cdot (V_{OUT_MIN} - V_{OUT_IDEAL}) / V_{OUT_IDEAL}$$

$$\text{Error}_{1\mu\text{A}} = -3.51\%$$

$$\text{Error}_{6\mu\text{A}} = -0.91\%$$

2. Ensure the sensed current range fits within the output dynamic range of the device. This depends upon two specifications: Swing-to-V_{VS} (V_{SP}) and Zero-current Output Voltage (V_{ZL}). V_{ZL} is specified over -40°C to +125°C at V_{VS} = 1.8 V, V_{REF} = 0 V, V_{SENSE} = 0 mV, V_{CM} = 12 V, and R_L = 10 kΩ. Since data sheet conditions do not match the conditions of this design, extrapolate what the maximum V_{ZL} would be.
 - a. Calculate the maximum possible positive offset for testing conditions of V_{ZL}. Call this V_{OS_TestConditions}.
 - b. Convert this input offset into an output offset by multiplying by maximum possible gain.
 - c. Determine the Headroom voltage by taking difference between the V_{ZL_MAX} from data sheet and the previously determined maximum output offset.
 - d. Calculate V_{ZL_MAX} in this design by adding the Headroom voltage to the maximum possible output offset for this design.
 - e. Ensure that the minimum V_{OUT} at 1µA is greater than V_{ZL_MAX}. Note V_{OUT_MIN} at 1µA assumes worst-case scenario of -1% tolerance for R_{SHUNT} and negative input offsets.

$$V_{OS_TestConditions} = V_{OSI_MAX} + |0.9V - 0V| \cdot RVRR_{MAX} + |125^{\circ}C + 40^{\circ}C| \cdot \left(\frac{dV_{OS}}{dT} \right)_{MAX}$$

$$V_{OS_TestConditions} = +15\mu V + 9\mu V + 13.2\mu V = 37.2\mu V$$

$$\text{Headroom } V_{ZL_MAX_DATASHEET} - V_{OS_TestConditions} \cdot \text{Gain}_{MAX}$$

$$\text{Headroom } 3mV - 0.933mV = 2.07mV$$

$$V_{ZL_MAX} = \text{Headroom} + V_{OS_MAX} \cdot \text{Gain}_{MAX} = 2.07mV + (39.4\mu V \cdot 25.061\mu V) = 3.06mV$$

$$V_{OUT_MIN_1\mu A} = 29.9mV > V_{ZL_MAX}$$

- f. Now ensure the maximum V_{OUT} at 104 µA is less than V_{SP_MIN}. Note V_{OUT_MAX} at 104 µA assumes worst-case scenario of +1% tolerance for R_{SHUNT} and positive input offsets.

$$V_{SP_MIN} = V_{VS} - 40mV = 3.26V$$

$$V_{OUT_MAX} = [R_{SHUNT} \cdot (1 + R_{shunt_tolerance}) \cdot I_{LOAD_MAX} + V_{OS_MAX}] \cdot \text{Gain}_{MAX}$$

$$V_{OUT_MAX} = [1240\Omega \cdot (1.001) \cdot 104\mu A - 29.6\mu V] \cdot 25.061\mu V = 3.234V$$

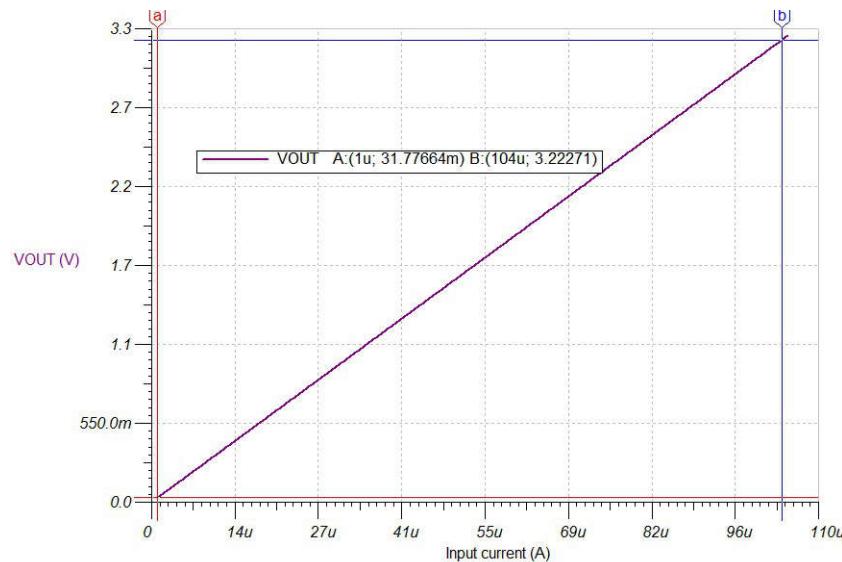
$$V_{OUT_MAX} < V_{SP_MIN}$$

3. Generate *Total Error vs Load Current* curves based upon the total error equations in Step 1. Do this for the typical and maximum data sheet specifications.

Design Simulations

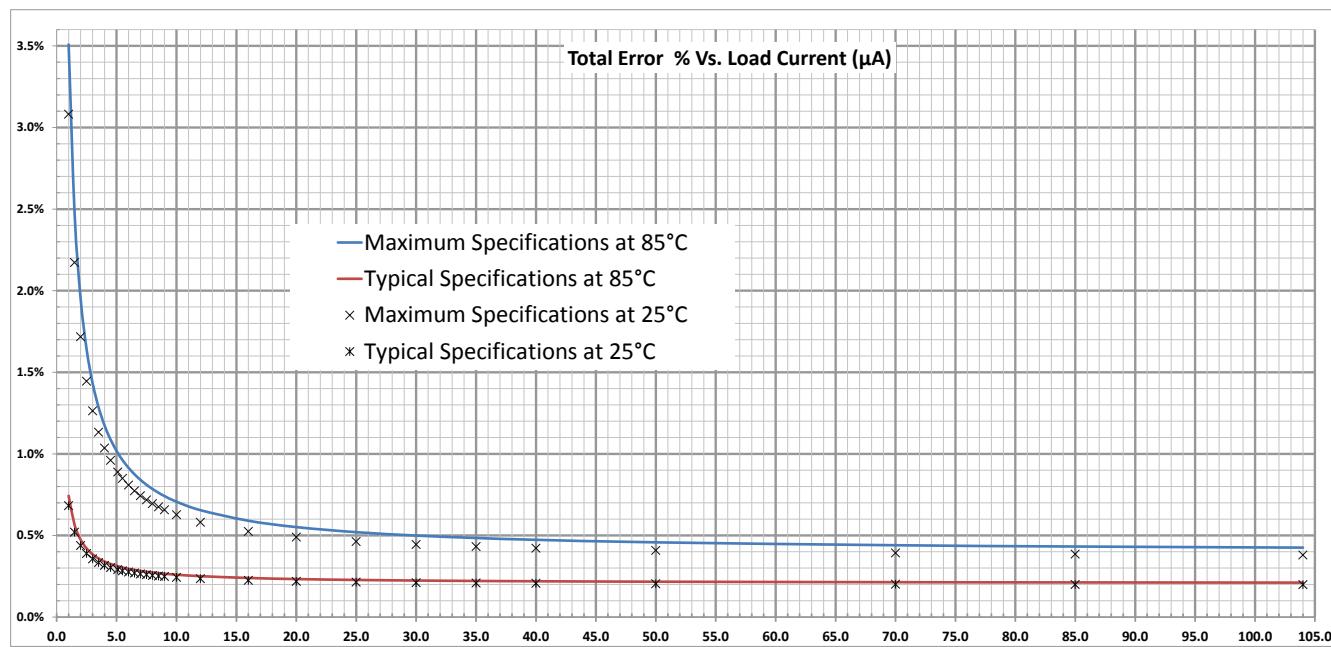
DC Simulation Results

The following graph shows a linear output response for load currents from 1 μ A to 104 μ A



Total Error Calculations

The following graph shows the total absolute error over temperature using both the assured limit specifications and the typical specifications. Note that accuracy is limited by the offset voltage at the lowest current sensed and limited by gain error at higher currents. Active offset chopping limits the error due to temperature.



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOMAI6](#).

Getting Started with Current Sense Amplifiers video series

[Getting started with current sense amplifiers](#)

Application Note on Power-Saving Topologies for TI Current Shunt Monitors

[Extending Voltage Range of Current Shunt Monitor](#)

Current Sense Amplifiers on TI.com

[Current sense amplifiers – Products](#)

For direct support from TI Engineers use the E2E community

[TI E2E™ design support forums](#)

Design Featured Current Shunt Monitor

INA190A1	
V_{VS}	1.8 V to 5 V (operating)
V_{CM}	-0.3 V to 42 V (survivability)
V_{OUT}	Up to (V_{VS}) + 0.3 V
V_{OS}	$\pm 3 \mu V$ to $\pm 15 \mu V$
I_Q	48 μA to 65 μA
I_{IB}	0.5 nA to 3 nA
BW	45 kHz at 25 V/V (A1 gain variant)
# of Channels	1
INA190	

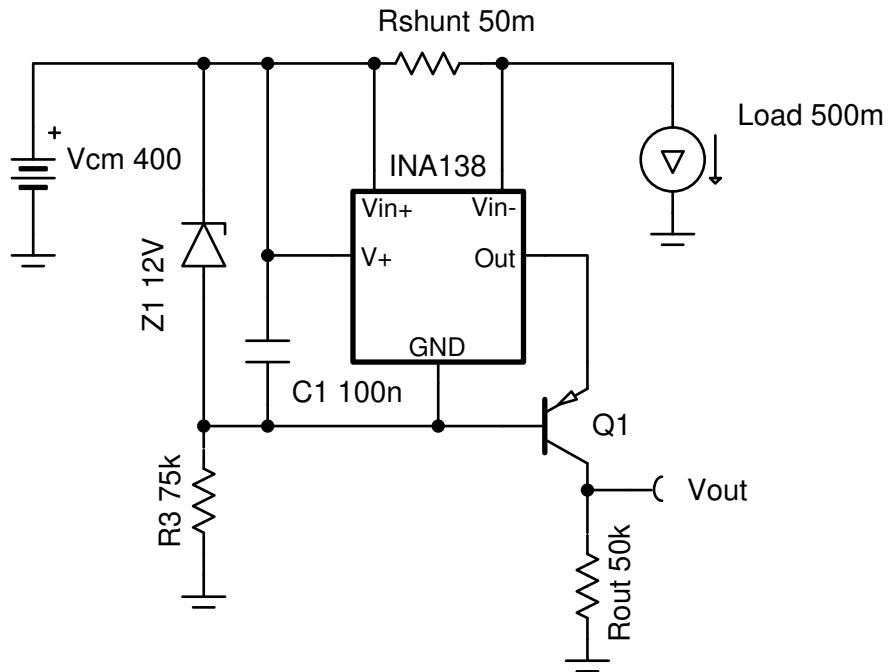
High-Voltage, High-Side Floating Current Sensing Circuit Using Current Output, Current Sense Amplifier



Input		Output		Supply		
I _{load} Min	I _{load} Max	V _{out} Min	V _{out} Max	V _{cm} Min	V _{cm} Max	V _{ee}
0.5 A	9.9 A	250 mV	4.95 V	12 V	400 V	GND (0 V)

Design Description

This cookbook is intended to demonstrate a method of designing an accurate current sensing solution for systems with high common mode voltages. The principle aspect of this design uses a unidirectional circuit to monitor a system with $V_{cm} = 400$ V by floating the supplies of the device across a Zener diode from the supply bus (V_{cm}). This cookbook is based on the [High Voltage 12 V – 400 V DC Current Sense Reference Design](#).



Design Notes

1. The [Getting Started with Current Sense Amplifiers](#) video series introduces implementation, error sources, and advanced topics for using current sense amplifiers.
2. This example is for high V_{CM} , high-side, unidirectional, DC sensing.
3. To minimize error, make the shunt voltage as large as the design will allow. For the INA138 device, keep $V_{sense} \gg 15\text{ mV}$.
4. The relative error due to input offset increases as shunt voltage decreases, so use a current sense amplifier with low offset voltage. A precision resistor for R_{shunt} is necessary because R_{shunt} is a major source of error.
5. The INA138 is a current-output device, so voltages referenced to ground are achieved with a high voltage bipolar junction transistor (BJT).
 - Ensure the transistor chosen for Q1 can withstand the maximum voltage across the collector and emitter (for example, need 400 V, but select > 450 V for margin).
 - Multiple BJTs can be stacked and biased in series to achieve higher voltages
 - High beta of this transistor reduces gain error from current that leaks out of the base

Design Steps

1. Determine the operating load current and calculate R_{shunt} :
 - Recommended V_{sense} is 100mV and maximum recommended is 500 mV, so the following equation can be used to calculate R_{shunt} where $V_{sense} \leq 500\text{ mV}$:
$$R_{shunt} = \frac{V_{sense\ max}}{I_{load\ max}} \rightarrow \frac{0.5\text{V}}{10\text{A}} = 50\text{m}\Omega$$
 - For more accurate and precise measurements over the operating temperature range, a current monitor with integrated shunt resistor can be used in some systems. The benefits of using these devices are explained in [Getting Started with Current Sense Amplifiers, Session 16: Benefits of Integrated Precision Shunt Resistor](#).
2. Choose a Zener diode to create an appropriate voltage drop for the INA138 supply:
 - The Zener voltage of the diode should fall in the INA138 supply voltage range of 2.7 V to 36 V and needs to be larger than the maximum output voltage required.
 - The Zener diode voltage regulates the INA138 supply and protects from transients.
 - Data sheet parameters are defined for 12 V V_{int+} to the GND pin so a 12 V Zener is chosen.
3. Determine the series resistance with the Zener diode:
 - This resistor (R_3) is the main power consumer due to its voltage drop (up to 388 V in this case). If R_3 is too low, it will dissipate more power, but if it is too high R_3 will not allow the Zener diode to avalanche properly. Since the data sheet specifies I_Q for $V_S = 5\text{ V}$, estimate the maximum quiescent current of the INA138 device at $V_S = 12\text{ V}$ to be 108 μA and calculate R_3 using the bias current of the Zener diode, 5 mA, as shown:

$$R_3 = \frac{V_{CM} - V_{zener}}{I_{zener} + I_{INA138}} = \frac{400\text{V} - 12\text{V}}{5\text{mA} + 108\mu\text{A}} \approx 75.96\text{k}\Omega$$

standard value $\rightarrow 75\text{k}\Omega$

- The power consumption of this resistor is calculated using the following equation:
- $$\text{Power}_{R3} = \frac{(V_{cm} - V_{Zener})^2}{R3} \rightarrow \frac{(400\text{V} - 12\text{V})^2}{75\text{k}\Omega} \approx 2.007\text{W}$$
4. Calculate R_{out} using the equation for output current in the INA138 data sheet.
 - This system is designed for 10 V/V gain where $V_{out} = 1\text{ V}$ if $V_{sense} = 100\text{ mV}$:

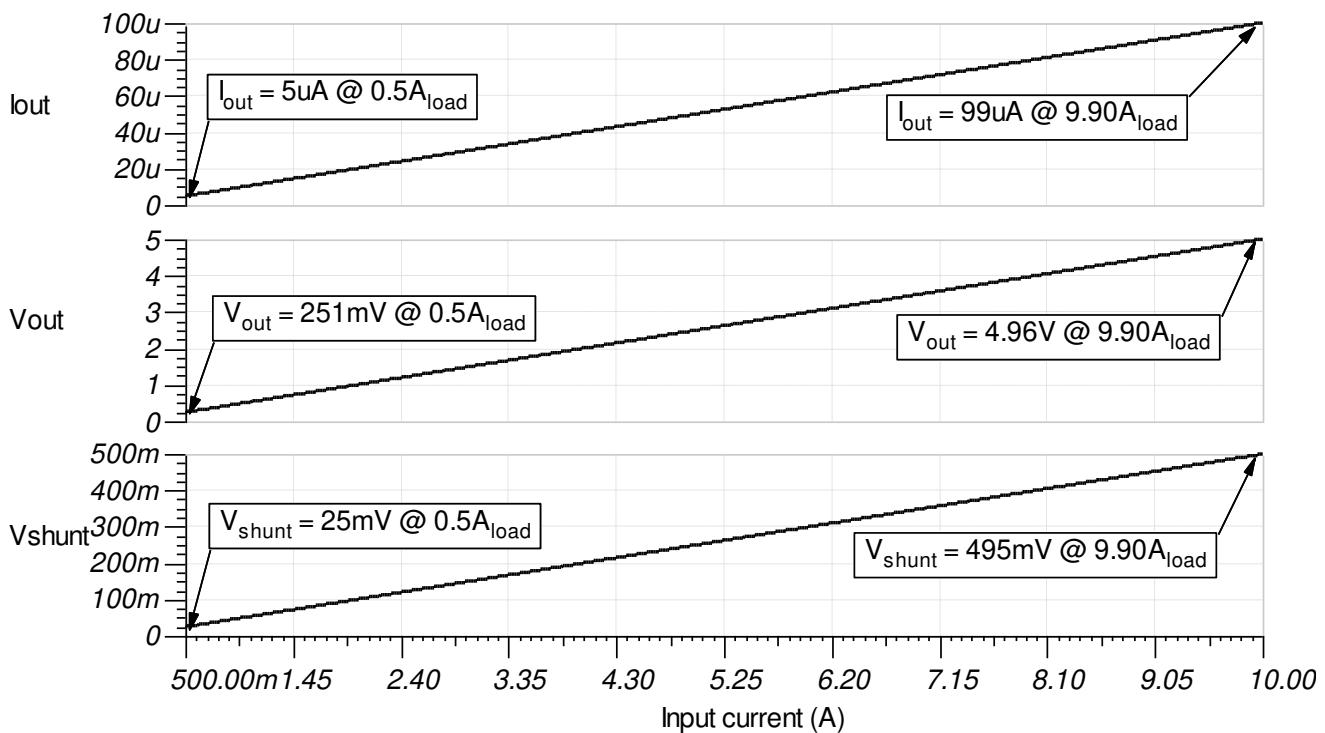
$$I_{\text{out INA138}} = 200 \frac{\mu\text{A}}{\text{V}} \times (V_{\text{sense max}}) \rightarrow 200 \frac{\mu\text{A}}{\text{V}} \times (0.5\text{V}) = 100\mu\text{A}$$

$$R_{\text{out}} = \frac{V_{\text{out max}}}{I_{\text{out INA138}}} \rightarrow \frac{5\text{V}}{100\mu\text{A}} = 50\text{k}\Omega$$

Design Simulations

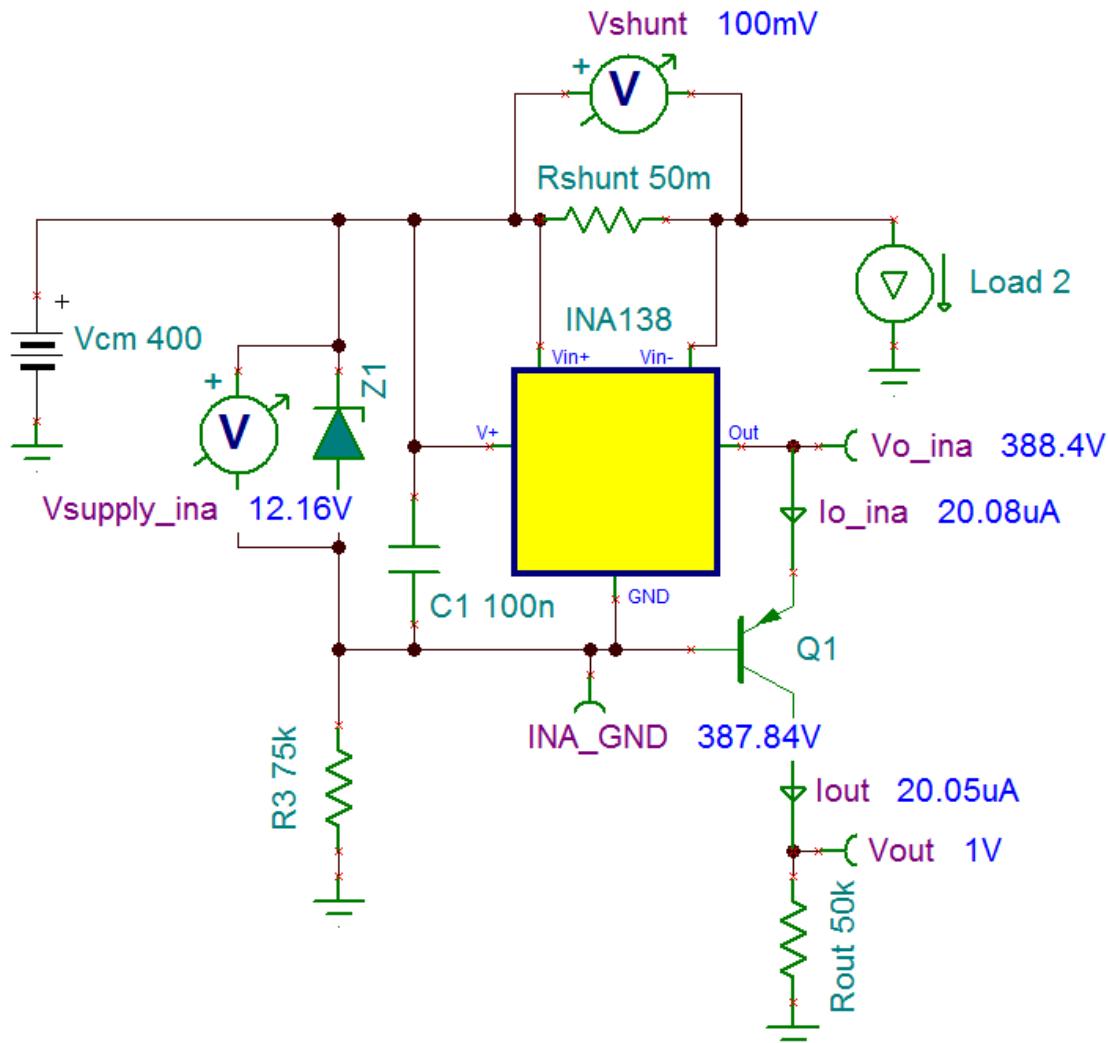
DC Simulation Results

The following graph shows a linear output response for load currents from 0.5 A to 10 A and $12 \text{ V} \leq V_{\text{cm}} \leq 400 \text{ V}$. I_{out} and V_{out} remain constant over a varying V_{cm} once the Zener diode is reverse biased.



Steady State Simulation Results

The following image shows this system in DC steady state with a 2 A load current. The output voltage is 10× greater than the measured voltage across R_{shunt} .



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SGLC001](#).

Getting Started with Current Sense Amplifiers video series:

<https://training.ti.com/getting-started-current-sense-amplifiers>

Abstract on Extending Voltage Range of Current Shunt Monitor:

Extending Voltage Range of Current Shunt Monitor

High Voltage 12 V – 400 V DC Current Sense Reference Design:

[TIDA=00332](#)

Cookbook Design Files:

[SGLC001](#)

Current Sense Amplifiers on TI.com:

[Current sense amplifiers - Products](#)

For direct support from TI Engineers use the E2E community:

[TI E2E™ design support forums](#)

Design Featured Current Shunt Monitor

INA138	
V_{ss}	2.7 V to 36 V
$V_{in\ cm}$	2.7 V to 36 V
V_{out}	Up to (V_+) -0.8 V
V_{os}	$\pm 0.2\text{ mV}$ to $\pm 1\text{ mV}$
I_q	25 μA to 45 μA
I_b	2 μA
UGBW	800 kHz
# of Channels	1
INA138	

Design Alternate Current Shunt Monitor

INA168	
V_{ss}	2.7 V to 60 V
$V_{in\ cm}$	2.7 V to 60 V
V_{out}	Up to (V_+) -0.8 V
V_{os}	$\pm 0.2\text{ mV}$ to $\pm 1\text{ mV}$
I_q	25 μA to 45 μA
I_b	2 μA
UGBW	800 kHz
# of Channels	1
INA168	

AC-coupled transimpedance amplifier circuit



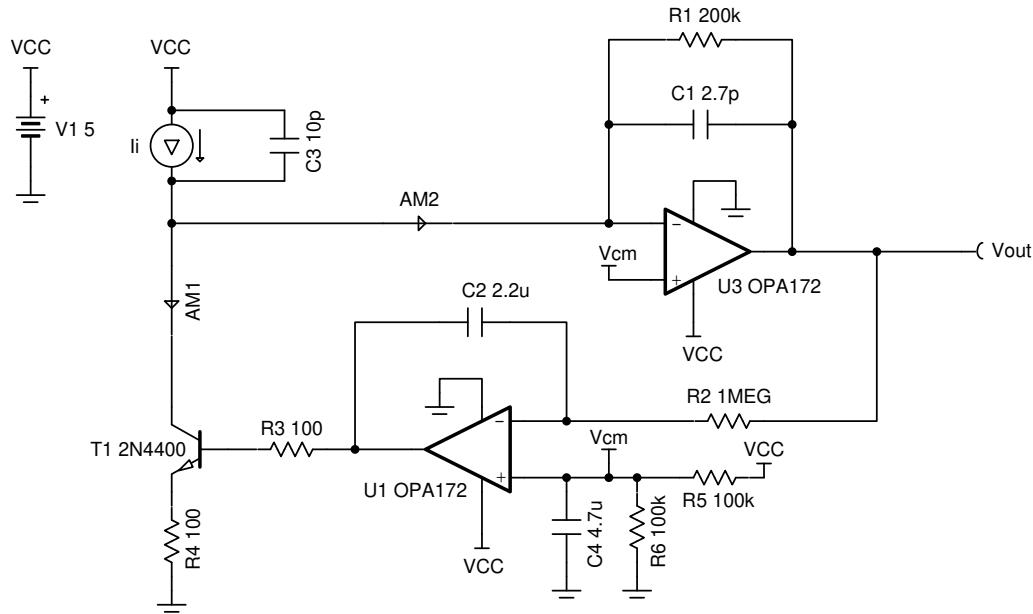
Amplifiers

Design Goals

Input Current		Ambient light current	Output voltage		Target Bandwidth	Supply	
I _{iMin}	I _{iMax}		V _{oMin}	V _{oMax}		V _{cc}	V _{ee}
-10µA	10µA	100µA	0.5V	4.5V	300kHz	5V	0V

Design Description

This circuit uses an op amp configured as a transimpedance amplifier to amplify the AC signal of a photodiode (modeled by I_i and C_3). The circuit rejects DC signals using a transistor to sink DC current out of the photodiode through the use of an integrator in a servo loop. The bias voltage applied to the non-inverting input prevents the output from saturating to the negative supply rail in the absence of input current.



Design Notes

1. Use a JFET or CMOS input op amp with low-bias current to reduce DC errors.
2. A capacitor placed in parallel with the feedback resistor will limit bandwidth, improve stability and help reduce noise.
3. The junction capacitance of photodiode changes with reverse bias voltage which will influence the stability of the circuit.
4. Reverse-biasing the photodiode can reduce the effects of dark current.
5. A resistor, R_3 , may be needed on the output of the integrator amplifier.
6. An emitter degeneration resistor, R_4 , should be used to help stabilize the BJT.
7. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions.

Design Steps

The transfer function of the circuit is:

$$V_{\text{out}} = -I_i \times R_1$$

1. Calculate the value of the feedback resistor, R_1 , to produce the desired output swing.

$$R_1 = \frac{V_{\text{oMax}} - V_{\text{oMin}}}{I_{\text{iMax}} - I_{\text{iMin}}} = \frac{4.5V - 0.5V}{10\mu A - (-10\mu A)} = 200k\Omega$$

2. Calculate the feedback capacitor to limit the signal bandwidth.

$$C_1 = \frac{1}{2\pi \times R_1 \times f_p} = \frac{1}{2\pi \times 200k\Omega \times 300\text{kHz}} = 2.65\text{pF} \approx 2.7\text{pF} \text{ (Standard Value)}$$

3. Calculate the gain bandwidth of the amplifier needed for the circuit to be stable.

$$\text{GBW} = \frac{C_i + C_1}{2\pi \times R_1 \times C_1^2} = \frac{23\text{pF} + 2.7\text{pF}}{2\pi \times 200k\Omega \times (2.7\text{pF})^2} = 2.97\text{MHz}$$

Where:

$$C_i = C_{\text{pd}} + C_b + C_d + C_{\text{cm}} = 10\text{pF} + 5\text{pF} + 4\text{pF} + 4\text{pF} = 23\text{pF}$$

Given:

- C_{pd} : Junction capacitance of photodiode
- C_b : Output capacitance of BJT
- C_d : Differential input capacitance of the amplifier
- C_{cm} : Common-mode input capacitance of the inverting input

4. Set the cutoff frequency of the integrator circuit, f_l , to 0.1Hz to only allow signals near DC to be subtracted from the photodiode output current. The cutoff frequency is set by R_2 and C_2 . Select R_2 as $1M\Omega$.

$$C_2 = \frac{1}{2\pi \times R_2 \times f_l} = \frac{1}{2\pi \times 1M\Omega \times 0.1\text{Hz}} = 1.59\mu F \approx 2.2\mu F \text{ (Standard Value)}$$

5. Select R_3 as 100Ω to isolate the capacitance of the BJT from op amp and stabilize the amplifier. For more information on stability analysis, see the [Design References](#) section [2].
6. Bias the output of the circuit by setting the input common mode voltage of the integrator circuit to mid-supply. Select R_5 and R_6 as $100k\Omega$.

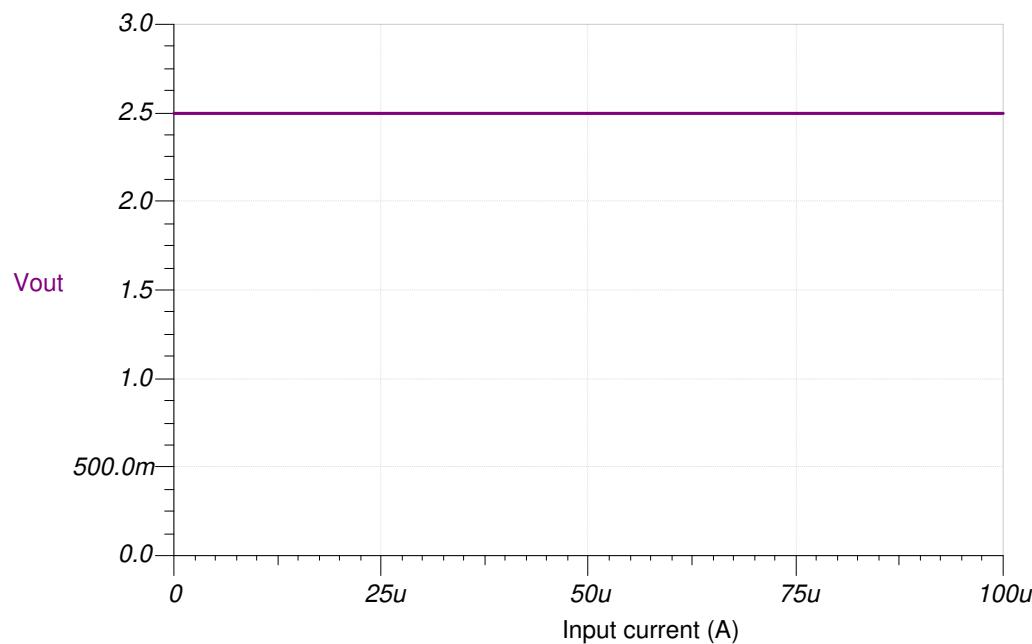
$$V_{\text{cm}} = \frac{R_6}{R_5 + R_6} \times V_{\text{cc}} = \frac{100k\Omega}{100k\Omega + 100k\Omega} \times 5V = 2.5V$$

7. Calculate capacitor C_2 to filter the power supply and resistor noise. Set the cutoff frequency to 1Hz.

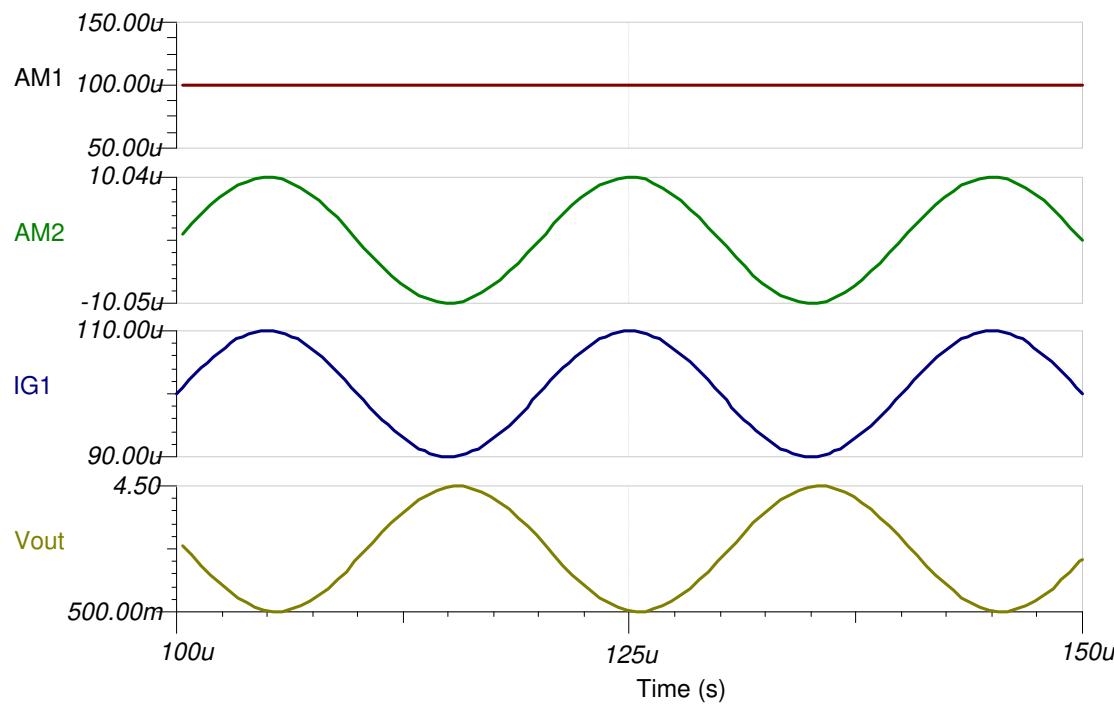
$$C_2 = \frac{1}{2\pi \times (R_2 || R_3) \times 1\text{Hz}} = \frac{1}{2\pi \times (100k\Omega || 100k\Omega) \times 1\text{Hz}} = 3.183\mu F \approx 4.7\mu F$$

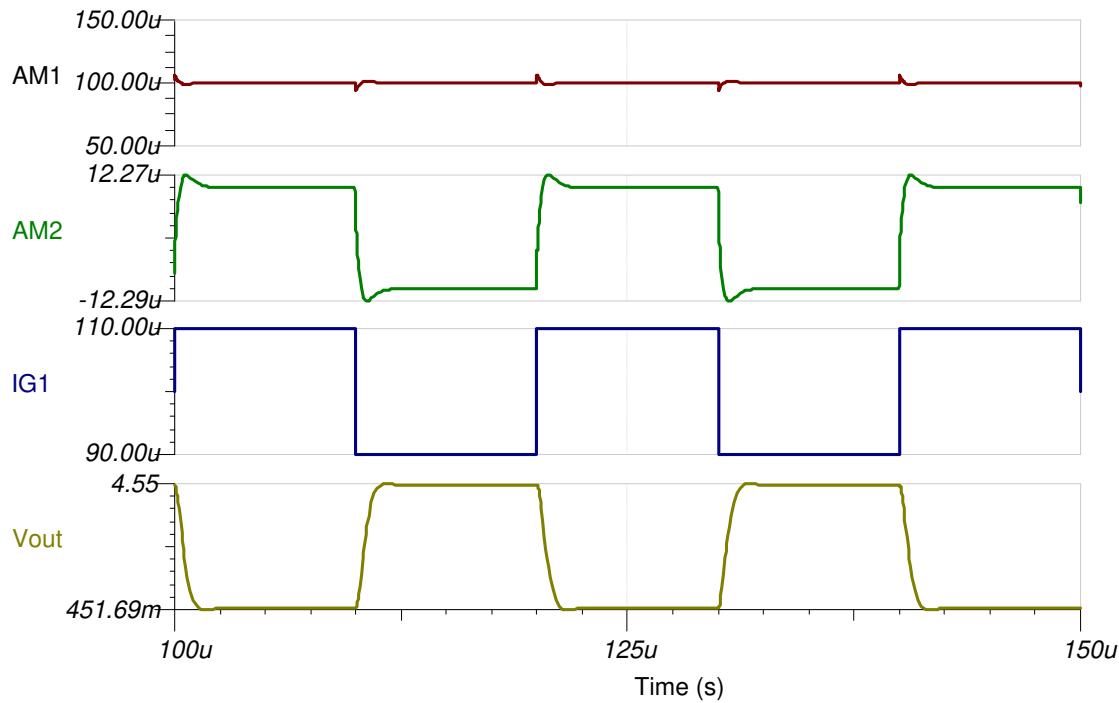
Design Simulations

DC Simulation Results

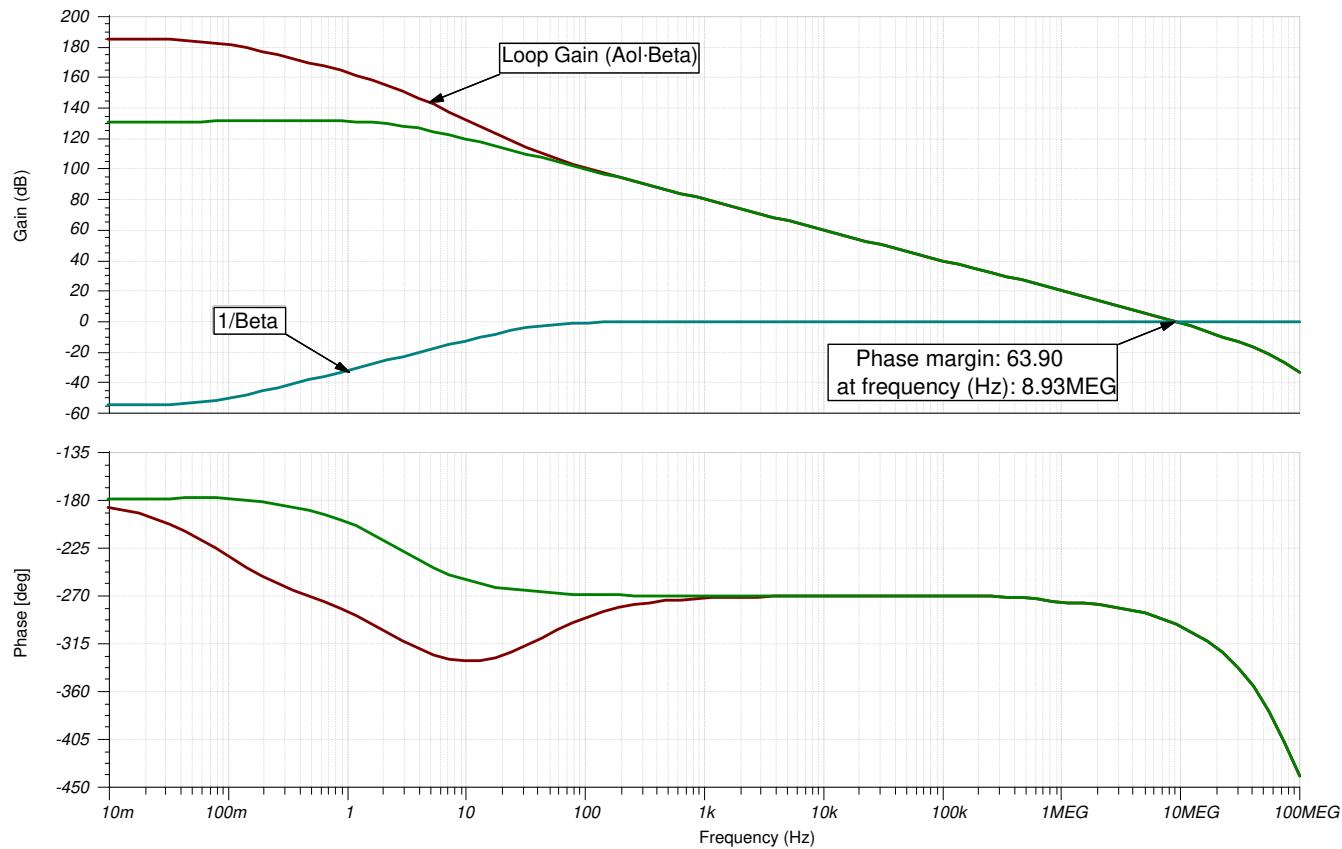


Transient Simulation Results

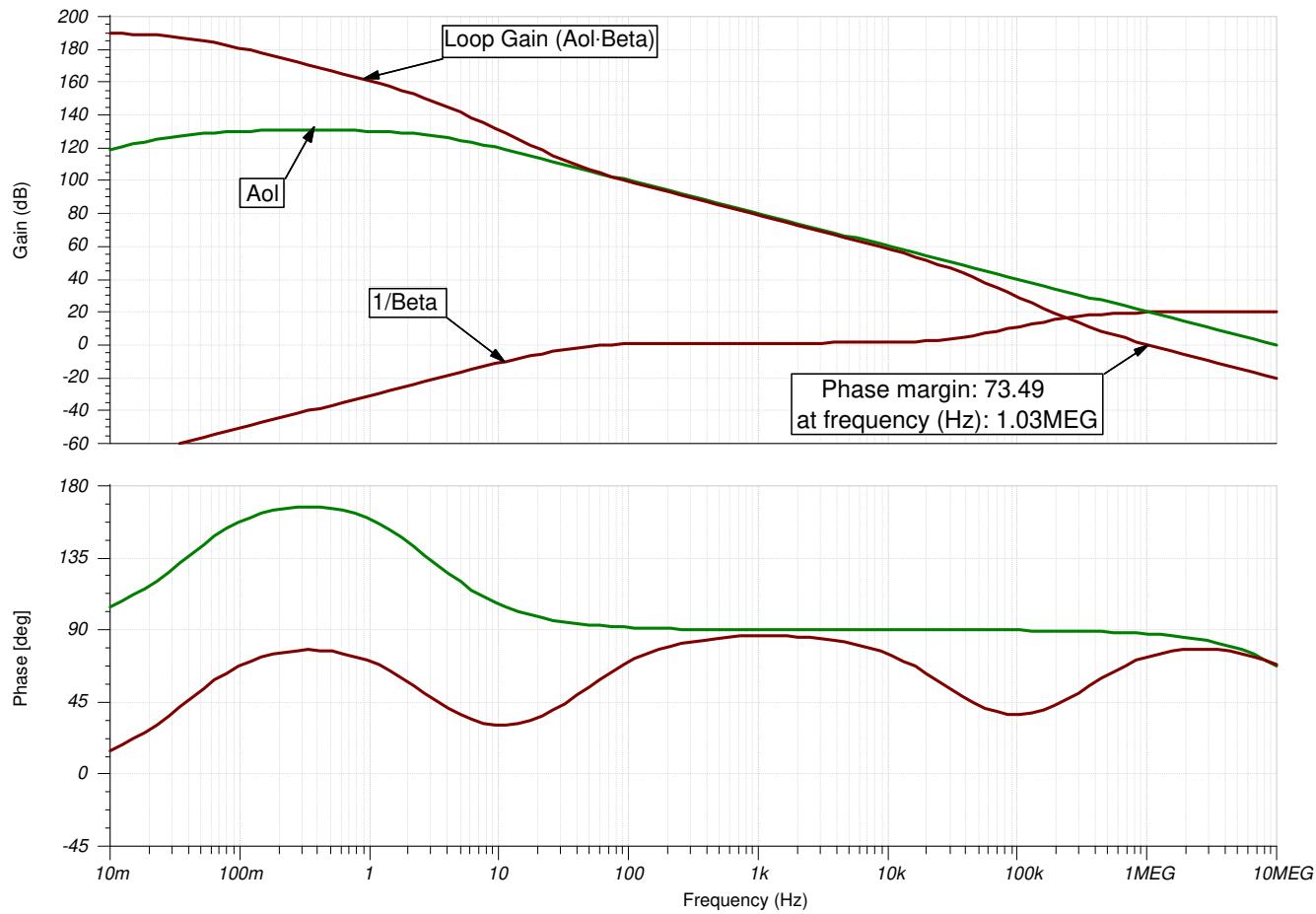




Integrator Open Loop Stability



TIA Stability Results



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.
2. [TI Precision Labs](#)

Design Featured Op Amp

OPA172	
V_{cc}	±2.25V to ±18V, 4.5V to 36V
V_{inCM}	(V-) – 0.1V to (V+) – 2V
V_{out}	Rail-to-rail
V_{os}	0.2mV
I_q	1.6mA
I_b	8pA
UGBW	10MHz
SR	10V/µs
#Channels	1,2,4
www.ti.com/product/OPA172	

Design Alternate Op Amps

	OPA2991	TLV9042
V_{ss}	±1.35V to ±20V, 2.7V to 40V	±0.6V to ±2.75V, 1.2V to 5.5V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{out}	Rail-to-rail	Rail-to-rail
V_{os}	125µV	0.6mV
I_q	560µV	10uA
I_b	1pA	1pA
UGBW	4.5MHz	350kHz
SR	20V/µs	0.2V/us
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/OPA2991	www.ti.com/product/TLV9042

Transimpedance amplifier with T-network circuit



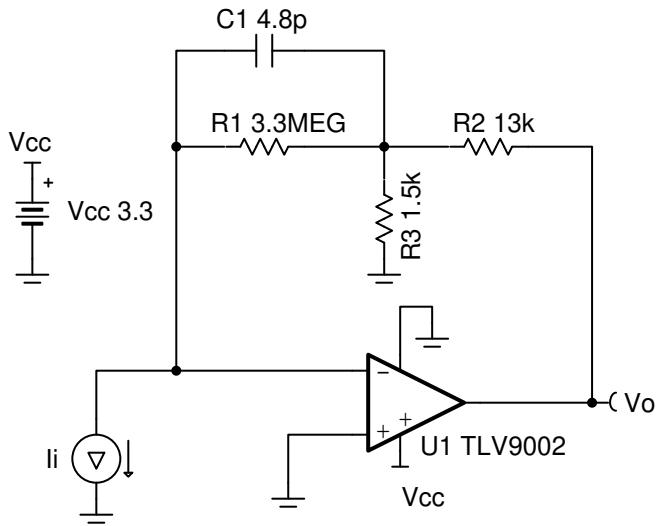
Amplifiers

Design Goals

Input		Output		BW	Supply	
I _{iMin}	I _{iMax}	V _{oMin}	V _{oMax}	f _p	V _{cc}	V _{ee}
0A	100nA	0V	3.2V	10kHz	3.3V	0V

Design Description

This transimpedance amplifier with a T-network feedback configuration converts an input current into an output voltage. The current-to-voltage gain is based on the T-network equivalent resistance which is larger than any of the resistors used in the circuit. Therefore, the T-network feedback configuration circuit allows for very high gain without the use of large resistors in the feedback or a second gain stage, reducing noise, stability issues, and errors in the system.



Design Notes

1. C₁ and R₁ set the input signal cutoff frequency, f_p.
2. Capacitor C₁ in parallel with R₁ helps limit the bandwidth, reduce noise, and also improve the stability of the circuit if high-value resistors are used.
3. The common-mode voltage is the voltage at the non-inverting input and does not vary with input current.
4. A bias voltage can be added to the non-inverting input to bias the output voltage above the minimum output swing for 0A input current.
5. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
6. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth see the [Design References](#) section.

Design Steps

The transfer function of this circuit follows:

$$V_o = I_i \times \left(\frac{R_2 \times R_1}{R_3} + R_1 + R_2 \right)$$

1. Calculate the required gain:

$$\text{Gain} = \frac{V_{o\text{Max}}}{I_{o\text{Max}}} = \frac{3.2V}{100nA} = 3.2 \times 10^7 \frac{V}{A}$$

2. Choose the resistor values to set the pass-band gain:

$$\text{Gain} = \left(\frac{R_2 \times R_1}{R_3} + R_1 + R_2 \right)$$

Since R_1 will be the largest resistor value in the system choose this value first then choose R_2 and calculate R_3 . Select $R_1 = 3.3M\Omega$ and $R_2 = 13k\Omega$. R_1 is very large due to the large transimpedance gain of the circuit. R_2 is in the $\sim 10k$ ohm range so the op amp can drive it easily.

$$R_3 = \left(\frac{R_2 \times R_1}{\text{Gain} - R_1 - R_2} \right) = \left(\frac{13k\Omega \times 3.3M\Omega}{3.2 \times 10^7 \frac{V}{A} - 3.3M\Omega - 13k\Omega} \right) = 1.5k\Omega$$

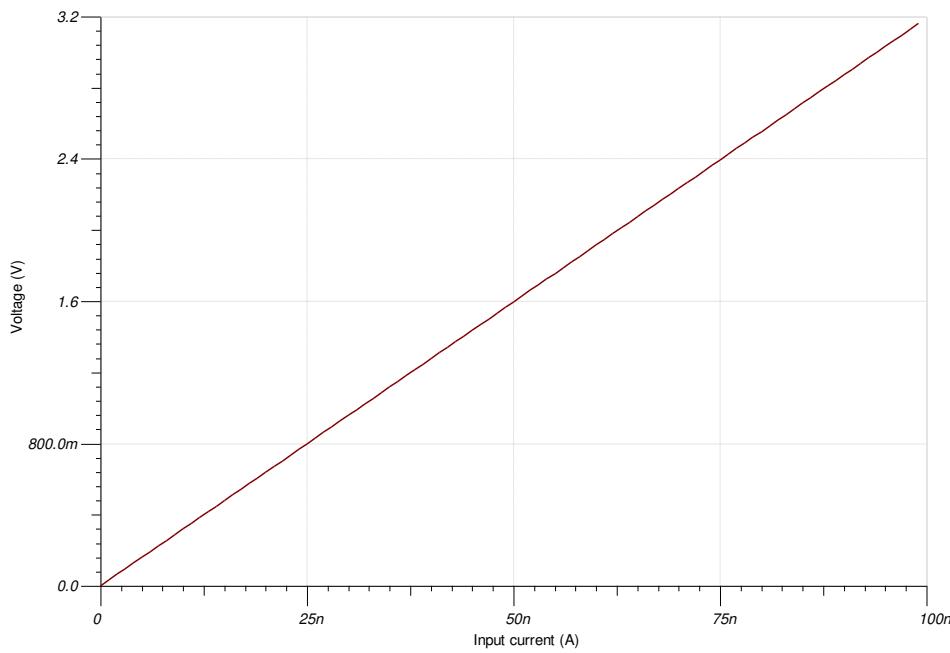
3. Calculate C_1 to set the location of f_p .

$$C_1 = \frac{1}{2\pi \times R_1 \times f_p} = \frac{1}{2\pi \times 3.3M\Omega \times 10kHz} = 4.82pF \approx 4.8pF \text{ (Standard Value)}$$

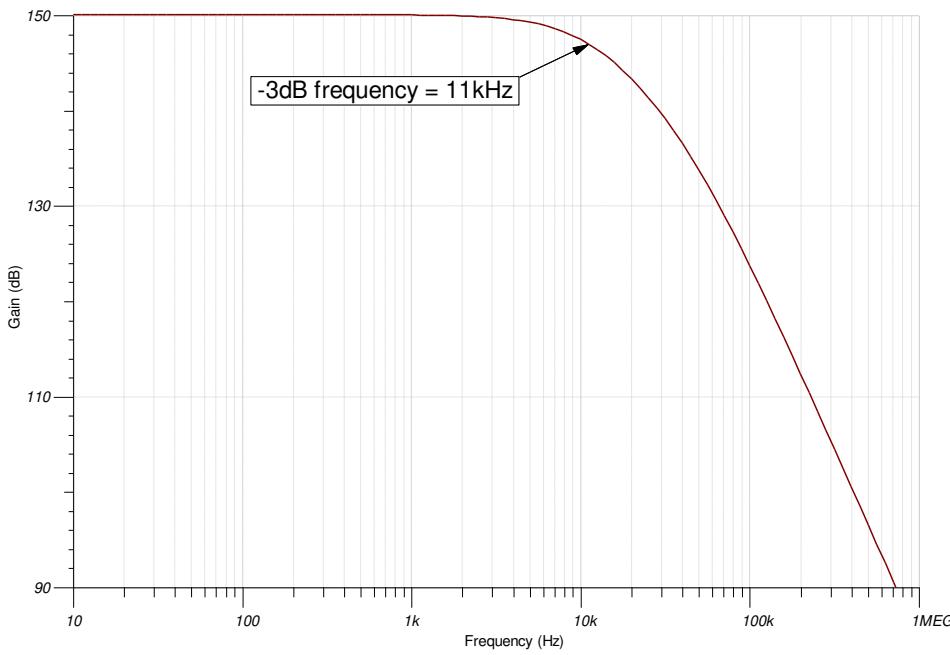
4. Run a stability analysis to make sure that the circuit is stable. For more information on how to run a stability analysis see the [TI Precision Labs - Op amp: Stability](#) video.

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.
2. See SPICE file, [SBOMB39](#).
3. See TIPD176, [www.ti.com/tool/tipd176](#).
4. For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit [TI Precision Labs](#).

Design Featured Op Amp

TLV9002	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.4mV
I_q	60µA
I_b	5pA
UGBW	1MHz
SR	2V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9002	

Design Alternate Op Amp

OPA375	
V_{cc}	2.25V to 5.5V
V_{inCM}	V _{ee} to (V _{cc} − 1.2V)
V_{out}	Rail-to-rail
V_{os}	0.15mV
I_q	890µA
I_b	10pA
UGBW	10MHz
SR	4.75V/µs
#Channels	1
www.ti.com/product/OPA375	

Low-Drift, Low-Side, Bidirectional Current Sensing Circuit with Integrated Precision Gain

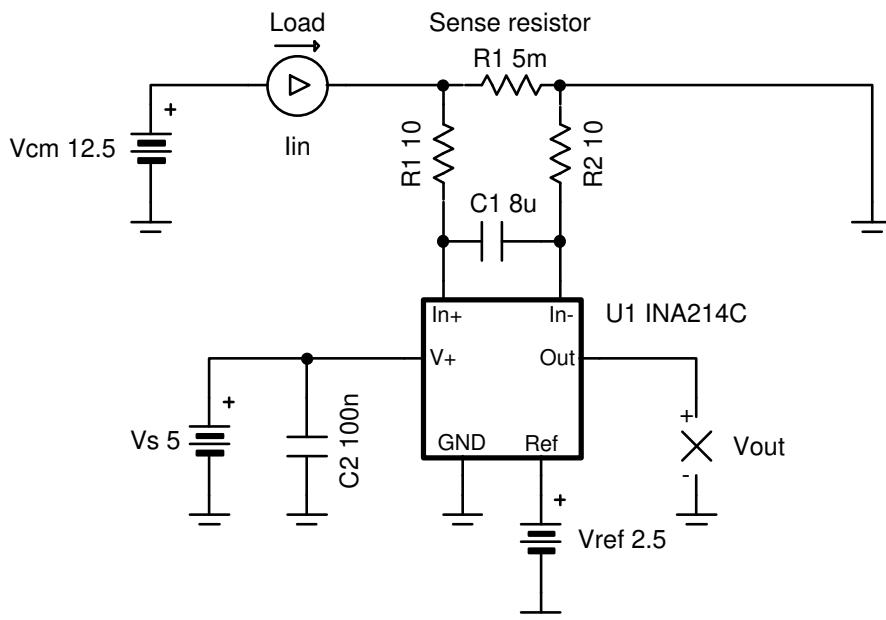


Design Goals

Input			Output		Supply	
I _{inMin}	I _{inMax}	V _{cm}	V _{outMin}	V _{outMax}	V _s	V _{ref}
-4A	4A	12.5 V	0.5 V	4.5 V	5	2.5 V

Design Description

The low-side bidirectional current-shunt monitor solution illustrated in the following image can accurately measure currents from -4A to 4A, and the design parameters can easily be changed for different current measurement ranges. Current-shunt monitors from the INA21x family have integrated precision gain resistors and a zero-drift architecture that enables current sensing with maximum drops across the shunt as low as 10mV full-scale.



Design Notes

- To avoid additional error, use $R_1 = R_2$ and keep the resistance as small as possible (no more than 10Ω , as stated in [INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors](#)).
- Low-side sensing should not be used in applications where the system load cannot withstand small ground disturbances or in applications that need to detect load shorts.
- The [Getting Started with Current Sense Amplifiers](#) video series introduces implementation, error sources, and advanced topics that are good to know when using current sense amplifiers.

Design Steps

- Determine V_{ref} based on the desired current range:

With a current range of -4A to 4A, then half of the range is below 0V, so set:

$$V_{ref} = \frac{1}{2} V_s = \frac{5}{2} = 2.5 \text{ V}$$

- Determine the desired shunt resistance based on the maximum current and maximum output voltage:

To not exceed the swing-to-rail and to allow for some margin, use $V_{outMax} = 4.5\text{V}$. This, combined with maximum current of 4A and the V_{ref} calculated in step 1, can be used to determine the shunt resistance using the equation:

$$R_1 = \frac{V_{outMax} - V_{ref}}{\text{Gain} \times I_{loadMax}} = \frac{4.5 - 2.5}{100 \times 4} = 5 \text{ m}\Omega$$

- Confirm V_{out} will be within the desired range:

At the maximum current of 4A, with Gain = 100V/V, $R_1 = 5\text{m}\Omega$, and $V_{ref} = 2.5\text{V}$:

$$V_{out} = I_{load} \times \text{Gain} \times R_1 + V_{ref} = 4 \times 100 \times 0.005 + 2.5 = 4.5 \text{ V}$$

At the minimum current of -4A, with Gain = 100V/V, $R_1 = 5\text{m}\Omega$, and $V_{ref} = 2.5\text{V}$:

$$V_{out} = I_{load} \times \text{Gain} \times R_1 + V_{ref} = -4 \times 100 \times 0.005 + 2.5 = 0.5 \text{ V}$$

- Filter cap selection:

To filter the input signal at 1kHz, using $R_1 = R_2 = 10\Omega$:

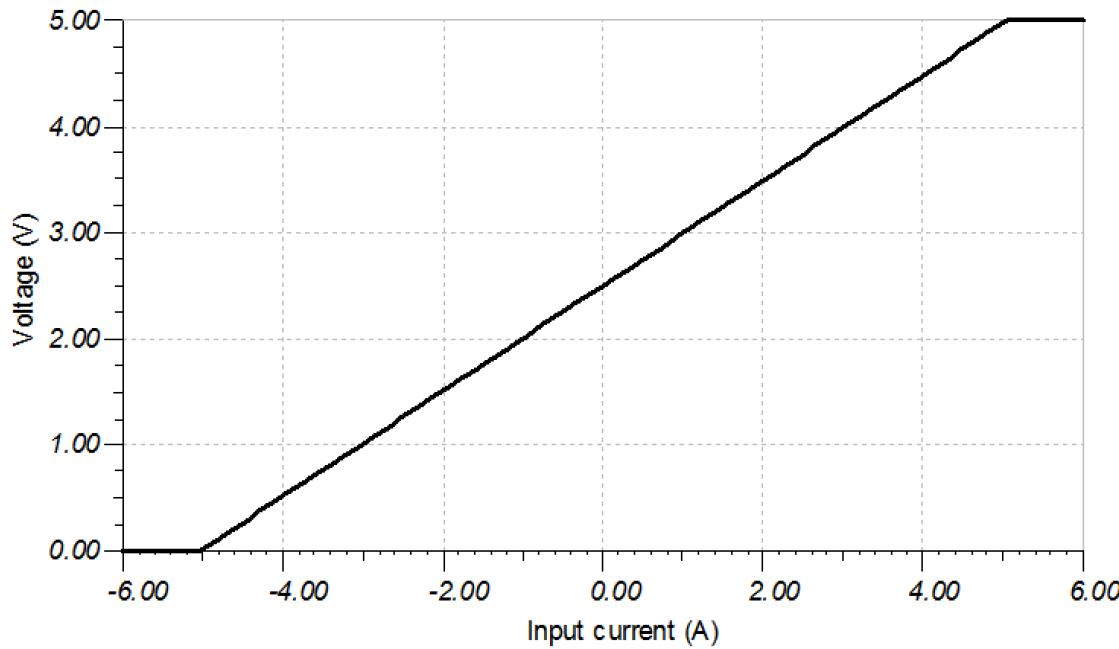
$$C_1 = \frac{1}{2 \pi (R_1 + R_2) F_{-3 \text{ dB}}} = \frac{1}{2 \pi (10 + 10) 1000} = 7.958 \times 10^{-6} \approx 8 \mu\text{F}$$

For more information on signal filtering and the associated gain error, see [INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors](#).

Design Simulations

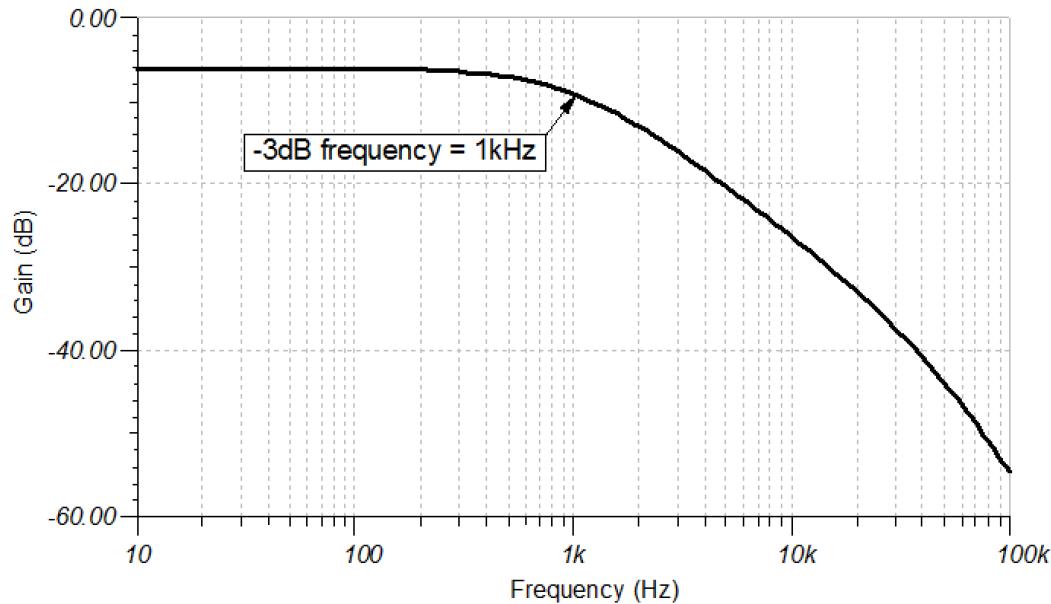
DC Analysis Simulation Results

The following plot shows the simulated output voltage V_{out} for the given input current I_{in} .



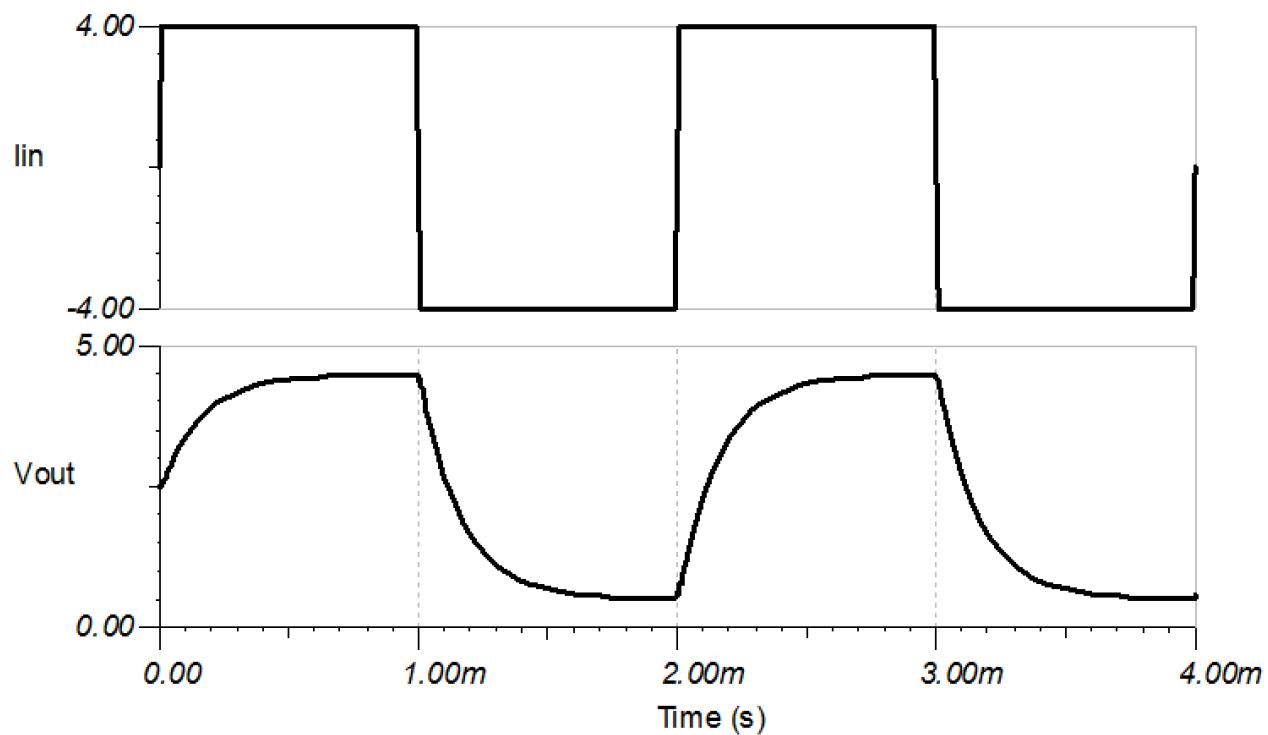
AC Analysis Simulation Results

The following plot shows the simulated gain vs frequency, as designed for in the design steps.



Transient Analysis Simulation Results

The following plot shows the simulated delay and settling time of the output V_{out} for a step response in I_{in} from $-4A$ to $4A$.



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

Circuit SPICE simulation File: <http://proddms.itg.ti.com/fnview/sboc518>

Getting Started with Current Sense Amplifiers video series: <https://training.ti.com/getting-started-current-sense-amplifiers>

Current Sense Amplifiers on TI.com: <http://www.ti.com/amplifier-circuit/current-sense/products.html>

For direct support from TI Engineers use the E2E community: <http://e2e.ti.com>

Design Featured Current Sense Amplifier

INA214C	
V_s	2.7 V to 26 V
V_{cm}	GND-0.1 V to 26 V
V_{out}	GND-0.3 V to $V_s+0.3$ V
V_{os}	$\pm 1\mu V$ typical
I_q	65 μA typical
I_b	28 μA typical
http://www.ti.com/product/INA214	

Design Alternate Current Sense Amplifiers

INA199C	
V_s	2.7 V to 26 V
V_{cm}	GND-0.1 V to 26 V
V_{out}	GND-0.3 V to $V_s+0.3$ V
V_{os}	$\pm 5\mu V$ typical
I_q	65 μA typical
I_b	28 μA typical
http://www.ti.com/product/INA199	

INA181	
V_s	2.7 V to 5.5 V
V_{cm}	GND-0.2 V to 26 V
V_{out}	GND-0.3 V to $V_s+0.3$ V
V_{os}	$\pm 100\mu V$ typical
I_q	65 μA typical
I_b	195 μA typical
http://www.ti.com/product/INA181	

Revision History

Revision	Date	Change
A	December 2020	Changed step three from "At the minimum current of 4A" to "At the minimum current of -4A"

Single-supply, low-side, unidirectional current-sensing circuit

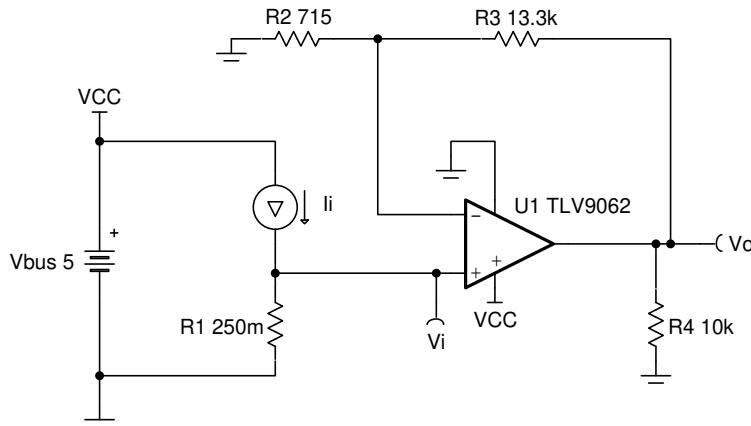


Design Goals

Input		Output		Supply		Full-Scale Range Error
$I_{i\text{Max}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	V_{cc}	V_{ee}	$\text{FSR}_{\text{Error}}$
1A	250mV	50mV	4.9V	5V	0V	0.2%

Design Description

This single-supply, low-side, current sensing solution accurately detects load current up to 1A and converts it to a voltage between 50mV and 4.9V. The input current range and output voltage range can be scaled as necessary and larger supplies can be used to accommodate larger swings.



Design Notes

1. Use the op amp linear output operating range, which is usually specified under the test conditions.
2. The common-mode voltage is equal to the input voltage.
3. Tolerance of the shunt resistor and feedback resistors will determine the gain error of the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. If trying to detect zero current with output swing to GND, a negative charge pump (such as LM7705) can be used as the negative supply in this design to maintain linearity for output signals near 0V. [5]
6. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
7. The small-signal bandwidth of this circuit depends on the gain of the circuit and gain bandwidth product (GBP) of the amplifier.
8. Filtering can be accomplished by adding a capacitor in parallel with R_3 . Adding a capacitor in parallel with R_3 will also improve stability of the circuit if high-value resistors are used.
9. For more information on op amp linear operating region, stability, capacitive load drive, driving ADCs, and bandwidth please see the Design References section.

Design Steps

The transfer function for this circuit is given below.

$$V_o = I_i \times R_1 \times \left(1 + \frac{R_3}{R_2}\right)$$

1. Define the full-scale shunt voltage and calculate the maximum shunt resistance.

$$V_{iMax} = 250 \text{ mV} \quad \text{at} \quad I_{iMax} = 1 \text{ A}$$

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{250 \text{ mV}}{1 \text{ A}} = 250 \text{ m} \Omega$$

2. Calculate the gain required for maximum linear output voltage.

$$V_{iMax} = 250 \text{ mV} \quad \text{and} \quad V_{oMax} = 4.9 \text{ V}$$

$$\text{Gain} = \frac{V_{oMax}}{V_{iMax}} = \frac{4.9 \text{ V}}{250 \text{ mV}} = 19.6 \frac{\text{V}}{\text{mV}}$$

3. Select standard values for R_2 and R_3 .

From [Analog Engineer's calculator](#), use "Find Amplifier Gain" and get resistor values by inputting gain ratio of 19.6.

$$R_2 = 715 \Omega \text{ (0.1\% Standard Value)}$$

$$R_3 = 13.3 \text{ k}\Omega \text{ (0.1\% Standard Value)}$$

4. Calculate minimum input current before hitting output swing-to-rail limit. I_{iMin} represents the minimum accurately detectable input current.

$$V_{oMin} = 50 \text{ mV}; \quad R_1 = 250 \text{ m} \Omega$$

$$V_{iMin} = \frac{V_{oMin}}{\text{Gain}} = \frac{50 \text{ mV}}{19.6 \frac{\text{V}}{\text{mV}}} = 2.55 \text{ mV}$$

$$I_{iMin} = \frac{V_{iMin}}{R_1} = \frac{2.55 \text{ mV}}{250 \text{ m} \Omega} = 10.2 \text{ mA}$$

5. Calculate Full scale range error and relative error. V_{os} is the typical offset voltage found in data sheet.

$$\text{FSR}_{\text{error}} = \left(\frac{V_{os}}{V_{iMax} - V_{iMin}} \right) \times 100 = \left(\frac{0.3 \text{ mV}}{247.45 \text{ mV}} \right) \times 100 = 0.121 \text{ \%}$$

$$\text{Relative Error at } I_{iMax} = \left(\frac{V_{os}}{V_{iMax}} \right) \times 100 = \left(\frac{0.3 \text{ mV}}{250 \text{ mV}} \right) \times 100 = 0.12 \text{ \%}$$

$$\text{Relative Error at } I_{iMin} = \left(\frac{V_{os}}{V_{iMin}} \right) \times 100 = \left(\frac{0.3 \text{ mV}}{2.5 \text{ mV}} \right) \times 100 = 12 \text{ \%}$$

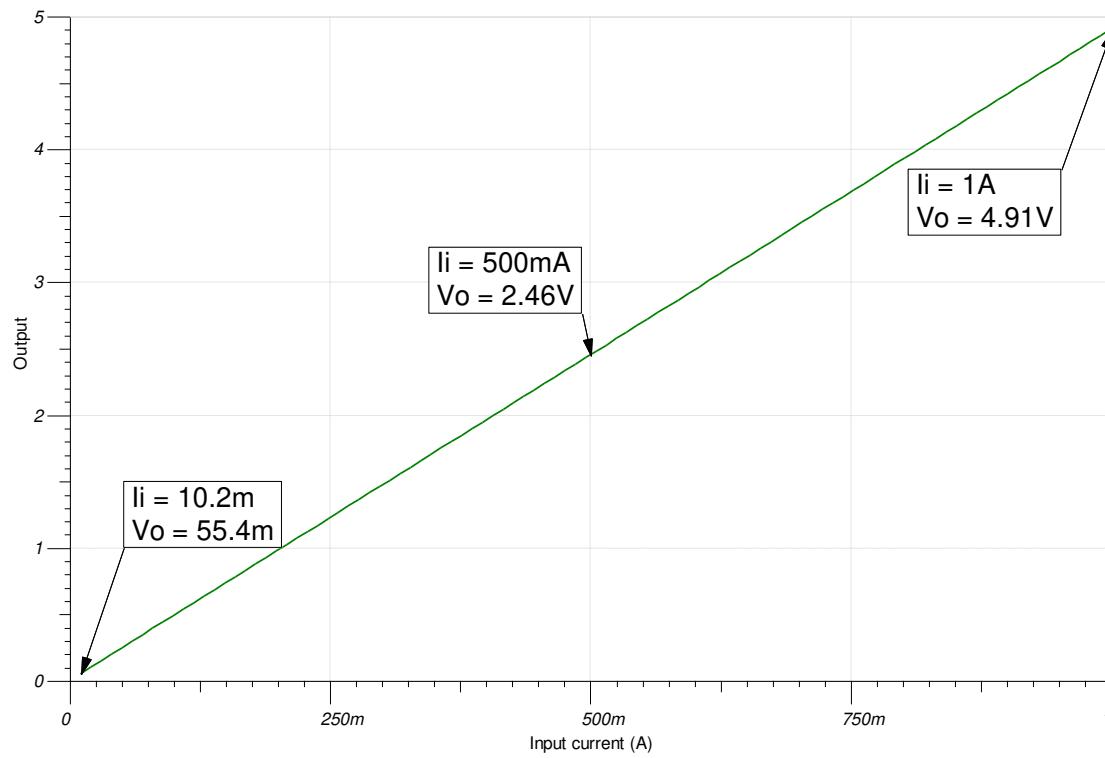
6. To maintain sufficient phase margin, ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit

$$\frac{1}{2\pi \times (C_{cm} + C_{diff}) \times (R_2 || R_3)} > \frac{\text{GBP}}{G}$$

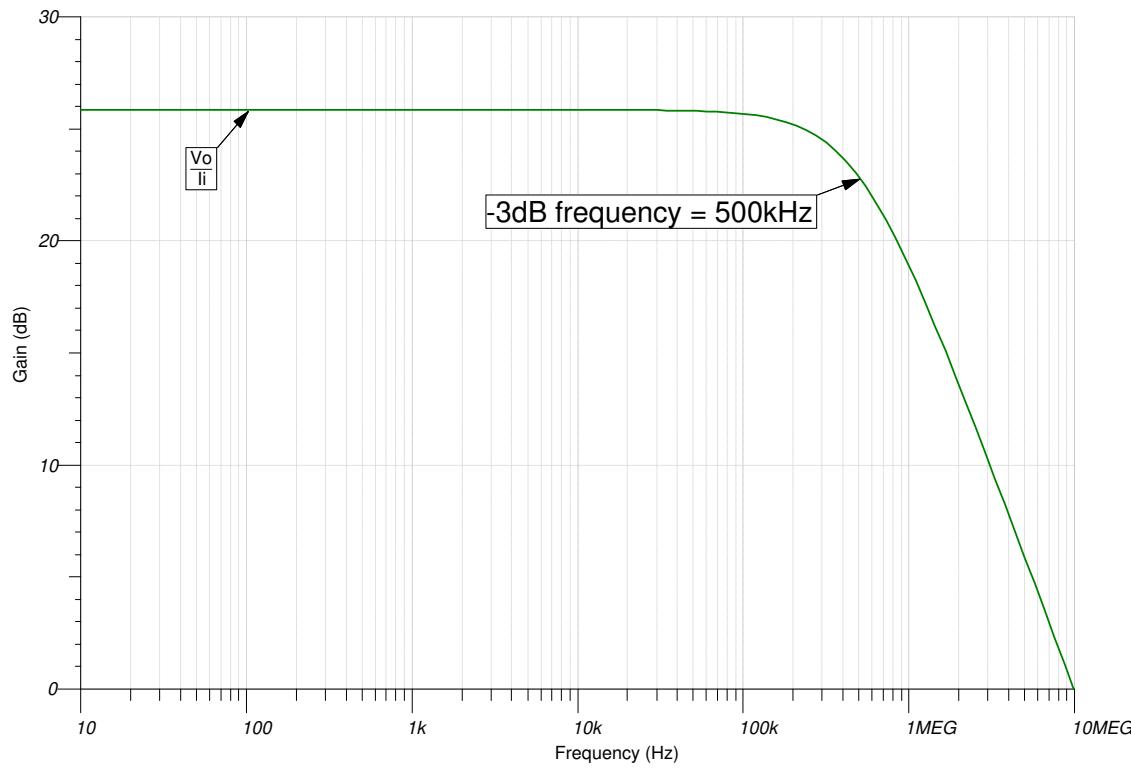
$$\frac{1}{2\pi \times (3\text{pF} + 3\text{pF}) \times \left(\frac{715 \Omega \times 13.3 \text{ k}\Omega}{715 \Omega + 13.3 \text{ k}\Omega} \right)} > \frac{10 \text{ MHz}}{19.6 \frac{\text{V}}{\text{V}}} = 39.1 \text{ MHz} > 510 \text{ kHz}$$

Design Simulations

DC Simulation Results



AC Simulation Results



References:

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOC523](#)
3. [TI Precision Designs TIPD129, TIPD104](#)
4. [TI Precision Labs](#)
5. [Single-Supply, Low-Side, Unidirectional Current-Sensing Solution with Output Swing to GND Circuit](#)

Design Featured Op Amp

TLV9061	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	538 μ A
I_b	0.5pA
UGBW	10MHz
SR	6.5V/ μ s
#Channels	1,2,4
www.ti.com/product/tlv9061	

Design Alternate Op Amp

OPA375	
V_{cc}	2.25V to 5.5V
V_{inCM}	(V_-) to ($(V_+)-1.2V$)
V_{out}	Rail-to-rail
V_{os}	0.15mV
I_q	890 μ A
I_b	10pA
UGBW	10MHz
SR	4.75V/ μ s
#Channels	1
www.ti.com/product/OPA375	

For battery operated or power conscious designs, outside of the original design goals described earlier, where lowering total system power is desired.

LPV821	
V_{cc}	1.7V to 3.6V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1.5 μ V
I_q	650nA/Ch
I_b	7pA
UGBW	8kHz
SR	3.3V/ms
#Channels	1
www.ti.com/product/LPV821	

Fast-Response Overcurrent Event Detection Circuit

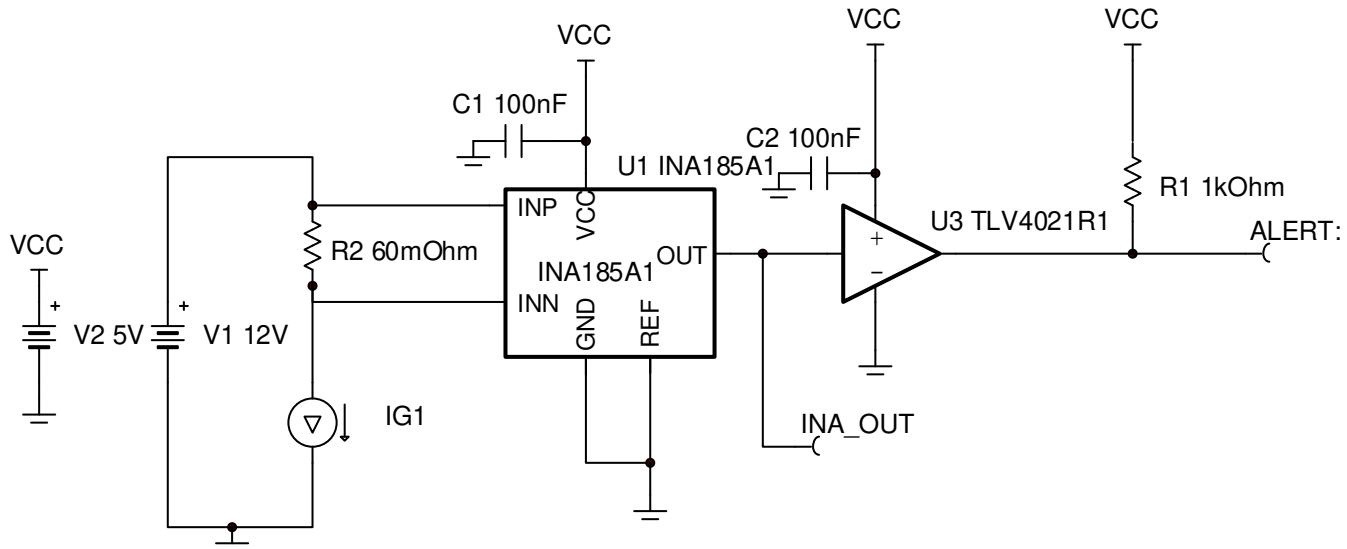


Design Goals

Input		Overcurrent Conditions		Output		Supply	
I _{load} Min	I _{load} Max	I _{OC_TH}	t _{resp}	V _{out_OC}	V _{out_release}	V _S	V _{REF}
80 mA	900 mA	1 A	< 2 μ s	1.2 V	1.18 V	5 V	0 V

Design Description

This is a fast-response unidirectional current-sensing solution, generally referred to as overcurrent protection (OCP), that can provide a $< 2 \mu$ s time response, t_{resp} , overcurrent alert signal to power off a system exceeding a threshold current. In this particular setup, the normal operating load is from 80 mA to 900 mA, with the overcurrent threshold defined at 1 A ($I_{\text{OC_TH}}$). The current shunt monitor is powered from a 5 V supply rail. OCP can be applied to both high-side and low-side topologies. The solution presented in this circuit is a high-side implementation. This circuit is useful in [smart speakers](#) and [docking stations](#).



Design Notes

1. Use decoupling capacitors C1 and C2 to ensure the device supply is stable. Place the decoupling capacitor as close to the device supply pin as possible.
2. If a larger dynamic current measurement range is required with a higher trip point, a voltage divider from the INA185 OUT pin to ground can be incorporated with the divider output going to the TLV4021R1 input.

Design Steps

1. Determine the slew rate, SR, needed to facilitate a fast enough response when paired with the propagation delay of a comparator. In this example, the TLV4021 device is selected as the external comparator due to its quick propagation delay ($t_p = 450$ ns) and its quick fall time ($t_f = 4$ ns). The worst case occurs when the load ramps from 0 A to 1 A ($\Delta V_{out} = V_{trip} - 0$ V). Device offset ($V_{OS} \times$ gain) can be subtracted from V_{trip} in the numerator for less aggressive slew rates.

$$SR = \frac{\Delta V_{out}}{t_{resp} - t_p - t_f} = \frac{1.2V}{2\mu s - 450ns - 4ns} = 0.78V/\mu s$$

2. Choose a current shunt monitor with a slew rate greater than or equal 0.78 V/ μ s. The INA185 device satisfies the requirement with a typical slew of 2 V/ μ s.
3. For maximum headroom between the lowest measured current level and the overcurrent level, select the smallest gain variant of the chosen current shunt monitor. A 20 V/V current shunt monitor paired with 1.2 V comparator reference is adequate in this case.
4. Calculate the R_{shunt} value given 20 V/V gain. Use the nearest standard value shunt, preferably lower than the calculated shunt to avoid railering the output prematurely.

$$R_{shunt} = \frac{V_{trip}}{\text{gain} \times I_{trip}} = \frac{1.2V}{20V/V \times 1A} = 0.06\Omega$$

$R_{\text{standard shunt}} = 60m\Omega$ (standard 1% value)

5. Check that the minimum meaningful current measurement is significantly higher than the current shunt monitor input offset voltage. The recommended maximum error from offset, $\text{error}_{V_{OS}}$ is 10%.

$$I_{\text{Device_min}} = \frac{V_{OS}}{\text{error}_{V_{OS}} \times R_{shunt}} = \frac{450\mu V}{\frac{10}{100} \times 0.06\Omega} = 75mA$$

6. Check that $I_{\text{Load Max}}$ is below the hysteresis threshold, $I_{\text{Release_TH}}$, to ensure that the ALERT signal is cleared after the system has taken corrective action to bring the load back under the upper limit of the normal operating range. In this case there is 83mA of margin between the 900 mA normal operating region maximum and the hysteresis level imposed by the comparator.

$$I_{\text{Release_TH}} = \frac{V_{trip} - 20mV}{\text{gain} \times R_{shunt}} = \frac{1.2V - 20mV}{20V/V \times 0.06\Omega} = 0.983A$$

Design Simulations

DC Simulation Results

The DC transfer characteristic curve confirms that the OCP trigger occurs from a 1 A load.

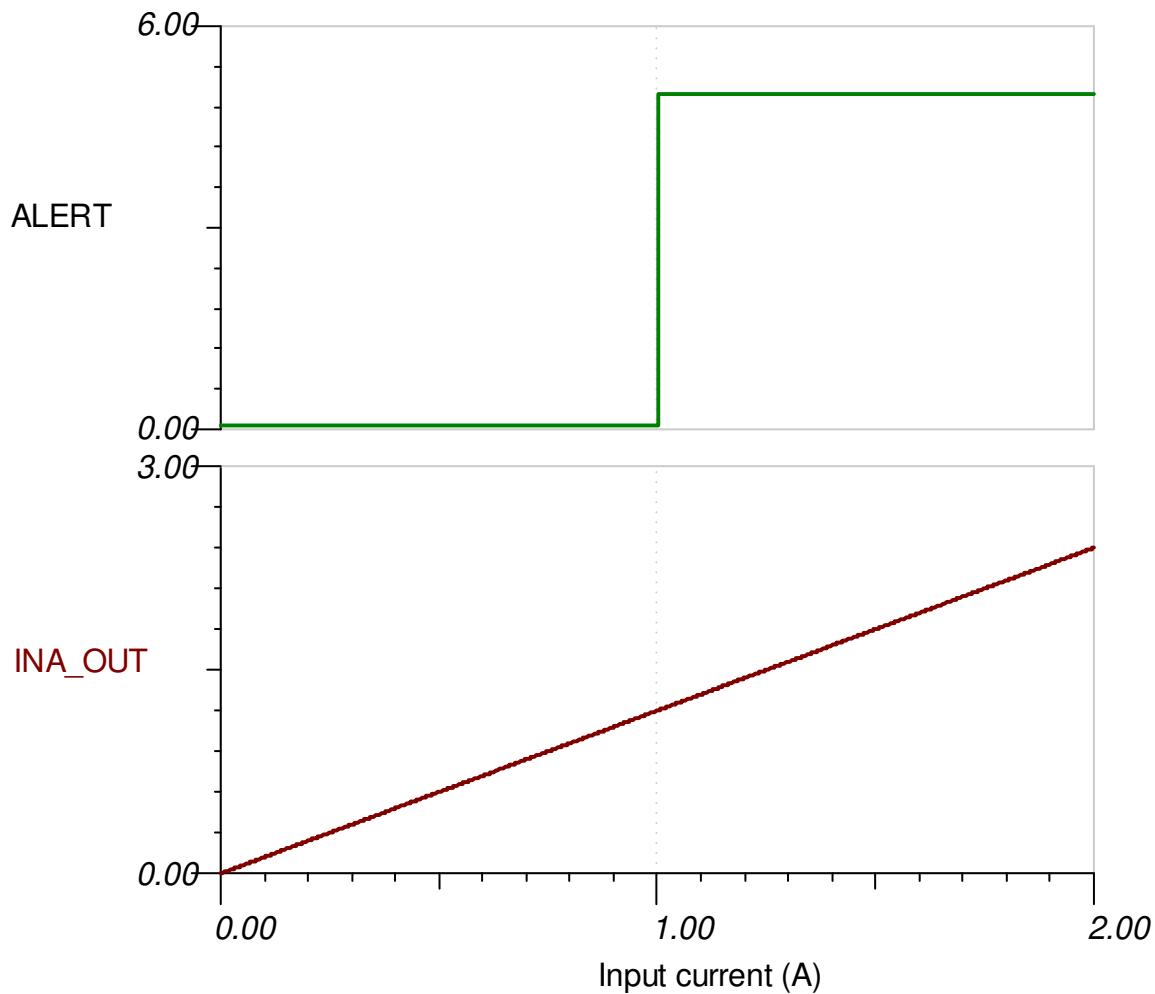
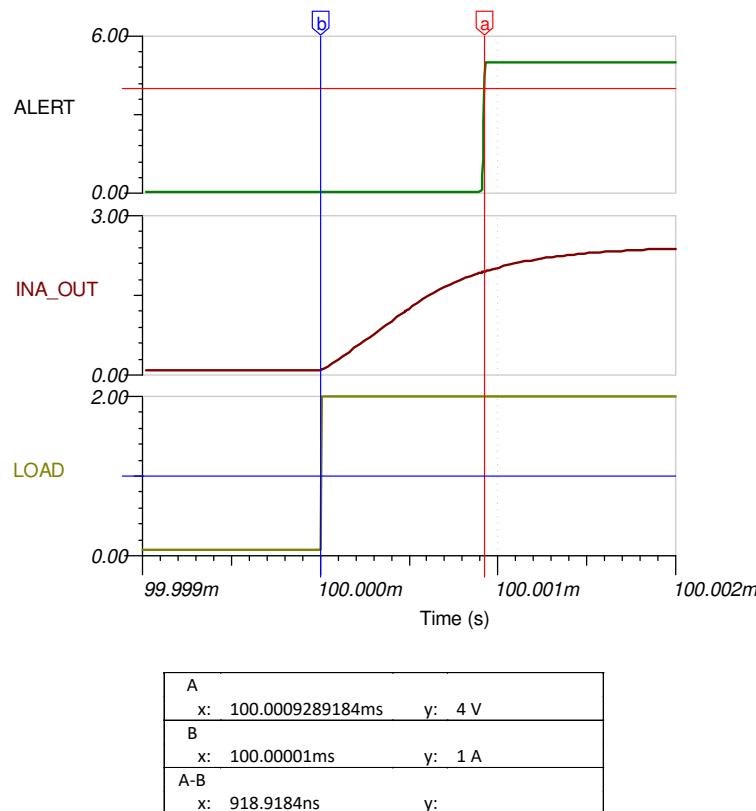


Figure 1-1.

Transient Simulation Results

The following result confirms that the INA185 device paired with the TLV4021 device can trigger an ALERT within 2 μ s of the overcurrent threshold being exceeded. In this case, a typical value of almost 1 μ s is achieved. Please keep in mind that models used in these simulations are designed around typical device characteristics. Real-world performance may vary based on normal device variations.



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

Key Files for Overcurrent Protection Circuit

Source files for this design:

[High-Side OCP Tina Model](#)

[Low-Side OCP Tina Model](#)

Getting Started With Current Sense Amplifiers Video Series

[Getting started with current sense amplifiers](#)

Design Featured Current Sense Amplifier

INA185	
V_S	2.7 V to 5.5 V
V_{CM}	GND-0.2 V to 26 V
V_{OUT}	GND + 500 μ V to V_S – 0.02 V
Gain	20 V/V, 50 V/V, 100 V/V, 200 V/V
V_{OS}	\pm 100 μ V typical
SR	2 V/ μ s typical
I_q	200 μ A typical
I_B	75 μ A typical
INA185	

Design Alternate Current Sense Monitor

	INA181	INA180
V_S	2.7 V to 5.5 V	2.7 V to 5.5 V
V_{CM}	GND-0.2 V to 26 V	GND-0.2 V to 26 V
V_{OUT}	GND + 500 μ V to V_S – 0.02 V	GND + 500 μ V to V_S – 0.02 V
Gain	20 V/V, 50 V/V, 100 V/V, 200 V/V	20 V/V, 50 V/V, 100 V/V, 200 V/V
V_{OS}	\pm 100 μ V typical	\pm 100 μ V typical
SR	2 V/ μ s typical	2 V/ μ s typical
I_q	195 μ A typical	197 μ A typical
I_B	75 μ A typical	80 μ A typical
	INA181	INA180

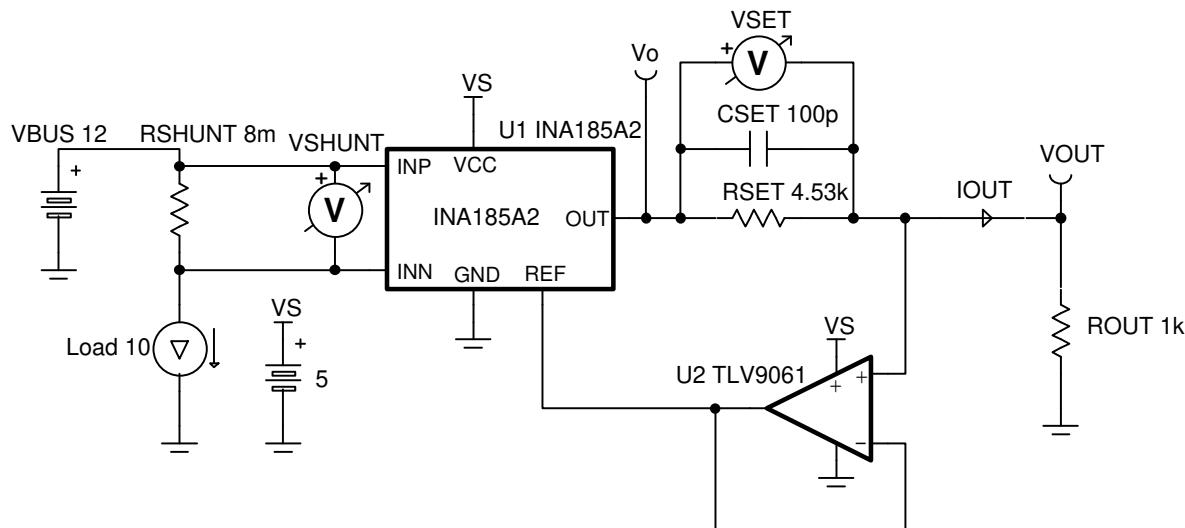
Adjustable-gain, current-output, high-side current-sensing circuit



Input			Output			Error	Supply		
I _{LOAD} Min	I _{LOAD} Max	V _{CM}	I _{OUT} Min	I _{OUT} Max	Bandwidth	at I _{LOAD} Min	I _Q Max	V _S	V _{ee}
1A	10A	12V	88.3 μ A	883 μ A	200kHz	2.2% maximum, 0.3% typical	260 + 750 μ A	5V	GND (0V)

Design Description

This circuit demonstrates how to convert a voltage-output, current-sense amplifier (CSA) into a current-output circuit using an operational amplifier (op amp) and a current-setting resistor (R_{SET}). Taking advantage of the matched internal resistor gain network of the current-sense amplifier, this circuit utilizes the Howland Current Pump method to create a current source that is proportional to the sense current. The overall circuit gain is adjustable by changing the load resistor value (R_{OUT}). Additionally, multiple circuits can be summed together to determine total current from multiple sources.



Design Notes

1. The [Getting Started with Current Sense Amplifiers](#) video series introduces implementation, error sources, and advanced topics for using current sense amplifiers.
2. Choose precision 0.1% resistors to limit gain error at higher currents.
3. The output current (I_{OUT}) is sourced from the VS supply, which adds to the I_Q of the current sense amplifier.
4. Use the V_{OUT} versus I_{OUT} curve ("claw-curve") of the CSA (U1) to set the I_{OUT} limit during I_{LOAD_Max} . If a higher amount of current is needed, then consider adding a buffer to the output of the current sense amplifier. A buffer on the output allows for smaller R_{OUT} .
5. For applications with higher bus voltages, simply substitute in a bidirectional current sense amplifier with a higher rated input voltage.
6. The V_{OUT} voltage is the input common-mode voltage (V_{CM}) for the op amp.
7. Offset errors can be calibrated out with one-point calibration given that a known sense current is applied and the circuit is operating in the linear region. Gain error calibration requires a two-point calibration.
8. Include a small feed-forward capacitor (C_{SET}) to increase BW and decrease V_{OUT} settling time to a step response in current. Increasing C_{SET} too much introduces gain peaking in the system gain curve, which results in output overshoot to a step response.
9. Multiple circuits can sum their current outputs into a single load resistor, but note that the headroom voltage for each individual circuit will decrease. The INA2181 and INA4181 devices are multi-channel CSAs that have similar performance to the INA185 device.
10. Follow best practices for printed-circuit board (PCB) layout according to the data sheet: decoupling capacitor close to the VS pin, routing the input traces for IN+ and IN- as a differential pair, and so forth.

Design Steps

1. To satisfy system requirements, the minimum shunt (V_{SHUNT_MIN}) voltage value must be sufficiently greater than the known offsets of the amplifiers. Here is the equation for the worst-case maximum output current:

$$I_{OUT_MAX_Worst-Case} = \frac{V_{SET_MAX}}{R_{SET} \cdot (1 - \text{Tolerance}_{Rset})}$$

$$I_{OUT_MAX_Worst-Case} = \frac{\text{Gain}_{INA185} \cdot (1 + \text{GainError}) \cdot [V_{SHUNT_MIN} + V_{OS_INA185}] + V_{OS_TLV9061}}{R_{SET} \cdot (1 - \text{Tolerance}_{Rset})}$$

2. Since offset errors dominate at the low currents, negate resistor tolerance and gain error for establishing V_{SHUNT_MIN} . Set the error of V_{SET} to 2.2% to determine the following condition:

$$V_{SHUNT_MIN} > \left(\frac{1}{2.2\%} \right) \cdot \left\{ V_{OS_INA185} + \frac{V_{OS_TLV9061}}{\text{Gain}_{INA185}} \right\}$$

3. V_{OUT_MIN} also needs to be large enough so the common-mode voltage (V_{CM}) and output voltage ($V_{OUT_TLV9061}$) of the TLV9061 device are in the optimal operating region. The TLV9061 device is a rail-to-rail-input-output (RRIO) op amp so it can operate with very small V_{CM} and output voltages, but A_{OL} will vary. Testing conditions for data sheet CMRR and A_{OL} show that choosing $V_{OUT_MIN} > 50$ mV will provide sufficient A_{OL} when circuit sensing minimum load current.

$$V_{OUT_TLV9061} = V_{CM_TLV9061} = V_{OUT}$$

$$V_{OUT_MIN} > 50\text{mV} \text{ for good TLV9061 } A_{OL}$$

4. The scaling of R_{OUT} and R_{SET} can be determined by setting three parameters: V_{O_MAX} , I_{OUT_MAX} , and R_{OUT} . It is critical that I_{OUT_MAX} does not exceed the driving capability of the CSA or else V_{O_MAX} will droop and the circuit will loose headroom voltage. Use the swing-to-rail specification and the V_{OUT} versus I_{OUT} data sheet curve to determine optimal values.

- a. Choose $V_{O_MAX} = 4.9\text{V}$
- b. Choose $I_{OUT_MAX} = 900\mu\text{A}$

- c. Choose $R_{OUT} = 1k\Omega$
5. Using the system of equations for V_{OUT} , solve for R_{SET} . Choose the closest larger 1% resistor value. Note that rounding up the R_{SET} value will decrease the I_{OUT_MAX} from initially chosen 900 μ A.

$$V_{SET_MAX} = I_{OUT_MAX} \cdot R_{SET}$$

$$V_{OUT_MAX} = I_{OUT_MAX} \cdot R_{OUT}$$

$$V_{OUT_MAX} = V_{O_MAX} - V_{SET_MAX}$$

$$R_{SET} = \frac{V_{O_MAX} - I_{OUT_MAX} \cdot R_{OUT}}{I_{OUT_MAX}} = 4444.3\Omega$$

$$R_{SET} = 4530\Omega, 1\%$$

6. Now choose an INA185 gain variant and solve for R_{SHUNT} . Choose a 1% resistor value. Note that R_{SET} is independent of gain and R_{SHUNT} can be calculated for each gain variant.

$$V_{OUT_MAX} = I_{OUT_MAX} \cdot R_{OUT} = 900mV$$

$$V_{SET_MAX} = V_{O_MAX} - V_{OUT_MAX} = 4V$$

$$V_{IN_MAX} = \frac{V_{SET_MAX}}{\text{Gain}_{INA185A2}} = \frac{4V}{50\frac{V}{V}} = 80mV$$

$$R_{SHUNT} = \frac{V_{IN_MAX}}{I_{LOAD_MAX}} = \frac{80mV}{10A} = 8m\Omega$$

$$R_{SHUNT} = 8m\Omega$$

7. Now check if V_{OUT_MIN} and V_{SHUNT_MIN} are large enough to achieve 2% error at 1A with updated values. Use the maximum offset specifications of the devices when calculating error.

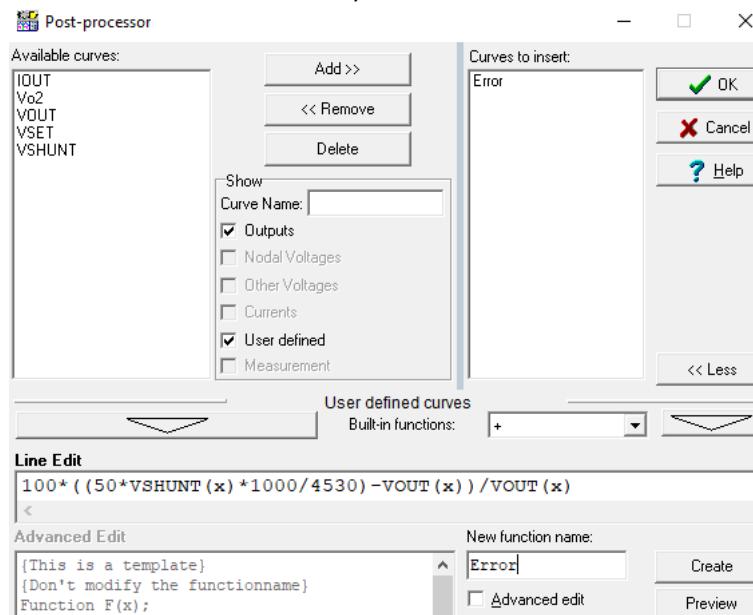
$$V_{SHUNT_MIN} > \left(\frac{1}{2.2\%} \right) \cdot \left\{ V_{OS_INA185A2} + \frac{V_{OS_TLV9061}}{\text{GAIN}_{INA185A2}} \right\} = 45.45 \cdot \left\{ 130\mu V + \frac{2mV}{50\frac{V}{V}} \right\} = 7.73mV$$

$$V_{SHUNT_MIN} = 1A \cdot 8m\Omega = 8mV > 7.73mV$$

$$V_{OUT_MIN} = V_{SHUNT_MIN} \cdot \text{Gain}_{INA185A2} \cdot \frac{R_{OUT}}{R_{SET}}$$

$$V_{OUT_MIN} = 8mV \cdot 50\frac{V}{V} \cdot \frac{1k\Omega}{4.53k\Omega} = 88mV > 50mV$$

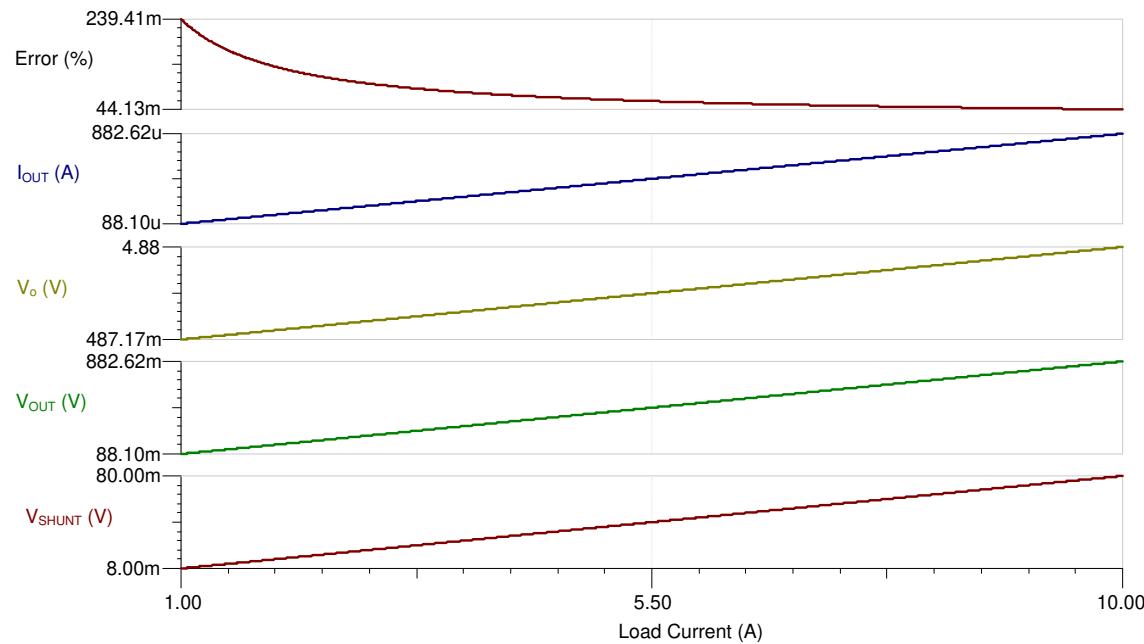
8. Run a simulation in TINA-TI software using available models. Note that these models use typical specifications. Calculate *Error* in the TINA-TI *Post-processor* window.



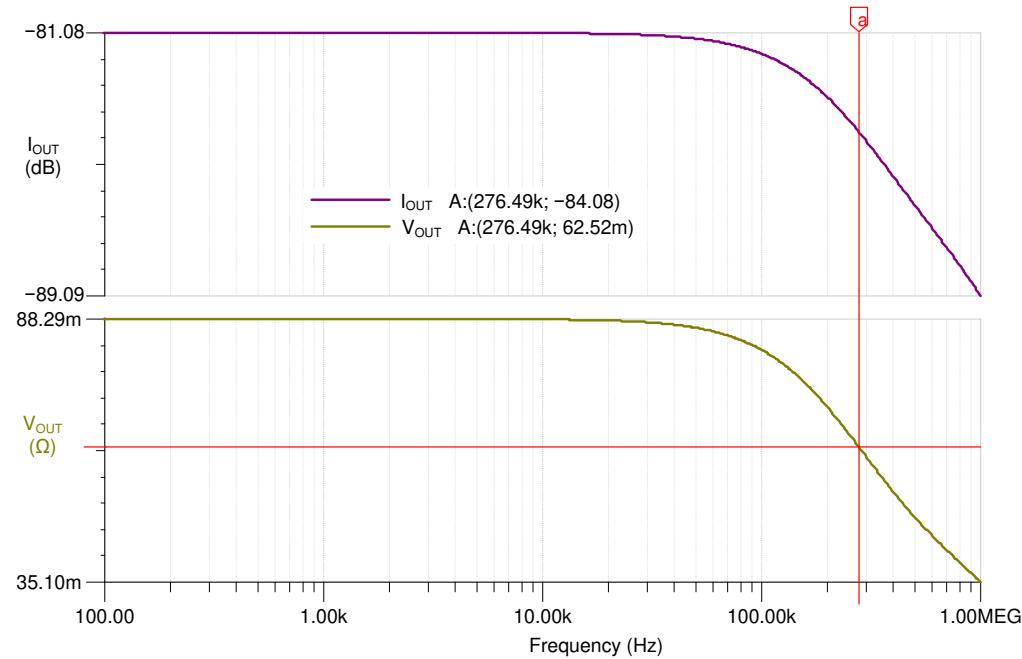
Design Simulations

DC Simulation Results

The following graph shows a linear output response for load currents from 1A to 10A.



AC Simulation Result – I_{LOAD} to I_{OUT} (V_{OUT}) circuit gain



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOMAI6](#).

Getting Started with Current Sense Amplifiers video series

<https://training.ti.com/getting-started-current-sense-amplifiers>

Current Sense Amplifiers on TI.com

<http://www.ti.com/amplifier-circuit/current-sense/products.html>

Comprehensive Study of the Howland Current Pump

[http://www.ti.com/analog/docs/litabsmultiplefilelist.tsp?
literatureNumber=snoa474a&docCategoryId=1&familyId=78](http://www.ti.com/analog/docs/litabsmultiplefilelist.tsp?literatureNumber=snoa474a&docCategoryId=1&familyId=78)

For direct support from TI Engineers use the E2E community

<http://e2e.ti.com>

Design Featured Current Sense Amplifier

INA185A2	
V_S	2.7V to 5.5V (operational)
V_{CM}	0V to 26V
Swing to V_S (V_{SP})	$V_S - 0.02V$
V_{OS}	$\pm 25\mu V$ to $\pm 130\mu V$ at 12V V_{CM}
I_Q	200 μA to 260 μA
I_{IB}	75 μA at 12V
BW	210kHz at 50V/V (A2 gain variant)
# of channels	1
Body size (including pins)	1.60 mm \times 1.60 mm
http://www.ti.com/product/ina185	

Design Featured Operational Amplifier

TLV9061 (TLV9061S is shutdown version)	
V_S	1.8V to 5.5V
V_{CM}	(V-) - 0.1V < V_{CM} < (V+) + 0.1V
CMRR	103dB
A_{OL}	130dB
V_{OS}	$\pm 1.6mV$ maximum
I_Q	750 μA maximum
I_B (input bias current)	$\pm 0.5pA$
GBP (gain bandwidth product)	10MHz
# of channels	1 (2 and 4 channel packages available)
Body size (including pins)	0.80 mm \times 0.80 mm
http://www.ti.com/product/tlv9061	

Current Limiting with Comparator Circuit

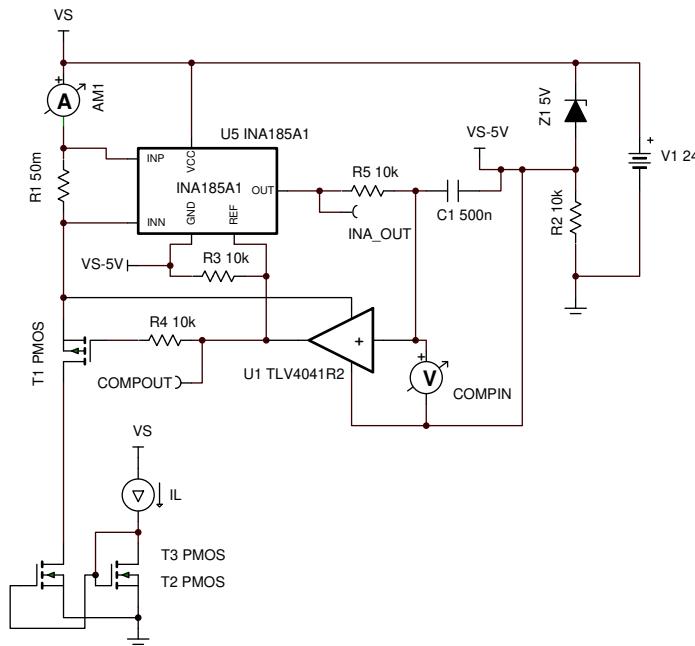


Design Goals

LOAD CURRENT (I_L)	SYSTEM SUPPLY (V_S)	CURRENT SENSE AMP	COMPARATOR OUTPUT STATUS	
Over Current (loc)	Typical	Gain	Over Current	Normal Operation
200 mA	24 V	20 V/V	$V_{OH} = V_S$	$V_{OL} = V_S - 5 \text{ V}$

Design Description

This high-side, current sensing solution uses a current sense amplifier, a comparator with an integrated reference, and a P-channel MOSFET to create an over-current latch circuit. When a load current greater than 200 mA is detected, the circuit disconnects the system from its power source. Since the comparator drives the gate of the P-channel MOSFET and feeds the signal back into the reference pin of the current sense amplifier, the comparator output will latch (hold the gate source voltage of the P-channel MOSFET to 0 V) until power to the circuit is cycled.



Design Notes

1. Select a precision, current sense amplifier (INA) with an external reference pin so its output voltage can be adjusted.
2. Select a comparator with a rail-to-rail input so its output will be valid over the entire operating voltage range of the current sense amplifier.
3. Select a comparator with a push-pull output stage that can drive the gate of a MOSFET and an integrated reference to optimize circuit accuracy.
4. Create a floating 5 V supply that can power the INA and comparator.

Design Steps

1. Select the value of R_1 so V_{SHUNT} is at least 100x greater than the current sense amplifier input offset voltage (V_{OS}). Note that making R_6 very large will improve OC detection accuracy but will reduce supply headroom and power dissipation.

$$V_{SHUNT} = (I_{OC} \times R_1) \geq 100 \times V_{OS}$$

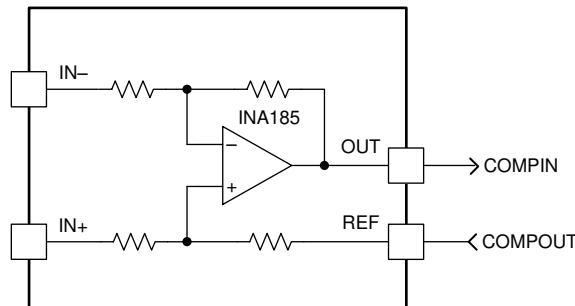
$$\text{Set } R_1 \geq \frac{100 \times V_{OS}}{I_{OC}} = 50\text{m}\Omega \text{ for } I_{OC} = 200\text{mA} \text{ & } V_{OS} = 100\mu\text{V}$$

2. Determine the desired gain (A_V) option for the INA based on the switching threshold of the comparator. When the load current (I_L) reaches the over-current threshold (I_{OC}), the INA output must cross the switching threshold (V_{TH}) of the comparator.

$$V_{TH} = (I_{OC} \times R_1) \times A_V = 0.2\text{V}$$

$$\text{Set } A_V = \frac{V_{TH}}{I_{OC} \times R_1} = \frac{0.2}{0.2 \times 0.05} = 20\text{V/V} \text{ for } R_1 = 50\text{m}\Omega$$

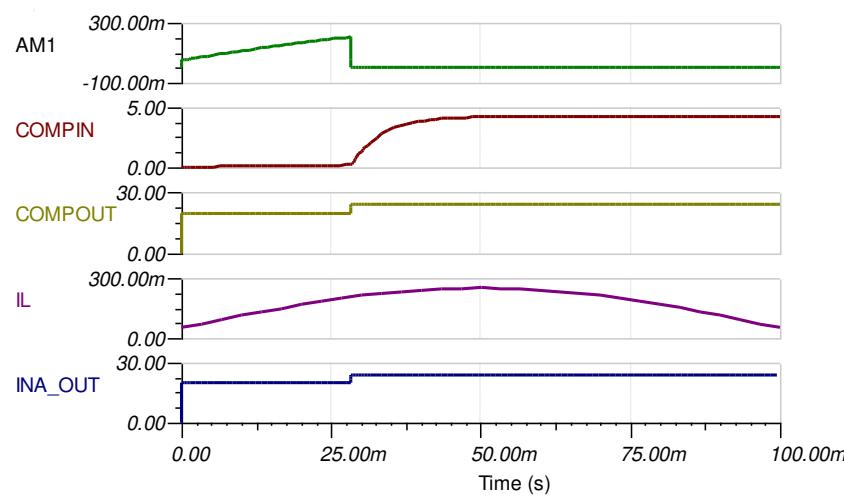
3. Since many INA's and comparators have 5 V operating voltage ranges, a 5 V supply voltage needs to be derived from the system supply V_S . In addition, the 5 V supply needs to float below V_S so the comparator output can drive the source-gate voltage of the P-channel MOSFET to 0 V when an over-current condition occurs and 5 V when the load current is less than I_{OC} . The method used in this circuit is a 5 V zener diode with a 10 k Ω bias resistor (R_2). Other options such as shunt regulators can also be utilized as long as proper bias current through the device is maintained.
4. A low pass filter is added between the INA output and the comparator input to attenuate any high frequency current spikes. It is more important to trigger the over-current latch with a delay than to falsely disconnect the system from the supply voltage. The low pass filter is derived from R_5 and C_1 . Since the switching threshold of the comparator is 0.2 V, the delay is less than 1 time constant ($R_5 \times C_1 = 5 \text{ ms}$).
5. A current limiting resistor R_4 is inserted between the comparator output and the gate of the P-channel MOSFET. Setting R_4 to 10 k Ω reduces current spikes on the supply when the comparator output needs to charge the MOSFET gate-source capacitance as a compromise to increasing the charge time. Inserting R_4 also serves the purpose of protecting the comparator output from any supply transients that can be present on the supply line.
6. The output of the comparator is directly connected to the REF pin of the INA in order to apply an offset to the INA's output voltage. When $I_L < I_{OC}$, the comparator output is low (equal to $V_S - 5 \text{ V}$) and no offset is added to the INA. However, when $I_L > I_{OC}$, the comparator output goes high (equal to V_S) and a 5 V offset is added to the INA. This offset causes the INA output to saturate at a level equal to V_S . Since an INA output level of V_S is higher than the V_{TH} of the comparator, the comparator output will remain high. This condition is referred to as a *latched* output state since the circuit will remain in this state until power to the circuit is cycled.



7. R_3 is added between the INA reference pin (REF) and GND ($V_S - 5 \text{ V}$) to ensure a proper ground path as the 5 V supply ramps up to the comparator minimum operating voltage.
8. If a latching feature is not preferred, the comparator output can be disconnected from the current sense amplifier reference pin and R_3 can be replaced with a short. In this configuration, the circuit will behave as a 200 mA current limiter.

Design Simulations

Transient Simulation Results



Design References

See Circuit SPICE Simulation File, [SBVM944](#).

Design Featured Comparator

TLV4041R2	
V_S	1.6 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{OUT}	Push-Pull
Integrated Reference	200 mV \pm 3 mV
I_Q	2 μ A
t_{PD}	360 ns
TLV4041R2	

Design Featured Current Sense Amplifier

INA185	
V_S	2.7 V to 5.5 V
V_{inCM}	-0.2 V to 26 V
Gain Options	20 V/V, 50 V/V, 100 V/V, 200 V/V
Gain Error	0.2 %
V_{os}	100 μ V (A1), 25 μ V (A2, A3, and A4)
I_Q	200 μ A
INA185	

Low-side, bidirectional current sensing circuit

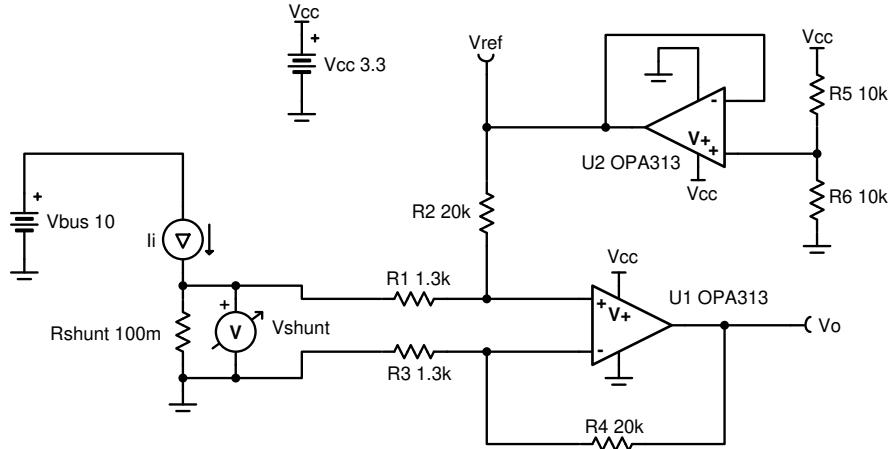


Design Goals

Input		Output		Supply		
I _{iMin}	I _{iMax}	V _{oMin}	V _{oMax}	V _{cc}	V _{ee}	V _{ref}
-1A	1A	110mV	3.19V	3.3V	0V	1.65V

Design Description

This single-supply low-side, bidirectional current sensing solution can accurately detect load currents from -1A to 1A. The linear range of the output is from 110mV to 3.19V. Low-side current sensing keeps the common-mode voltage near ground, and is thus most useful in applications with large bus voltages.



Design Notes

1. To minimize errors, set $R_3 = R_4$ and $R_1 = R_2$.
2. Use precision resistors for higher accuracy.
3. Set output range based on linear output swing (see A_{ol} specification).
4. Low-side sensing should not be used in applications where the system load cannot withstand small ground disturbances or in applications that need to detect load shorts.

Design Steps

- Determine the transfer equation given $R_4 = R_2$ and $R_1 = R_3$.

$$V_o = \left(I_i \times R_{\text{shunt}} \times \frac{R_4}{R_3} \right) + V_{\text{ref}}$$

$$V_{\text{ref}} = V_{\text{cc}} \times \left(\frac{R_6}{R_5 + R_6} \right)$$

- Determine the maximum shunt resistance.

$$R_{\text{shunt}} = \frac{V_{\text{shunt}}}{I_{i\text{max}}} = \frac{100\text{mV}}{1 \text{ A}} = 100\text{m}\Omega$$

- Set reference voltage.

- a. Since the input current range is symmetric, the reference should be set to mid supply. Therefore, make R_5 and R_6 equal.

$$R_5 = R_6 = 10\text{k}\Omega$$

- Set the difference amplifier gain based on the op amp output swing. The op amp output can swing from 100mV to 3.2V, given a 3.3-V supply.

$$\text{Gain} = \frac{V_{o\text{Max}} - V_{o\text{Min}}}{R_{\text{shunt}} \times (I_{i\text{Max}} - I_{i\text{Min}})} = \frac{3.2 \text{ V} - 100\text{mV}}{100\text{m}\Omega \times (1 \text{ A} - (-1 \text{ A}))} = 15.5 \frac{\text{V}}{\text{V}}$$

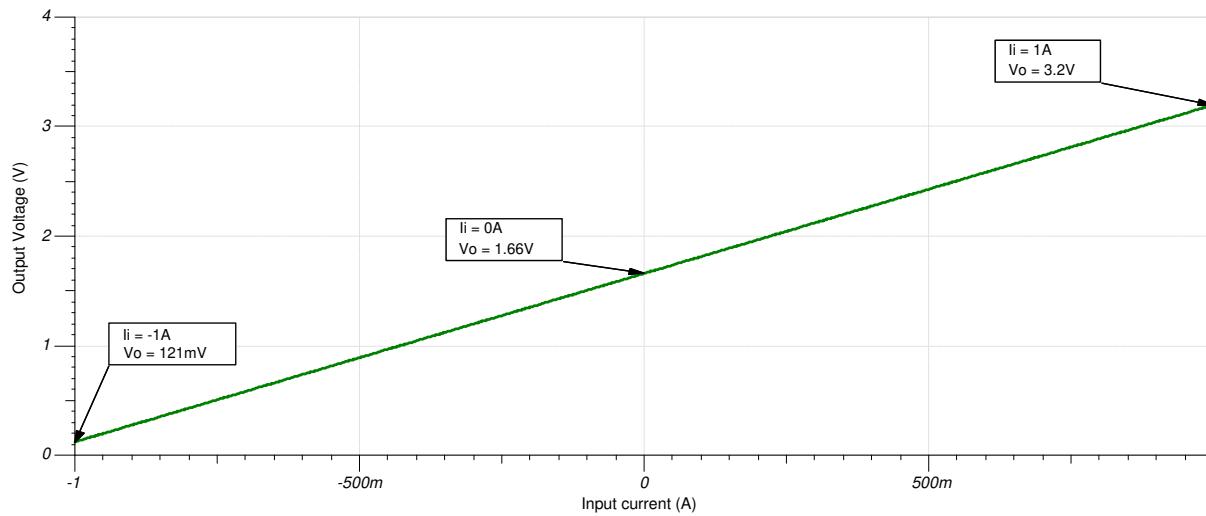
$$\text{Gain} = \frac{R_4}{R_3} = 15.5 \frac{\text{V}}{\text{V}}$$

Choose $R_1 = R_3 = 1.3\text{k}\Omega$ (Standard Value)

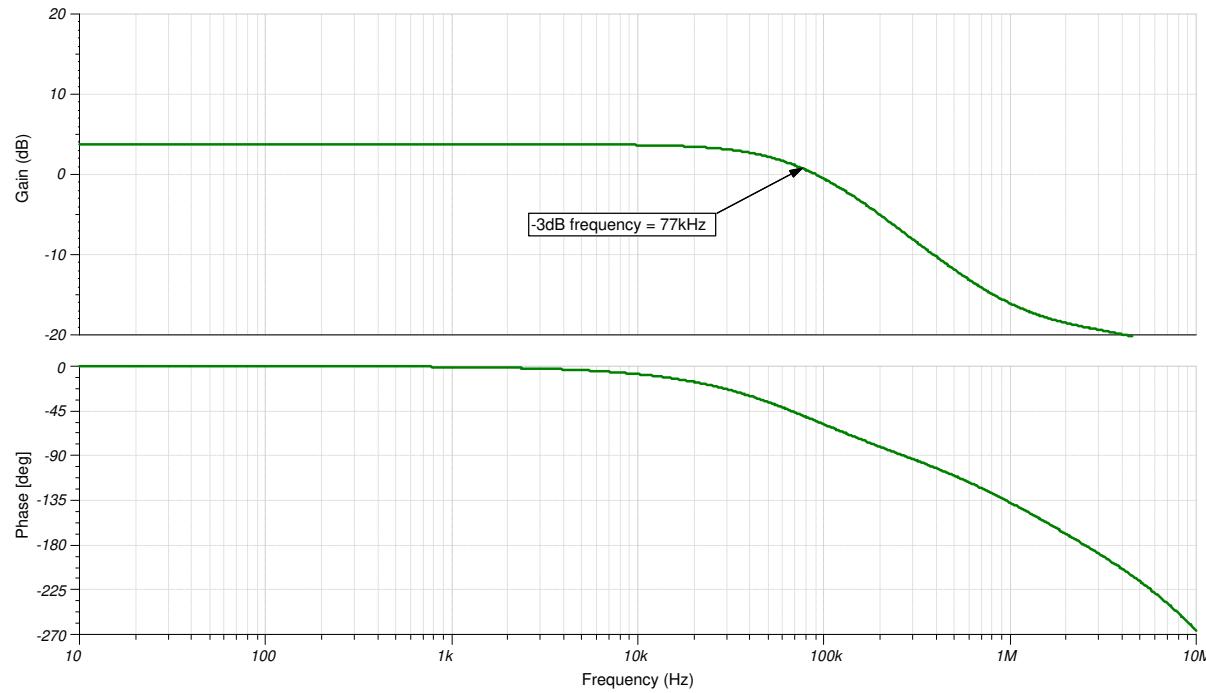
$$R_2 = R_4 = 15.5 \frac{\text{V}}{\text{V}} \times 1.3\text{k}\Omega = 20.15 \text{ k}\Omega \approx 20\text{k}\Omega \text{ (Standard Value)}$$

Design Simulations

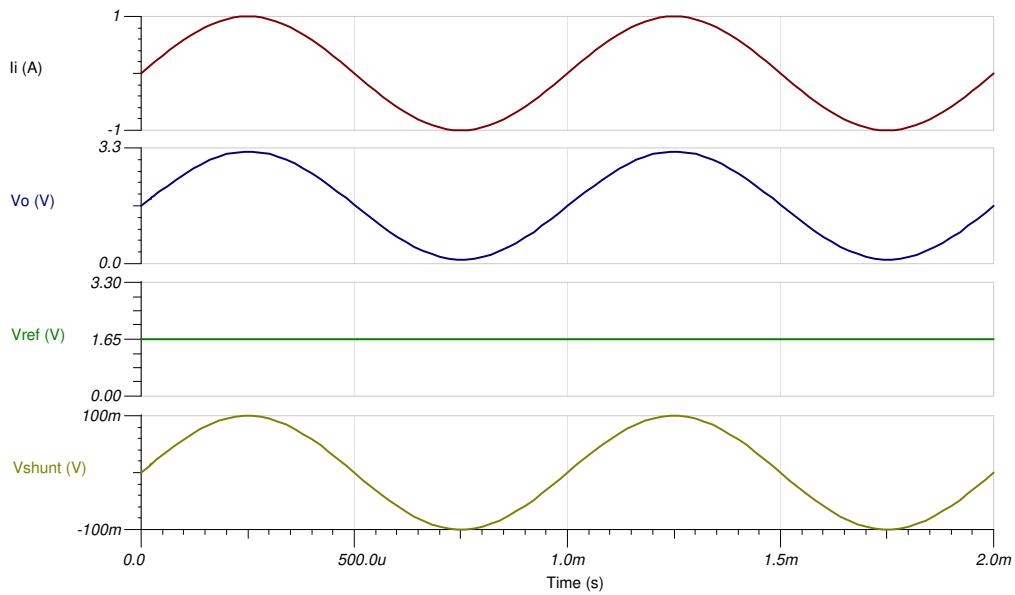
DC Simulation Results



Closed Loop AC Simulation Results



Transient Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC500](#).

See TIPD175, www.ti.com/tipd175.

Design Featured Op Amp

OPA313	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	500 μ V
I_q	50 μ A/Ch
I_b	0.2pA
UGBW	1MHz
SR	0.5V/ μ s
#Channels	1, 2, 4
www.ti.com/product/opa313	

Design Alternate Op Amp

	TLV9062	OPA376
V_{cc}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{out}	Rail-to-rail	Rail-to-rail
V_{os}	300 μ V	5 μ V
I_q	538 μ A/Ch	760 μ A/Ch
I_b	0.5pA	0.2pA
UGBW	10MHz	5.5MHz
SR	6.5V/ μ s	2V/ μ s
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/tlv9062	www.ti.com/product/opa376

For battery-operated or power-conscious designs, outside of the original design goals described earlier, where lowering total system power is desired.

LPV821	
V_{cc}	1.7V to 3.6V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1.5 μ V
I_q	650nA/Ch
I_b	7pA
UGBW	8KHz
SR	3.3V/ms
#Channels	1
www.ti.com/product/lpv821	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2018) to Revision B (January 2019)	Page
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• Cookbook landing page	1
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Changes from Revision * (February 2018) to Revision A (May 2018)	Page
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• Changed title role to 'Amplifiers'.....	1
• Added SPICE simulation file link.....	1
• Added LPV821 as a <i>Design Alternate Op Amp</i> for battery-operated or power-conscious designs.....	1

Bidirectional Current Sensing with a Window Comparator Circuit

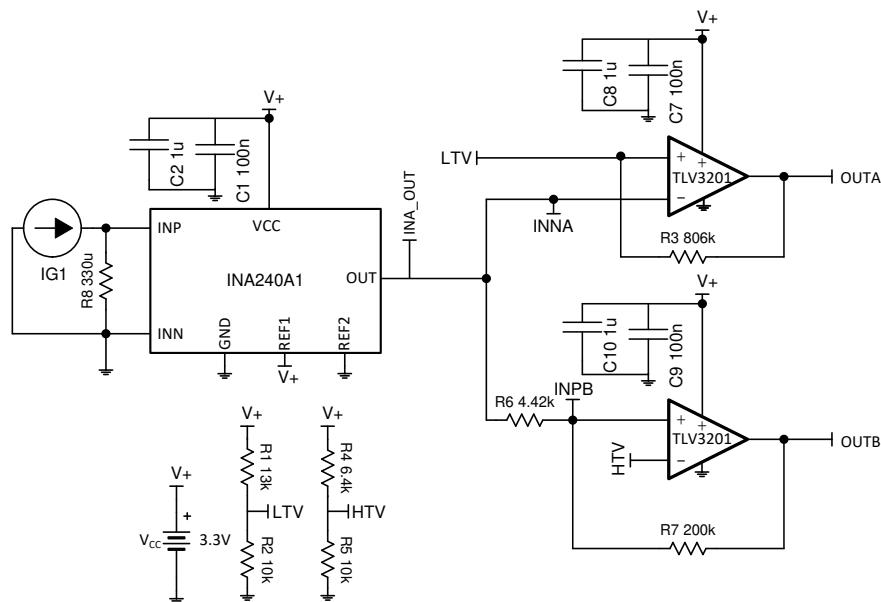


Design Goals

SYSTEM CURRENT LEVELS				SUPPLY	
Falling OC Threshold	Falling OC Recovery	Rising OC Threshold	Rising OC Recovery	V+	V-
IG1 < -35 A	IG1 > -31 A	IG1 > 100 A	IG1 < 90 A	3.3 V	0 V

Design Description

This bidirectional current sensing solution uses a current-sense amplifier and a high speed dual comparator with a rail-to-rail input common mode range to create over-current (OC) alert signals at the comparator outputs (OUTA and OUTB) if the input current (IG1) rises above 100 A or falls below -35 A. In this implementation, both over-current alert signals are active high, so when the 100 A or -35 A thresholds are crossed, the comparator outputs will go high. External hysteresis is implemented on both comparators so that the comparator outputs will return to logic low states when the current reduces by 10% (90 A and -31 A). While the circuit below has shunt resistor R8 connected to ground, the same circuit is applicable for high side current sensing up to the common mode voltage range of the INA.



Design Notes

1. Select a comparator with rail-to-rail input common mode range.
2. Select a current sense amplifier with low offset voltage and a common mode input range that matches the requirements of the system.

Design Steps

- To determine the comparator threshold voltages, first calculate the INA240A1 output voltages that correspond to the desired current thresholds. The calculations depend on the gain of the INA240 (20, 50, 100, 200 for A1, A2, A3, A4, respectively), the input current (IG1) and sense resistor (R8), and the reference voltage when the input current is 0 (VREF). Per section 8.3.2 in the INA240 data sheet, R8 is a function of the differential input voltage and the maximum input current to the INA240. Given that the input current in this system swings above 100 A, by keeping R8 small, the power dissipation across R8 will be lessened.

$$\text{INA_OUT} = \text{VREF} + G \times (\text{INP} - \text{INN})$$

$$\text{INP} - \text{INN} = \text{IG1} \times \text{R8}$$

$$\text{VREF} = \frac{(\text{V}+) - 0}{2} = \frac{3.3\text{V}}{2} = 1.65\text{V}$$

Using these equations and the desired current thresholds, the following table is generated:

DESCRIPTION		IG1	INA-OUT
V _{H, CHB}	Overcurrent threshold in forward direction	100 A	1.65 V + 20 x (100 A x 0.33 mΩ) = 2.31 V
V _{L, CHB}	Recovery threshold in forward direction	90 A	1.65 V + 20 x (90 A x 0.33 mΩ) = 2.244 V
V _{H, CHA}	Overcurrent threshold in reverse direction	-35 A	1.65 V + 20 x (-35 A x 0.33 mΩ) = 1.419 V
V _{L, CHA}	Recovery threshold in reverse direction	-31.5 A	1.65 V + 20 x (-31.5 A x 0.33 mΩ) = 1.4421 V

First, focus on the top comparator (channel A), which is in an inverting comparator configuration. This comparator will swing to a logic high when the current in the reverse direction exceeds -35 A, and will return to a logic low when the current in the reverse direction recovers to -31.5 A. These current levels correspond to voltage levels of 1.419 V and 1.4421 V, respectively.

- Assume a value for R₂ (the bottom resistor in the resistor divider). In this circuit, 10 kΩ is chosen.
- Derive two equations for R₁ in terms of V₊, V_L, V_H, R₂, R₃ by analyzing the circuit when INNA = V_L and when INNA = V_H:

$$R_1 = \left(\frac{V_+}{V_L} - 1 \right) \left(\frac{R_2 R_3}{R_2 + R_3} \right)$$

$$R_1 = \frac{\frac{V_+ - V_H}{V_H} - 1}{\frac{V_H}{R_2} - \frac{V_+ - V_H}{R_3}}$$

- Set these two equations equal to each other and then solve for R₃.

$$\left(\frac{\frac{V_+ - V_H}{V_+} - 1}{\frac{V_+ - V_H}{V_H}} \right) R_3^2 + \left(\frac{\frac{V_+ - V_H}{V_+} + V_+ - V_H}{\frac{V_+ - V_H}{V_L}} \right) R_2 R_3 = 0$$

$$\left(\frac{\frac{3.3 - 1.4421}{3.3} - 1.4421}{\frac{3.3 - 1.4421}{1.419}} \right) R_3^2 + \left(\frac{\frac{3.3 - 1.4421}{3.3} + 3.3 - 1.4421}{\frac{3.3 - 1.4421}{1.419}} \right) (10k) R_3 = 0$$

$$R_3 = 0, \quad R_3 = 804.29\text{k}\Omega$$

The standard 1% resistor value closest to this is 806 kΩ.

5. Solve for R_1 using any of the two equations derived in 3:

$$R_1 = \left(\frac{V_+}{V_L} - 1 \right) \left(\frac{R_2 R_3}{R_2 + R_3} \right)$$

$$R_1 = \left(\frac{3.3}{1.419} - 1 \right) \left(\frac{(10 \text{ k}\Omega)(806 \text{ k}\Omega)}{10 \text{ k}\Omega + 806 \text{ k}\Omega} \right)$$

$$R_1 = 13.093 \text{ k}\Omega$$

The standard 1% resistor value closest to this is 13 kΩ.

The next step is to focus on the bottom comparator (channel B), which is in a non-inverting configuration. This comparator will swing to a logic high when the current in the forward direction exceeds 100A, and will return to a logic low when the current in the forward direction recovers to 90A. These current levels correspond to voltage levels of 2.31 V and 2.244 V, respectively.

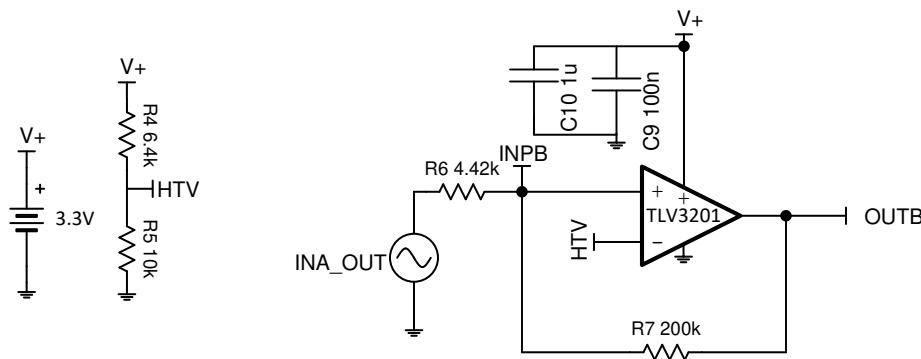


Figure 1-1.

SBOA306 (*High-side current sensing with comparator circuit*) derives two equations for V_{TH} (the voltage on the non-inverting pin) when the comparator output is in a logic low state and a high-impedance state (SBOA306 uses an open-drain comparator). These equations are then set equal to each other creating a quadratic equation to solve for R_6 . Since TLV3202 is a push-pull device, the output will go to a logic high state instead of a high-impedance state. Thus, the pull-up resistor value is 0 and V_{PU} is V_+ .

6. Rewrite the quadratic equation to match this circuit:

$$0 = V_+ \times R_6^2 + (V_+ \times R_7 + V_L \times (R_7) - V_H \times R_7) \times R_6 + (V_L - V_H) \times (R_7^2)$$

$$0 = 3.3 \times R_6^2 + (3.3 \times R_7 + 2.244 \times (R_7) - 2.31 \times R_7) \times R_6 + (2.244 - 2.31) \times (R_7^2)$$

7. Choose a value for R_7 . This resistor dictates the load current of the comparator, and should thus be large. For this circuit, R_7 is assumed to be 200 kΩ.

$$0 = 3.3 \times R_6^2 + (3.3 \times 200\text{k} + 2.244 \times (200\text{k}) - 2.31 \times 200\text{k}) \times R_6 + (2.244 - 2.31) \times (200\text{k})^2$$

$$R_6 = 4.47 \text{ k}\Omega$$

The standard 1% resistor value closest to this is 4.42kΩ.

8. Calculate V_{TH} using R_6 .

$$V_{TH} = V_H \times \left(\frac{R_7}{R_6 + R_7} \right) = 2.31 \times \frac{200\text{k}}{4.42\text{k} + 200\text{k}} = 2.26\text{V}$$

9. Choose a value for R_5 . In this case, R_5 is chosen to be 10 kΩ.

$$V_{TH} = V_H \times \left(\frac{R_2}{R_1 + R_2} \right) = 9.802\text{V}$$

10. Solve for R_4 .

$$R_4 = \frac{R_5 \times (V_s - V_{TH})}{V_{TH}} = \frac{10k \times (3.3 - 2.6)}{2.26} = 4.602 \text{ k}\Omega$$

The standard 1% resistor value closest to this is 4.64 k Ω .

Design Simulations

Transient Simulation Results

The below simulation results use a -70A to 130A, 100Hz sine wave for IG1.

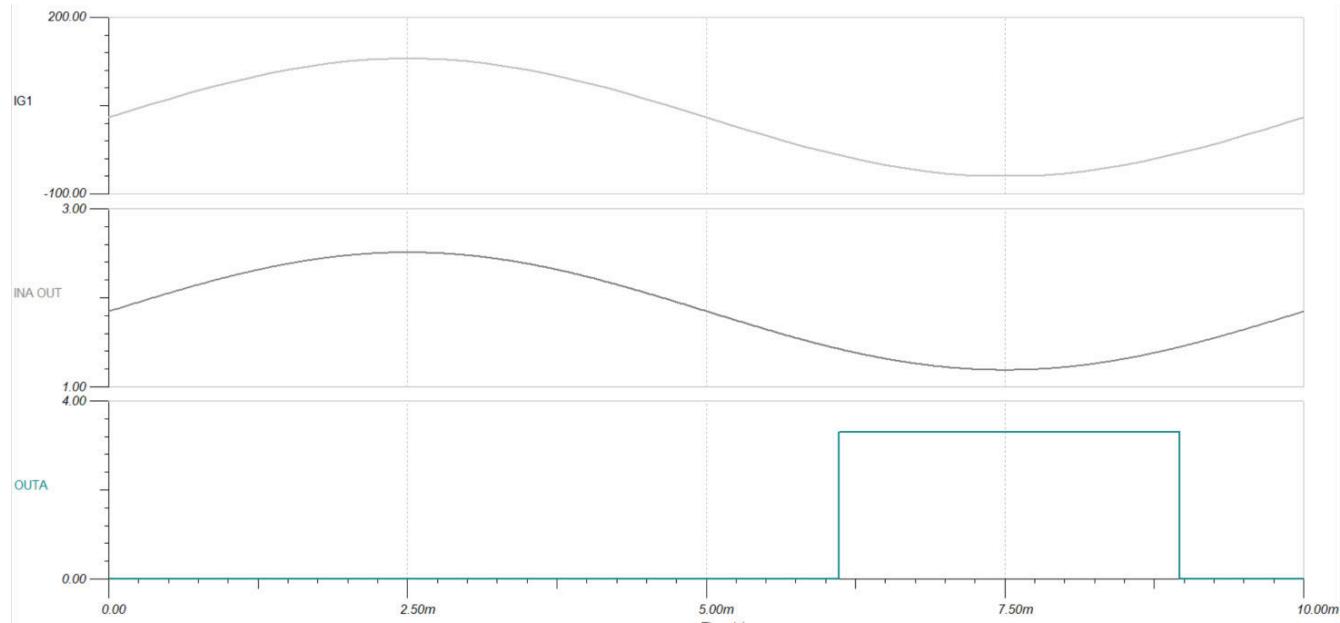


Figure 1-2. Channel A

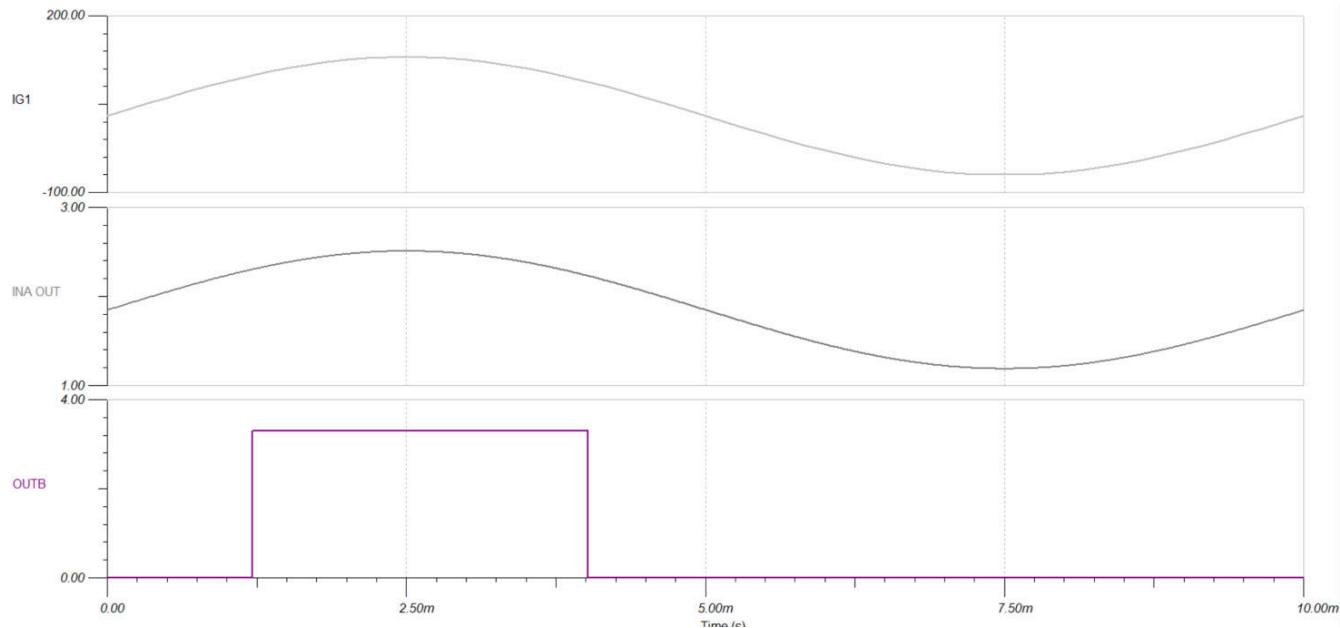


Figure 1-3. Channel B

Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See Circuit SPICE Simulation File [SBOMB05](#).

Design Featured Comparator

TLV320x	
V_S	2.7 V to 5.5 V
V_{inCM}	200 mV beyond either rail
V_{OUT}	Push-Pull, Rail-to-rail
V_{OS}	1 mV
I_Q	40 μ A/channel
$t_{PD(HL)}$	40 ns
#Channels	1, 2
TLV3201-Q1 and TLV3202-Q1	

Design Featured Op Amp

INA240	
V_S	1.6 V to 5.5 V
V_{inCM}	-4 V to 80 V
V_{OUT}	Rail-to-rail
V_{OS}	5 μ V
V_{OS} Drift	50 nV/ $^{\circ}$ C
I_Q	260 ns
Gain Options	20 V/V, 50 V/V, 100 V/V, 200 V/V
INA240	

Single-Supply, Low-Side, Unidirectional Current-Sensing Solution With Output Swing to GND Circuit

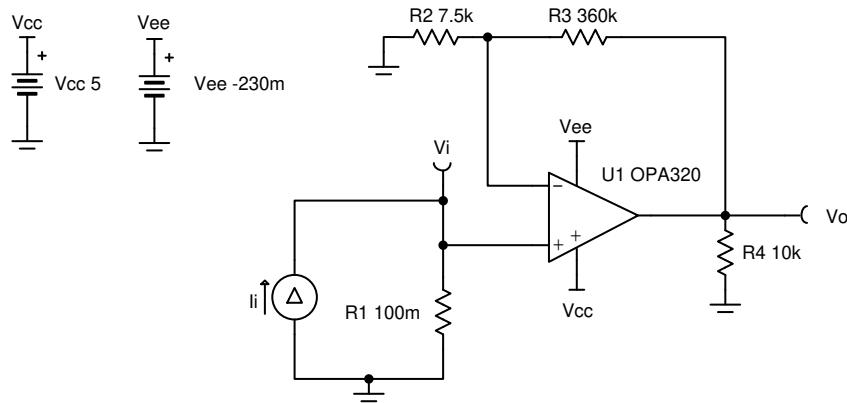


Design Goals

Input		Output		Supply		
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
0 A	1 A	0 V	4.9 V	5 V	0 V	0 V

Design Description

This single-supply, low-side, current sensing solution accurately detects load current between 0 A to 1 A and converts it to a voltage between 0 V to 4.9 V. The input current range and output voltage range can be scaled as necessary and larger supplies can be used to accommodate larger swings. A negative charge pump (such as the LM7705) is used as the negative supply in this design to maintain linearity for output signals near 0 V.



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Design Notes

1. Use precision resistors to minimize gain error.
2. For light load accuracy, the negative supply should extend slightly below ground.
3. A capacitor placed in parallel with the feedback resistor will limit bandwidth and help reduce noise.

Design Steps

1. Determine the transfer function.

$$V_o = I_i \times R_1 \times \left(1 + \frac{R_3}{R_2}\right)$$

2. Define the full-scale shunt voltage and shunt resistance.

$$V_{i\text{Max}} = 100\text{mV} \text{ at } I_{i\text{Max}} = 1A$$

$$R_1 = \frac{V_{i\text{Max}}}{I_{i\text{Max}}} = \frac{100\text{mV}}{1A} = 100\text{m}\Omega$$

3. Select gain resistors to set the output range.

$$V_{i\text{Max}} = 100\text{mV} \text{ and } V_{o\text{Max}} = 4.9V$$

$$\text{Gain} = \frac{V_{o\text{Max}}}{V_{i\text{Max}}} = \frac{4.9V}{100\text{mV}} = 49\frac{V}{V}$$

$$\text{Gain} = 1 + \frac{R_3}{R_2} = 49\frac{V}{V}$$

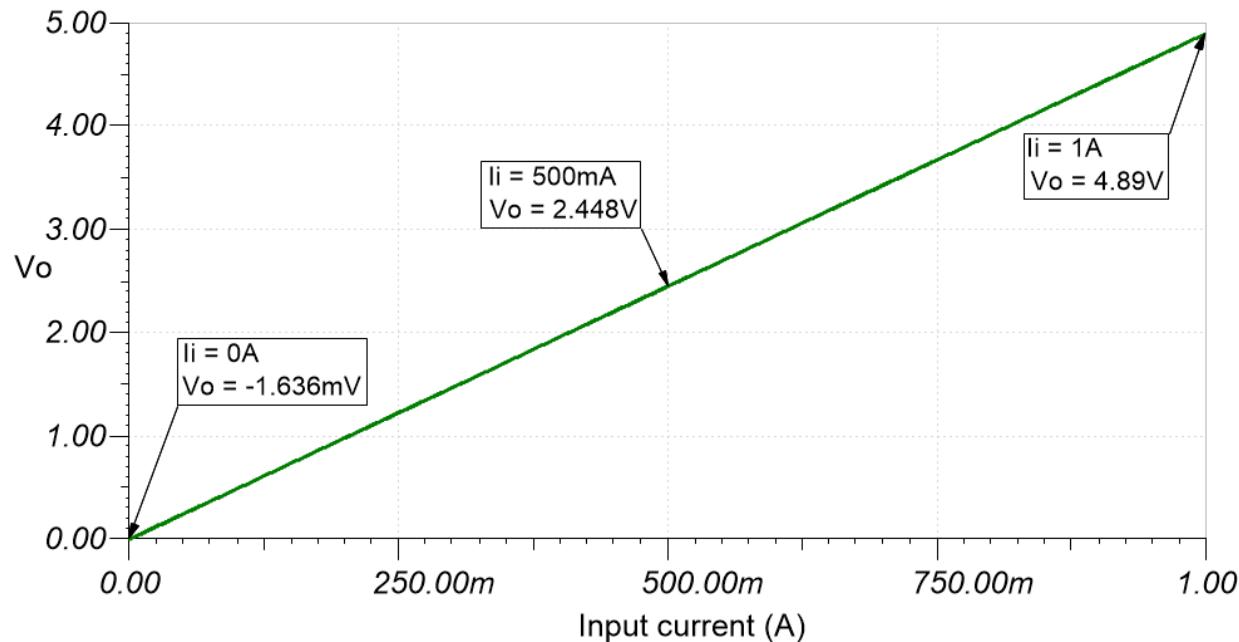
4. Select a standard value for R_2 and R_3 .

$$R_2 = 7.5\text{k}\Omega \text{ (0.05% Standard Value)}$$

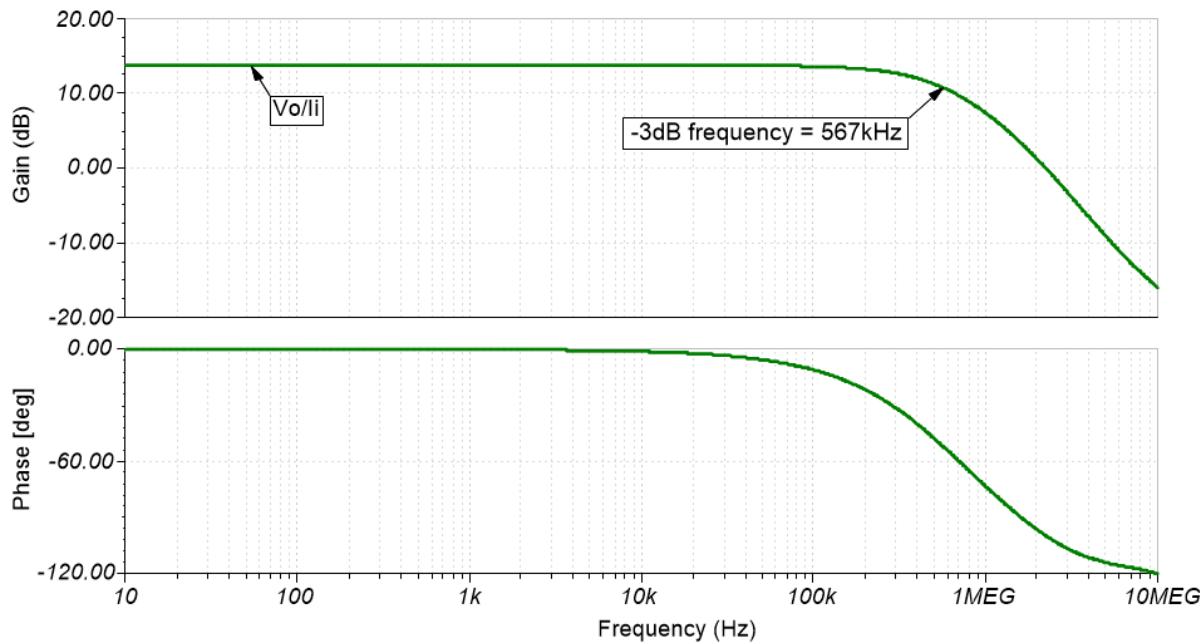
$$R_3 = 48 \times R_2 = 360\text{k}\Omega \text{ (0.05% Standard Value)}$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC499](#).

See [TIPD129](#).

Design Featured Op Amp

OPA320	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	40 μ V
I_q	1.5 mA/Ch
I_b	0.2 pA
UGBW	10 MHz
SR	10 V/ μ s
#Channels	1 and 2
OPA320	

Design Alternate Op Amp

TLV9002	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	400 μ V
I_q	60 μ A
I_b	5 pA
UGBW	1 MHz
SR	2 V/ μ s
#Channels	1, 2, and 4
TLV9002	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 1, 2019

Page

- Downscale the title and changed title role to *Amplifiers*. Added link to circuit cookbook landing page.....[1](#)

High-Side, Bidirectional Current-Sensing Circuit with Transient Protection

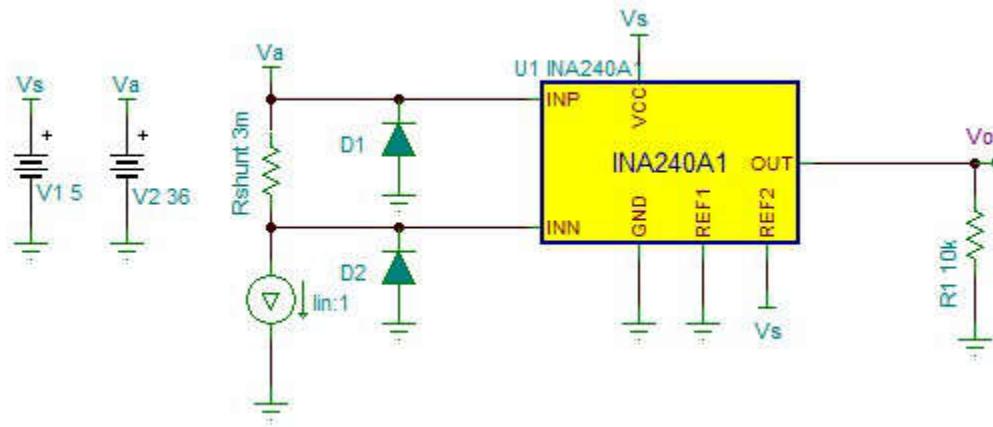


Design Goals

Input		Output		Supply			Standoff and Clamp Voltages		EFT Level
I _{inMin}	I _{inMax}	V _{oMin}	V _{oMax}	V _s	GND	V _{ref}	V _{wm}	V _c	V _{pp}
-40 A	40 A	100 mV	4.9 V	5 V	0 V	2.5 V	36 V	80 V	2 kV 8/20 μ s

Design Description

This high-side, bidirectional current sensing solution can accurately measure current in the range of -40 A to 40 A for a 36 V voltage bus. The linear voltage output is 100 mV to 4.90 V. This solution is also designed to survive IEC61000-4-4 level 4 EFT stress ($V_{oc} = 2 \text{ kV}$; $I_{sc} = 40 \text{ A}$; 8/20 μs).



Design Notes

1. This solution is targeted toward high-side current sensing.
2. The sense resistor value is determined by minimum and maximum load currents, power dissipation and Current Shunt Amplifier (CSA) gain.
3. Bidirectional current sensing requires an output reference voltage (V_{ref}). Device gain is achieved through internal precision matched resistor network.
4. The expected maximum and minimum output voltage must be within the device linear range.
5. The TVS diode must be selected based on bus voltage, the CSA common-mode voltage specification, and EFT pulse characteristics.

Design Steps

- Determine the maximum output swing:

$$V_{swN} = V_{ref} - V_{oMin} = 2.5V - 0.1V = 2.4V$$

$$V_{swP} = V_{oMax} - V_{ref} = 4.9V - 2.5V = 2.4V$$

- Determine the maximum value of the sense resistor based on maximum load current, swing and device gain. In this example, a gain of 20 was chosen to illustrate the calculation, alternative gain versions may be selected as well:

$$R_{shunt} \leq \frac{V_{swP}}{I_{in_max} \times \text{Gain}} = \frac{2.4V}{40A \times 20} = 3m\Omega$$

- Calculate the peak power rating of the sense resistor:

$$P_{shunt} = I_{in_max}^2 \times R_{shunt} = 40A^2 \times 3m\Omega = 5W$$

- Determine TVS standoff voltage and clamp voltage:

$$V_{wm} = 36V \text{ and } V_c \leq 80V$$

- Select a TVS diode.

For example, SMBJ36A from Littelfuse™ satisfies the previous requirement, with peak pulse power of 600 W (10/1000 μ s) and current of 10.4 A.

- Make sure the TVS diode satisfies the design requirement based on the TVS operating curve.

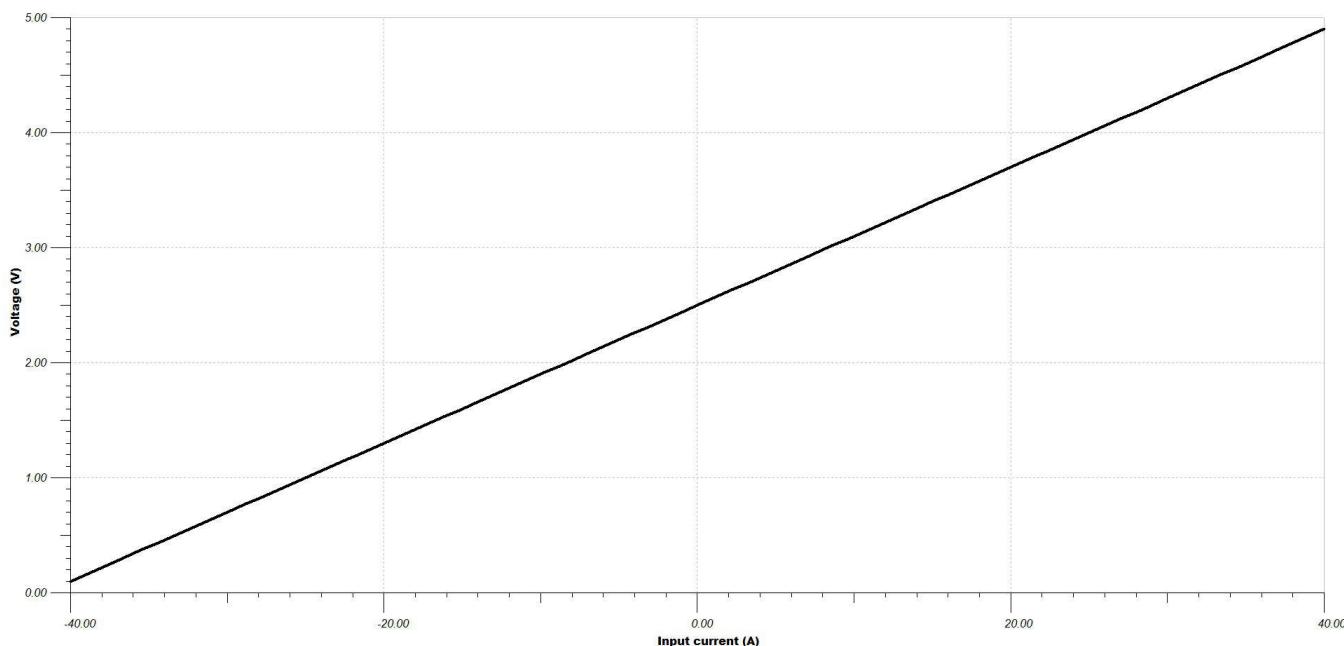
Peak pulse power at given excitation (8/20 μ s) is estimated to be around 3.5 kW, which translates to peak pulse current:

$$I_{pp} = \frac{3.5kW}{600W} \times 10.4A = 60A$$

This is above the maximum excitation (short circuit) current of 40 A. The select TVS effectively protects the circuit against the specified EFT strike.

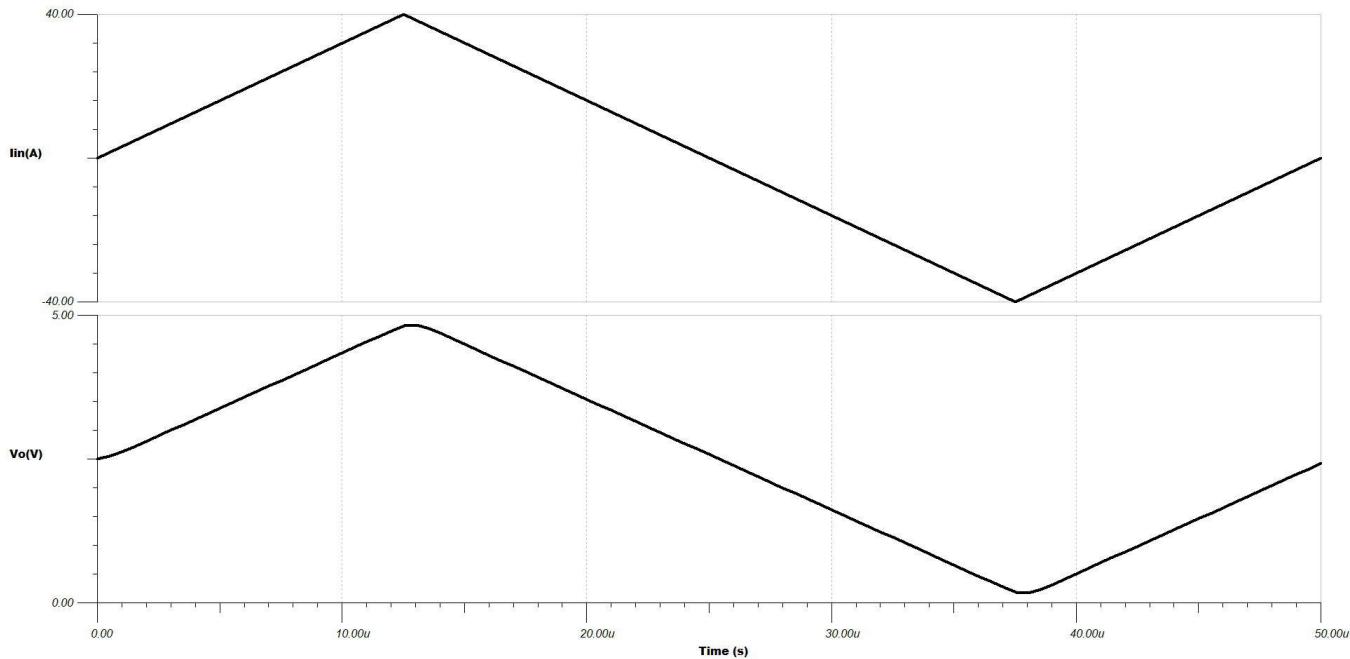
Design Simulations

DC Transfer Characteristics

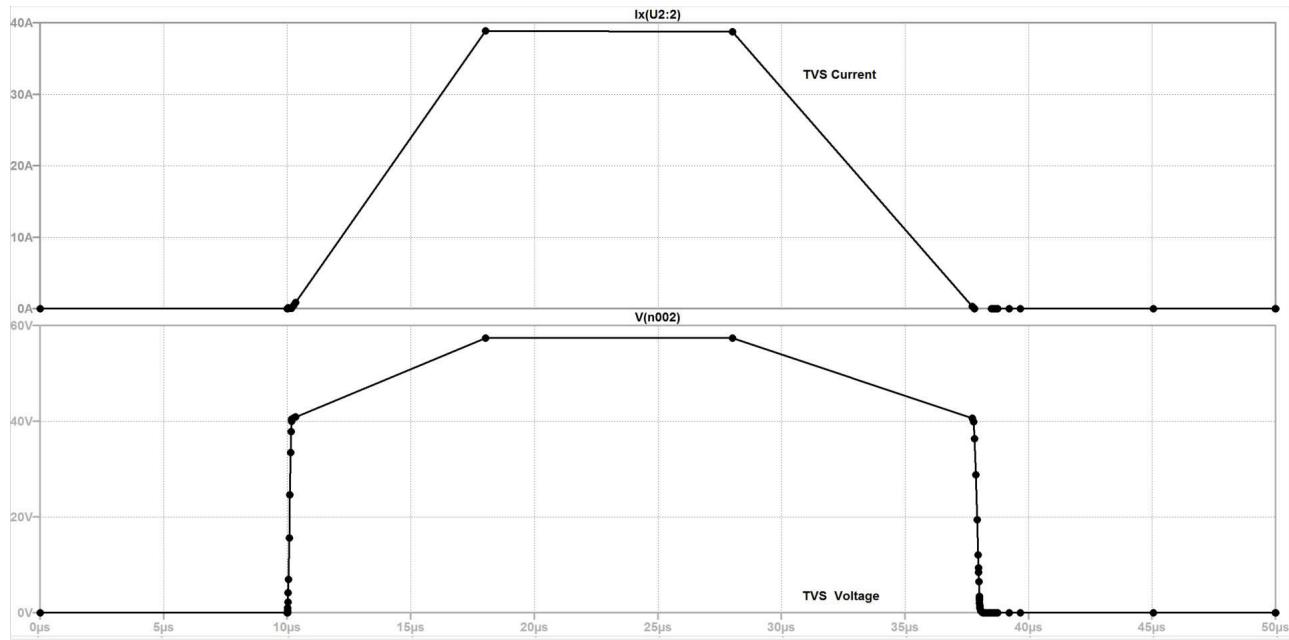


Transient Simulation Results

The output is a scaled version of the input.



TVS Diode Transient Response Under EFT Excitation



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

For more information on transient protection of the current sense amplifiers, see [TIDA-00302](#) and the [Current Sense Amplifier Training Videos](#).

Design Featured Current Sense Amplifier

INA240A1	
V_s	2.7 V to 5.5 V
V_{CM}	-4 V to 80 V
V_{os}	Rail-to-rail
V_{os}	5 μ V
I_B	80 μ A
BW	400 kHz
Vos Drift	50 nV/ $^{\circ}$ C
INA240A1	

Design Alternate

INA282	
V_s	2.7 V to 18 V
V_{CM}	-14 V to 80 V
V_{os}	20 μ V
I_B	25 μ A
BW	10 kHz
Vos Drift	0.3 μ V/ $^{\circ}$ C
INA282	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from May 15, 2018 to February 19, 2019

Page

- Changed VinMin and VinMax in the *Design Goals* table to linMin and linMax, respectively.....1

3-Decade, Load-Current Sensing Circuit

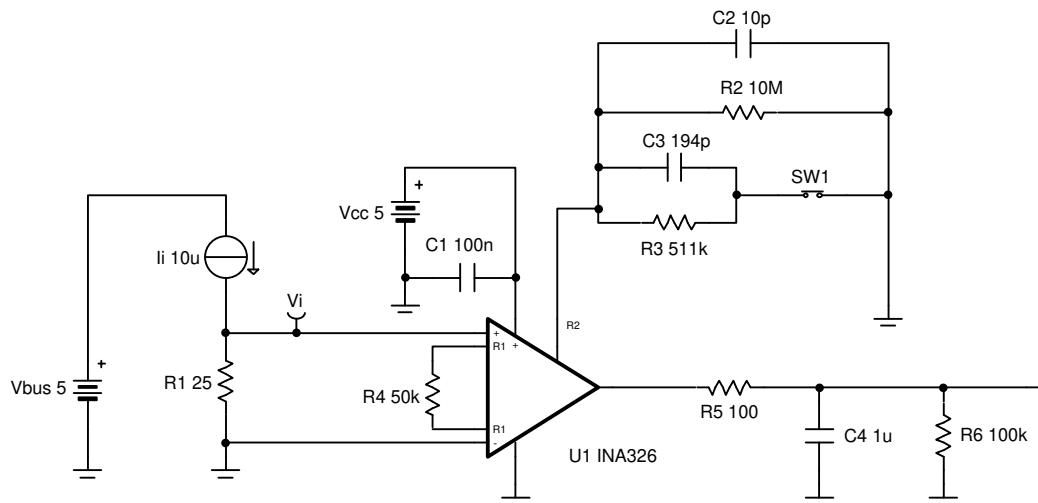


Design Goals

Input		Output		Supply		
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
10 μ A	10 mA	100 mV	4.9 V	5.0 V	0 V	0 V

Design Description

This single-supply, low-side, current-sensing solution accurately detects load current between 10 μ A and 10 mA. A unique yet simple gain switching network was implemented to accurately measure the three-decade load current range.



Design Notes

1. Use a maximum shunt resistance to minimize relative error at minimum load current.
2. Select 0.1% tolerance resistors for R_1 , R_2 , R_3 , and R_4 in order to achieve approximately 0.1% FSR gain error.
3. Use a switch with low on-resistance (R_{on}) to minimize interaction with feedback resistances, preserving gain accuracy.
4. Minimize capacitance on INA326 gain setting pins.
5. Scale the linear output swing based on the gain error specification.

Design Steps

1. Define full-scale shunt resistance.

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{250mV}{10mA} = 25\Omega$$

2. Select gain resistors to set output range.

$$G_{iMax} = \frac{V_{oMax}}{V_{iMax}} = \frac{V_{oMax}}{R_1 \times I_{iMax}} = \frac{4.9V}{25\Omega \times 10mA} = 19.6\frac{V}{V}$$

$$G_{iMin} = \frac{V_{oMin}}{V_{iMin}} = \frac{V_{oMin}}{R_1 \times I_{iMin}} = \frac{100mV}{25\Omega \times 10\mu A} = 400\frac{V}{V}$$

$$R_2 = \frac{R_4 \times G_{iMin}}{2} = \frac{50k\Omega \times 400\frac{V}{V}}{2} = 10M\Omega$$

$$R_2 \parallel R_3 = \frac{R_4 \times G_{iMax}}{2} = \frac{50k\Omega \times 19.6\frac{V}{V}}{2} = 490k\Omega$$

$$R_3 = \frac{490k\Omega \times R_2}{R_2 - 490k\Omega} = 515.25k\Omega \approx 511k\Omega \text{ (Standard Value)}$$

3. Select a capacitor for the output filter.

$$f_p = \frac{1}{2 \times \pi \times R_5 \times C_4} = \frac{1}{2 \times \pi \times 100\Omega \times 1 \mu F} = 1.59kHz$$

4. Select a capacitor for gain and filtering network.

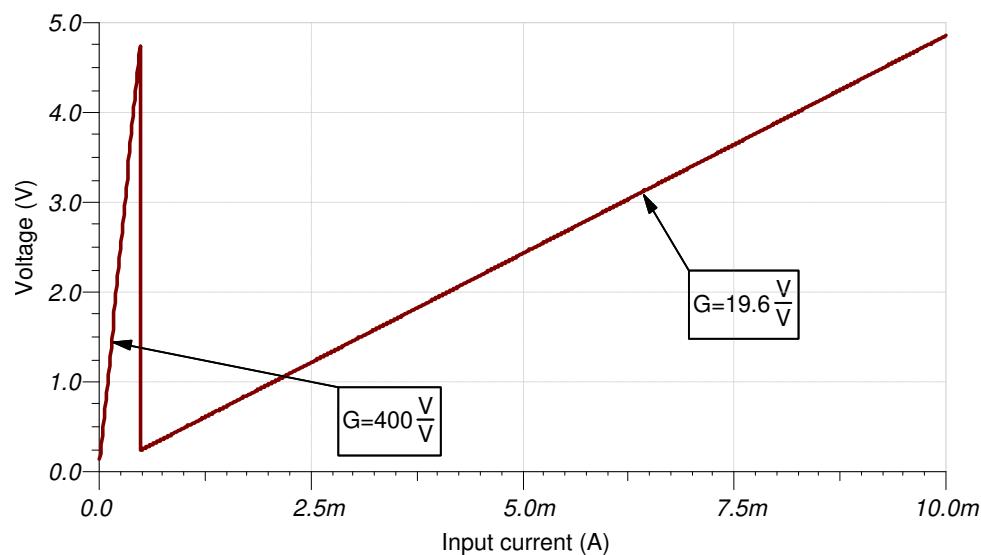
$$C_2 = \frac{1}{2 \times \pi \times R_2 \times f_p} = \frac{1}{2 \times \pi \times 10M\Omega \times 1.59kHz} = 10pF$$

$$C_3 = \frac{1}{2 \times \pi \times (R_2 \parallel R_3) \times f_p} - C_2 = \frac{1}{2 \times \pi \times (10M\Omega \parallel 511k\Omega) \times 1.59kHz} - 10pF$$

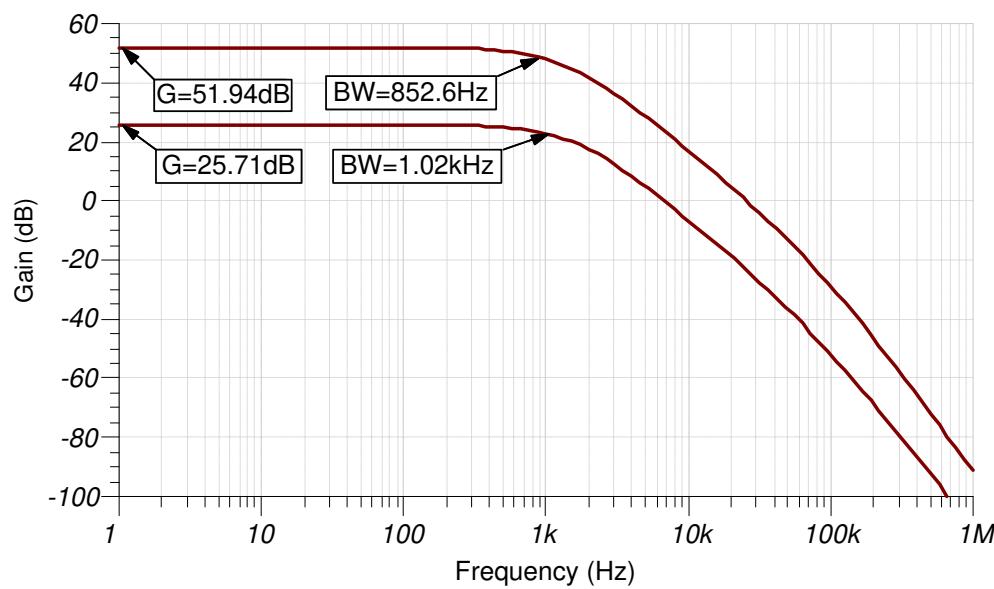
$$C_3 = 196pF \approx 194pF \text{ (Standard Value)}$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC498](#).

See TIPD104, [Current Sensing Solution, 10 µA-10 mA, Low-Side, Single Supply](#).

Design Featured Op Amp

INA326	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.1 mV
I_q	3.4 mA
I_b	2 nA
UGBW	1 kHz
SR	Filter limited
#Channels	1
INA326	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from January 28, 2018 to February 1, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.....1

Analog Engineer's Circuit

PWM Generator Circuit

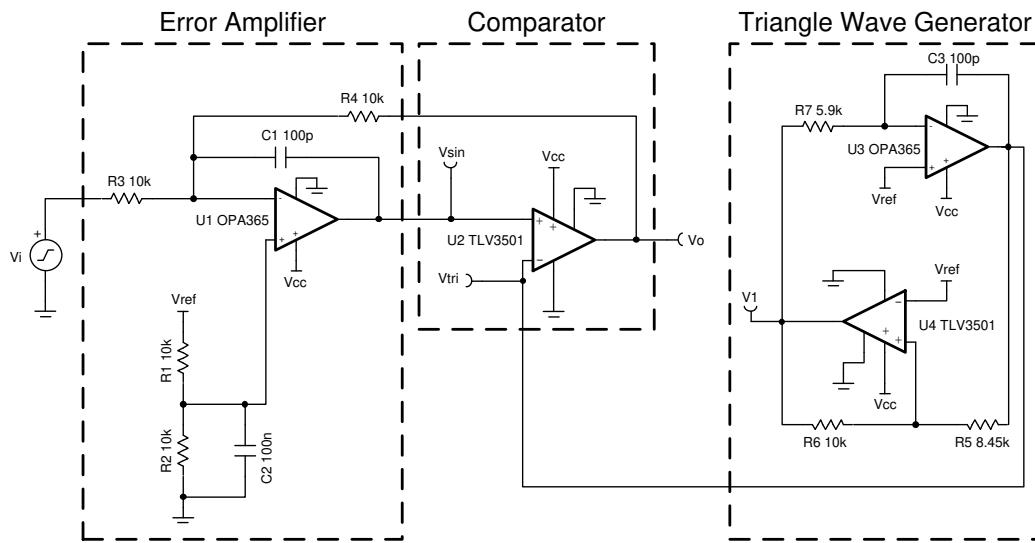


Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	V_{cc}	V_{ee}	V_{ref}
-2.0 V	2.0 V	0 V	5 V	5 V	0 V	2.5 V

Design Description

This circuit utilizes a triangle wave generator and comparator to generate a 500 kHz pulse-width-modulated (PWM) waveform with a duty cycle that is inversely proportional to the input voltage. An op amp and comparator (U_3 and U_4) generate a triangle waveform which is applied to the inverting input of a second comparator (U_2). The input voltage is applied to the non-inverting input of U_2 . By comparing the input waveform to the triangle wave, a PWM waveform is produced. U_2 is placed in the feedback loop of an error amplifier (U_1) to improve the accuracy and linearity of the output waveform.



Design Notes

1. Use a comparator with push-pull output and minimal propagation delay.
2. Use an op amp with sufficient slew rate, GBW, and voltage output swing.
3. Place the pole created by C_1 below the switching frequency and well above the audio range.
4. V_{ref} must be low impedance (for example, output of an op amp).

Design Steps

- Set the error amplifier inverting signal gain.

$$\text{Gain} = -\frac{R_4}{R_3} = -1 \frac{V}{V}$$

Select $R_3 = R_4 = 10k\Omega$

- Determine R_1 and R_2 to divide V_{ref} to cancel the non-inverting gain.

$$V_{o_dc} = \left(1 + \frac{R_4}{R_3}\right) \left(\frac{R_2}{R_1 + R_2}\right) \times V_{\text{ref}}$$

$R_1 = R_2 = R_3 = R_4 = 10k\Omega, V_{o_dc} = 2.5V$

- The amplitude of V_{tri} must be chosen such that it is greater than the maximum amplitude of V_i (2.0 V) to avoid 0% or 100% duty cycle in the PWM output signal. Select V_{tri} to be 2.1 V. The amplitude of $V_1 = 2.5V$.

$$V_{\text{tri}} (\text{Amplitude}) = \frac{R_5}{R_6} \times V_1 (\text{Amplitude})$$

Select R_6 to be $10k\Omega$, then compute R_5

$$R_5 = \frac{V_{\text{tri}} (\text{Amplitude}) \times R_6}{V_1 (\text{Amplitude})} = 8.4k\Omega \approx 8.45k\Omega \text{ (Standard Value)}$$

- Set the oscillation frequency to 500 kHz.

$$f_t = \frac{R_6}{4 \times R_7 \times R_5 \times C_3}$$

Set $C_3 = 100\text{pF}$, then compute R_7

$$R_7 = \frac{R_6}{4 \times f_t \times R_5 \times C_3} = 5.92k\Omega \approx 5.90k\Omega \text{ (Standard Value)}$$

- Choose C_1 to limit amplifier bandwidth to below switching frequency.

$$f_p = \frac{1}{2 \times \pi \times R_4 \times C_1}$$

$$C_1 = 100\text{pF} \rightarrow f_p = 159\text{kHz}$$

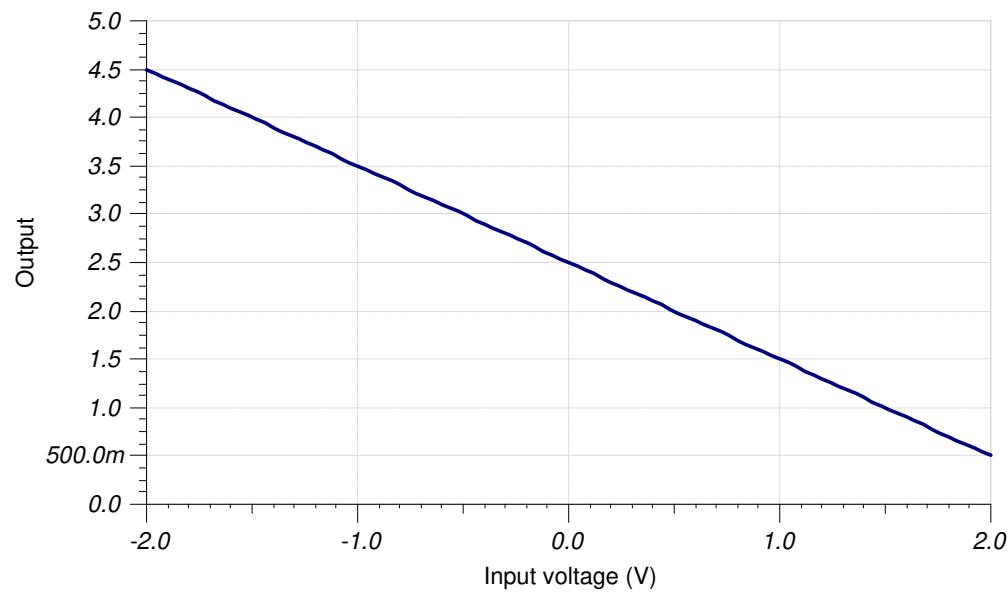
- Select C_2 to filter noise from V_{ref} .

$$C_2 = 100\text{nF} \text{ (Standard Value)}$$

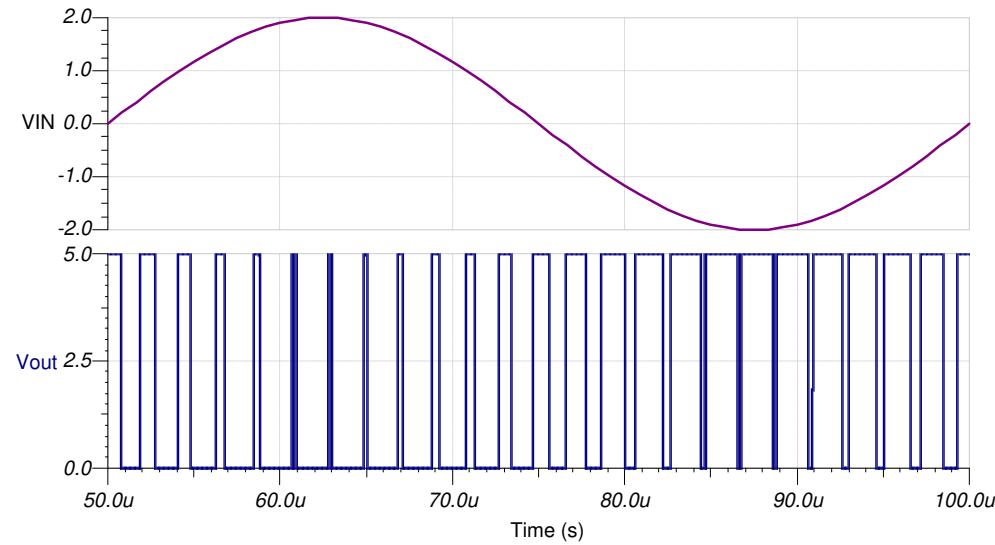
$$f_{\text{div}} = \frac{1}{2 \times \pi \times C_2 \times \frac{R_1 \times R_2}{R_1 + R_2}} = 320\text{Hz}$$

Design Simulations

DC Simulation Results



Transient Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC502](#).

See TIPD108, [Analog PWM Generator 5V, 500 kHz PWM Output](#)

Design Featured Op Amp

OPA2365	
V_{ss}	2.2 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	100 μ V
I_q	4.6 mA
I_b	2 pA
UGBW	50 MHz
SR	25 V/ μ s
#Channels	2
OPA2365	

Design Comparator

TLV3502	
V_{ss}	2.2 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1 mV
I_q	3.2 mA
I_b	2 pA
UGBW	—
SR	—
#Channels	2
TLV3502	

Design Alternate Op Amp

OPA2353	
V_{ss}	2.7 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	3 mV
I_q	5.2 mA
I_b	0.5 pA
UGBW	44 MHz
SR	22 V/ μ s
#Channels	2
OPA2353	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from January 19, 2018 to February 1, 2019	Page
• Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page..... 1	

Analog Engineer's Circuit

Sine wave generator circuit



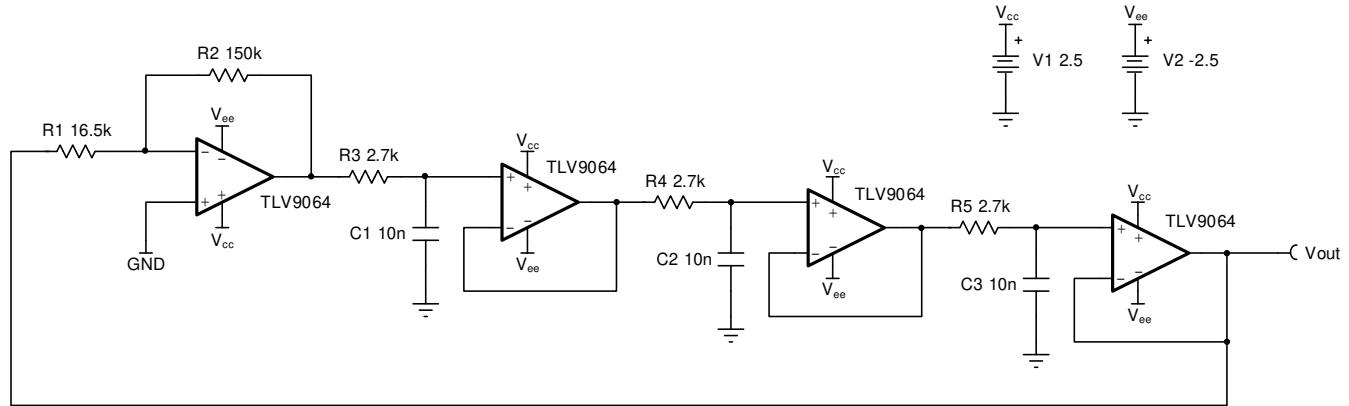
Amplifiers

Design Goals

AC Specifications		Supply	
AC Gain	$f_{\text{oscillation}}$	V_{cc}	V_{ee}
8V/V	10kHz	2.5V	-2.5V

Design Description

This circuit uses a quad channel op amp with ± 2.5 -V supplies to generate a 10kHz, low-distortion sine wave. The amplifiers buffer each RC filter stage, which yields a low-distortion output.



Design Notes

1. Using excessively large feedback resistors, R_1 and R_2 , can lead to a shift in oscillation frequency, and an increase in noise and distortion.
2. The first stage resistors, R_1 and R_2 , must be selected to provide a sufficiently large gain. Otherwise, oscillations at the output will dampen. However, an excessively large gain at the first stage will lead to higher output distortion and a decreased frequency of oscillation.
3. Heavy loading of the output leads to degradation in the oscillation frequency.
4. At higher frequencies (> 10 kHz), the phase delay of the amplifier becomes significant. The result will be a frequency of oscillation that is lower than calculated or expected. Thus, some margin must be included when selecting values for the loading elements of the first, second, and third stages (R_3 , R_4 , R_5 , C_1 , C_2 , and C_3) for higher-frequency designs to ensure the desired oscillation frequency is achieved.
5. Choose an amplifier with at least 100 times the required gain bandwidth product. This will ensure the actual and calculated oscillation frequencies match.
6. For more precise control of the oscillation frequency, use passive components with lower tolerances.

Design Steps

For a classical feedback system, oscillation occurs when the product of the open loop gain, A_{OL} , and the feedback factor, β , is equal to -1 , or 1 at 180° . Therefore, each RC stage in the design must contribute 60° of phase shift. Since each stage is isolated by a buffer, the feedback factor, β , of the first stage must have a magnitude of $(1/2)^3$. Therefore the gain $(1/\beta)$ must be at least $8V/V$.

$$1. \quad A_{OL} \times \beta = A_{OL} \times \left(\frac{1}{RC_s} + 1 \right)^3$$

Select the first stage feedback resistors for the gain necessary to maintain oscillation.

$$\text{Gain} = \frac{R_2}{R_1} \geq 8\text{V}$$

$$R_1 = 16.5k\Omega, R_2 = 150k\Omega \text{ (Standard Values)}$$

2. Calculate components R_3 , R_4 , R_5 , C_1 , C_2 , and C_3 to set the oscillation frequency. Select C_1 , C_2 , and C_3 as $10nF$.

$$f_{\text{oscillation}} = \frac{\tan(60^\circ)}{2\pi \times R \times C} = 10\text{kHz}$$

$$C_{1,2,3} = 10nF \text{ (Standard Values)}$$

$$R_{3,4,5} = \frac{\tan(60^\circ)}{2\pi \times C \times f_{\text{oscillation}}} = \frac{1.73}{2\pi \times 10nF \times 10\text{kHz}} = 2757\Omega \approx 2.7k\Omega \text{ (Standard Values)}$$

3. Ensure the selected op amp has the bandwidth to oscillate at the desired frequency.

$$f_{\text{oscillation}} \ll \frac{\text{GBW}}{\text{Gain}} = \frac{\text{GBW}}{\left(\frac{R_2}{R_1}\right) + 1}$$

$$10\text{kHz} \ll \frac{10\text{MHz}}{\left(\frac{150k\Omega}{16.5k\Omega}\right) + 1} \cong 991\text{kHz}$$

4. Ensure the selected op amp has the slew rate necessary to oscillate at the desired frequency. Use the full power bandwidth equation to calculate the necessary slew rate and ensure it is less than the slew rate of the amplifier. While the exact amplitude of oscillation is difficult to predict, you can ensure that our amplifier is fast enough to generate the needed sine wave by ensuring that the output can swing from rail-to-rail.

$$SR_{\text{req}} = V_{\text{peak}} \times 2\pi f_{\text{oscillation}} = 2.5V \times 2\pi \times 10\text{kHz} = 0.157 \frac{V}{\mu s}, \text{ given } V_{\text{cc}} = V_{\text{peak}}$$

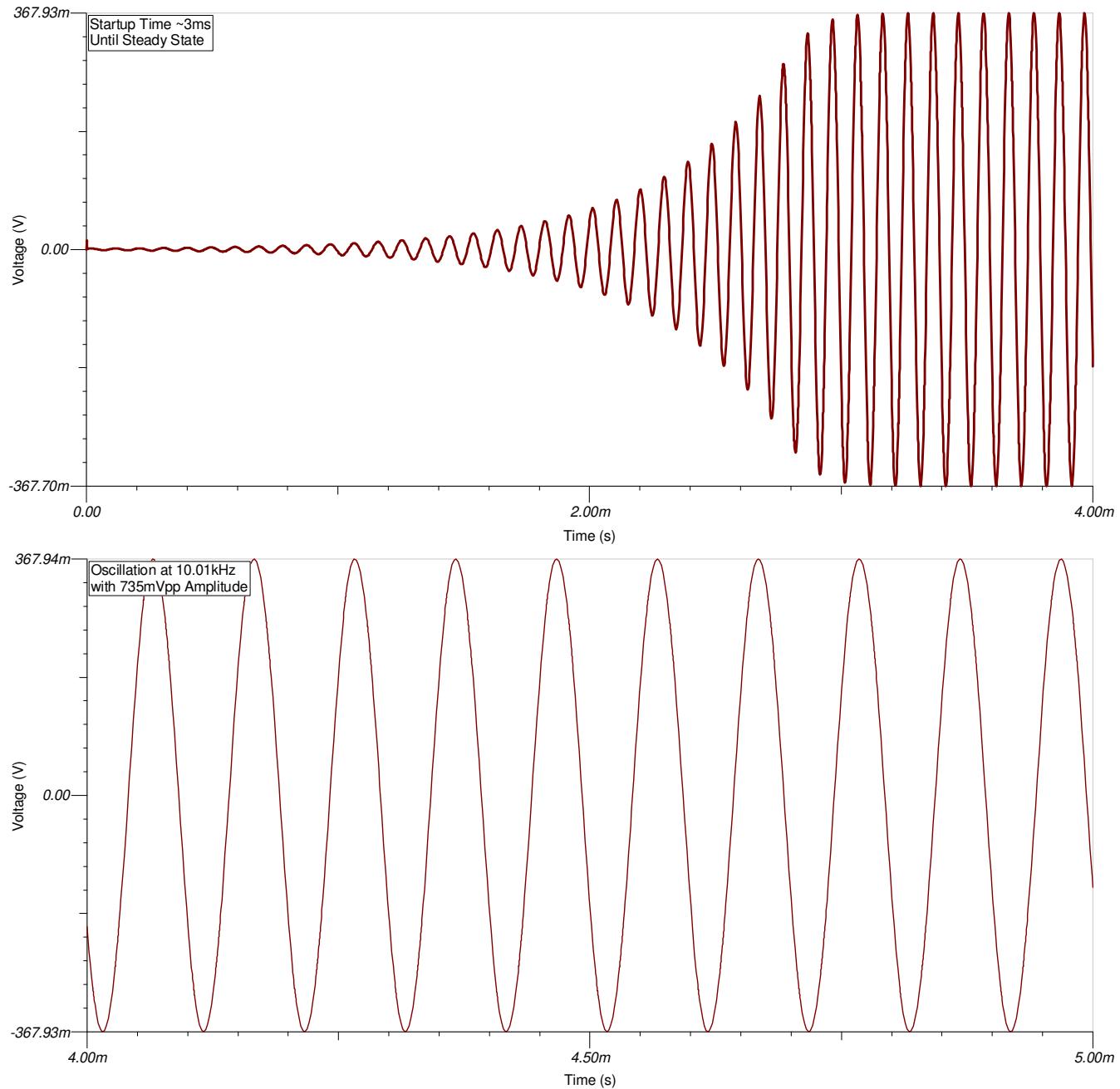
$$SR_{\text{req}} < SR_{\text{TLV9064}}$$

$$0.157 \frac{V}{\mu s} < 6.5 \frac{V}{\mu s}$$

Design Simulations

The resulting simulations demonstrate a sinusoidal oscillator that reaches steady state after about 3ms to a 10.01-kHz sine wave with a 735-mV_{pp} amplitude.

Transient Simulation Results



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.
2. SPICE Simulation File: [SLOC355](#).
3. [TI Precision Labs](#)
4. [Sine-Wave Oscillator Application Report](#)
5. [Design of Op Amp Sine Wave Generators Application Report](#)

Design Featured Op Amp

TLV9064	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	300µV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9064	

Design Alternate Op Amps

	TLV9052	OPA4325
V_{ss}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{out}	Rail-to-rail	Rail-to-rail
V_{os}	330µV	40µV
I_q	330µA	650µA
I_b	2pA	0.2pA
UGBW	5MHz	10MHz
SR	15V/µs	5V/µs
#Channels	2	4
	www.ti.com/product/TLV9052	www.ti.com/product/OPA4325

Adjustable Reference Voltage Circuit

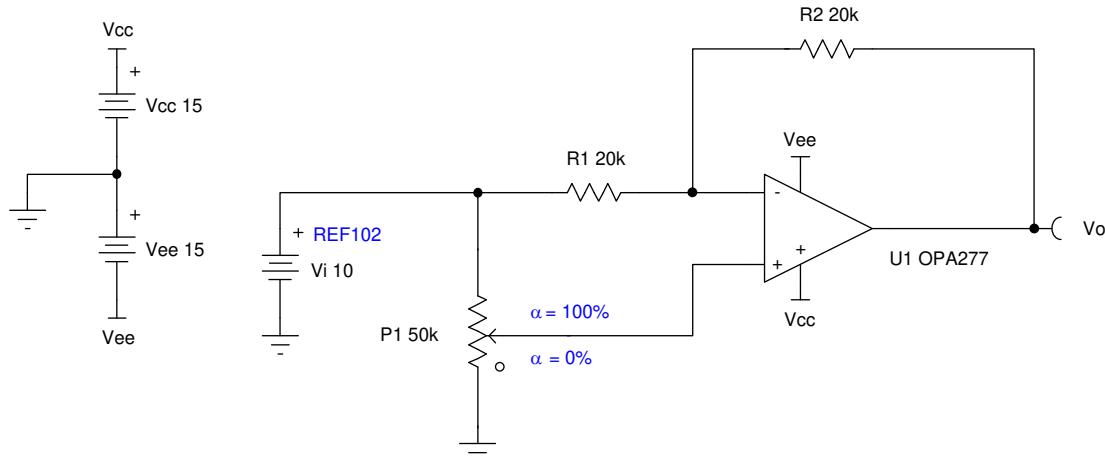


Design Goals

Input	Output		Supply	
V_i	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
10 V	-10 V	10 V	15 V	-15 V

Design Description

This circuit combines an inverting and non-inverting amplifier to make a reference voltage adjustable from the negative of the input voltage up to the input voltage. Gain can be added to increase the maximum negative reference level.

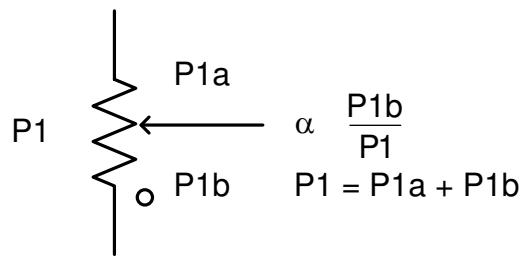


Design Notes

1. Observe the common-mode and output swing limitations of the op amp.
2. Mismatch in R_1 and R_2 results in a gain error. Selecting $R_2 > R_1$ increases the maximum negative voltage, and selecting $R_2 < R_1$ decreases the maximum negative voltage. In either case, the maximum positive voltage is always equal to the input voltage. This relationship is inverted if a negative input reference voltage is used.
3. Select the potentiometer based on the desired resolution of the reference. Generally, the potentiometers can be set accurately to within one-eighth of a turn. For a 10-turn pot this means alpha (α) may be off by as much as 1.25%.

Design Steps

Alpha represents the potentiometer setting relative to ground. This is the fraction of the input voltage that will be applied to the non-inverting terminal of the op amp and amplified by the non-inverting gain.



The transfer function of this circuit follows:

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1} + \alpha \left(1 + \frac{R_2}{R_1}\right)$$

1. If $R_2 = R_1 = 20 \text{ k}\Omega$, then the equation for V_o simplifies as the following shows:

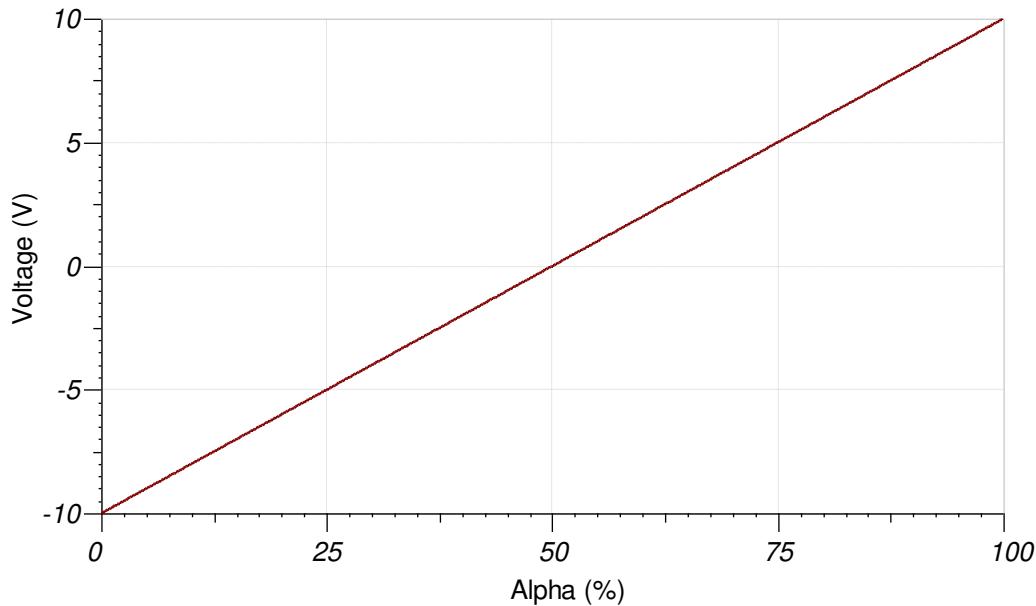
$$V_o = (2\alpha - 1) \times V_i$$

2. If $V_i = 10\text{V}$ and $\alpha = 0.75$, the value of V_o can be determined.

$$V_o = (2 \times 0.75 - 1) \times 10 = 5\text{V}$$

Design Simulations

DC Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the TINA-TI™ circuit simulation file, [SBOMAU2](#).

See [TI Precision Labs - Op Amps](#).

Design Featured Op Amp

OPA277	
V_{ss}	4 V to 36 V
V_{inCM}	V _{ee} +2 V to V _{cc} -2 V
V_{out}	V _{ee} +0.5 V to V _{cc} -1.2 V
V_{os}	10 μ V
I_q	790 μ A/Ch
I_b	500 pA
UGBW	1 MHz
SR	0.8 V/ μ s
#Channels	1, 2, and 4
OPA277	

Design Alternate Op Amp

OPA172	
V_{ss}	4.5 V to 36 V
V_{inCM}	V _{ee} -0.1 V to V _{cc} -2 V
V_{out}	Rail-to-rail
V_{os}	200 μ V
I_q	1.6 mA/Ch
I_b	8 pA
UGBW	10 MHz
SR	10 V/ μ s
#Channels	1, 2, and 4
OPA172	

Voltage-to-current (V-I) converter circuit with BJT



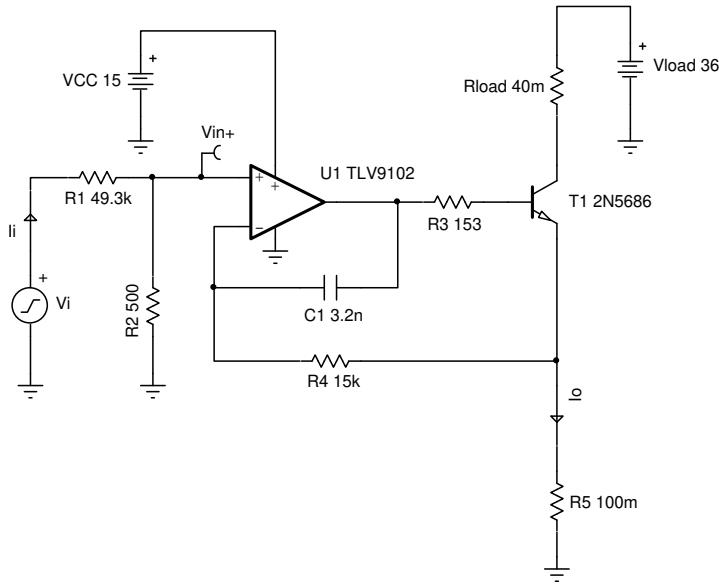
Amplifiers

Design Goals

Input			Output		Supply		
V_{iMin}	V_{iMax}	I_{iMax}	I_{oMin}	I_{oMax}	V_{cc}	V_{ee}	V_{load}
0V	10V	200 μ A	0A	1A	15V	0V	36V

Design Description

This low-side voltage-to-current (V-I) converter delivers a well-regulated current to a load which can be connected to a voltage greater than the op amp supply voltage. The circuit accepts an input voltage from 0V to 10V and converts it to a current from 0A and 1A. The current is accurately regulated by feeding back the voltage drop across a low-side current-sense resistor (R_5) to the op amp.



Design Notes

1. Resistor divider (R_1 and R_2) is implemented to limit the maximum voltage at the non-inverting input, V_{in+} , and sense resistor, R_5 , at full-scale.
2. For an op amp that is not rail-to-rail input (RRI), a voltage divider may be needed to reduce the input voltage to be within the common-mode voltage of the op amp.
3. Use low resistance values for R_5 to maximize load compliance voltage and reduce the power dissipated at full-scale.
4. Using a high-gain BJT reduces the output current requirement for the op amp.
5. Feedback components R_3 , R_4 , and C_1 provide compensation to ensure stability. R_3 isolates the input capacitance of the bipolar junction transistor (BJT), R_4 provides a DC feedback path directly at the current-setting resistor (R_5), and C_1 provides a high-frequency feedback path that bypasses the BJT.
6. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions in the device data sheet.

Design Steps

The transfer function of the circuit is:

$$I_o = \frac{R_2}{R_5 \times (R_1 + R_2)} \times V_i$$

1. Calculate the sense resistor, R_5 . The sense resistor should be sized as small as possible to maximize the load compliance voltage and reduce power dissipation. Set the maximum voltage across the sense resistor to 100mV. Limiting the voltage drop to 100mV limits the power dissipated in the sense resistor to 100mW at full-scale output.

Let $V_{in-}(max) = 100mV$ at $I_{oMax} = 1A$

$$R_5 = \frac{V_{in-}(max)}{I_{oMax}} = \frac{100mV}{1A} = 100m\Omega$$

2. Select resistors, R_1 and R_2 , for the voltage divider at the input. At the maximum input voltage, the voltage divider should reduce the input voltage to the op amp, $V_{in+}(max)$, to the maximum voltage across the sense resistor, R_5 . R_1 and R_2 should be chosen such that the maximum input current is not exceeded.

$$V_{in-}(max) = V_{in+}(max) = I_{iMax} \times R_2 = 100mV$$

$$R_2 = \frac{V_{in+}(max)}{I_{iMax}} = \frac{100mV}{200\mu A} = 500\Omega \sim 499\Omega \text{ (Standard value)}$$

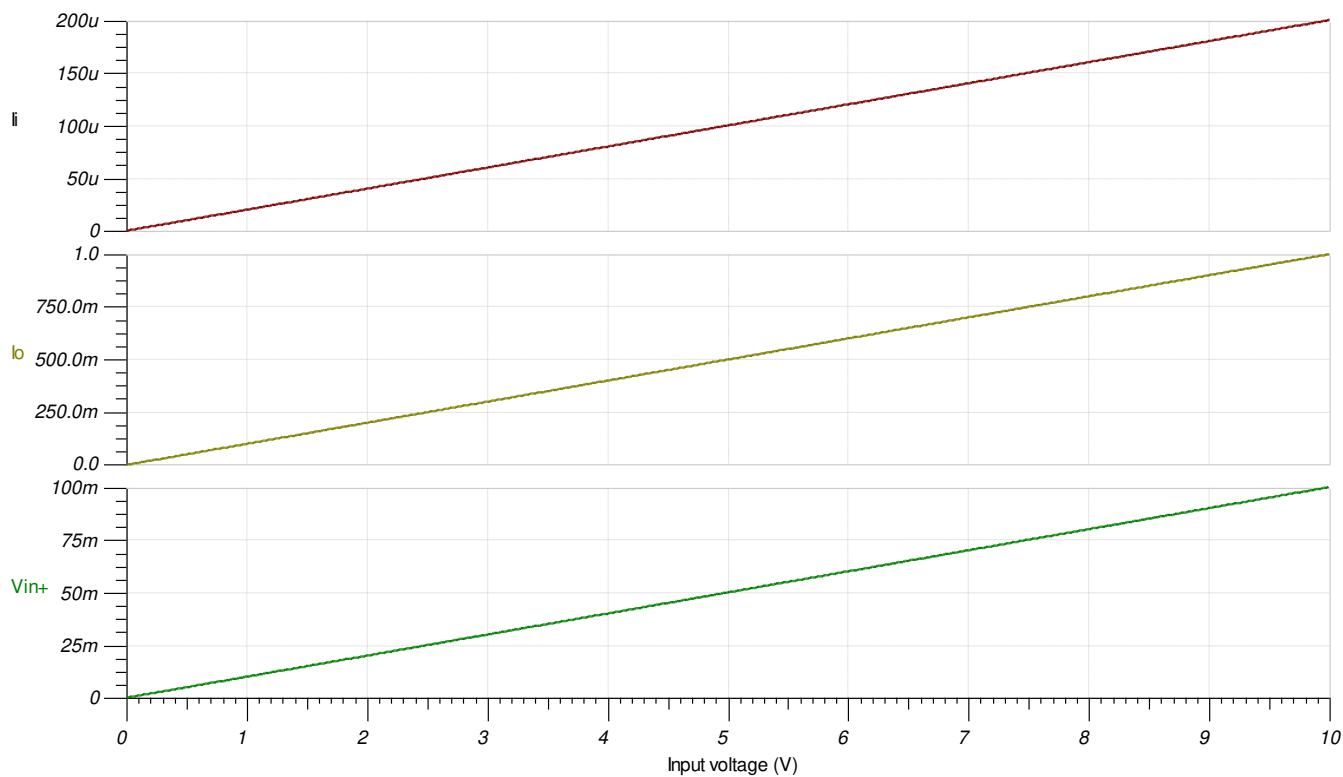
$$V_{in+}(max) = V_{iMax} \times \left(\frac{R_2}{R_1 + R_2} \right)$$

$$R_1 = 49.5k\Omega \sim 49.3k\Omega \text{ (Standard value)}$$

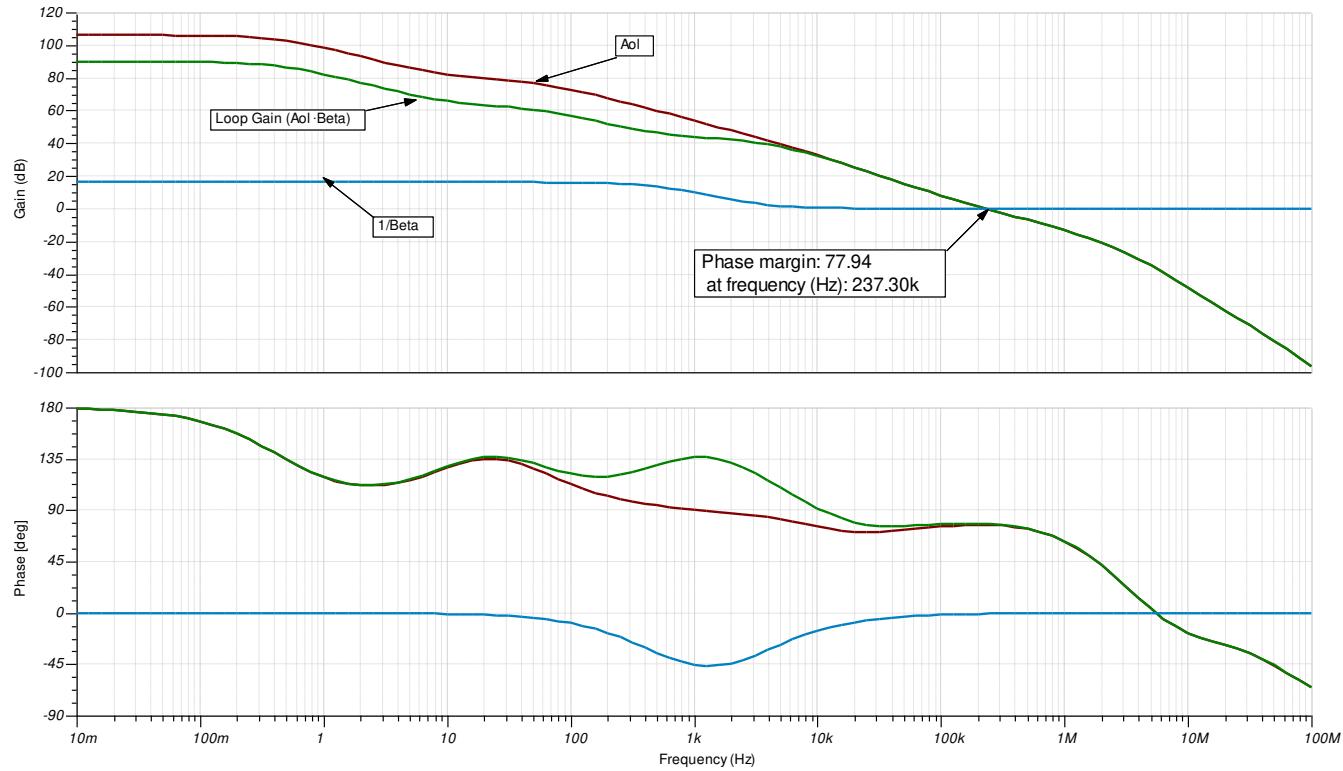
3. See the [Design References](#) section [3] for the design procedure on how to properly size the compensation components, R_3 , R_4 , and C_1 .

Design Simulations

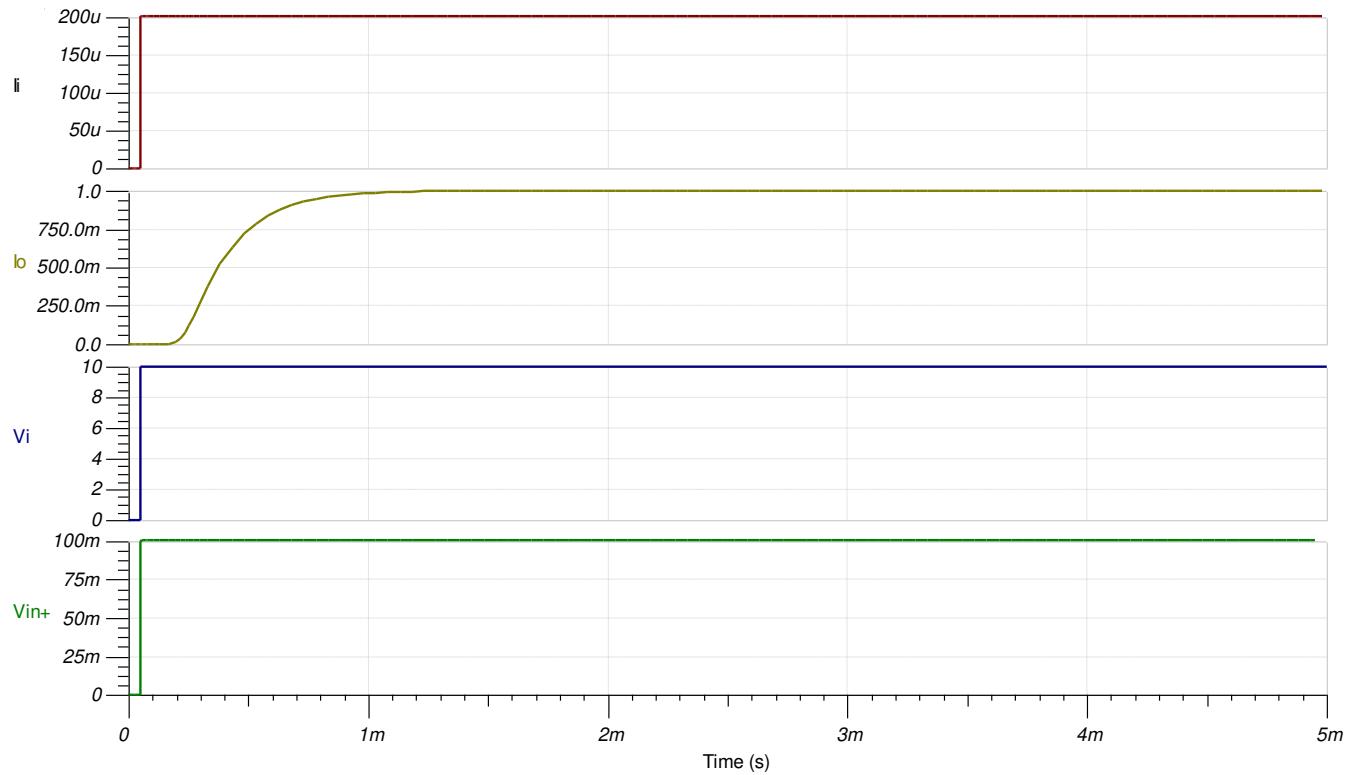
DC Simulation Results



AC Simulation Results



Transient Simulation Results



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.
2. SPICE Simulation File: [SBOMB58](#).
3. [TI Precision Labs](#)

Design Featured Op Amp

TLV9102	
V_{ss}	$\pm 1.35V$ to $\pm 8V$, $2.7V$ to $16V$
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	120 μA
I_b	10pA
UGBW	1.1MHz
SR	4.5V/ μs
#Channels	1, 2, 4
www.ti.com/product/TLV9102	

Design Alternate Op Amp

TLV9152	
V_{ss}	$\pm 1.35V$ to $\pm 8V$, $2.7V$ to $16V$
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	125 μV
I_q	560 μA
I_b	10pA
UGBW	4.5MHz
SR	20V/ μs
#Channels	1, 2, 4
www.ti.com/product/TLV9152	

Voltage-to-current (V-I) converter circuit with MOSFET



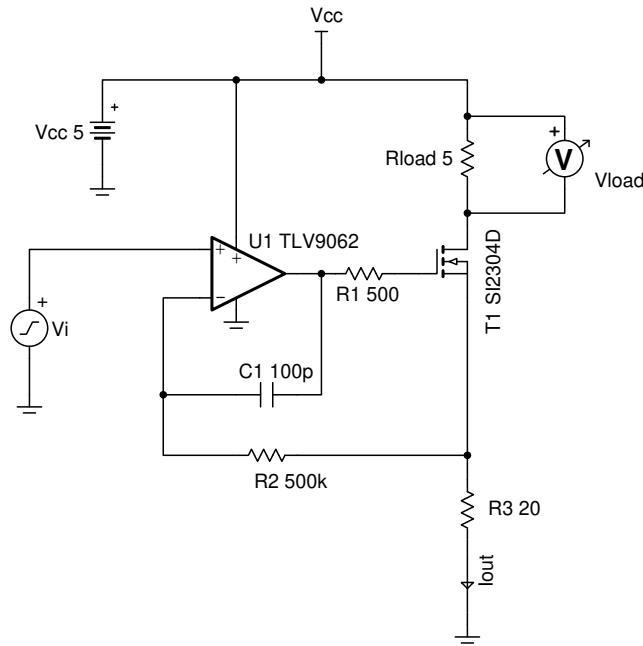
Amplifiers

Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	I_{oMin}	I_{oMax}	V_{cc}	V_{ee}
0V	2V	0mA	100mA	5V	0V

Design Description

This single-supply, low-side, V-I converter delivers a well-regulated current to a load which can be connected to a voltage greater than the op-amp supply voltage. The circuit accepts an input voltage between 0V and 2V and converts it to a current between 0mA and 100mA. The current is accurately regulated by feeding back the voltage drop across a low-side current-sense resistor, R_3 , to the inverting input of the op amp.



Design Notes

1. A device with a rail-to-rail input (RRI) or common-mode voltage that extends to GND is required.
2. R_1 helps isolate the amplifier from the capacitive load of the MOSFET gate.
3. Feedback components R_2 and C_1 provide compensation to ensure stability during input or load transients, which also helps reduce noise. R_2 provides a DC feedback path directly at the current setting resistor (R_3) and C_1 provides a high-frequency feedback path that bypasses the MOSFET.
4. The input bias current will flow through R_2 , which will cause a DC error. Therefore, ensure that this error is minimal compared to the offset voltage of the op amp.
5. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions provided in the op amp data sheet.

Design Steps

1. Determine the transfer function.

$$I_o = \frac{V_i}{R_3}$$

2. Calculate the sense resistor, R_3 .

$$R_3 = \frac{V_{iMax} - V_{iMin}}{I_{oMax} - I_{oMin}} = \frac{2V - 0V}{100mA - 0mA} = 20\Omega$$

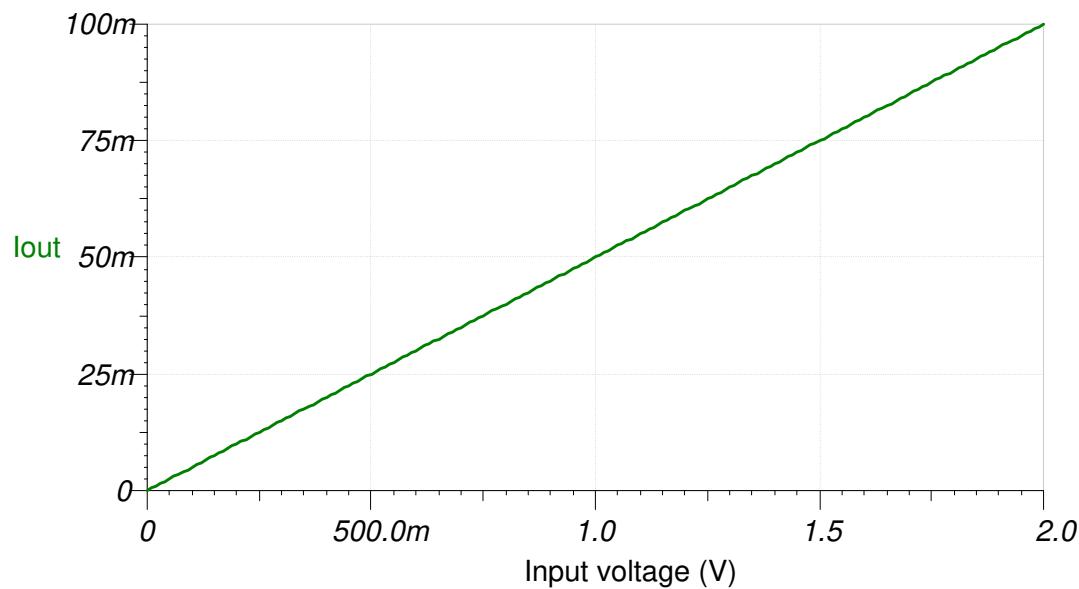
3. Calculate the maximum power dissipated into the sense resistor, R_3 , to ensure the resistor power ratings are not exceeded.

$$P_{R_3} = \frac{V_{iMax}^2}{R_3} = \frac{2V^2}{20\Omega} = 0.2W$$

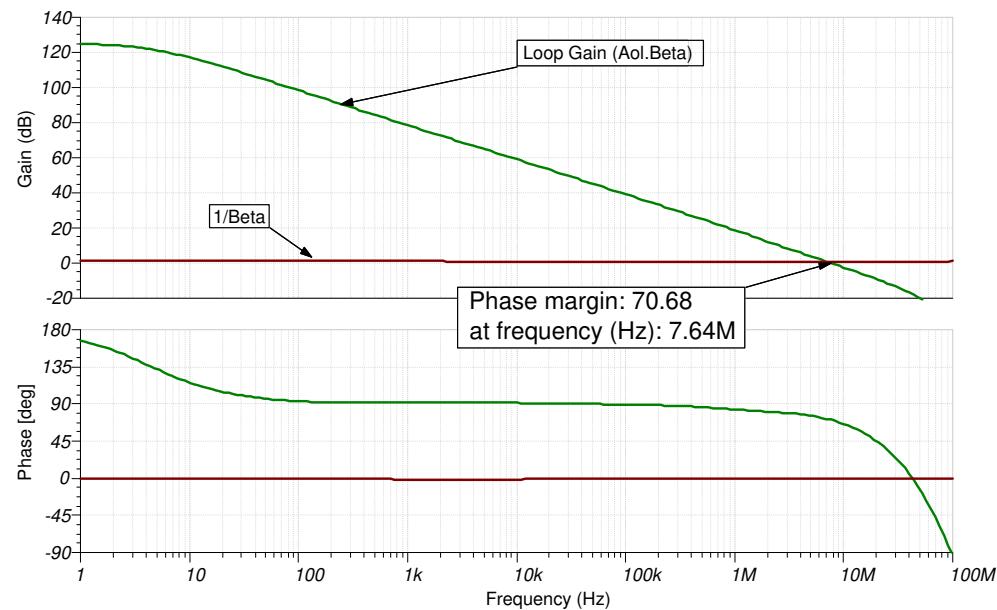
4. See the [Design References](#) section, [2] for the design procedure on how to properly size the compensation components, R_1 , R_2 , and C_1 .

Design Simulations

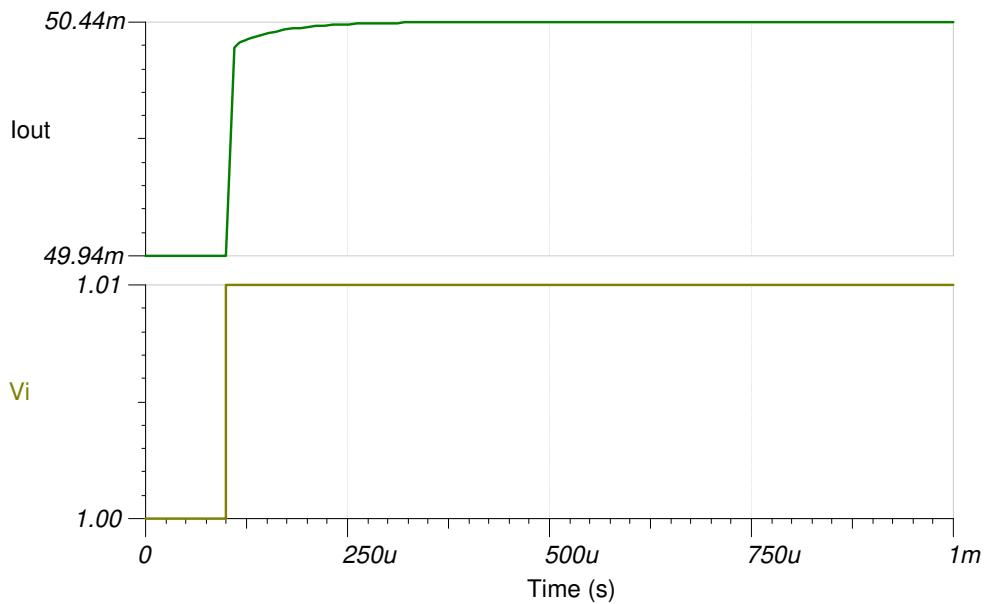
DC Simulation Results



Loop Stability Simulation Results

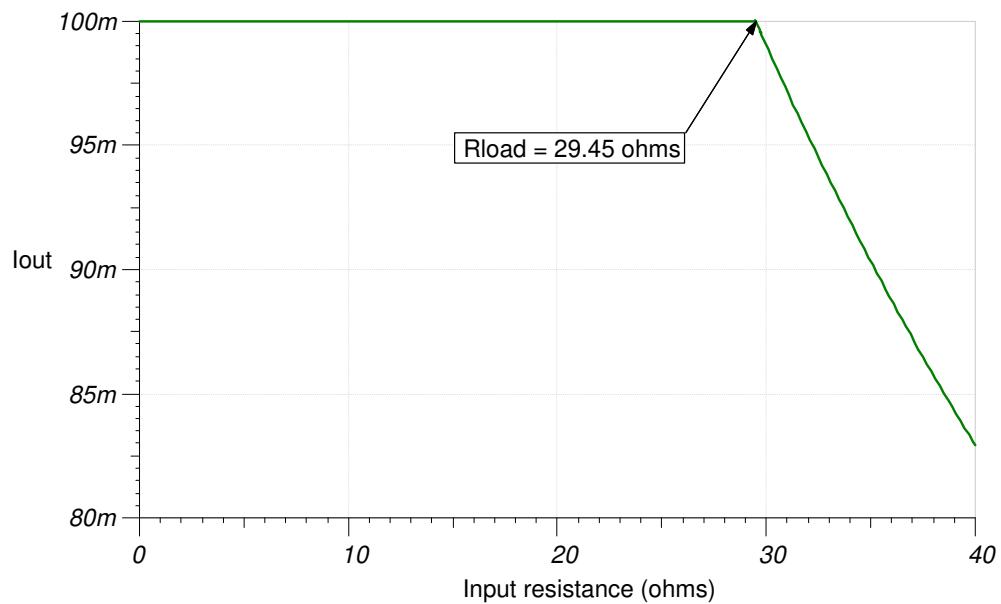


Step Response



Compliance Voltage

Set output to full-scale (100 mA) and test the maximum load resistance.



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.
2. [TI Precision Labs](#)

Design Featured Op Amp

TLV9062	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	($V_{cc} + 60\text{mV}$) to ($V_{ee} - 60\text{mV}$) at $R_L = 2\text{k}\Omega$
V_{os}	1.6mV
I_q	0.538mA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/ μs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

	TLV9042	OPA2182
V_{ss}	1.2V to 5.5V	4.5V to 36V
V_{inCM}	Rail-to-rail	($V_{ee} - 0.1\text{V}$) to ($V_{cc} - 2.5\text{V}$)
V_{out}	Rail-to-rail	Rail-to-rail
V_{os}	$\pm 0.6\text{mV}$	$\pm 0.45\mu\text{V}$
I_q	0.01mA	0.85mA
I_b	$\pm 1\text{pA}$	$\pm 50\text{pA}$
UGBW	350kHz	5MHz
SR	0.2V/ μs	10V/ μs
#Channels	1,2,4	2
	www.ti.com/product/TLV9042	www.ti.com/product/OPA2182

Analog Engineer's Circuit Amplifiers
“Improved” Howland current pump circuit

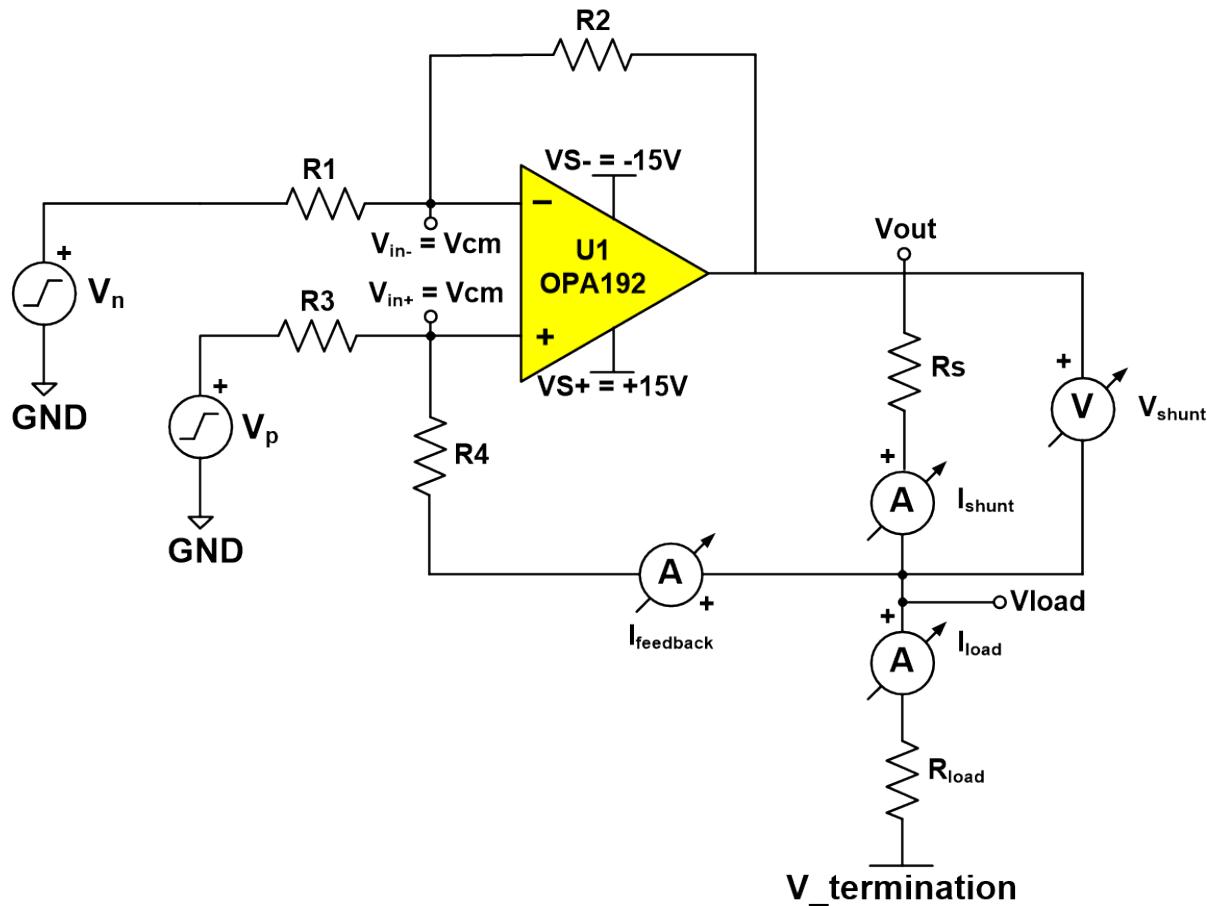


Design Goals

Input V_{in} ($V_p - V_n$)		Output		Supply		
V_{inMin}	V_{inMax}	I_{Min}	I_{Max}	$VS+$	$VS-$	V_{ref}
-5V	5V	-25mA	25mA	15V	-15V	0V

Design Description

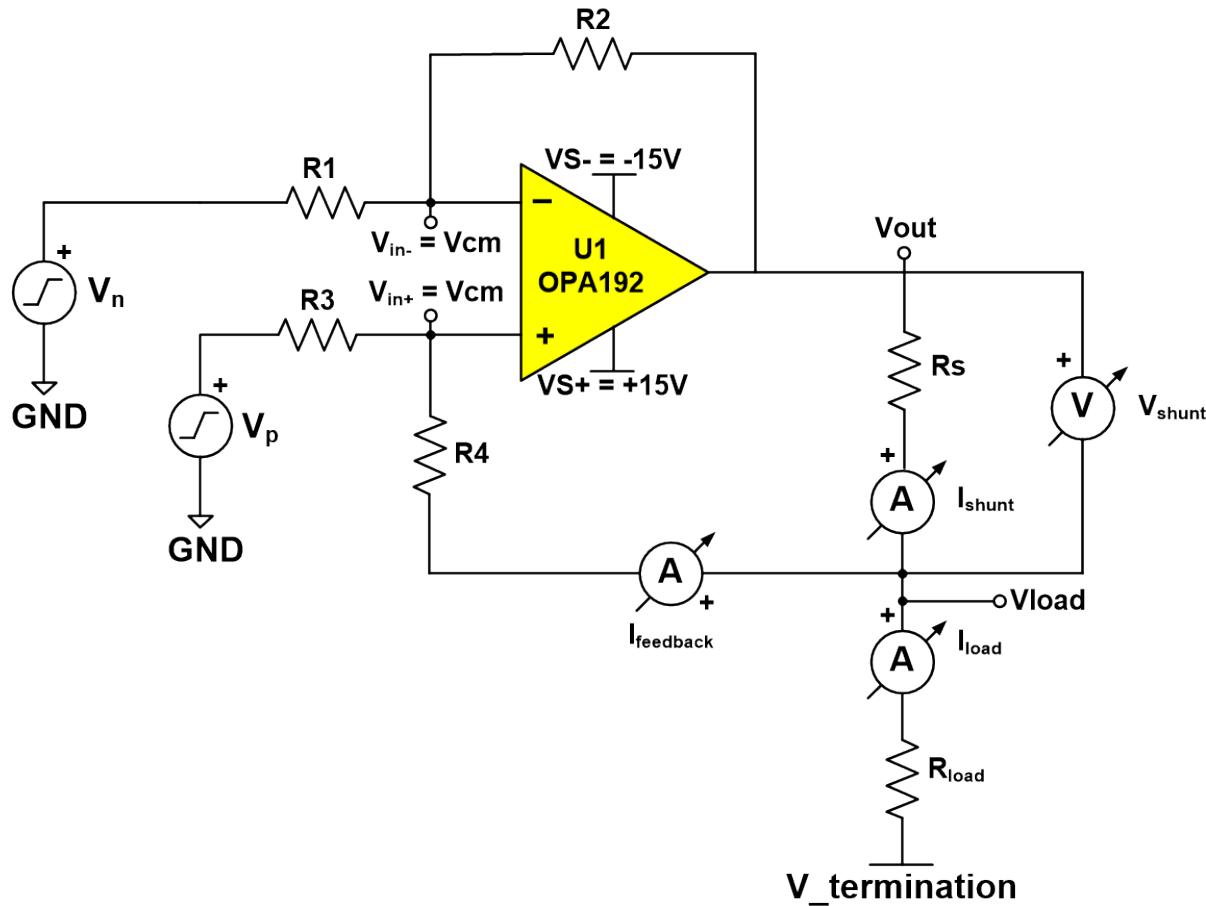
The “Improved” Howland current pump is a circuit that uses a difference amplifier to impose a voltage across a shunt resistor (R_s), creating a voltage-controlled bipolar (source or sink) current source capable of driving a wide range of load resistance. See the [AN-1515 A Comprehensive Study of the Howland Current Pump Application Report](#) for more information on the functionality of the “Improved” Howland current pump.



Design Notes

1. Ensure common-mode voltages at the inputs (V_{cm} nodes) of the op amp are within the V_{cm} range listed under Electrical Characteristics in the data sheet of the op amp.
2. Refer to the typical "Output Voltage Swing vs. Output Current" graphs in the data sheet of the op amp to account for output swing from rails (V_{out} node).
3. Resistor mismatch will contribute gain error and degrade CMRR of the circuit.
4. Error in final results can be expected due to $I_{feedback}$ current. Placing high-value resistors will limit the effect of this current, but will add thermal noise to the circuit. Possible bandwidth limitations and stability issues caused by large resistances and parasitic capacitances in the circuit also become more prevalent.
5. In an ideal "Improved" Howland current pump, resistor R4 is usually set equal to R2-Rs, which slightly alters the feedback network but results in the expected I_{load} value. Accuracy of these resistors will limit the effectiveness of the technique at reducing errors.
6. Special precautions should be taken when driving reactive loads.
7. A typical design procedure first calculates the gain for a known output current and shunt resistor; then sets R1 and scales R2 through R4 accordingly. This can be an iterative process.

Design Steps



- Calculating gain (G) for a given I_{load} and shunt resistor:

$$G(V / V) = \frac{I_{load} \times R_s}{V_p - V_n}$$

$$G(V / V) = \frac{R_2}{R_1}, \quad \frac{R_2}{R_1} = \frac{R_4 + R_s}{R_3}$$

- Ensure V_{out} is within the voltage output swing from rails (V_{out_Min} , V_{out_Max}) of the op amp at a specific output current specified in the data sheet of the op amp:

$$V_{out_Min} < V_{out} < V_{out_Max}$$

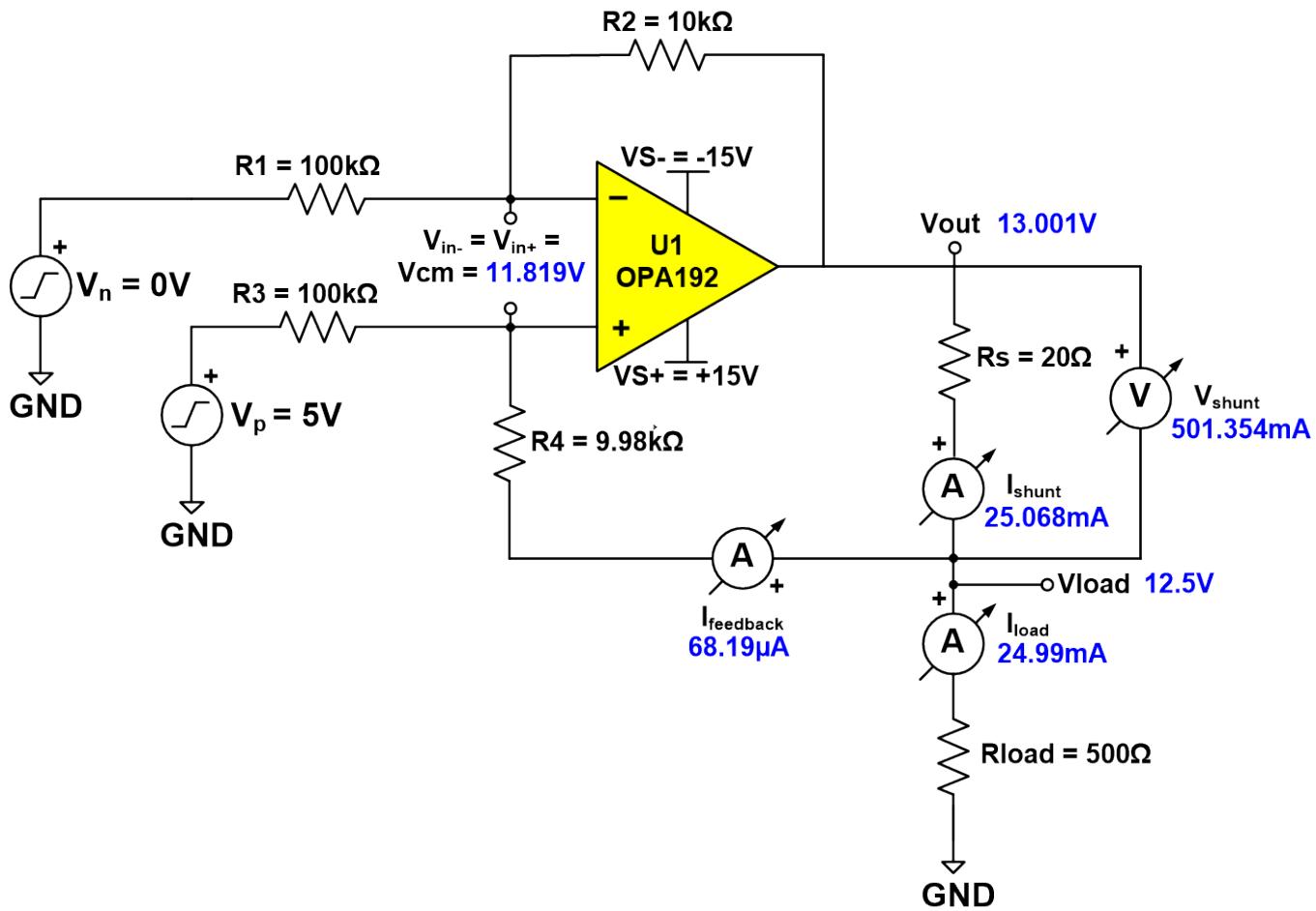
$$U1_V_{out} = V_{termination} + (I_{load} \times R_{load}) + V_{shunt}$$

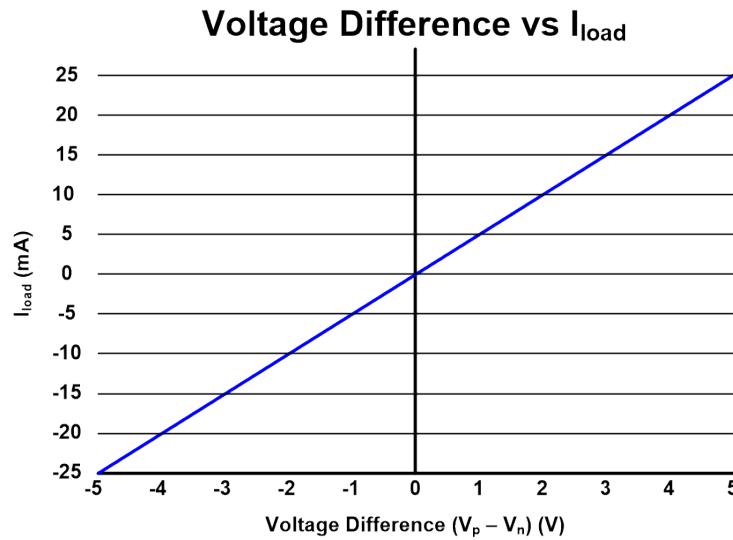
Design Simulations

A design goal of $\pm 25\text{mA}$ of output current from an input voltage difference of $\pm 5\text{V}$ and a $500\text{-}\Omega$ load results in a V_{load} value of $\pm 12.5\text{V}$ assuming a $V_{\text{termination}}$ voltage of 0V . The remaining ± 2.5 volts must accommodate the selected output swing-to-rail of the op amp as well as the maximum voltage across the shunt. For these reasons, a $20\text{-}\Omega$ shunt resistor and a gain of $1/10$ (V/V) was chosen.

A DC input voltage difference sweep is simulated with a fixed V_n input of 0V and the V_p input swept from -5V to 5V . As the following image shows, the input common-mode range, output swing-to-rail, and output current are within the specifications of the selected op amp. The configuration and results are seen in the following images.

DC Simulation Results





Design References

See the [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the [AN-1515 A Comprehensive Study of the Howland Current Pump Application Report](#) for more information on the functionality of the "Improved" Howland current pump resource.

The TI E2E support forum on [Difference Amplifiers](#) contains information on the importance of matching difference amplifier resistors.

Design Featured Op Amp

OPA192	
V_{ss}	4.5V–36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5µV
I_q	1mA
I_b	5pA
UGBW	10MHz
SR	20V/µs
#Channels	1
www.ti.com/product/OPA192	

Design Alternate Op Amp

OPA990	
V_{ss}	2.7V–40V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	130µA
I_b	10pA
UGBW	1.1MHz
SR	4.5V/µs
#Channels	1
www.ti.com/product/OPA990	

Voltage-to-current (V-I) converter circuit with a Darlington transistor



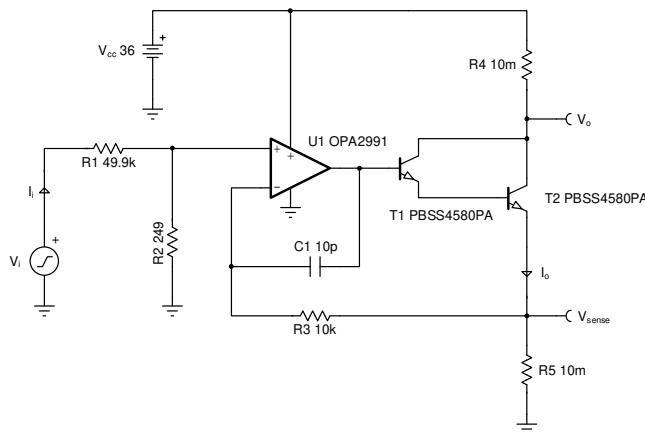
Amplifiers

Design Goals

Input			Output			Supply	
V _{iMin}	V _{iMax}	I _{iMax}	I _{oMin}	I _{oMax}	P _{R5Max}	V _{cc}	V _{ee}
0V	10V	200µA	0A	5A	0.25W	36V	0V

Design Description

This high-side voltage-to-current (V-I) converter delivers a well-regulated current to a load, R₄. The circuit accepts an input voltage from 0V to 10V and converts it to an output current from 0A to 5A. The current is regulated by feeding the voltage across a low-side, current-sense resistor back to the op amp. The output Darlington pair allows for higher current gain than when using a single, discrete transistor.



Design Notes

1. A resistor divider, formed by R₁ and R₂, is implemented at the input to limit the full-scale voltage at the non-inverting terminal of the amplifier and the output sense resistor (R₅).
2. The high current gain of the Darlington pair reduces the demand on the output current of the op amp.
3. Smaller values of R₄ and R₅ lead to an increased load compliance voltage and a reduction in power dissipated in the full-scale, output state.
4. Feedback components R₃ and C₁ provide frequency compensation to ensure the stability of the circuit during transients. They also help reduce noise. R₃ provides a DC feedback path directly at the current setting resistor, R₅, and C₁ provides a high-frequency feedback path that bypasses the NPN pair.
5. The input bias current will flow through R₃, which will cause a DC error. Therefore, ensure that this error is minimal compared to the offset voltage of the op amp.
6. Select an op amp whose linear output voltage swing includes at least $2 \times V_{be} + V_{sense}$. The output voltage of the op amp will be greater than the voltage at the sense resistor by approximately double the base-to-emitter voltage, V_{be}.
7. Use the op amp in its linear operating region, specified under the A_{OL} test conditions of the data sheet.
8. If needed, an isolation resistor may be placed between the high-frequency feedback path and the base of T1 for stability.

Design Steps

The transfer function of this circuit is provided in the following steps:

$$I_o = V_i \times \frac{R_2}{R_5 \times (R_1 + R_2)}$$

1. Using the specifications for the maximum output power dissipation and the maximum output current, determine the maximum value of V_{sense} .

$$V_{R5\text{Max}} = V_{\text{senseMax}} = \frac{P_{R5\text{Max}}}{I_{o\text{Max}}} = \frac{0.25 \text{ W}}{5\text{A}} = 50\text{mV}$$

2. Calculate the sense resistance, R_5 .

$$R_5 = \frac{V_{\text{senseMax}}}{I_{o\text{Max}}} = \frac{50\text{mV}}{5\text{A}} = 10\text{m}\Omega$$

3. Select values for R_1 and R_2 based on the maximum allowable input current, $I_{i\text{Max}}$, and the desired V_{senseMax} voltage.

$$R_1 = \frac{V_{\text{senseMax}}}{I_{i\text{Max}}} = \frac{50\text{mV}}{200\mu\text{A}} = 250\Omega \approx 249\Omega(\text{Standard Value})$$

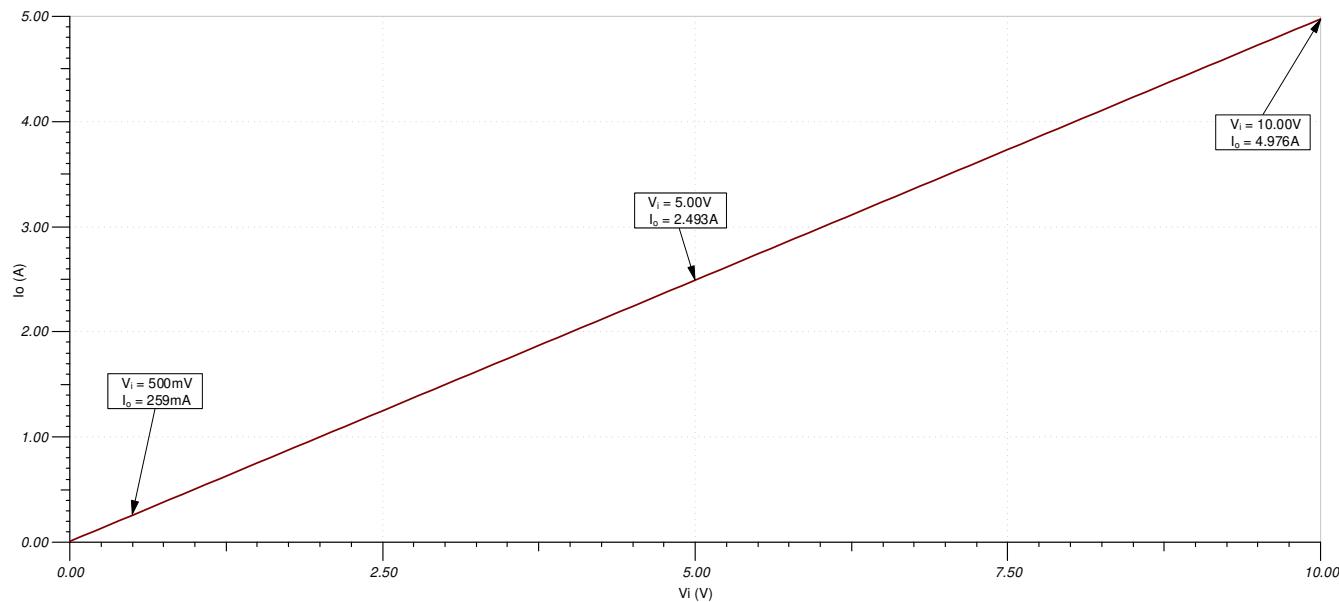
$$V_{\text{senseMax}} = V_{i\text{Max}} \times \left(\frac{R_2}{R_1 + R_2} \right)$$

$$R_2 = 49.6\text{k}\Omega \approx 49.9\text{k}\Omega \text{ (Standard Value)}$$

4. See the [Design References](#) section [2] for the design procedure on how to properly size the compensation components, R_3 and C_1 .

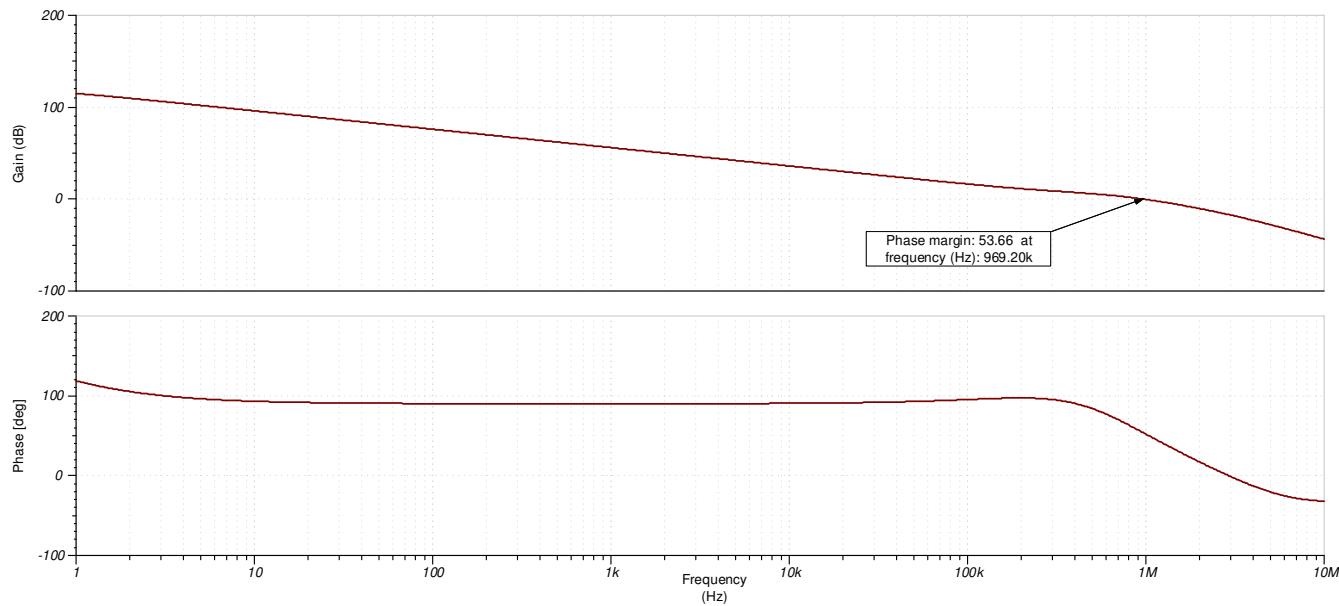
Design Simulations

DC Simulation Results

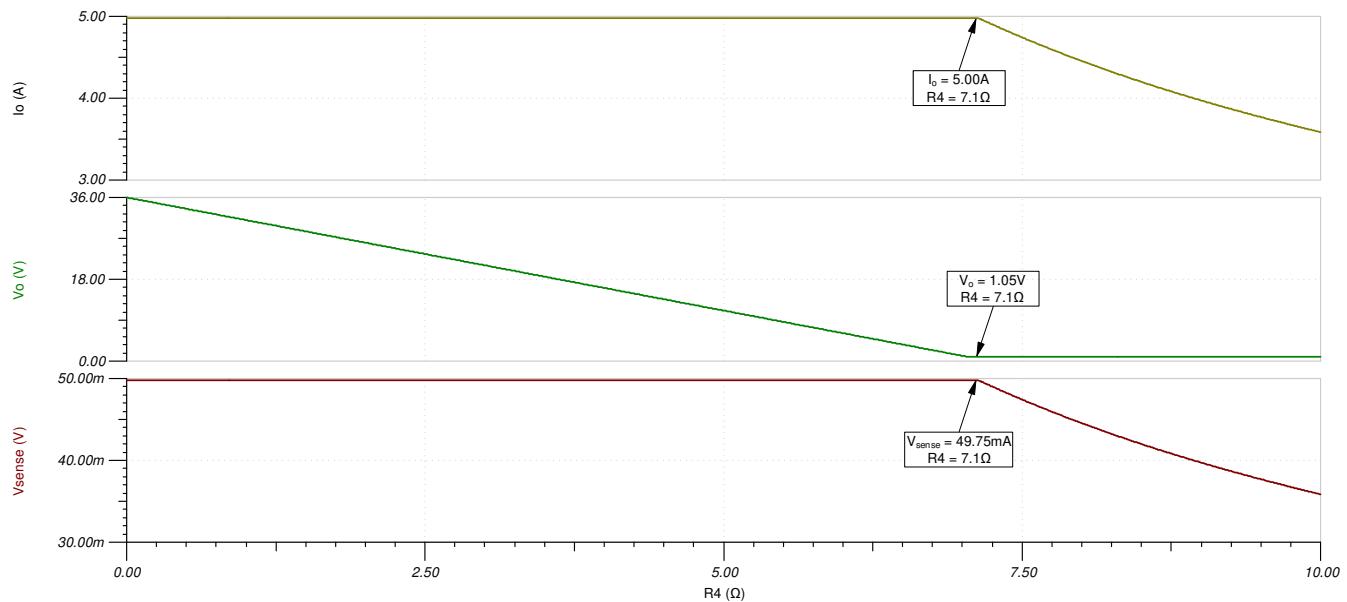


Loop Stability Simulation Results

Loop gain phase is 53 degrees.



Compliance Voltage Simulation Results



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.
2. [TI Precision Labs](#)

Design Featured Op Amp

OPA2991	
V_{ss}	2.7V to 40V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	125µV
I_q	560µA
I_b	10pA
UGBW	4.5MHz
SR	21V/µs
#Channels	1, 2, 4
www.ti.com/product/opa2991	

Design Alternate Op Amp

OPA197	
V_{ss}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	25µV
I_q	1mA
I_b	5pA
UGBW	10MHz
SR	20V/µs
#Channels	1, 2, 4
www.ti.com/product/opa197	

Analog Engineer's Circuit Amplifiers

"Improved" Howland current pump with buffer circuit

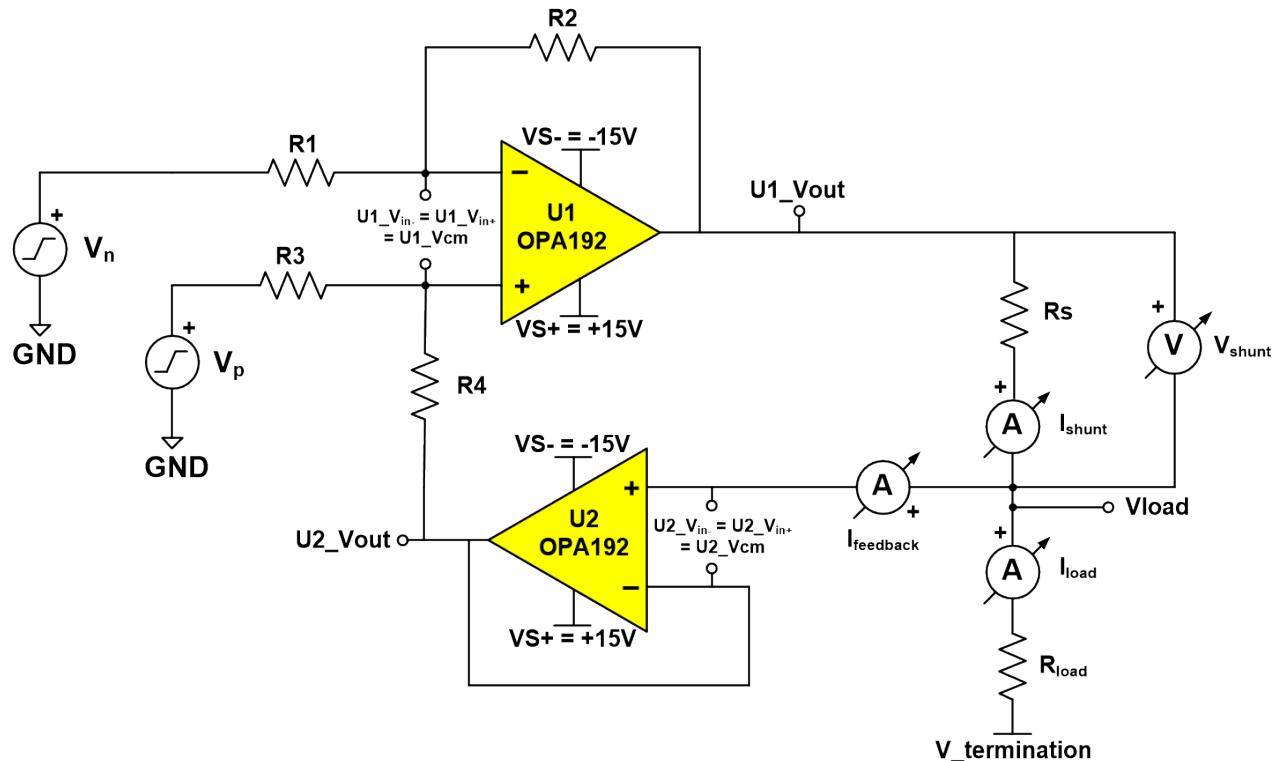


Design Goals

Input V_{in} ($V_p - V_n$)		Output		Supply		
V_{inMin}	V_{inMax}	I_{Min}	I_{Max}	$VS+$	$VS-$	V_{ref}
-5V	5V	-25mA	25mA	15V	-15V	0V

Design Description

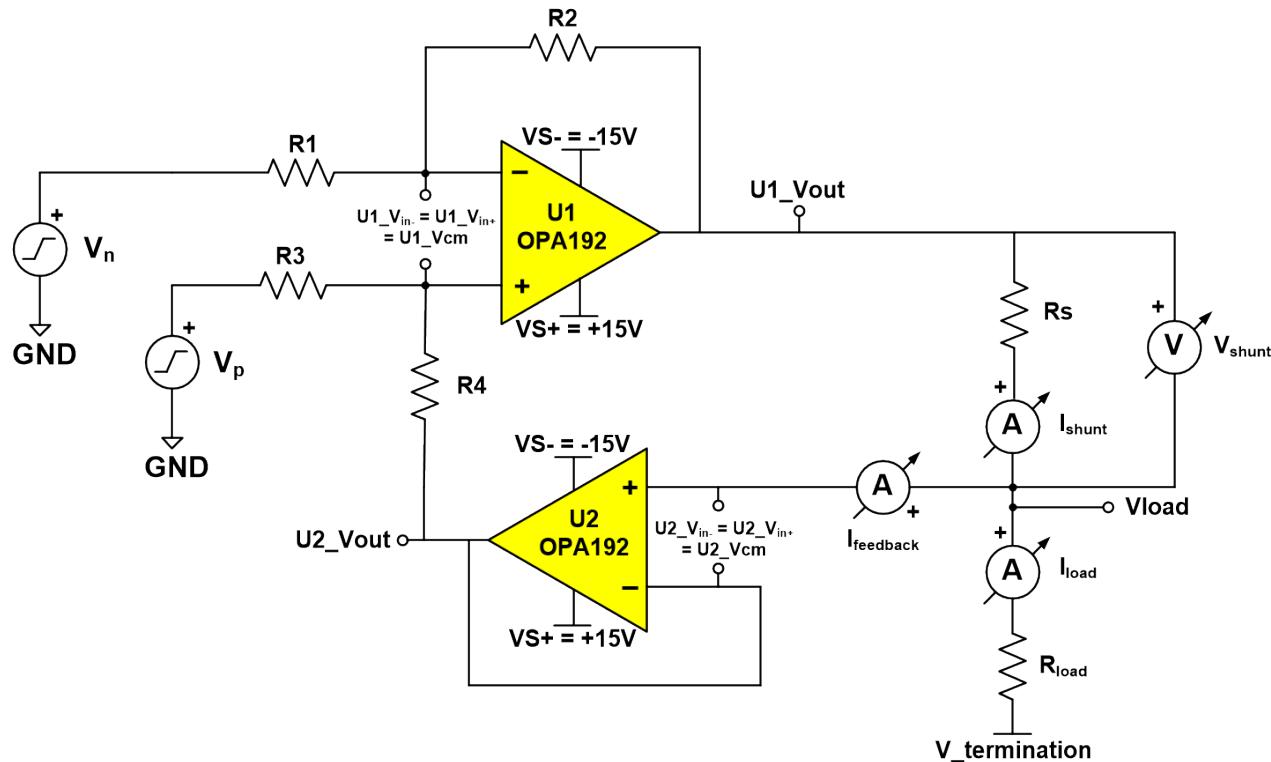
The "Improved" Howland current pump is a circuit that uses a difference amplifier to impose a voltage across a shunt resistor (R_s), creating a voltage-controlled bipolar (source or sink) current source capable of driving a wide range of load resistance. See the [AN-1515 A Comprehensive Study of the Howland Current Pump Application Report](#) for more information on the functionality of the "Improved" Howland current pump.



Design Notes

1. Ensure common-mode voltages at the inputs (V_{cm} nodes) of both op amps are within their V_{cm} range listed under Electrical Characteristics in the data sheet of the op amp.
2. Refer to the typical *Output Voltage Swing vs. Output Current* graphs in the data sheet to account for output swing from rails (V_{out} nodes) for both op amps.
3. Resistor mismatch will contribute gain error and degrade CMRR of the circuit.
4. The buffer offers improved output impedance of the current source nearly eliminating $I_{feedback}$ current. This allows the use of smaller resistor values for R1 through R4, reducing thermal noise. Possible bandwidth limitations and stability issues caused by large resistances and parasitic capacitances in the circuit are also reduced.
5. Special precautions should be taken when driving reactive loads.
6. A typical design procedure first calculates the gain for a known output current and shunt resistor; then sets R1 and scales R2 through R4 accordingly. This can be an iterative process.
7. The figures use two [OPA192](#) op amps, but in practice a single chip [OPA2192](#) can be used.

Design Steps



1. Calculating gain (G) for a given I_{load} and shunt resistor:

$$G(V / V) = \frac{I_{load} \times R_S}{V_p - V_n}$$

$$G(V / V) = \frac{R_2}{R_1}, \quad (R_1 = R_3, R_2 = R_4)$$

2. Ensure V_{out} for both op amps are within their voltage output swing from rails (V_{out_Min} , V_{out_Max}) at a specific output current specified in the data sheet. The following formula can be used to calculate $U1_V_{out}$ for U1 OPA192. $U2_V_{out}$ for U2 OPA192 will be V_{load} .

$$V_{out_Min} < V_{out} < V_{out_Max}$$

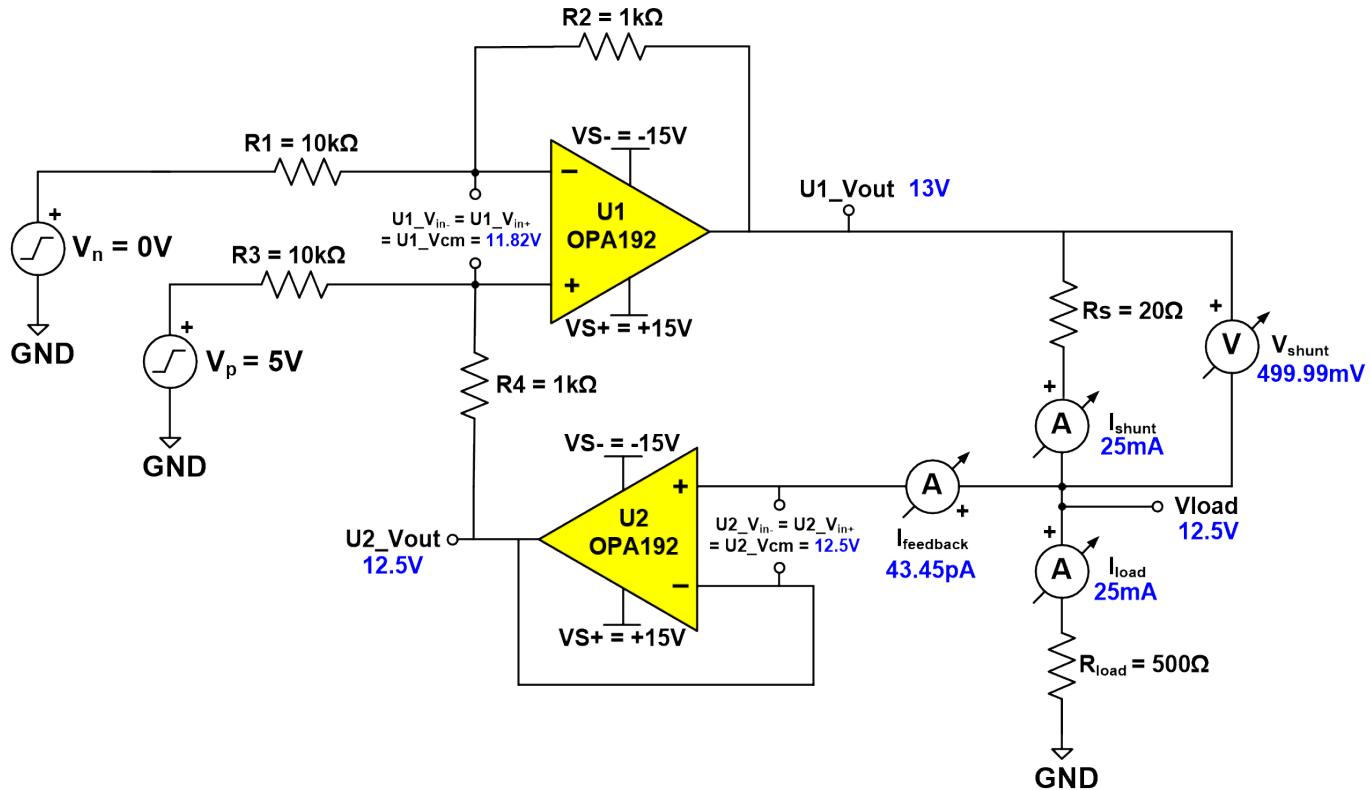
$$U1_V_{out} = V_{termination} + (I_{load} \times R_{load}) + V_{shunt}$$

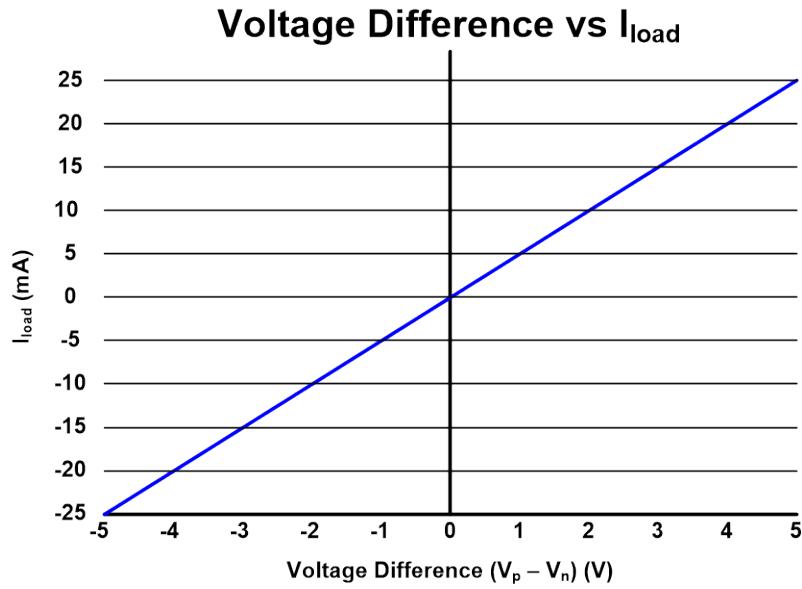
Design Simulations

A design goal of $\pm 25\text{mA}$ of output current from an input voltage difference of $\pm 5\text{V}$ and a $500\text{-}\Omega$ load results in a V_{load} value of $\pm 12.5\text{V}$, assuming a $V_{\text{termination}}$ voltage of 0V . The remaining ± 2.5 volts must accommodate the output swing-to-rail of the selected op amp as well as the maximum voltage across the shunt. For these reasons a $20\text{-}\Omega$ shunt resistor and a gain of $1/10$ (V/V) was chosen. This V_{load} value is also within the voltage compliance range of the buffer.

A DC input voltage difference sweep is simulated with a fixed V_n input of 0V and the V_p input swept from -5V to 5V . As the following image shows, the input common-mode range, output swing-to-rail, and output current are within the specifications of the selected op amps. The configuration and results follow.

DC Simulation Results





Design References

See the [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the [AN-1515 A Comprehensive Study of the Howland Current Pump Application Report](#) for more information on the functionality of the "Improved" Howland current pump resource.

The TI E2E support forum on [Difference Amplifiers](#) contains information on the importance of matching difference amplifier resistors.

Design Featured Op Amp

OPA2192	
V_{ss}	4.5V–36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 μ V
I_q	1mA
I_b	5pA
UGBW	10MHz
SR	20V/ μ s
#Channels	2
www.ti.com/product/OPA2192	

Design Alternate Op Amp

OPA2990	
V_{ss}	2.7V–40V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	120 μ A
I_b	10pA
UGBW	1.1MHz
SR	4.5V/ μ s
#Channels	2
www.ti.com/product/OPA2990	

Low-Level Voltage-to-Current Converter Circuit

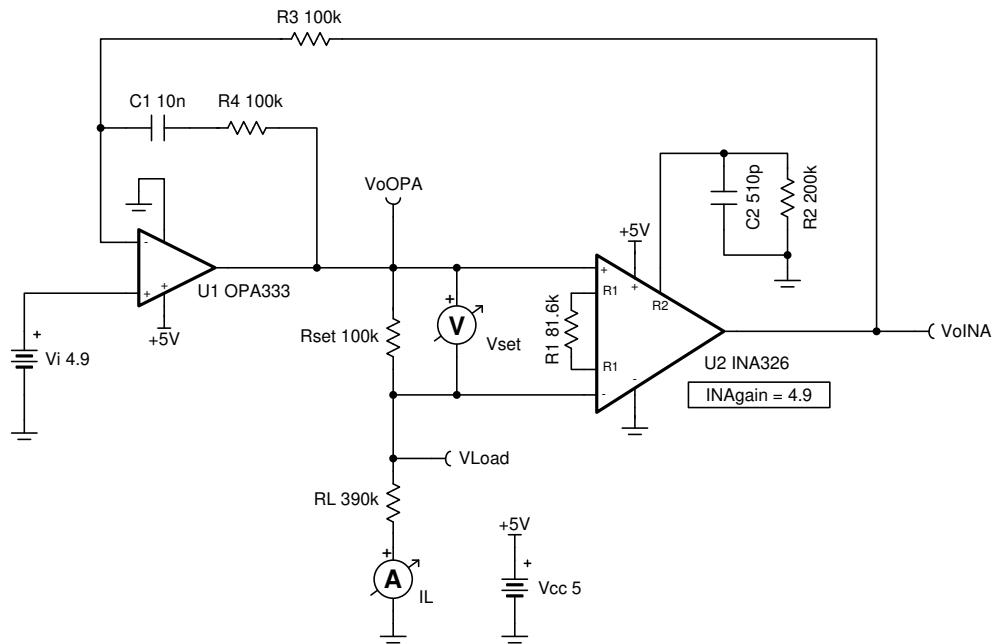


Design Goals

Input		Output		Supply		Load Resistance (R_L)	
V_{iMin}	V_{iMax}	I_{LMin}	I_{LMax}	V_{cc}	V_{ee}	R_{LMin}	R_{LMax}
0.49 V	4.9 V	1 μ A	10 μ A	5 V	0 V	0 Ω	390 k Ω

Design Description

This circuit delivers a precise low-level current, I_L , to a load, R_L . The design operates on a single 5 V supply and uses one precision low-drift op amp and one instrumentation amplifier. Simple modifications can change the range and accuracy of the voltage-to-current (V-I) converter.



Design Notes

1. Voltage compliance is dominated by op amp linear output swing (see data sheet A_{OL} test conditions) and instrumentation amplifier linear output swing. See the [Common-Mode Input Range Calculator for Instrumentation Amplifiers](#) for more information.
2. Voltage compliance, along with R_{LMin} , R_{LMax} , and R_{set} bound the I_L range.
3. Check op amp and instrumentation amplifier input common-mode voltage range.
4. Stability analysis must be done to choose R_4 and C_1 for stable operation.
5. Loop stability analysis to select R_4 and C_1 will be different for each design. The compensation shown is only valid for the resistive load ranges used in this design. Other types of loads, op amps, or instrumentation amplifiers, or both will require different compensation. See the [Design References](#) section for more op amp stability resources.

Design Steps

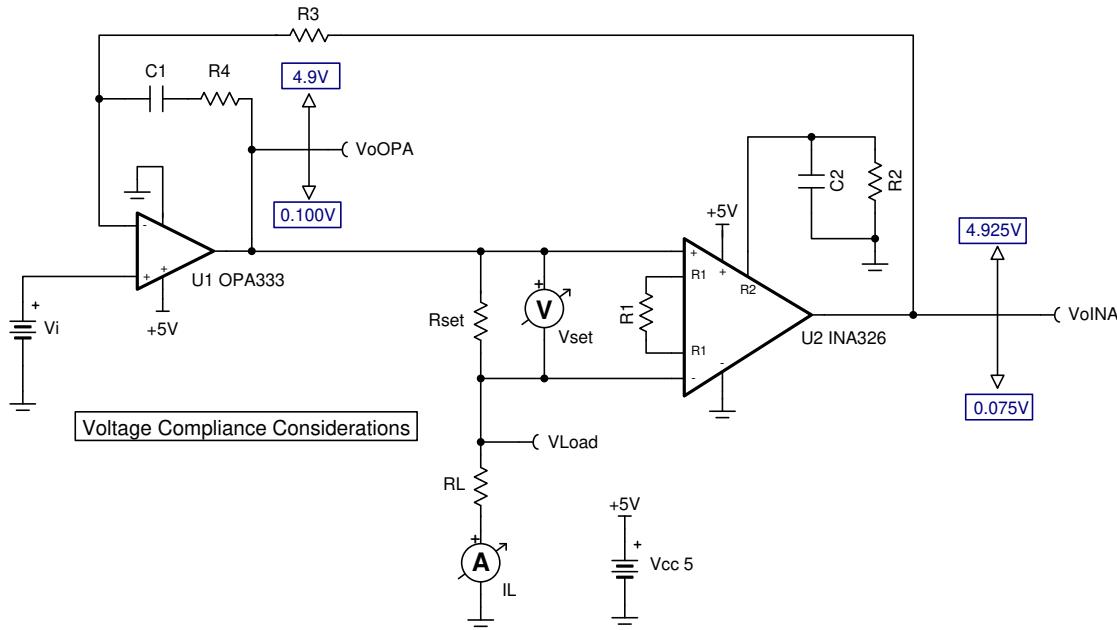
1. Select R_{set} and check I_{LMin} based on voltage compliance.

$$I_{LMax} = \frac{V_{oOPAMax}}{R_{set} + R_{LMax}}$$

$$10\mu A = \frac{4.9V}{R_{set} + 390k\Omega} \rightarrow R_{set} = 100k\Omega$$

$$I_{LMin} = \frac{V_{oOPAMin}}{R_{set} + R_{LMin}}$$

$$I_{LMin} = \frac{0.1V}{100k\Omega + 0\Omega} = 1\mu A$$



2. Compute instrumentation amplifier gain, G.

$$V_{setMin} = I_{LMin} \times R_{set} = 1\mu A \times 100k\Omega = 0.1V$$

$$V_{setMax} = I_{LMax} \times R_{set} = 10\mu A \times 100k\Omega = 1V$$

$$G = \frac{V_{iMax} - V_{iMin}}{V_{setMax} - V_{setMin}}$$

$$G = \frac{4.9V - 0.49V}{1V - 0.1V} = 4.9$$

3. Choose R_1 for INA326 instrumentation amplifier gain, G. Use data sheet recommended $R_2 = 200 k\Omega$ and $C_2 = 510 pF$.

$$G = 2 \times \left(\frac{R_2}{R_1} \right)$$

$$R_1 = \frac{2 \times R_2}{G}$$

$$R_1 = \left(\frac{2 \times 200k\Omega}{4.9} \right) = 81.6327k\Omega \approx 81.6k\Omega$$

4. The final transfer function of the circuit follows:

$$I_L = \frac{V_i}{G \times R_{\text{set}}}$$

$$I_L = \frac{V_i}{4.9 \times 100\text{k}\Omega} = \frac{V_i}{490\text{k}\Omega}$$

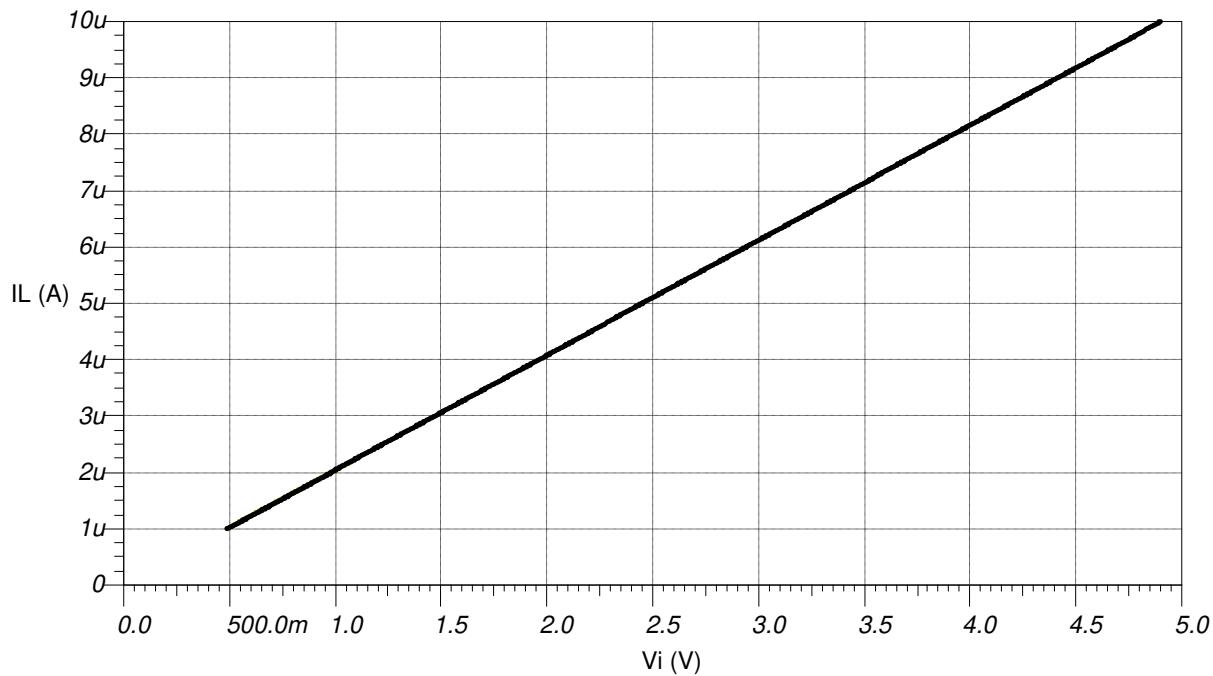
$$V_i = 0.49\text{V} \rightarrow I_L = 1\mu\text{A}$$

$$V_i = 4.9\text{V} \rightarrow I_L = 10\mu\text{A}$$

Design Simulations

DC Simulation Results

V_i	R_L	I_L	V_{oOPA}	V_{oOPA} Compliance	V_{oINA}	V_{oINA} Compliance
0.49 V	0 Ω	0.999627 μA	99.982723 mV	100 mV to 4.9 V	490.013346 mV	75 mV to 4.925 V
0.49 V	390 k Ω	0.999627 μA	489.837228 mV	100 mV to 4.9 V	490.013233 mV	75 mV to 4.925 V
4.9 V	0 Ω	9.996034 μA	999.623352 mV	100 mV to 4.9 V	4.900016 V	75 mV to 4.925 V
4.9 V	390 k Ω	9.996031 μA	4.898075 V	100 mV to 4.9 V	4.900015 V	75 mV to 4.925 V



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the TINA-TI™ circuit simulation file, [SBOMAT8](#).

See [TIPD107](#).

See [Solving Op Amp Stability Issues - E2E FAQ](#).

See [TI Precision Labs - Op Amps](#).

Design Featured Op Amp

OPA333	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	2 μ V
I_q	17 μ A/Ch
I_b	70 pA
UGBW	350 kHz
SR	0.16 V/ μ s
#Channels	1 and 2
OPA333	

Design Featured Instrumentation Amplifier

INA326	
V_{ss}	2.7 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	20 μ V
I_q	2.4 mA
I_b	0.2 nA
UGBW	1 kHz (set by 1 kHz filter)
SR	0.012 V/ μ s (set by 1 kHz filter)
#Channels	1
INA326	

Single-supply, 2nd-order, multiple feedback low-pass filter circuit

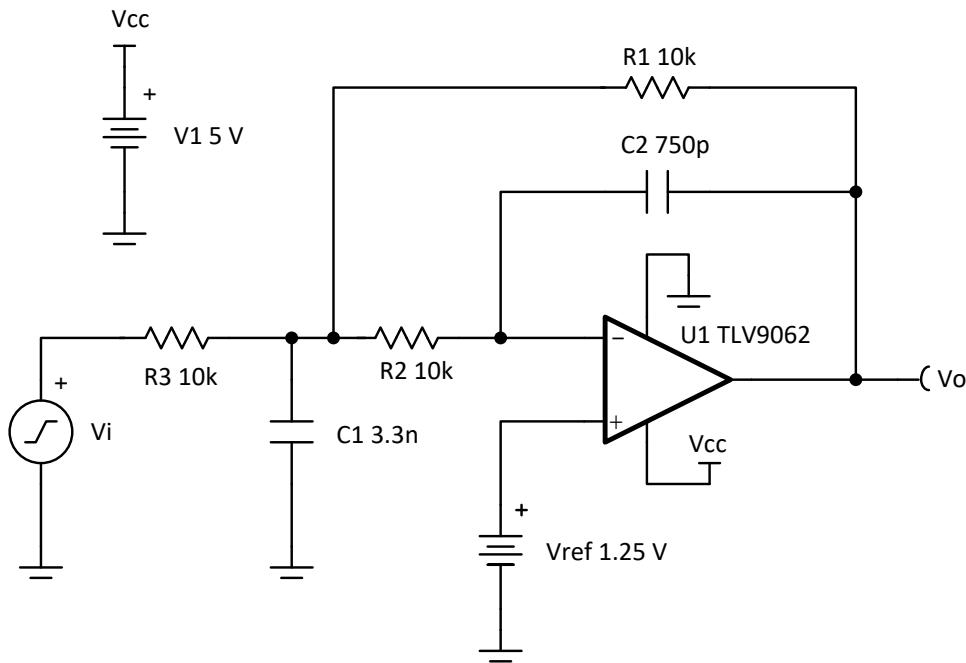


Amplifiers

Input		Output		Supply	
V _{iMin}	V _{iMax}	V _{oMin}	V _{oMax}	V _{cc}	V _{ee}
-2.45V	+2.45V	0.05V	4.95V	5V	0V
Gain		Cutoff Frequency (f _c)		V _{ref}	
-1V/V		10kHz		1.25V	

Design Description

The multiple-feedback (MFB) low-pass filter (LP filter) is a second-order active filter. V_{ref} provides a DC offset to accommodate for single-supply applications. This LP filter inverts the signal (Gain = -1V/V) for frequencies in the pass band. An MFB filter is preferable when the gain is high or when the Q-factor is large (for example, 3 or greater).



Design Notes

1. Select an op amp with sufficient input common-mode range and output voltage swing.
2. Add V_{ref} to bias the input signal to meet the input common-mode range and output voltage swing.
3. Select the capacitor values first since standard capacitor values are more coarsely subdivided than the resistor values. Use high-precision, low-drift capacitor values to avoid errors in f_c.
4. To minimize the amount of slew-induced distortion, select an op amp with sufficient slew rate (SR).

Design Steps

The first step in design is to find component values for the normalized cutoff frequency of 1 radian/second. In the second step the cutoff frequency is scaled to the desired cutoff frequency with scaled component values.

The transfer function for a second-order MFB low-pass filter is given by:

$$H(s) = \frac{\frac{1}{R_2 \times R_3 \times C_1 \times C_2}}{s^2 + s \times \frac{1}{C_1} \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right) + \frac{1}{R_1 \times R_2 \times C_1 \times C_2}}$$

$$H(s) = \frac{b_0}{s^2 + a_1 \times s + a_0}$$

$$\text{Here, } a_1 = \frac{1}{C_1} \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right), \quad a_0 = \frac{1}{R_1 \times R_2 \times C_1 \times C_2}$$

- Set normalized values of R_1 and R_2 (R_{1n} and R_{2n}) and calculate normalized values of C_1 and C_2 (C_{1n} and C_{2n}) by setting w_c to 1 radian/sec (or $f_c = 1 / (2 \times \pi)$ Hz). For a 2nd-order Butterworth filter, (see the *Butterworth Filter Table* in the [Active Low-Pass Filter Design Application Report](#)).

$$\omega_c = 1 \frac{\text{radian}}{\text{second}} \rightarrow a_0 = 1, a_1 = \sqrt{2}, \text{ let } R_{1n} = R_{2n} = R_{3n} = 1$$

$$\text{Then } C_{1n} \times C_{2n} = 1 \text{ or } C_{2n} = \frac{1}{C_{1n}}, \quad a_1 = \frac{3}{C_{1n}} = \sqrt{2}$$

$$\therefore C_{1n} = \frac{3}{\sqrt{2}} = 2.1213 \text{ F}, \quad C_{2n} = \frac{1}{C_{1n}} = 0.4714 \text{ F}$$

- Scale the component values and cutoff frequency. The resistor values are very small and capacitors values are unrealistic, hence these must be scaled. The cutoff frequency is scaled from 1 radian/second to w_0 . If m is assumed to be the scaling factor, increase the resistors by m times, then the capacitor values have to decrease by $1/m$ times to keep the same cutoff frequency of 1 radian/second. If the cutoff frequency is scaled to be w_0 , then the capacitor values have to be decreased by $1/w_0$. The component values for the design goals are calculated in steps 3 and 4.

$$R_1 = R_{1n} \times m, \quad R_2 = R_{2n} \times m, \quad R_3 = R_{3n} \times m$$

$$C_1 = \frac{C_{1n}}{m \times \omega_0} = \frac{2.1213}{m \times \omega_0} \text{ F}$$

$$C_2 = \frac{C_{2n}}{m \times \omega_0} = \frac{0.4714}{m \times \omega_0} \text{ F}$$

- Set R_1 , R_2 , and R_3 to $10k\Omega$.

$$R_1 = R_{1n} \times m = 10k\Omega, \quad R_2 = R_{2n} \times m = 10k\Omega, \quad R_3 = R_{3n} \times m = 10k\Omega$$

Therefore, $m = 10000$

4. Calculate C_1 and C_2 based on m and w_0 .

$$C_1 = \frac{2.1213}{m \times \omega_0} F = \frac{2.1213}{10k \times 2 \times \pi \times 10\text{kHz}} = 3.376\text{nF} \approx 3.3\text{nF} \text{ (Standard Value)}$$

$$C_2 = \frac{0.4714}{m \times \omega_0} F = \frac{0.4714}{10k \times 2 \times \pi \times 10\text{kHz}} = 0.75\text{nF} \approx 0.75\text{nF} \text{ (Standard Value)}$$

5. Calculate the minimum required GBW and SR for f_c . Be sure to use the noise gain for GBW calculations. Do not use the signal gain of -1V/V .

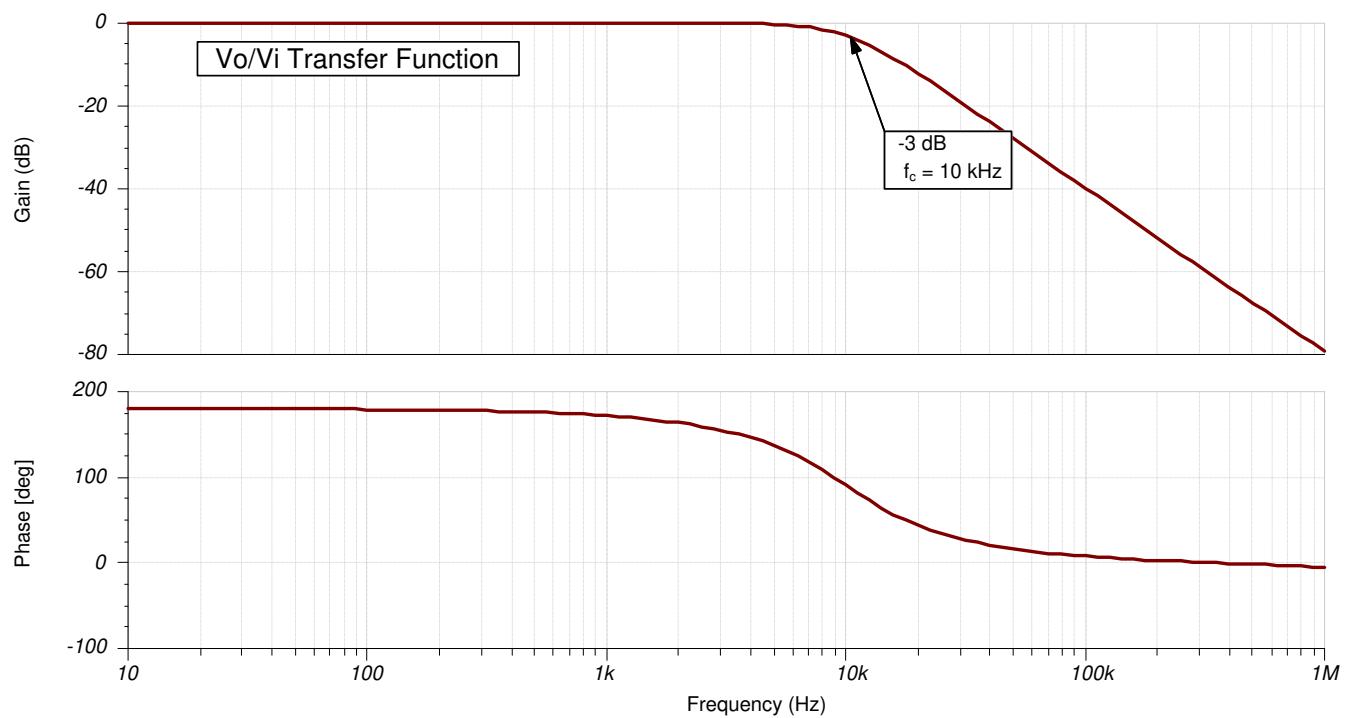
$$\text{GBW} = 100 \times \text{Noise Gain} \times f_c = 100 \times 2 \times 10\text{kHz} = 2\text{MHz}$$

$$\text{SR} = 2 \times \pi \times f_c \times V_{i\text{Max}} = 2 \times \pi \times 10\text{kHz} \times 2.45\text{V} = 0.154 \frac{\text{V}}{\mu\text{s}}$$

The TLV9062 device has GBW of 10MHz and SR of 6.5 V/ μs , so the requirements are met.

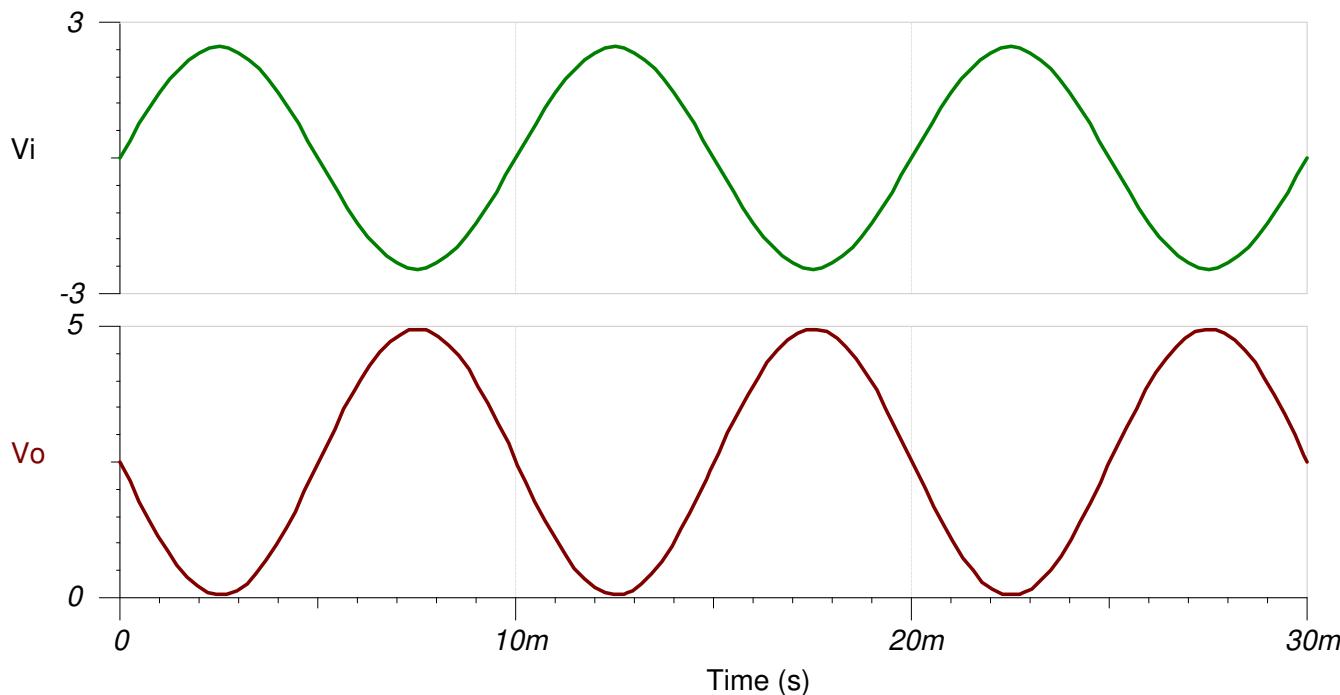
Design Simulations

AC Simulation Results

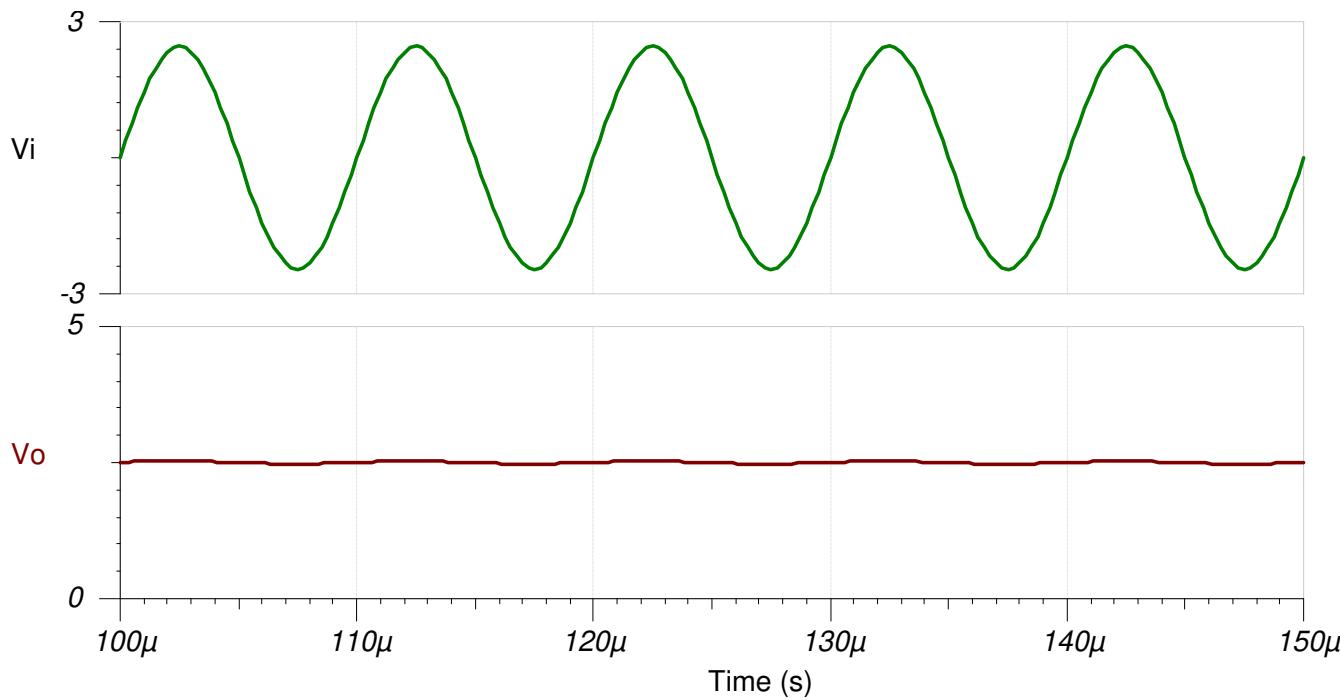


Transient Simulation Results

The following image shows the filter output in response to a 5-V_{pp}, 100-Hz input signal (gain = -1V/V).



The following image shows the filter output in response to a 5-V_{pp}, 10-kHz input signal (gain = -0.01V/V).



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.
2. SPICE Simulation File [SBOC597](#)
3. [TI Precision Labs](#).
4. [Active Low-Pass Filter Design Application Report](#)

Design Featured Op Amp

TLV9062	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-Rail
V_{out}	Rail-to-Rail
V_{os}	0.3mV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

	TLV316	OPA325
V_{ss}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-Rail	Rail-to-Rail
V_{out}	Rail-to-Rail	Rail-to-Rail
V_{os}	0.75mV	0.150mV
I_q	400µA	650µA
I_b	10pA	0.2pA
UGBW	10MHz	10MHz
SR	6V/µs	5V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/TLV316	www.ti.com/product/OPA325

Single-supply, 2nd-order, Sallen-Key low-pass filter circuit

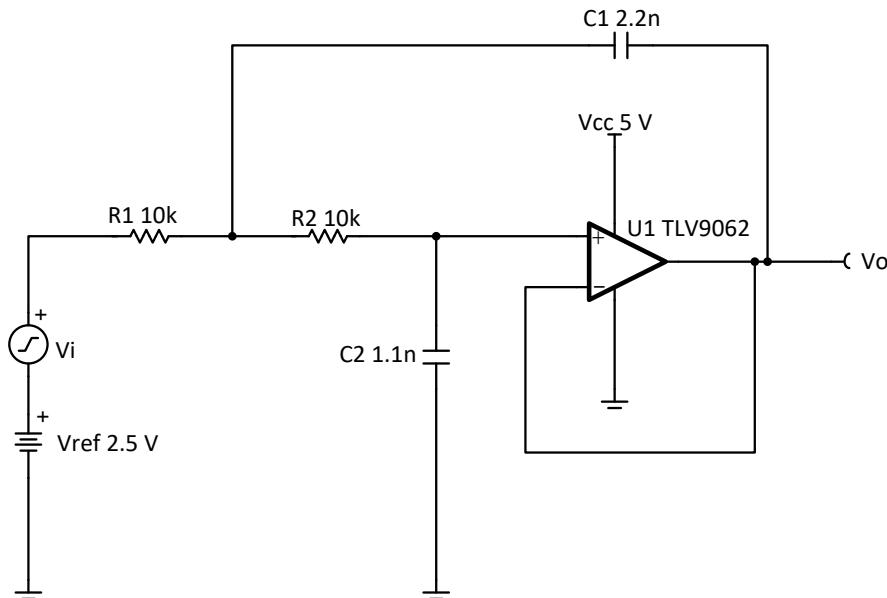


Amplifiers

Input		Output		Supply	
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	V_{cc}	V_{ee}
-2.45V	+2.45V	0.05V	4.95V	5V	0V
Gain		Cutoff Frequency (f_c)		V_{ref}	
1V/V		10kHz		2.5V	

Design Description

The Butterworth Sallen-Key low-pass filter is a second-order active filter. V_{ref} provides a DC offset to accommodate for single-supply applications. A Sallen-Key filter is usually preferred when small Q factor is desired, noise rejection is prioritized, and when a non-inverting gain of the filter stage is required. The Butterworth topology provides a maximally flat gain in the pass band.



Design Notes

1. Select an op amp with sufficient input common-mode range and output voltage swing.
2. Add V_{ref} to bias the input signal to meet the input common-mode range and output voltage swing.
3. Select the capacitor values first since standard capacitor values are more coarsely subdivided than the resistor values. Use high-precision, low-drift capacitor values to avoid errors in f_c .
4. To minimize the amount of slew-induced distortion, select an op amp with sufficient slew rate (SR).

Design Steps

The first step is to find component values for the normalized cutoff frequency of 1 radian/second. In the second step the cutoff frequency is scaled to the desired cutoff frequency with scaled component values.

The transfer function for second order Sallen-Key low-pass filter is given by:

$$H(s) = \frac{\frac{1}{R_1 \times R_2 \times C_1 \times C_2}}{s^2 + s\left(\frac{1}{R_1 \times C_1} + \frac{1}{R_2 \times C_1}\right) + \frac{1}{R_1 \times R_2 \times C_1 \times C_2}}$$

$$H(s) = \frac{a_0}{s^2 + a_1 \times s + a_0}$$

Here,

$$a_1 = \frac{1}{R_1 \times C_1} + \frac{1}{R_2 \times C_1}, a_0 = \frac{1}{R_1 \times R_2 \times C_1 \times C_2}$$

- Set normalized values of R_1 and R_2 (R_{1n} and R_{2n}) and calculate normalized values of C_1 and C_2 (C_{1n} and C_{2n}) by setting w_c to 1 radian/sec (or $f_c = 1 / (2 \times \pi)$ Hz). For the second-order Butterworth filter, (see the *Butterworth Filter Table* in the [Active Low-Pass Filter Design Application Report](#)).

$$\omega_c = 1 \frac{\text{radian}}{\text{second}} \rightarrow a_0 = 1, a_1 = \sqrt{2}, \text{ let } R_{1n} = R_{2n} = 1, \text{ then } C_{1n} \times C_{2n} = 1 \text{ or } C_{2n} = \frac{1}{C_{1n}}, a_1 = \frac{2}{C_{1n}} = \sqrt{2}$$

$$\therefore C_{1n} = \sqrt{2} = 1.414 \text{ F}, C_{2n} = \frac{1}{C_{1n}} = 0.707 \text{ F}$$

- Scale the component values and cutoff frequency. The resistor values are very small and capacitors values are unrealistic, hence these have to be scaled. The cutoff frequency is scaled from 1 radian/sec to w_0 . If m is assumed to be the scaling factor, increase the resistors by m times, then the capacitor values have to decrease by $1/m$ times to keep the same cutoff frequency of 1 radian/sec. If the cutoff frequency is scaled to be w_0 , then the capacitor values have to be decreased by $1/w_0$. The component values for the design goals are calculated in steps 3 and 4.

$$R_1 = R_{1n} \times m, R_2 = R_{2n} \times m \quad (6)$$

$$C_1 = \frac{C_{1n}}{m \times \omega_0} = \frac{1.414}{m \times \omega_0} \text{ F} \quad (7)$$

$$C_2 = \frac{C_{2n}}{m \times \omega_0} = \frac{0.707}{m \times \omega_0} \text{ F} \quad (8)$$

- Set R_1 and R_2 values:

$$m = 10000$$

$$R_1 = (R_{1n} \times m) = 10 \text{k}\Omega \quad (10)$$

$$R_2 = (R_{2n} \times m) = 10 \text{k}\Omega \quad (11)$$

4. Calculate C_1 and C_2 based on m and w_0 .

Given $\omega_0 = 2 \times \pi \times f_c$, where $f_c = 10\text{kHz}$ and $m = 10000 = 10\text{k}$

$$C_1 = \frac{1.414}{m \times \omega_0} \text{ F} = \frac{1.414}{10\text{k} \times 2 \times \pi \times 10\text{kHz}} = 2.25\text{nF} \approx 2.2\text{nF} \text{ (Standard Value)}$$

$$C_2 = \frac{0.707}{m \times \omega_0} \text{ F} = \frac{0.707}{10\text{k} \times 2 \times \pi \times 10\text{kHz}} = 1.125\text{nF} \approx 1.1\text{nF} \text{ (Standard Value)}$$

5. Calculate the minimum required GBW and SR for f_c .

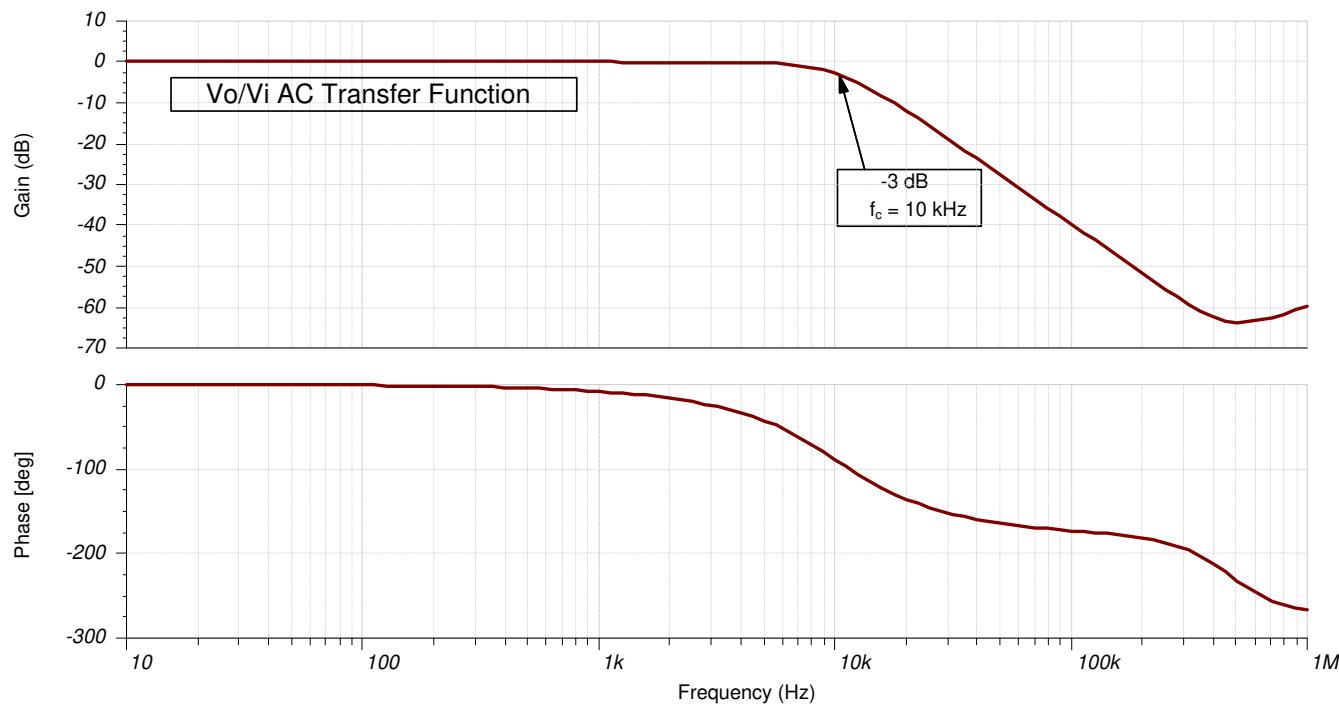
$$\text{GBW} = 100 \times \text{Gain} \times f_c = 100 \times 1 \times 10\text{kHz} = 1\text{MHz}$$

$$\text{SR} = 2 \times \pi \times f_c \times V_{i\text{peak}} = 2 \times \pi \times 10\text{kHz} \times 2.45\text{V} = 0.154 \frac{\text{V}}{\mu\text{s}}$$

The TLV9062 device has a GBW of 10MHz and SR of 6.5V/ μs , so the requirements are met.

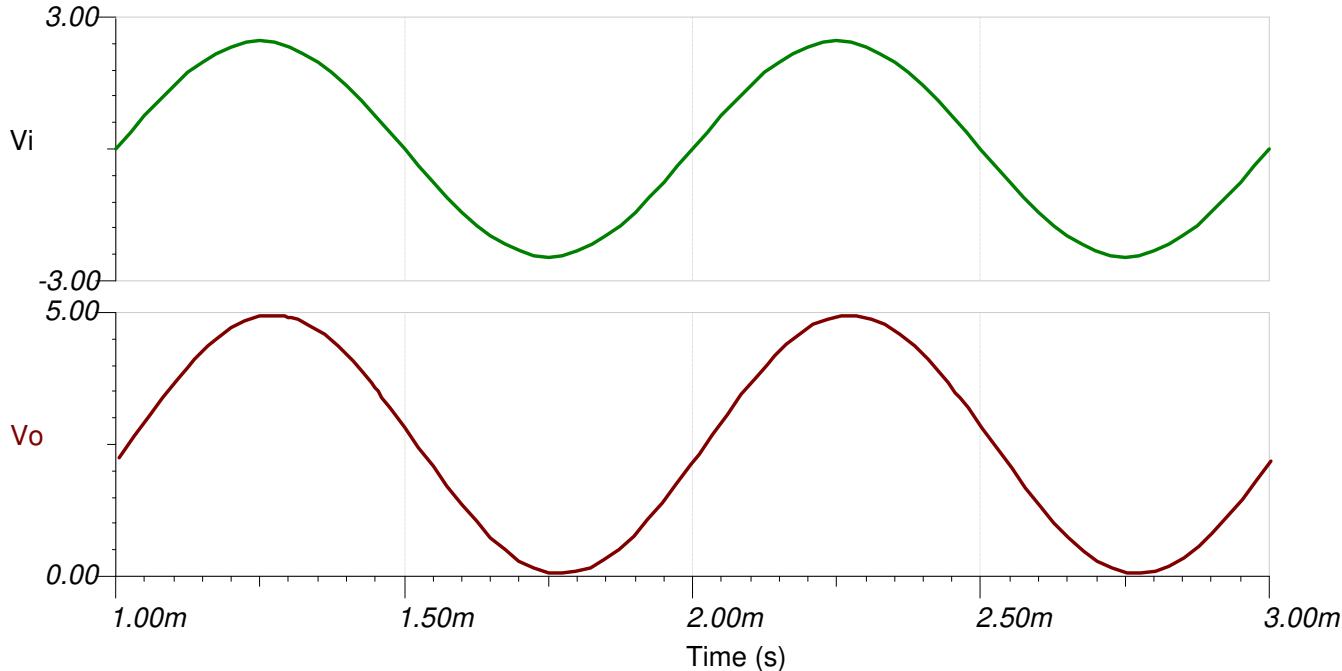
Design Simulations

AC Simulation Results

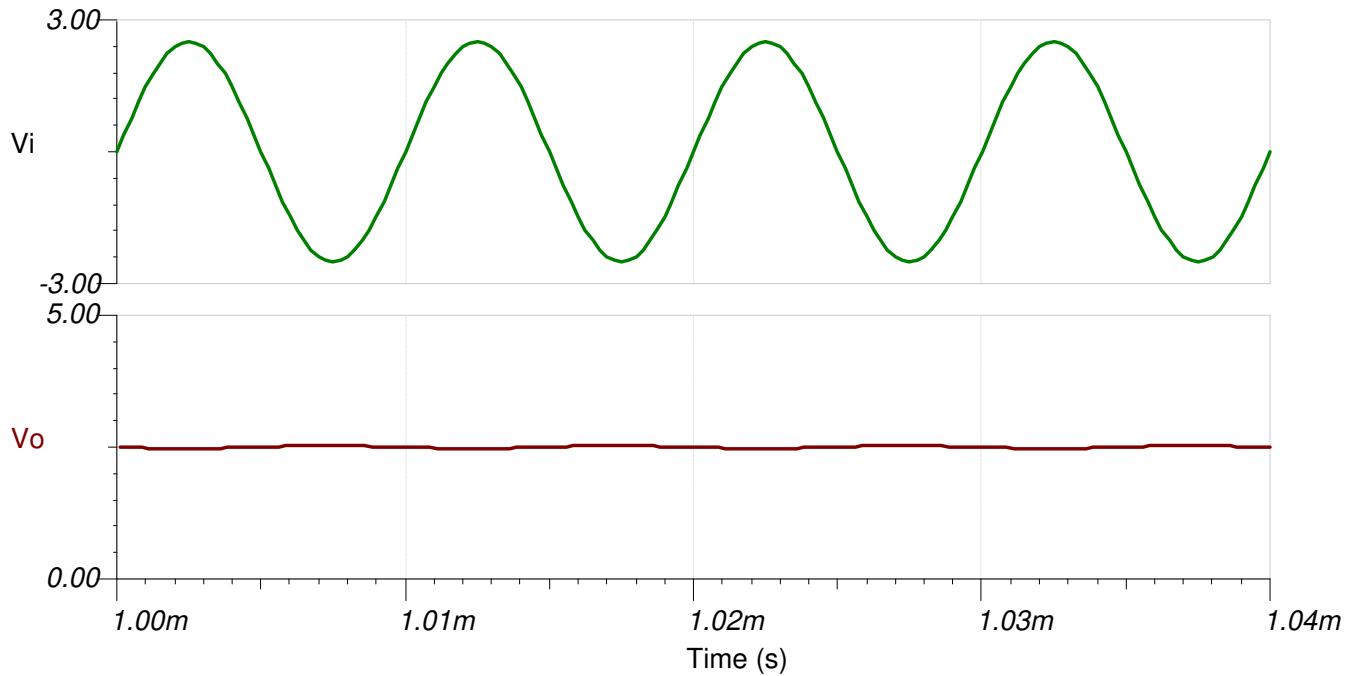


Transient Simulation Results

The following image shows the filter output in response to 5-Vpp, 1-kHz input signal (gain = 1V / V).



The following image shows the filter output in response to 5-Vpp, 100-kHz input signal (gain = 0.01 V/V).



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.
2. SPICE Simulation File [SBOC598](#).
3. [TI Precision Labs](#).
4. [Active Low-Pass Filter Design Application Report](#)

Design Featured Op Amp

TLV9062	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-Rail
V_{out}	Rail-to-Rail
V_{os}	0.3mV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

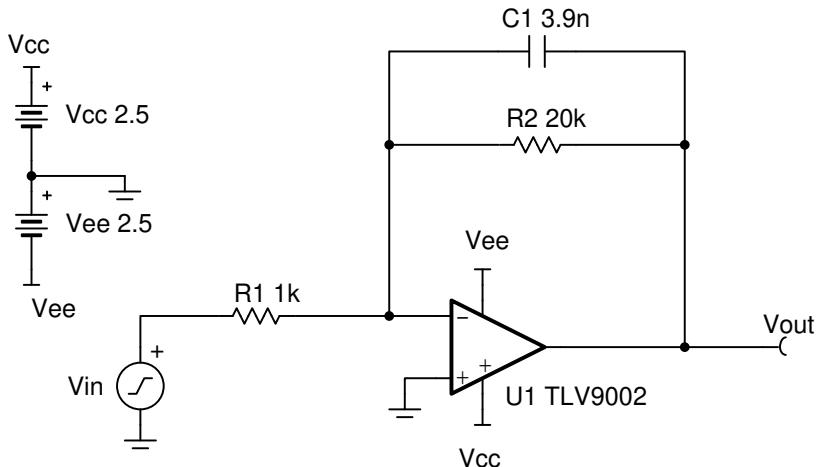
	TLV316	OPA325
V_{ss}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-Rail	Rail-to-Rail
V_{out}	Rail-to-Rail	Rail-to-Rail
V_{os}	0.75mV	0.150mV
I_q	400µA	650µA
I_b	10pA	0.2pA
UGBW	10MHz	10MHz
SR	6V/µs	5V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/TLV316	www.ti.com/product/OPA325

Low-Pass, Filtered, Inverting Amplifier Circuit**Design Goals**

Input		Output		BW	Supply	
V _{iMin}	V _{iMax}	V _{oMin}	V _{oMax}	f _p	V _{ee}	V _{cc}
-0.1V	0.1V	-2V	2V	2kHz	-2.5V	2.5V

Design Description

This tunable low-pass inverting amplifier circuit amplifies the signal level by 26dB or 20V/V. R₂ and C₁ set the cutoff frequency for this circuit. The frequency response of this circuit is the same as that of a passive RC filter, except that the output is amplified by the pass-band gain of the amplifier. Low-pass filters are often used in audio signal chains and are sometimes called bass-boost filters.

**Design Notes**

1. C₁ and R₂ set the low-pass filter cutoff frequency.
2. The common-mode voltage is set by the non-inverting input of the op amp, which in this case is mid-supply.
3. Using high value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. R₂ and R₁ set the gain of the circuit.
5. The pole frequency f_p of 2kHz is selected for an audio bass-boost application.
6. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
7. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
8. For more information on op amp linear operation region, stability, slew-induced distortion, capacitive load drive, driving ADCs and bandwidth please see the design references section.

Design Steps

The DC transfer function of this circuit is given below.

$$V_o = V_i \times \left(-\frac{R_2}{R_1} \right)$$

- Pick resistor values for given passband gain.

$$Gain = \frac{R_2}{R_1} = 20 \frac{V}{V} (26 dB)$$

$$R_1 = 1 k\Omega$$

$$R_2 = Gain \times (R_1) = 20 \frac{V}{V} \times 1 k\Omega = 20 k\Omega$$

- Select low-pass filter pole frequency f_p

$$f_p = 2 kHz$$

- Calculate C_1 using R_2 to set the location of f_p .

$$f_p = \frac{1}{2 \times \pi \times R_2 \times C_1} = 2 kHz$$

$$C_1 = \frac{1}{2 \times \pi \times R_2 \times f_p} = \frac{1}{2 \times \pi \times 20 k\Omega \times 2 kHz} = 3.98 nF \approx 3.9 nF (Standard Value)$$

- Calculate the minimum slew rate required to minimize slew-induced distortion.

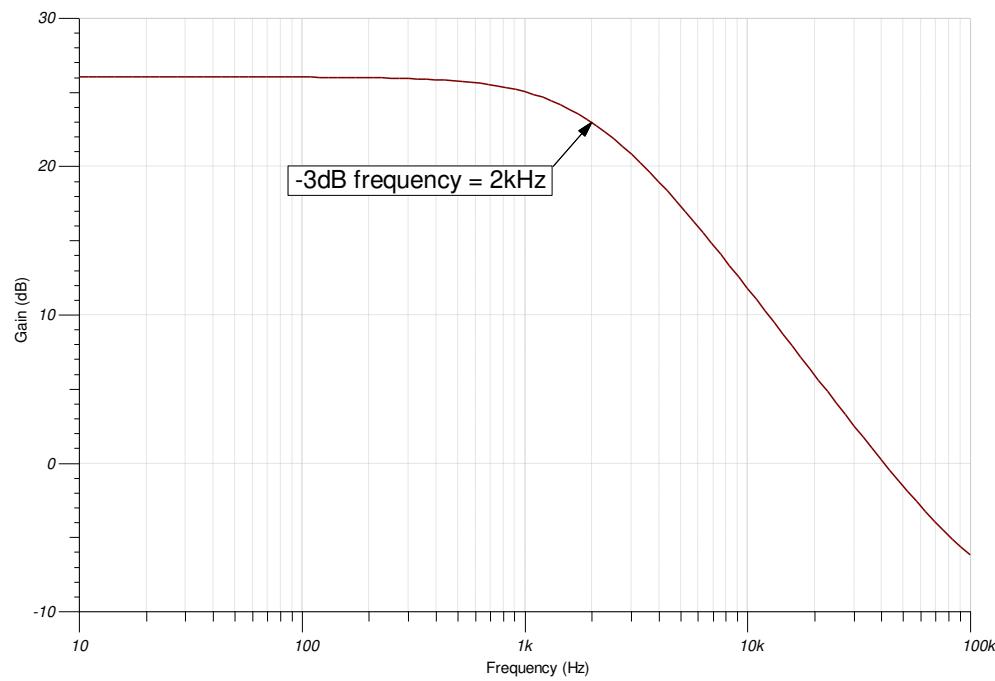
$$V_p = \frac{SR}{2 \times \pi \times f_p} \rightarrow SR > 2 \times \pi \times f_p \times V_p$$

$$SR > 2 \times \pi \times 2 kHz \times 2 V = 0.025 \frac{V}{\mu s}$$

- $SR_{TLV9002} = 2V/\mu s$, therefore it meets this requirement

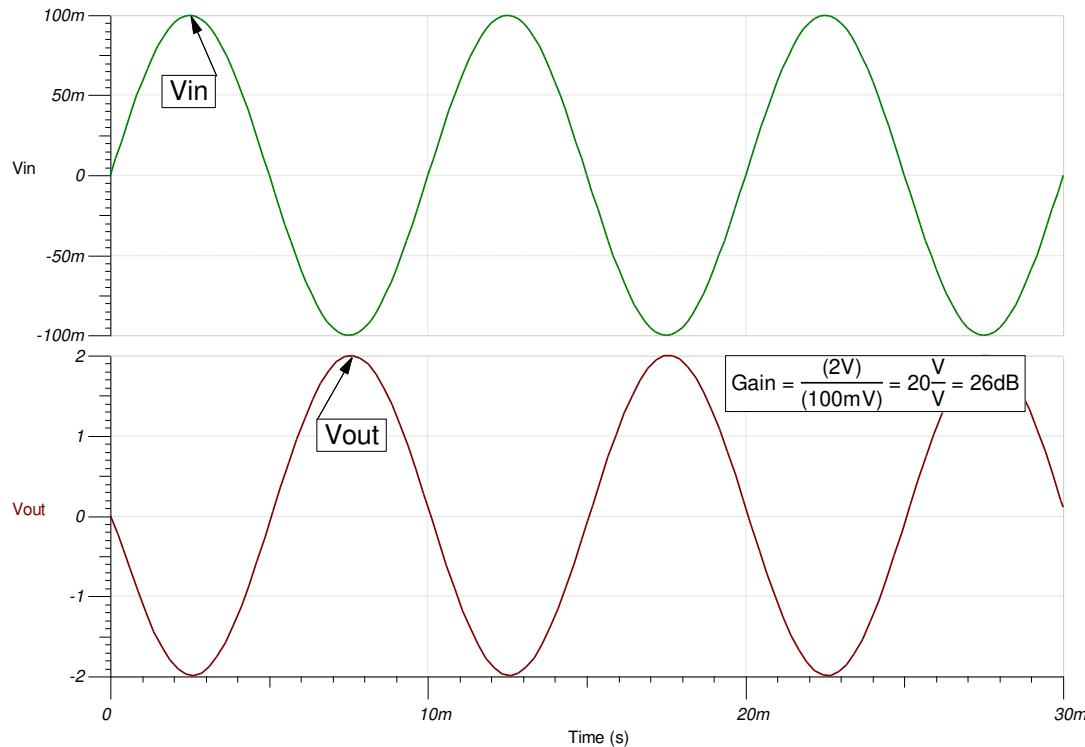
Design Simulations

AC Simulation Results

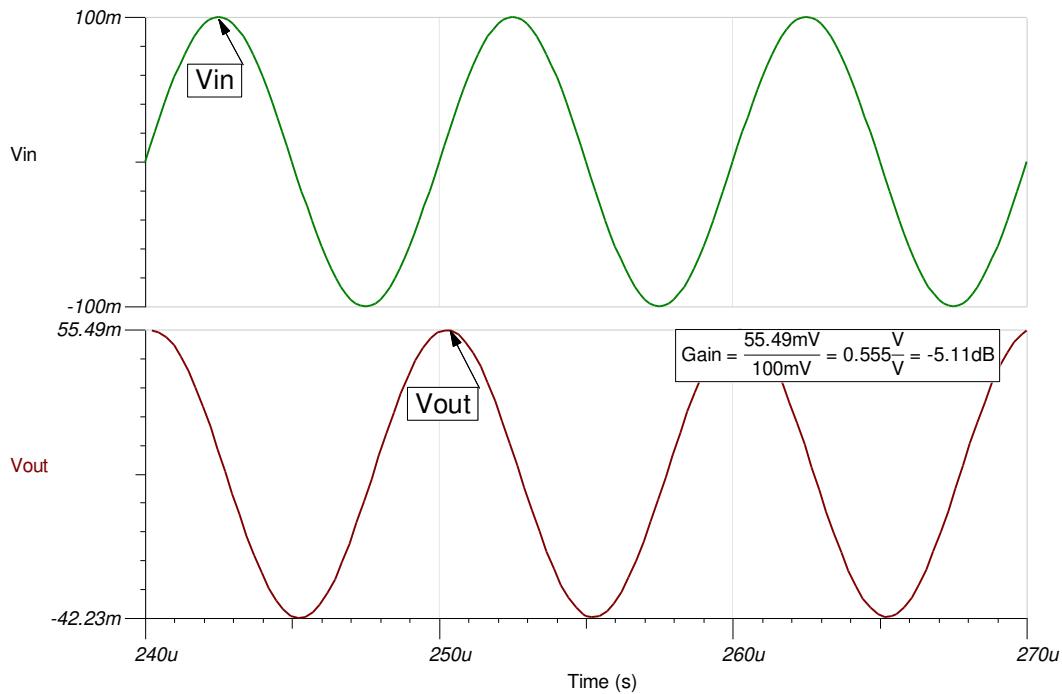


Transient Simulation Results

A 100 Hz, 0.2 V_{pp} sine wave yields a 4 V_{pp} output sine wave.



A 100 kHz, 0.2 V_{pp} sine wave yields a 0.1 V_{pp} output sine wave.



References:

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOC523](#)
3. [TI Precision Designs TIPD185](#)
4. [TI Precision Labs](#)

Design Featured Op Amp

TLV9002	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.4mV
I_q	60µA
I_b	5pA
UGBW	1MHz
SR	2V/µs
#Channels	1,2,4
www.ti.com/product/tlv9002	

Design Alternate Op Amp

OPA375	
V_{ss}	2.25V to 5.5V
V_{inCM}	V _{ee} to V _{cc} -1.2V
V_{out}	Rail-to-rail
V_{os}	0.15mV
I_q	890µA
I_b	10pA
UGBW	10MHz
SR	4.75V/µs
#Channels	1
www.ti.com/product/opa375	

Revision History

Revision	Date	Change
A	January 2021	Updated result in Design Step 4 from 0.25 to 0.025

Single-supply, 2nd-order, Sallen-Key band-pass filter circuit

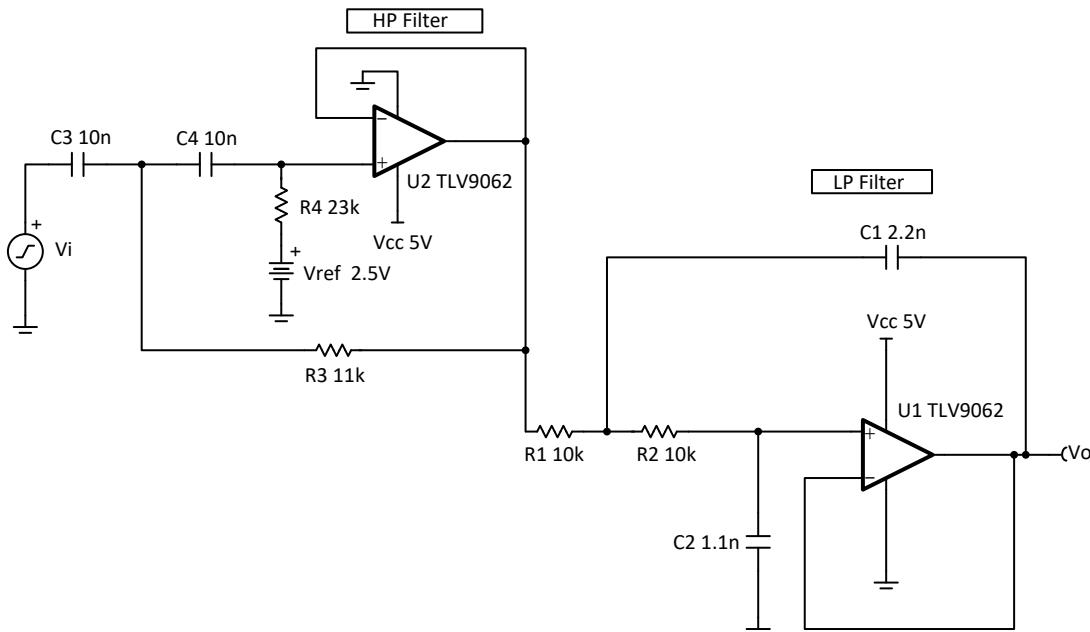


Amplifiers

Input		Output		Supply	
V _{iMin}	V _{iMax}	V _{oMin}	V _{oMax}	V _{cc}	V _{ee}
-2.45V	+2.45V	0.05V	4.95V	5V	0V
Gain		Low Cutoff Frequency (f _l)		High Cutoff Frequency (f _h)	
1V/V		1kHz		10kHz	
V _{ref}		2.5V			

Design Description

This circuit is a single-supply, 2nd-order Sallen-Key (SK) band-pass (BP) filter. It is designed by cascading an SK low-pass filter and an SK high-pass filter. Vref provides a DC offset to accommodate for a single supply.



Design Notes

1. Select an op amp with sufficient input common-mode range and output voltage swing.
2. Add V_{ref} to bias the input signal to meet the input common-mode range and output voltage swing.
3. Select the capacitor values first since standard capacitor values are more coarsely subdivided than the resistor values. Use high-precision, low-drift capacitor values to avoid errors in f_l and f_h.
4. To minimize the amount of slew-induced distortion, select an op amp with sufficient slew rate (SR).
5. For HP filters, the maximum frequency is set by the gain bandwidth (GBW) of the op amp. Therefore, be sure to select an op amp with sufficient GBW.

Design Steps

This BP filter design involves two cascaded filters, a low-pass (LP) filter and a high-pass (HP) filter. The lower cutoff frequency (f_l) of the BP filter is 1kHz and the higher cutoff frequency (f_h) is 10kHz. The design steps show an LP filter design with f_h of 10kHz and an HP filter design with f_l of 1kHz. See the SK LP filter design and SK HP filter design in the circuit cookbook for details on transfer function equations and calculations.

LP Filter Design

1. Use [SK low-pass filter design](#) to determine R_1 and R_2 .

$$R_1 = 10\text{k}\Omega, \\ R_2 = 10\text{k}\Omega$$

2. Use [SK low-pass filter design](#) to determine C_1 and C_2 .

$$C_1 = 2.2\text{nF} \text{ (Standard Value)}, \\ C_2 = 1.1\text{nF} \text{ (Standard Value)}$$

HP Filter Design

1. Use [SK high-pass filter design](#) to determine C_3 and C_4 .

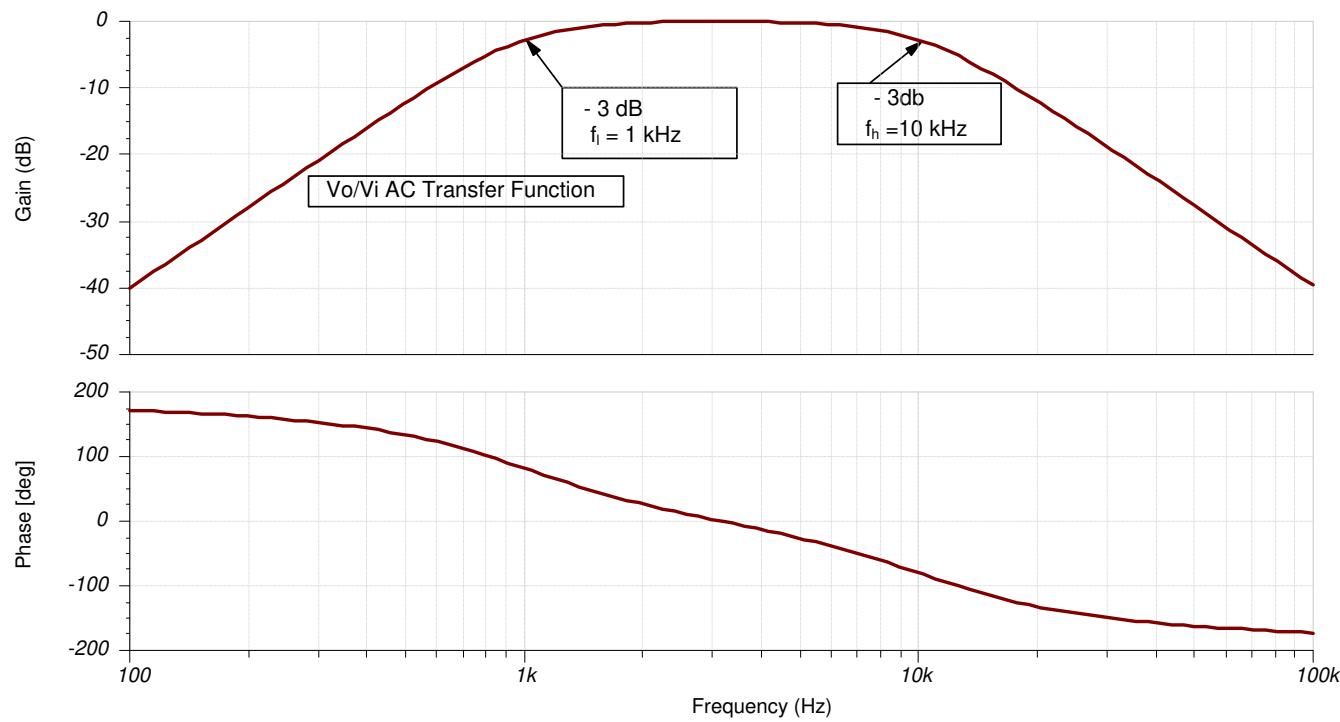
$$C_3 = 10\text{nF}, \\ C_4 = 10\text{nF}$$

2. Use [SK high-pass filter design](#) to determine R_3 and R_4 .

$$R_3 = 11\text{k}\Omega, \\ R_4 = 23\text{k}\Omega$$

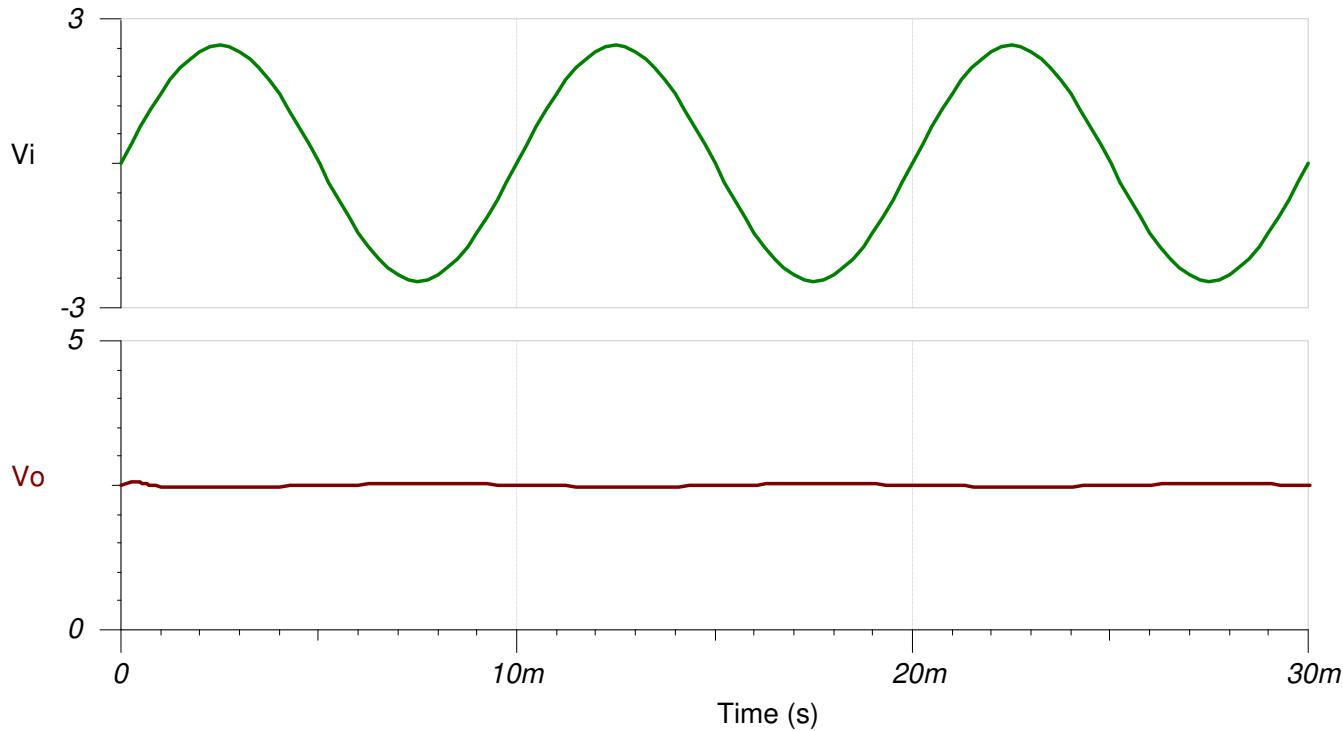
Design Simulations

AC Simulation Results

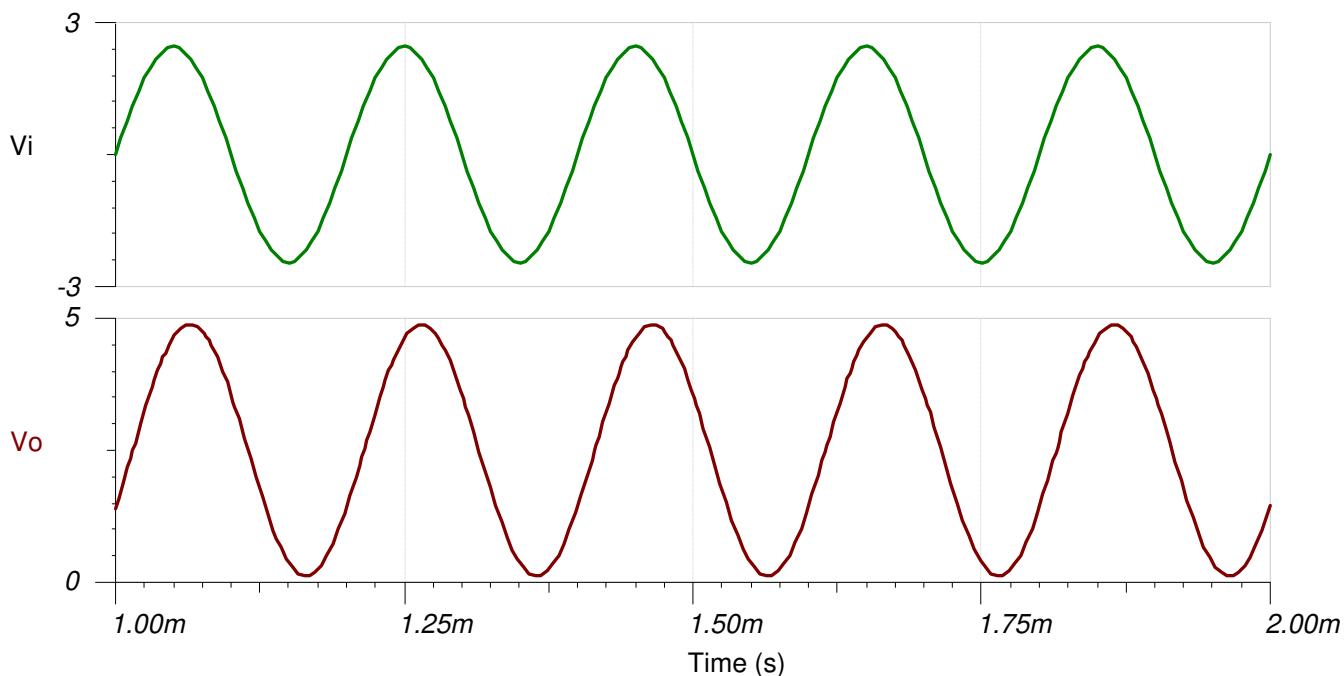


Transient Simulation Results

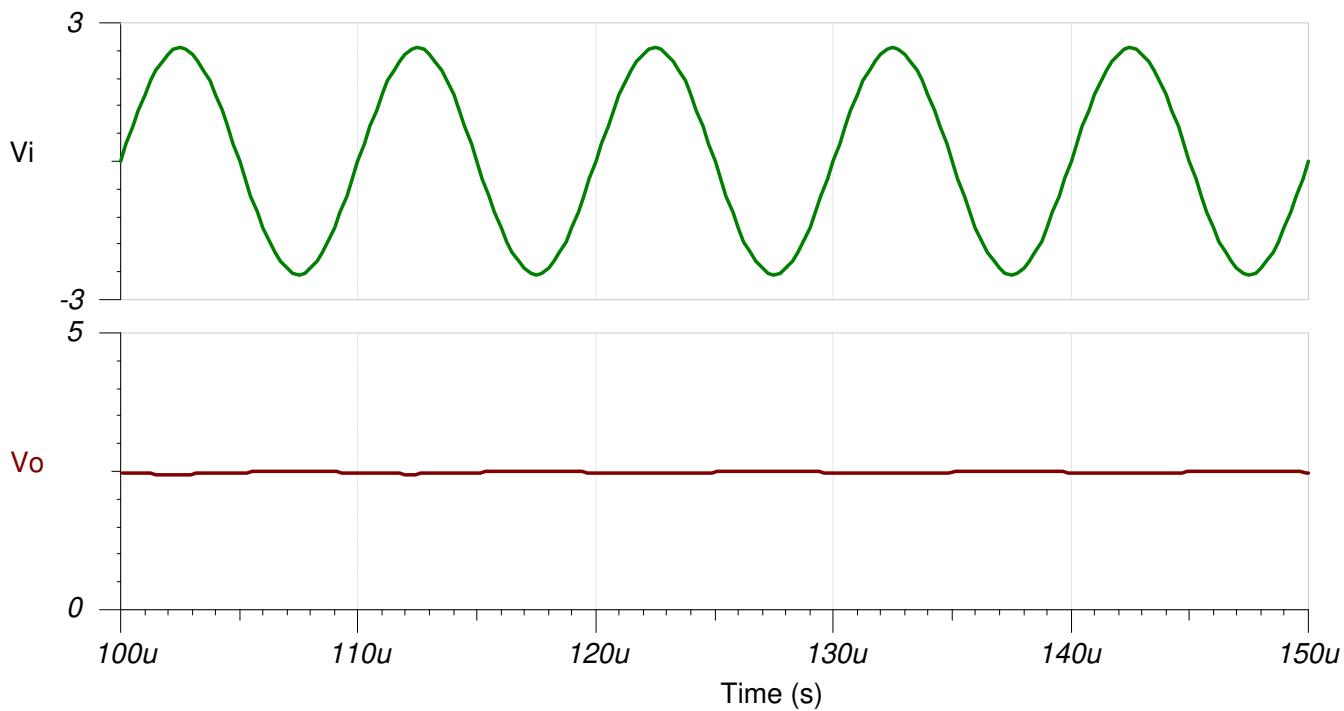
The following image shows a filter output in response to a 5-V_{pp}, 100-Hz input signal (gain = 0.01 V/V).



The following transient simulation result shows a filter output in response to a 5-V_{pp}, 5-kHz input signal (gain = 1V/V).



The following image shows a filter output in response to a 5-V_{pp}, 100-kHz input signal (gain = 0.01V/V).



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.
2. [TI Precision Labs](#).

Design Featured Op Amp

TLV9062	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-Rail
V_{out}	Rail-to-Rail
V_{os}	0.3mV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

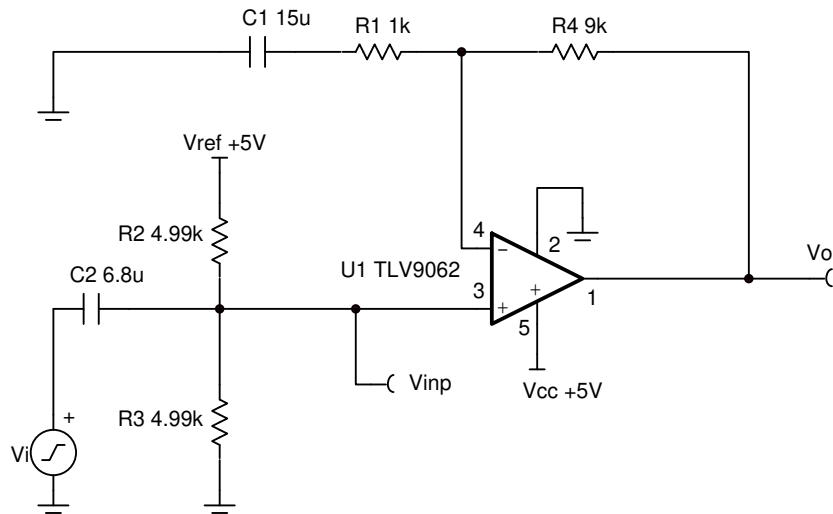
	TLV316	OPA325
V_{ss}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-Rail	Rail-to-Rail
V_{out}	Rail-to-Rail	Rail-to-Rail
V_{os}	0.75mV	0.150mV
I_q	400µA	650µA
I_b	10pA	0.2pA
UGBW	10MHz	10MHz
SR	6V/µs	5V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/TLV316	www.ti.com/product/OPA325

AC Coupled (HPF) Non-Inverting Amplifier Circuit**Design Goals**

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
-240 mV	240 mV	0.1 V	4.9 V	5 V	0 V	5 V
Lower Cutoff Freq. (f_L)		Upper Cutoff Freq. (f_H)			AC Gain (G_{ac})	
16 Hz		≥ 1 MHz			10 V/V	

Design Description

This circuit amplifies an AC signal, and shifts the output signal so that it is centered at one-half the power supply voltage. Note that the input signal has zero DC offset so it swings above and below ground. The key benefit of this circuit is that it accepts signals which swing below ground even though the amplifier does not have a negative power supply.

**Design Notes**

1. The voltage at V_{inp} sets the input common-mode voltage.
2. R_2 and R_3 load the input signal for AC frequencies.
3. Use low feedback resistance for low noise.
4. Set the output range based on linear output swing (see A_{ol} specification of op amp).
5. The circuit has two real poles that determine the high-pass filter -3 dB frequency. Set them both to $f_L/1.557$ to achieve -3 dB at the lower cutoff frequency (f_L).

Design Steps

1. Select R_1 and R_4 to set the AC voltage gain.

$$R_1 = 1 \text{ k}\Omega \text{ (Standard Value)}$$

$$R_4 = R_1 \times (G_{ac} - 1) = 1 \text{ k}\Omega \times \left(10\frac{V}{V} - 1\right) = 9\text{k}\Omega \text{ (Standard Value)}$$

2. Select R_2 and R_3 to set the DC output voltage (V_{DC}) to 2.5 V, or mid-supply.

$$R_3 = 4.99\text{k}\Omega \text{ (Standard Value)}$$

$$R_2 = \frac{R_3 \times V_{ref}}{V_{DC}} - R_3 = \frac{4.99\text{k}\Omega \times 5\text{V}}{2.5\text{V}} - 4.99\text{k}\Omega = 4.99\text{k}\Omega$$

3. Select C_1 based on f_L and R_1 .

$$f_L = 16\text{Hz}$$

$$C_1 = \frac{1}{2 \times \pi \times R_1 \times \left(\frac{f_L}{1.557}\right)} = \frac{1}{2 \times \pi \times 1 \text{ k}\Omega \times 10.3\text{Hz}} = 15.5\mu\text{F} \approx 15\mu\text{F} \text{ (Standard Value)}$$

4. Select C_2 based on f_L , R_2 , and R_3 .

$$R_{div} = \frac{R_2 \times R_3}{R_2 + R_3} = \frac{4.99\text{k}\Omega \times 4.99\text{k}\Omega}{4.99\text{k}\Omega + 4.99\text{k}\Omega} = 2.495\text{k}\Omega$$

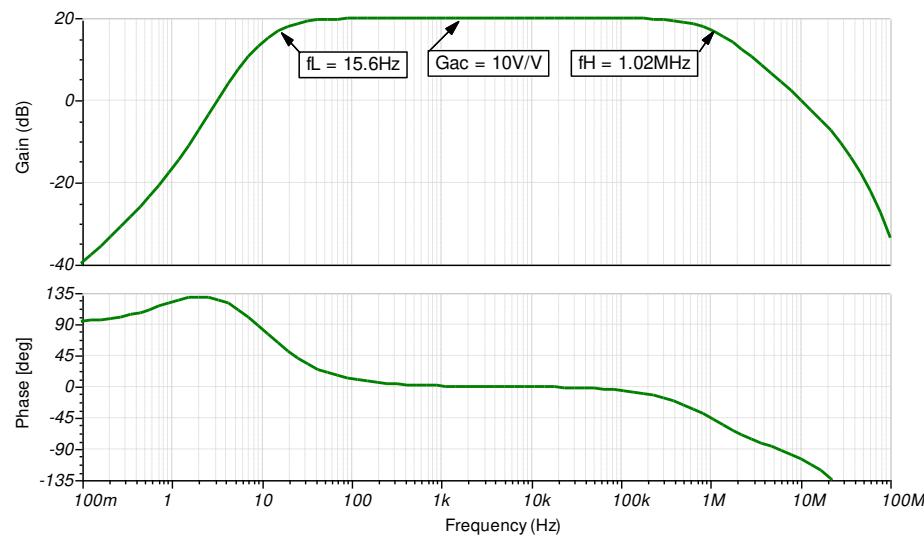
$$C_2 = \frac{1}{2 \times \pi \times R_{div} \times \left(\frac{f_L}{1.557}\right)} = \frac{1}{2 \times \pi \times 2.495\text{k}\Omega \times 10.3\text{Hz}} = 6.4\mu\text{F} \rightarrow 6.8\mu\text{F} \text{ (Standard Value)}$$

5. The upper cutoff frequency (f_H) is set by the non-inverting gain of this circuit and the gain bandwidth (GBW) of the device (TLV9062).

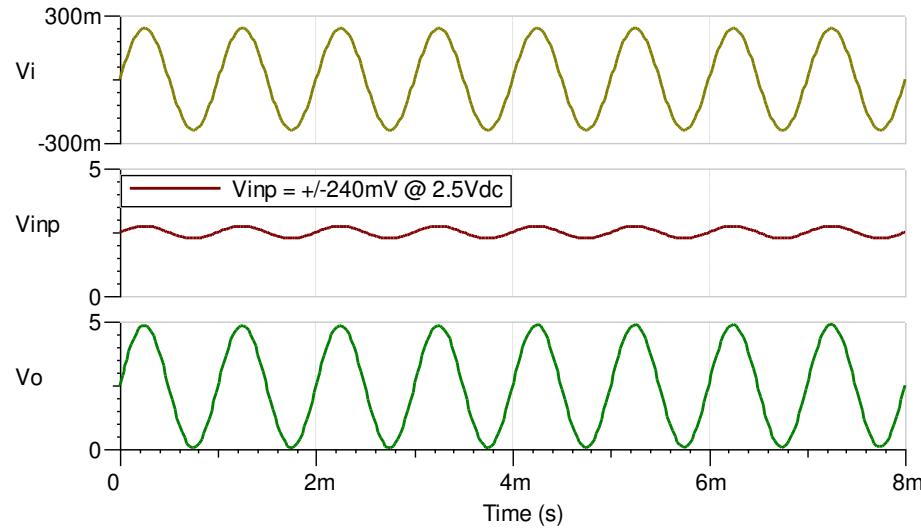
$$f_H = \frac{\text{GBW of TLV9062}}{G_{ac}} = \frac{10\text{MHz}}{10\frac{V}{V}} = 1 \text{ MHz}$$

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC505](#).

See [TIPD185](#).

Design Featured Op Amp

TLV9062	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	300 μ V
I_q	538 μ A
I_b	0.5 pA
UGBW	10 MHz
SR	6.5 V/ μ s
#Channels	1, 2, and 4
TLV9062	

Design Alternate Op Amp

OPA192	
V_{cc}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 μ V
I_q	1 mA/Ch
I_b	5 pA
UGBW	10 MHz
SR	20 V/ μ s
#Channels	1, 2, and 4
OPA192	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from August 2, 2017 to February 1, 2019

Page

- | | |
|--|-------------------|
| • Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page..... | 1 |
|--|-------------------|

Single-supply, 2nd-order, Sallen-Key high-pass filter circuit



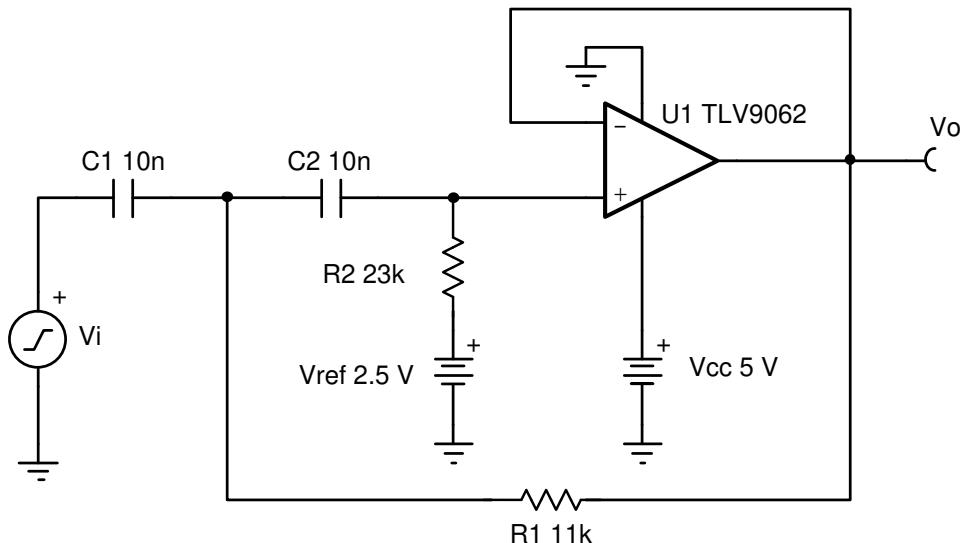
Amplifiers

Input		Output		Supply	
V _{iMin}	V _{iMax}	V _{oMin}	V _{oMax}	V _{cc}	V _{ee}
-2.45V	+2.45V	0.05V	4.95V	5V	0V
Gain		Cutoff Frequency (f _c)		Max Frequency (f _{max})	
1V/V		1kHz		10kHz	
V _{ref}		2.5V			

Design Description

The Butterworth Sallen-Key (SK) high-pass (HP) filter is a 2nd-order active filter. V_{ref} provides a DC offset to accommodate for single-supply applications.

An SK filter is usually preferred when small Q factor is desired, noise rejection is prioritized, and when a non-inverting gain of the filter stage is required. The Butterworth topology provides a maximally flat gain in the pass band.



Design Notes

1. Select an op amp with sufficient input common-mode range and output voltage swing.
2. Add V_{ref} to bias the input signal to meet the input common-mode range and output voltage swing.
3. Select the capacitor values first since standard capacitor values are more coarsely subdivided than the resistor values. Use high-precision, low-drift capacitor values to avoid errors in f_c.
4. To minimize the amount of slew-induced distortion, select an op amp with sufficient slew rate (SR).
5. For HP filters, the maximum frequency is set by the gain bandwidth (GBW) of the op amp. Therefore, be sure to select an op amp with sufficient GBW.

Design Steps

The first step is to find component values for the normalized cutoff frequency of 1 radian/second. In the second step the cutoff frequency is scaled to the desired cutoff frequency with scaled component values.

The transfer function for the second-order Sallen-Key high-pass filter is given by:

$$H(s) = \frac{s^2}{s^2 + s\left(\frac{1}{R_2 \times C_1} + \frac{1}{R_2 \times C_2}\right) + \frac{1}{R_1 \times R_2 \times C_1 \times C_2}}$$

$$H(s) = \frac{s^2}{s^2 + a_1 \times s + a_0}$$

where,

$$a_1 = \frac{1}{R_2 \times C_1} + \frac{1}{R_2 \times C_2}, a_0 = \frac{1}{R_1 \times R_2 \times C_1 \times C_2}$$

- Set normalized values of C_1 and C_2 (C_{1n} and C_{2n}) and calculate normalized values of R_1 and R_2 (R_{1n} and R_{2n}) by setting w_c to 1 radian/sec (or $f_c = 1 / (2 \times \pi)$ Hz). For the second-order Butterworth filter, (see the *Butterworth Filter Table* in the [Active Low-Pass Filter Design Application Report](#)).

$$a_0 = 1, a_1 = \sqrt{2}, \text{ let } C_{1n} = C_{2n} = 1 \text{ F, then } R_{1n} \times R_{2n} = 1 \text{ or } R_{2n} = \frac{1}{R_{1n}}, a_1 = \frac{2}{R_{2n}} = \sqrt{2}$$

$$\therefore R_{2n} = \sqrt{2} = 1.414\Omega, R_{1n} = \frac{1}{R_{2n}} = 0.707\Omega$$

- Scale the component values and cutoff frequency. The resistor values are very small and capacitors values are unrealistic, hence these have to be scaled. The cutoff frequency is scaled from 1 radian/sec to w_0 . If m is assumed to be the scaling factor, increase the resistors by m times, then the capacitor values have to decrease by $1/m$ times to keep the same cutoff frequency of 1 radian/sec. If the cutoff frequency is scaled to be w_0 , then the capacitor values have to be decreased by $1/w_0$. The component values for the design goals are calculated in steps 3 and 4.

$$R_1 = R_{1n} \times m, R_2 = R_{2n} \times m$$

$$C_1 = C_2 = \frac{C_{1n}}{m \times w_0} F$$

- Set C_1 and C_2 to 10nF, then calculate m .

$$w_0 = 2 \times \pi \times 1\text{kHz}, m = 15915.5$$

- Select R_1 and R_2 based on m .

$$R_1 = 0.707 \times 15915 = 11252\Omega \approx 11k\Omega \text{ (Standard Value)}$$

$$R_2 = 1.414 \times 15915 = 22504\Omega \approx 23k\Omega \text{ (Standard Value)}$$

- Calculate the minimum required GBW and SR for f_{max} .

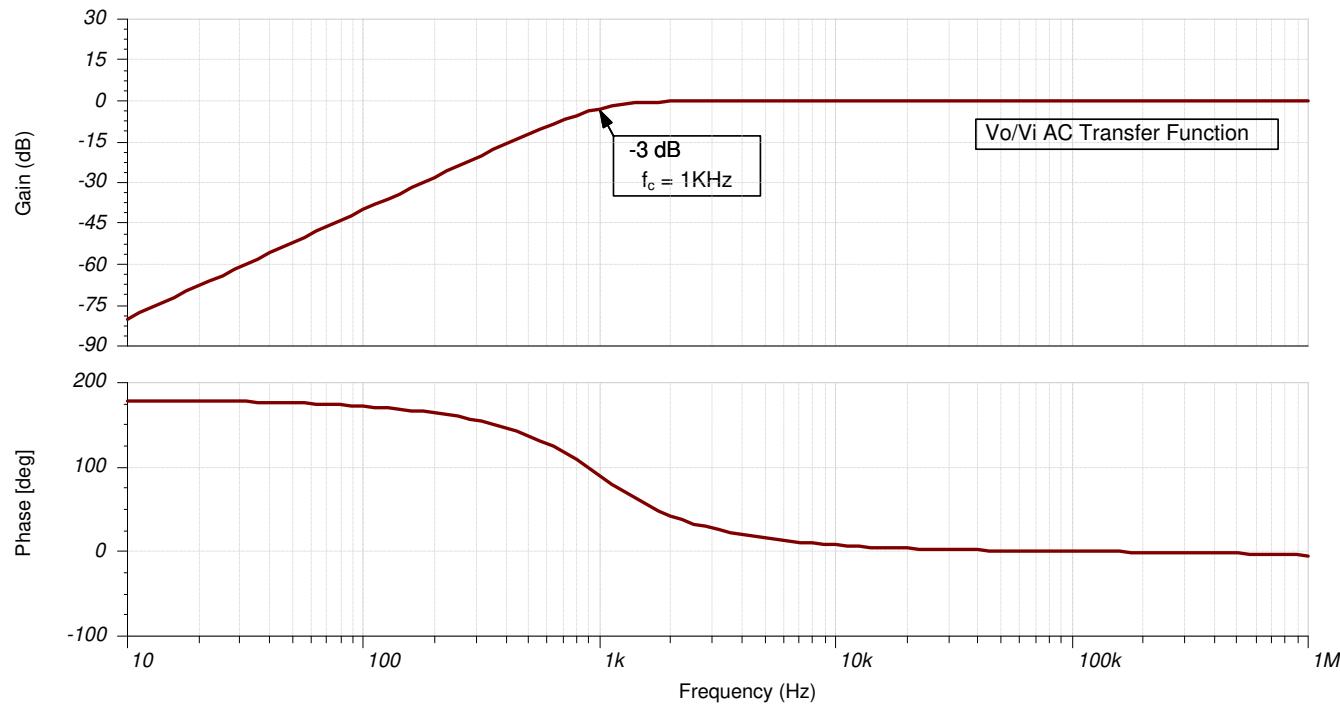
$$\text{GBW} = 100 \times \text{Gain} \times f_{max} = 100 \times 1 \times 10\text{kHz} = 1\text{MHz}$$

$$\text{SR} = 2 \times \pi \times f_{max} \times V_{ip} = 2 \times \pi \times 10\text{kHz} \times 2.45V = 0.154 \frac{V}{\mu s}$$

The TLV9062 device has a GBW of 10MHz and SR of 6.5V/ μ s, so it meets these requirements.

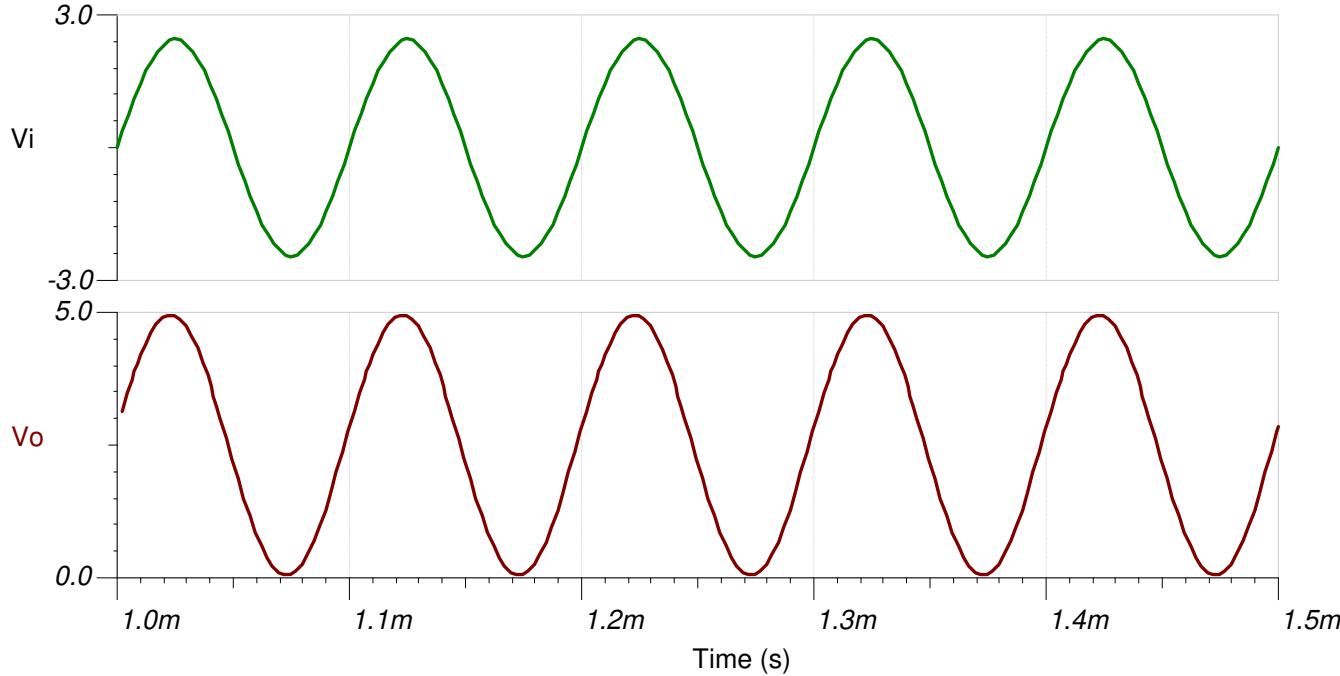
Design Simulations

AC Simulation Results

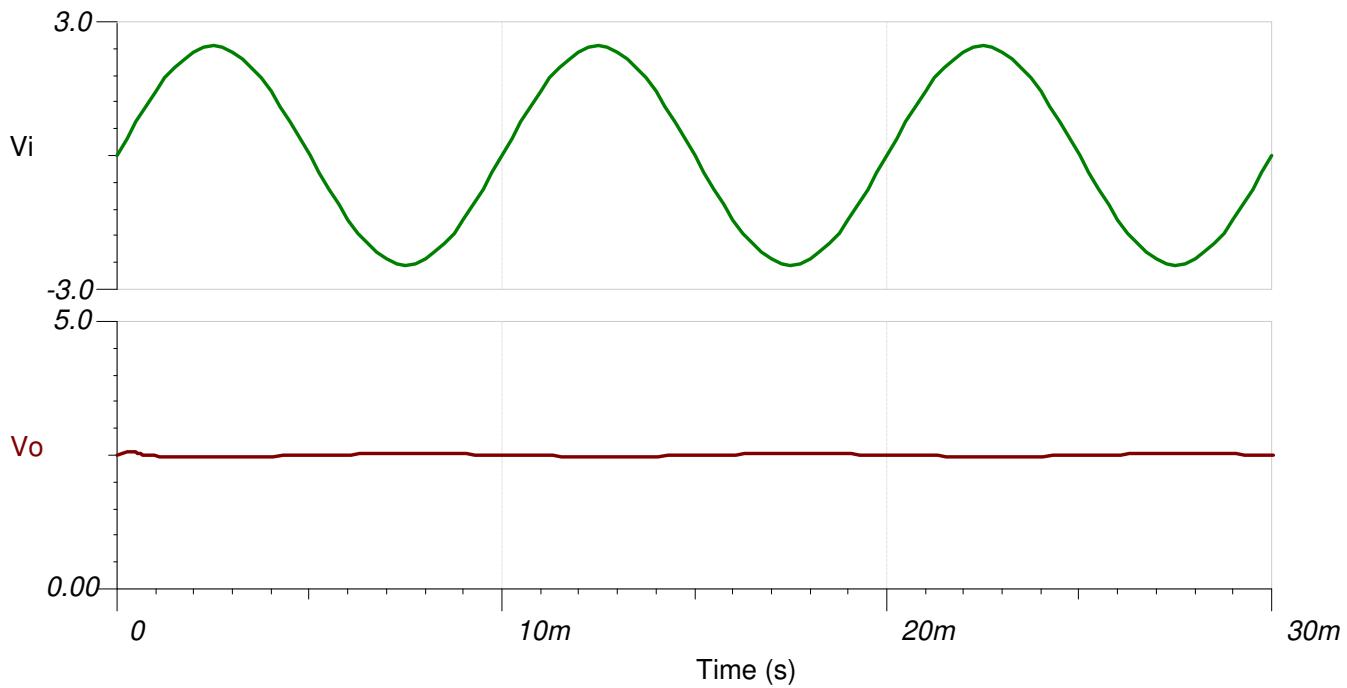


Transient Simulation Results

The following image shows the filter output in response to a $\pm 2.5\text{-V}$, 10-kHz input signal (gain is 1V / V).



The following image shows the filter output in response to a $\pm 2.5\text{-V}$, 10-Hz input signal (gain is 0.014V/V).



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.
2. SPICE Simulation File - [SBOMB38](#).
3. [TI Precision Labs](#)

Design Featured Op Amp

TLV9062	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-Rail
V_{out}	Rail-to-Rail
V_{os}	0.3mV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V / µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

	TLV316	OPA325
V_{ss}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-Rail	Rail-to-Rail
V_{out}	Rail-to-Rail	Rail-to-Rail
V_{os}	0.75mV	0.150mV
I_q	400µA	650µA
I_b	10pA	0.2pA
UGBW	10MHz	10MHz
SR	6V / µs	5V / µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/OPA316	www.ti.com/product/OPA325

Single-supply, 2nd-order, multiple feedback high-pass filter circuit

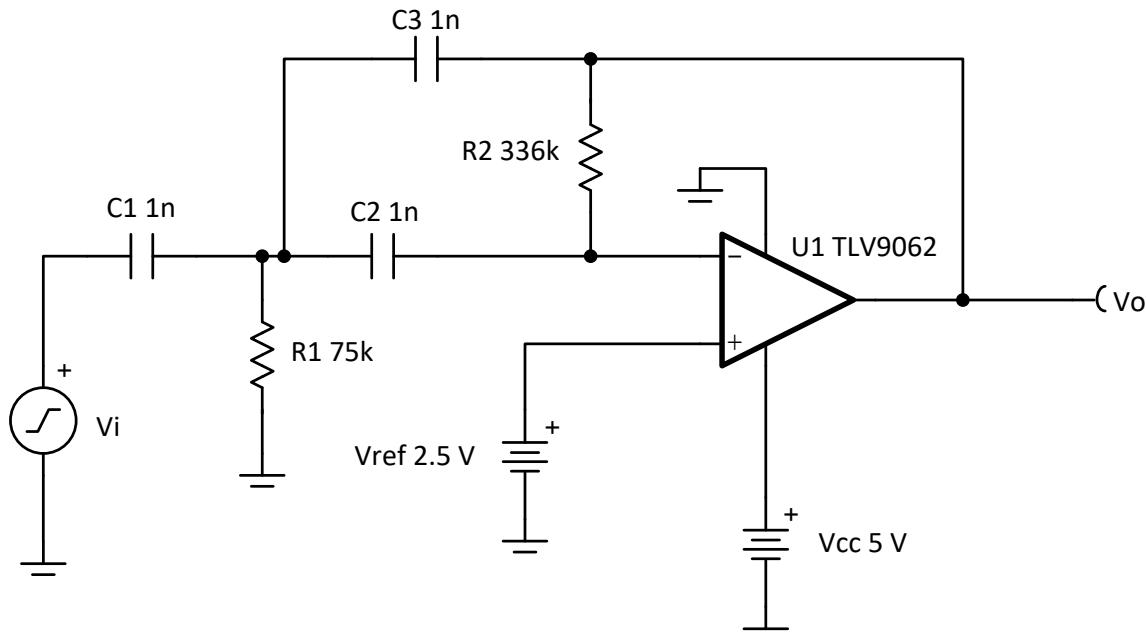


Amplifiers

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
-2.45V	+2.45V	0.05V	4.95V	5V	0V
Gain		Cutoff Frequency (f_c)		Max Frequency (f_{max})	
-1V/V		1kHz		10kHz	
V_{ref}		2.5V			

Design Description

The multiple-feedback (MFB) high-pass (HP) filter is a 2nd-order active filter. V_{ref} provides a DC offset to accommodate for single-supply applications. This HP filter inverts the signal (Gain = -1V/V) for frequencies in the pass band. An MFB filter is preferable when the gain is high or when the Q-factor is large (for example, 3 or greater).



Design Notes

1. Select an op amp with sufficient input common-mode range and output voltage swing.
2. Add V_{ref} to bias the input signal to meet the input common-mode range and output voltage swing.
3. Select the capacitor values first since standard capacitor values are more coarsely subdivided than the resistor values. Use high-precision, low-drift capacitor values to avoid errors in f_c .
4. To minimize the amount of slew-induced distortion, select an op amp with sufficient slew rate (SR).
5. For HP filters, the maximum frequency is set by the gain bandwidth (GBW) of the op amp. Therefore, be sure to select an op amp with sufficient GBW.

Design Steps

The first step in design is to find component values for the normalized cutoff frequency of 1 radian/second. In the second step, the cutoff frequency is scaled to the desired cutoff frequency with scaled component values.

The transfer function for a 2nd-order MFB high pass filter is given by:

$$H(s) = \frac{-s^2 \frac{C_1}{C_3}}{s^2 + s \frac{C_1 + C_2 + C_3}{R_2 \times C_2 \times C_3} + \frac{1}{R_1 \times R_2 \times C_2 \times C_3}}$$

$$H(s) = \frac{-s^2 \frac{C_1}{C_3}}{s^2 + a_1 \times s + a_0}$$

$$\text{Here, } a_1 = \frac{C_1 + C_2 + C_3}{R_2 \times C_2 \times C_3}, \quad a_0 = \frac{1}{R_1 \times R_2 \times C_2 \times C_3} \quad (3)$$

- Set normalized values of C_1 , C_2 , and C_3 (C_{1n} , C_{2n} , and C_{3n}) and calculate normalized values of R_1 and R_2 (R_{1n} and R_{2n}) by setting w_c to 1 radian/sec (or $f_c = 1 / (2 \times \pi) \text{Hz}$). For a 2nd-order Butterworth filter, (see the *Butterworth Filter Table* in the [Active Low-Pass Filter Design Application Report](#)).

$$\omega_c = 1 \frac{\text{radian}}{\text{second}} \rightarrow a_0 = 1, a_1 = \sqrt{2}, \text{ let } C_{1n} = C_{2n} = C_{3n} = 1 \text{ F}$$

$$\text{Then } R_{1n} \times R_{2n} = 1 \text{ or } R_{2n} = \frac{1}{R_{1n}}, \quad a_1 = \frac{3}{R_{2n}} = \sqrt{2}$$

$$\therefore R_{2n} = 2.1213, \quad R_{1n} = \frac{1}{R_{2n}} = 0.4714$$

- Scale the component values and cutoff frequency. The resistor values are very small and capacitors values are unrealistic, hence these have to be scaled. The cutoff frequency is scaled from 1 radian/sec to w_0 . If we assume m to be the scaling factor, increase the resistors by m times, then the capacitor values have to decrease by $1/m$ times to keep the same cutoff frequency of 1 radian/sec. If we scale the cutoff frequency to be w_0 then the capacitor values have to be decreased by $1/w_0$. The component values for the design goals are calculated in step 3 and 4.

$$R_1 = R_{1n} \times m = (0.4714 \times m), \quad R_2 = R_{2n} \times m = (2.1213 \times m)$$

$$C_1 = \frac{C_{1n}}{m \times \omega_0} = \frac{1}{m \times \omega_0} \text{F}$$

$$C_2 = \frac{C_{2n}}{m \times \omega_0} = \frac{1}{m \times \omega_0} \text{F}$$

$$C_3 = \frac{C_{3n}}{m \times \omega_0} = \frac{1}{m \times \omega_0} \text{F}$$

3. Set C_1 , C_2 , and C_3 to 1nF and calculate m .

Given $\omega_0 = 2 \times \pi \times f_c$, where $f_c = 1\text{kHz}$,

$$C_1 = C_2 = C_3 = \frac{1}{m \times \omega_0} F = \frac{1}{m \times 2 \times \pi \times 1\text{kHz}}$$

So, $m = 159155$

4. Calculate R_1 and R_2 based on m .

$$R_1 = R_{1n} \times m = 0.4714 \times 159155 \approx 75\text{k}\Omega \text{ (Standard Value)}$$

$$R_2 = R_{2n} \times m = 2.1213 \times 159155 \approx 336\text{k}\Omega \text{ (Standard Value)}$$

5. Calculate minimum required GBW and SR for f_{\max} . Be sure to use the noise gain for GBW calculations. Do not use the signal gain of -1V/V .

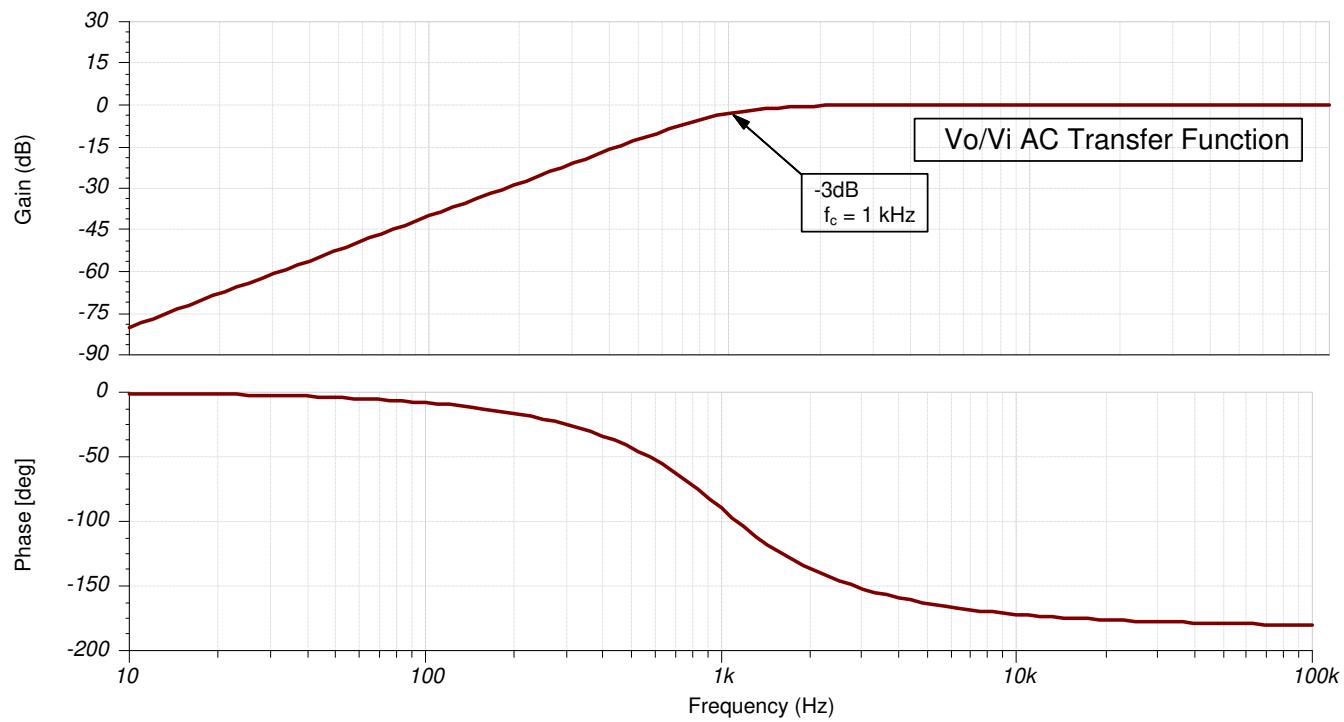
$$\text{GBW} = 100 \times \text{Noise Gain} \times f_{\max} = 100 \times 2 \times 10\text{kHz} = 2\text{MHz}$$

$$\text{SR} = 2 \times \pi \times f_{\max} \times V_{iMax} = 2 \times \pi \times 10\text{kHz} \times 2.45\text{V} = 0.154 \frac{\text{V}}{\mu\text{s}}$$

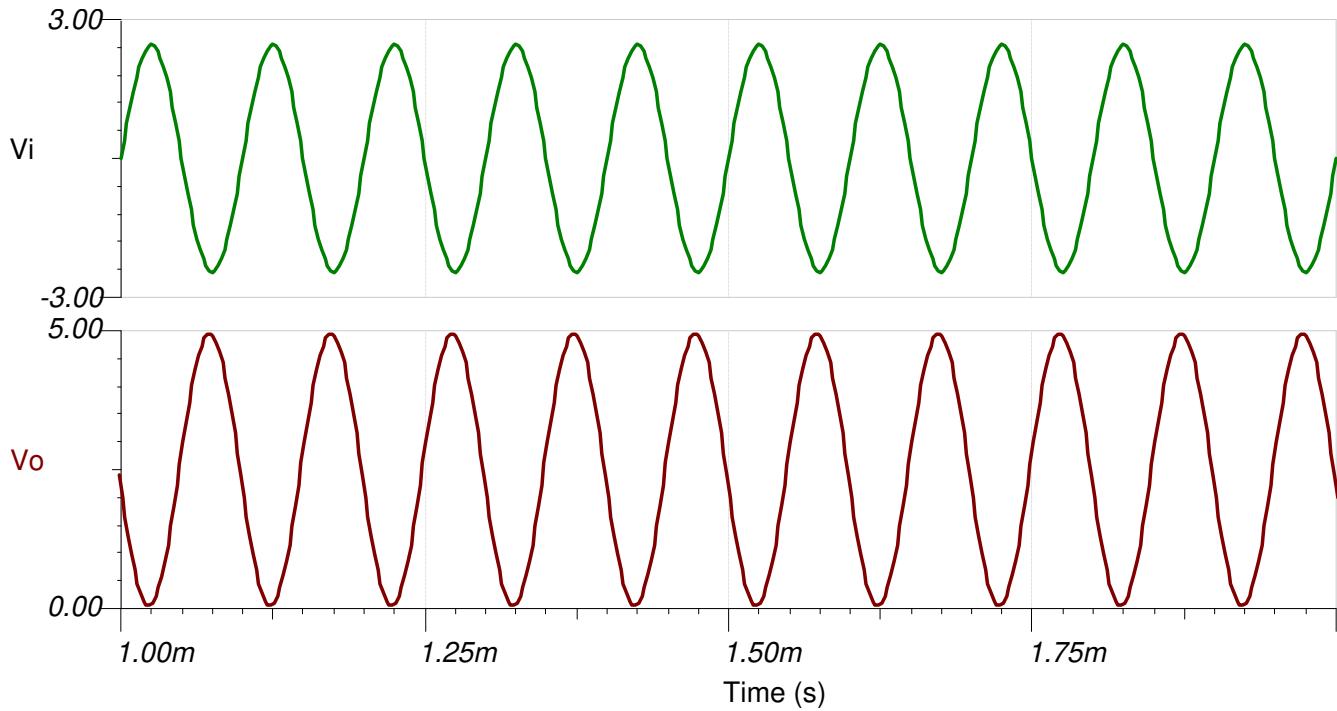
The TLV9062 device has GBW of 10MHz and SR of 6.5V/ μs , so the requirements are met.

Design Simulations

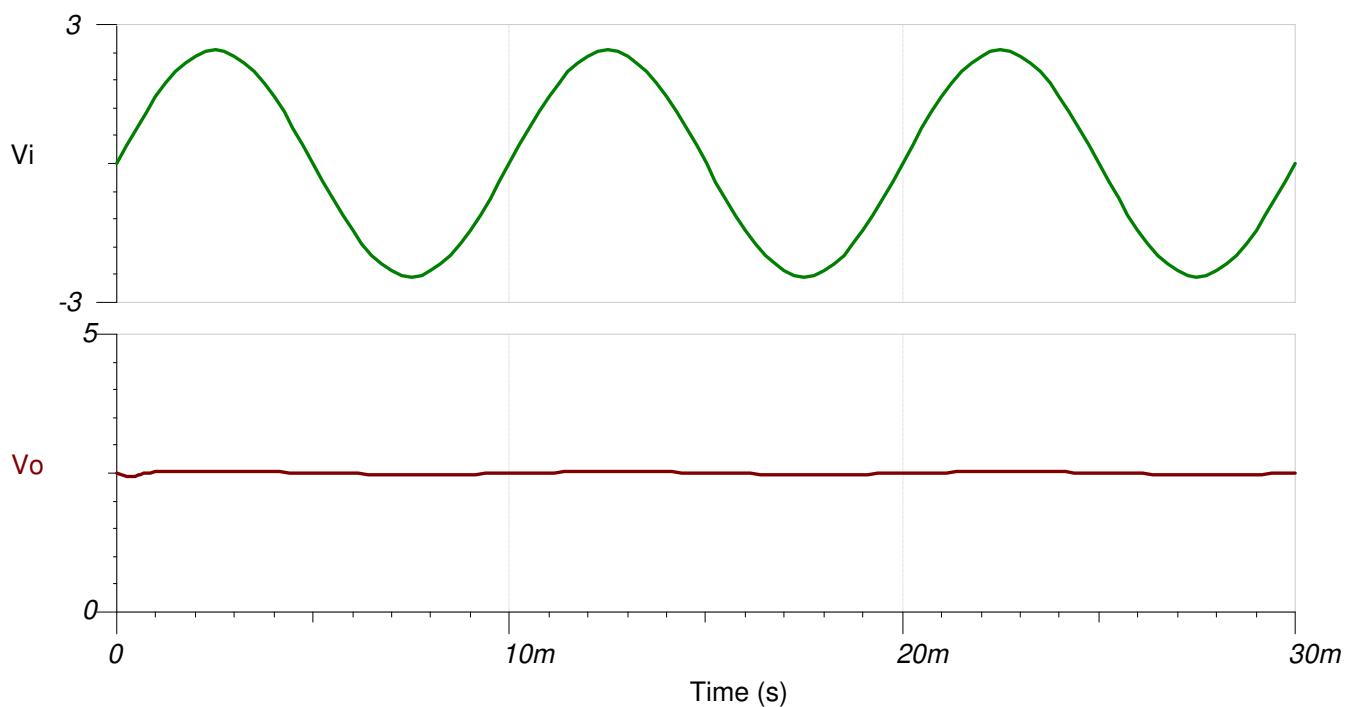
AC Simulation Results



Transient Simulation Results



Filter Output in Response to a 5-V_{pp}, 10-kHz Input-Signal (Gain = -1V/V).



Filter Output in Response to a 5-V_{pp}, 100-Hz Input-Signal (Gain = -0.01V/V)

Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.
2. SPICE Simulation File: [SBOC599](#).
3. [TI Precision Labs](#).
4. [Active Low-Pass Filter Design Application Report](#)

Design Featured Op Amp

TLV9062	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-Rail
V_{out}	Rail-to-Rail
V_{os}	0.3mV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

	TLV316	OPA325
V_{ss}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-Rail	Rail-to-Rail
V_{out}	Rail-to-Rail	Rail-to-Rail
V_{os}	0.75mV	0.150mV
I_q	400µA	650µA
I_b	10pA	0.2pA
UGBW	10MHz	10MHz
SR	6V/µs	5V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/TLV316	www.ti.com/product/OPA325

Analog Engineer's Circuit

Single-supply, 2nd-order, multiple feedback band-pass filter circuit

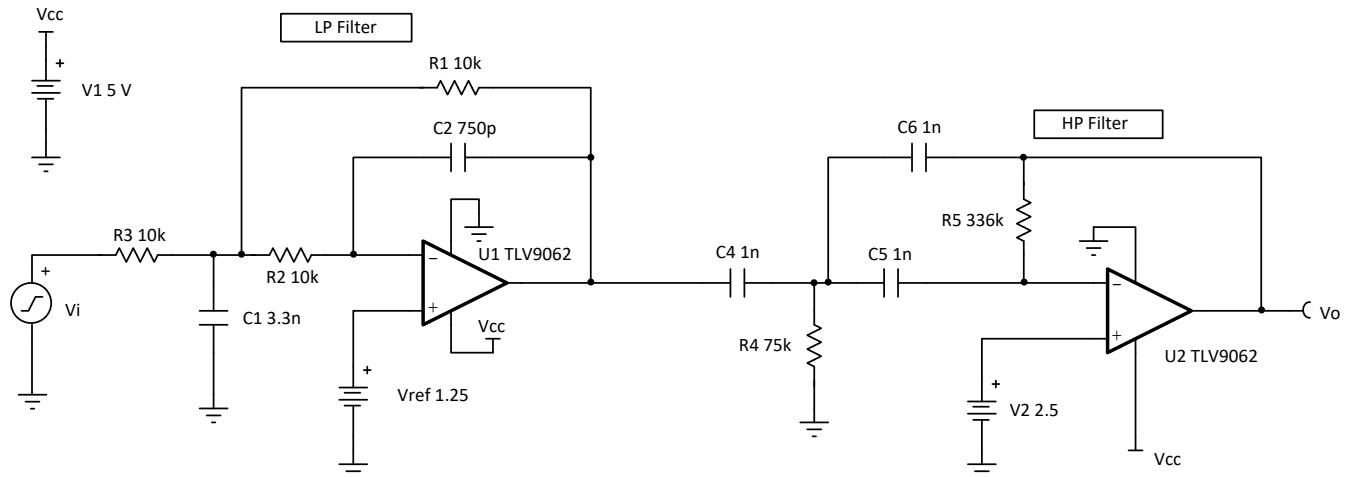


Amplifiers

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
-2.45V	+2.45V	0.05V	4.95V	5V	0V
Gain		Low Cut-off Frequency (f_l)		High Cut-off Frequency (f_h)	
1V/V		1kHz		10kHz	
V_{ref}		1.25V and 2.5V			

Design Description

This circuit is a 2nd-order multiple feedback (MFB) band-pass (BP) filter. This BP filter is created by cascading a low-pass and a high-pass filter. V_{ref} provides a DC offset to accommodate for single-supply applications.



Design Notes

1. Select an op amp with sufficient input common-mode range and output voltage swing.
2. Add V_{ref} to bias the input signal to meet the input common-mode range and output voltage swing.
3. Select the capacitor values first since standard capacitor values are more coarsely subdivided than the resistor values. Use high-precision, low-drift capacitor values to avoid errors in f_l and f_h .
4. To minimize the amount of slew-induced distortion, select an op amp with sufficient slew rate (SR).
5. For HP filters the maximum frequency is set by the gain bandwidth (GBW) of the op amp. Therefore, be sure to select an op amp with sufficient GBW.

Design Steps

This BP filter design involves two cascaded filters, a low-pass (LP) filter and a high-pass (HP) filter. The lower cutoff frequency (f_l) of the BP filter is 1kHz and the higher cutoff frequency (f_h) is 10kHz. The design steps show an LP filter design with f_h of 10kHz and a HP filter design with f_l of 1kHz. See [MFB low-pass filter design](#) and [MFB high-pass filter design](#) in the circuit cookbook for details on transfer function equations and calculations.

LP Filter Design

1. Use [MFB low-pass filter design](#) to determine R_1 , R_2 , and R_3 .

$$\begin{aligned} R_1 &= 10\text{k}\Omega, \\ R_2 &= 10\text{k}\Omega, \\ R_3 &= 10\text{k}\Omega \end{aligned}$$

2. Use [MFB low-pass filter design](#) to determine C_1 and C_2 .

$$C_1 = 3.3\text{nF} \text{ (Standard Value)}, C_2 = 750\text{pF} \text{ (Standard Value)}$$

HP Filter Design

1. Use [MFB high-pass filter design](#) to determine C_4 , C_5 , and C_6 .

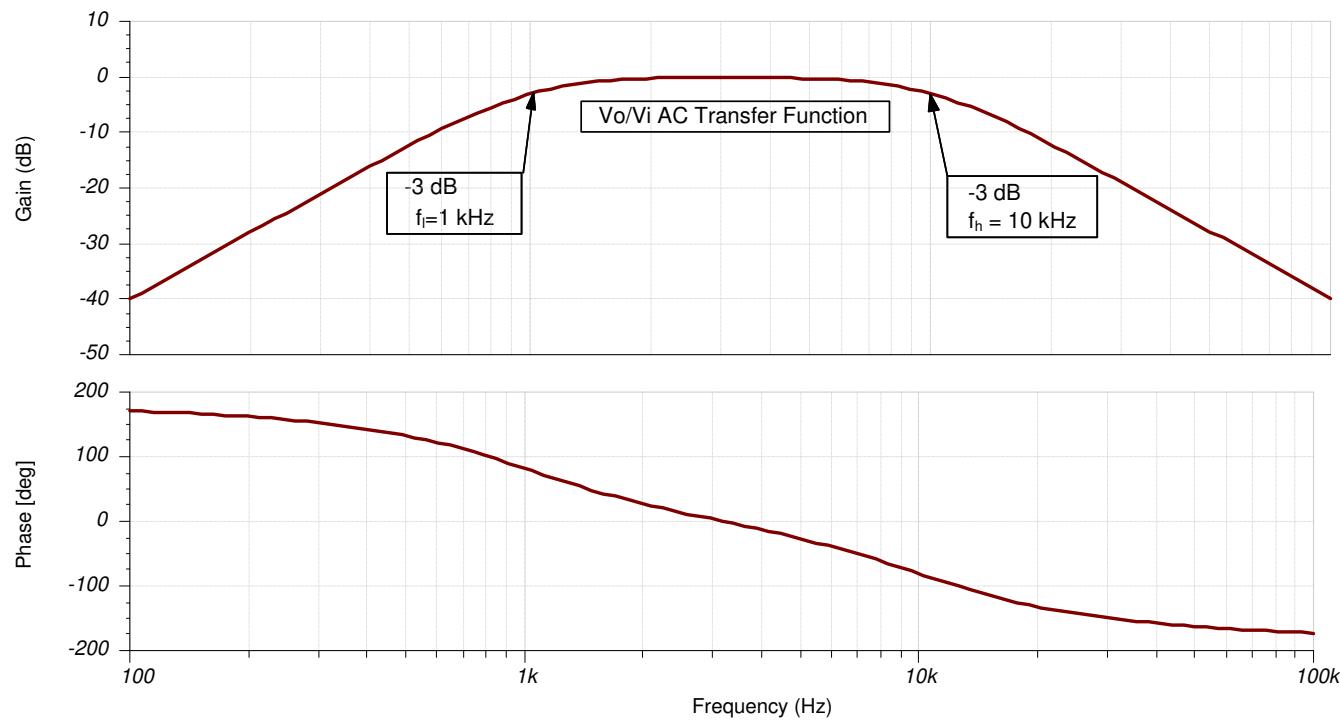
$$\begin{aligned} C_4 &= 1\text{nF}, \\ C_5 &= 1\text{nF}, \\ C_6 &= 1\text{nF} \end{aligned}$$

2. Use [MFB high-pass filter design](#) to determine R_4 and R_5 .

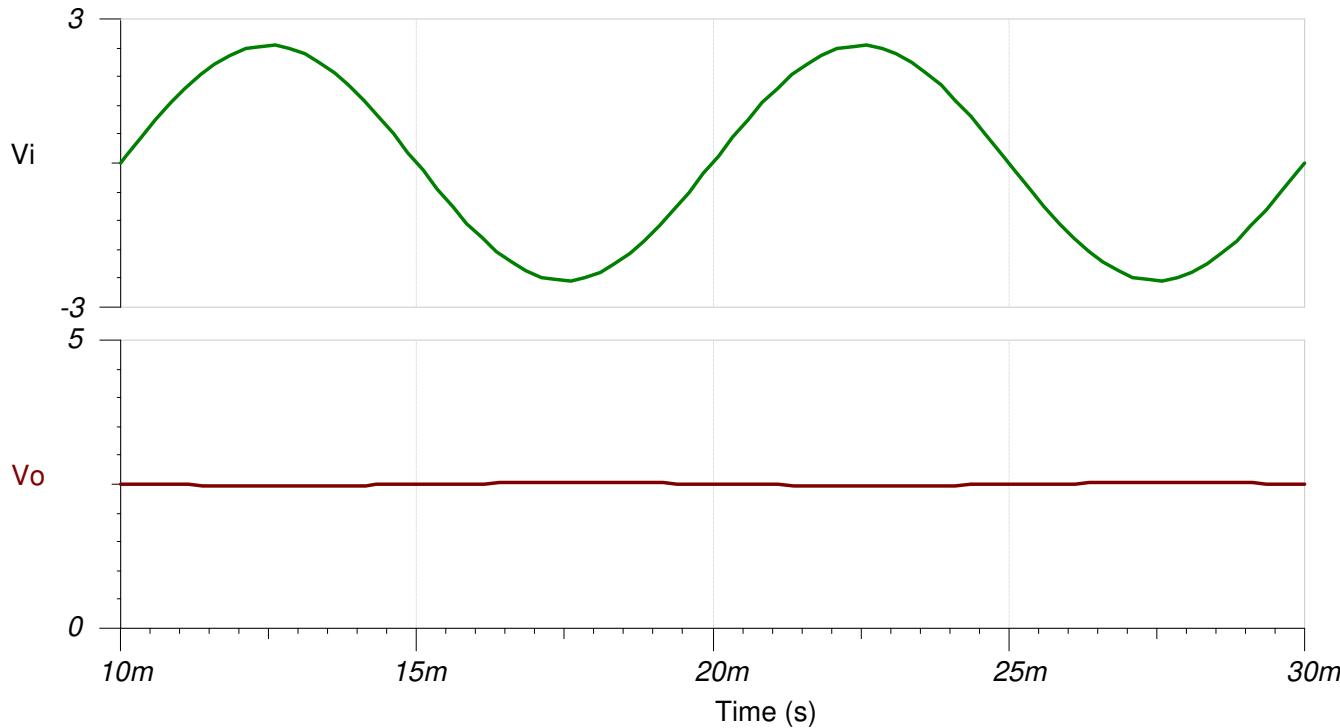
$$\begin{aligned} R_4 &= 75\text{k}\Omega, \\ R_5 &= 336\text{k}\Omega \end{aligned}$$

Design Simulations

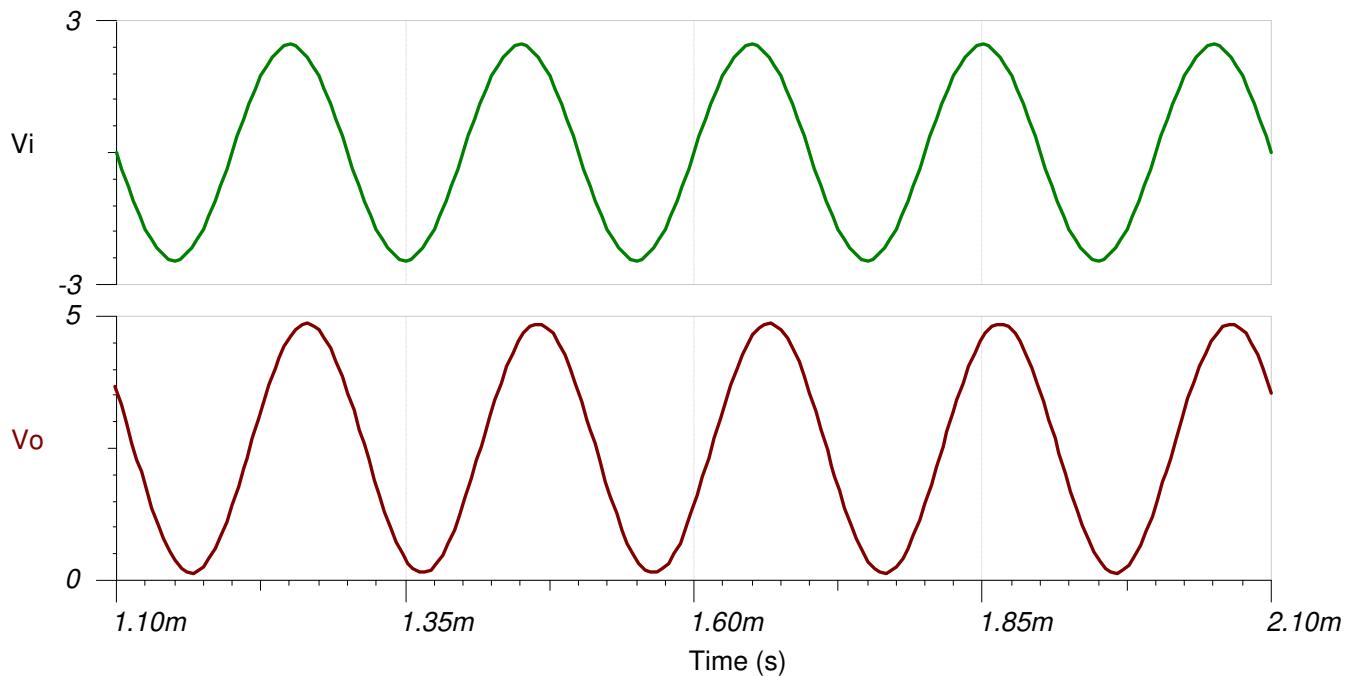
AC Simulation Results



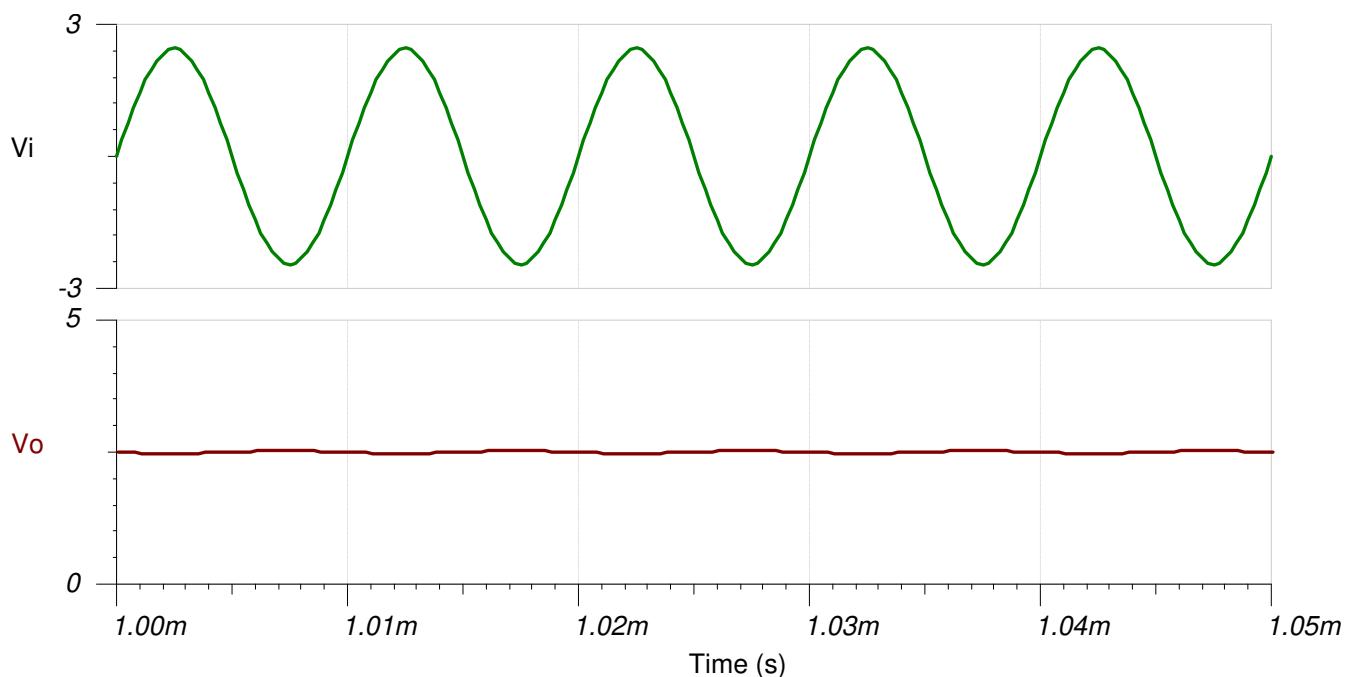
Transient Simulation Results



Filter Ouput in Response to a 5-Vpp, 100-Hz Input Signal (Gain = 0.01V/V)



Filter Ouput in Response to a 5-Vpp, 5-kHz Input Signal (Gain = 1V/V)



Filter Ouput in Response to a 5-Vpp, 100-kHz Input Signal (Gain = 0.01V/V)

Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.
2. SPICE Simulation File: [SBOC596](#).
3. [TI Precision Labs](#).

Design Featured Op Amp

TLV9062	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-Rail
V_{out}	Rail-to-Rail
V_{os}	0.3mV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

	TLV316	OPA325
V_{ss}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-Rail	Rail-to-Rail
V_{out}	Rail-to-Rail	Rail-to-Rail
V_{os}	0.75mV	0.150mV
I_q	400µA	650µA
I_b	10pA	0.2pA
UGBW	10MHz	10MHz
SR	6V/µs	5V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/TLV316	www.ti.com/product/OPA325

Fast-Settling Low-Pass Filter Circuit

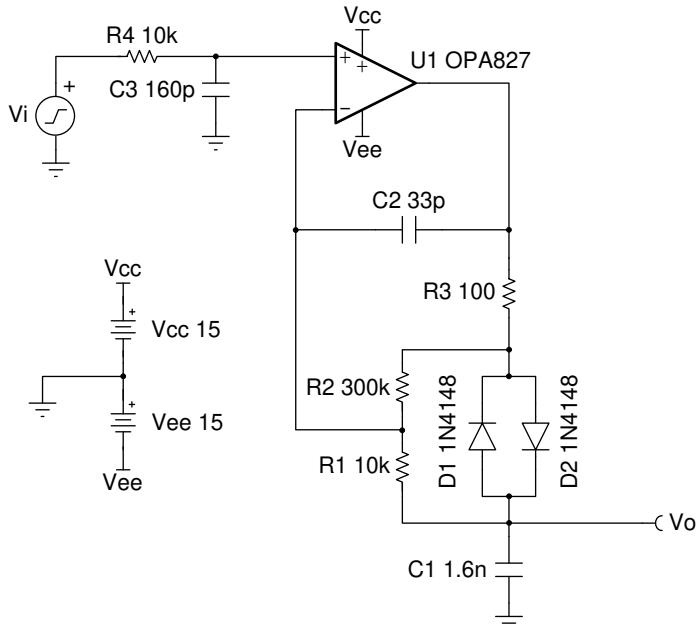


Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
-12 V	12 V	-12 V	12 V	15 V	-15 V
Cutoff Frequency (f_c)			Diode Threshold Voltage (V_t)		
10 kHz			20 mV		

Design Description

This low-pass filter topology offers a significant improvement in settling time over the conventional single-pole RC filter. This is achieved through the use of diodes D₁ and D₂, that allow the filter capacitor to charge and discharge much faster when there is a large enough difference between the input and output voltages.



Design Notes

1. Observe the common-mode input limitations of the op amp.
2. Keeping C₁ small will ensure the op amp does not struggle to drive the capacitive load.
3. For the fastest settling time, use fast switching diodes.
4. The selected op amp should have sufficient output drive capability to charge C₁. R₃ limits the maximum charge current.

Design Steps

1. Select standard values for R_1 and C_1 based on $f_C = 10\text{kHz}$.

$$R_1 = 10\text{k}\Omega$$

$$C_1 = \frac{1}{2\pi \times f_C \times R_1} = \frac{1}{2\pi \times 10\text{kHz} \times 10\text{k}\Omega} = 1.6\text{nF}$$

2. Set the diode threshold voltage (V_t). This threshold is the minimum difference in voltage between the input and output that will result in diode conduction (fast capacitor charging and discharging).

$$V_t = \frac{V_f}{1 + \frac{R_2}{R_1}} \approx \frac{0.6V}{1 + \frac{R_2}{R_1}} = 20\text{mV}$$

$$R_2 = \left(\frac{0.6V}{20\text{mV}} - 1 \right) \times R_1 = 290\text{k}\Omega \approx 300\text{k}\Omega \text{ (standard 5% value)}$$

3. Select components for noise pre-filtering.

$$f_{c2} = 10 \times f_C = 100\text{kHz}$$

$$f_{c2} = \frac{1}{2\pi \times R_4 \times C_3}$$

$$\text{Select } R_4 = R_1 = 10\text{k}\Omega$$

$$C_3 = \frac{C_1}{10} = 160\text{pF}$$

4. Add compensation components to stabilize U₁. R₃ limits the charge current into C₁ and also serves to isolate the capacitance from the op amp output when the diodes are conducting. Larger values will improve stability but increase C₁ charge time.

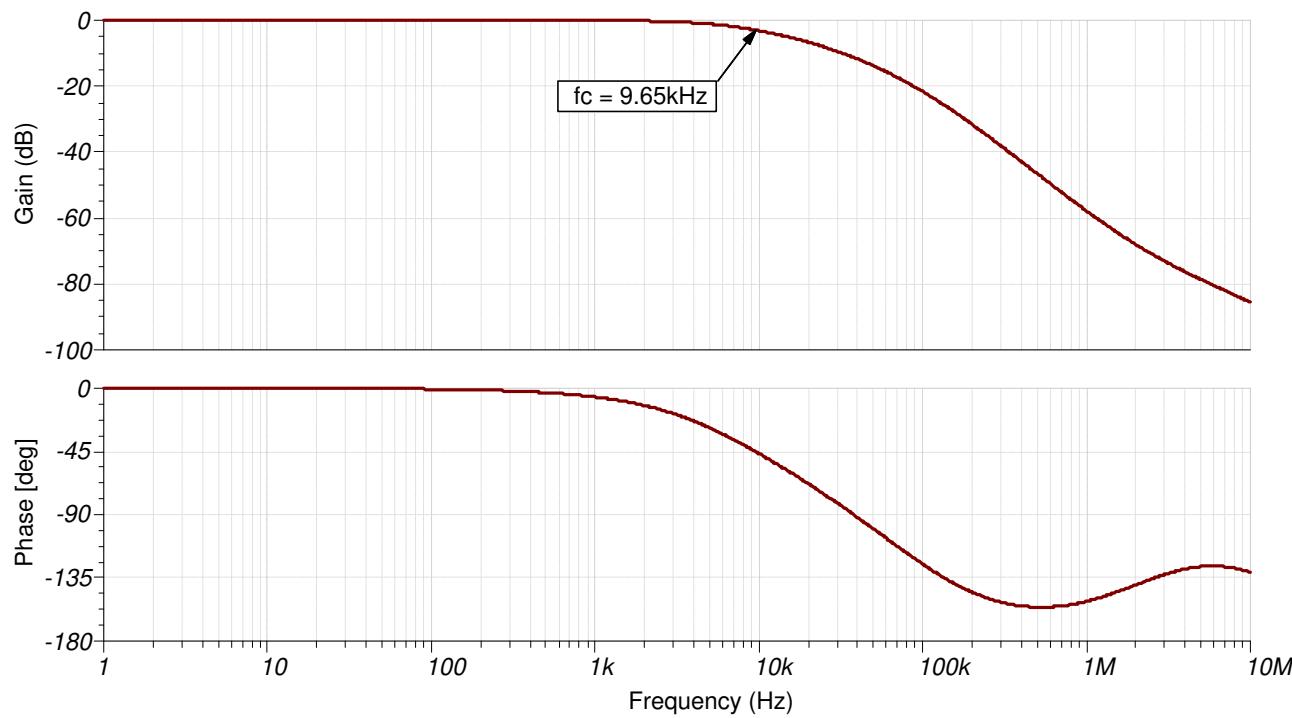
$$\text{Select } R_3 = 100\Omega$$

5. C₂ provides local high frequency feedback to counteract the interaction between the input capacitance with the parallel combination of R₁ and R₂. To prevent interaction with C₁, select C₂ as the following shows:

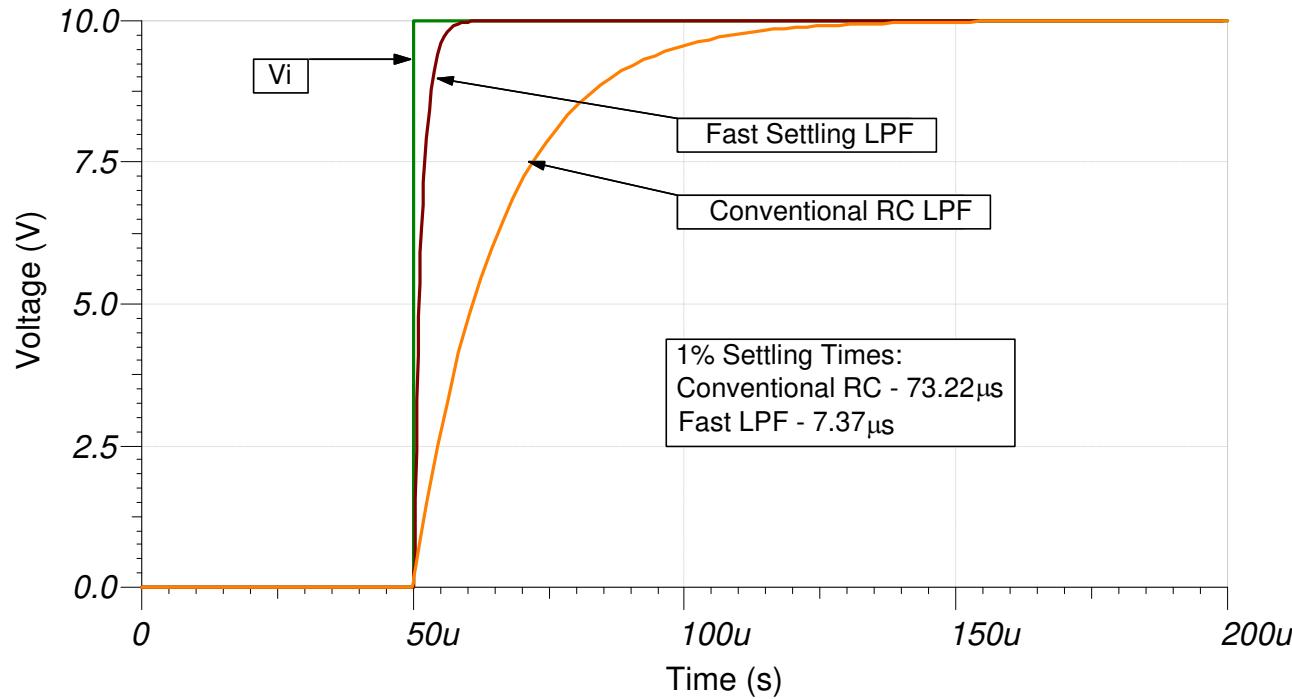
$$\text{Select } C_2 = \frac{C_1}{50} = 32\text{pF} \approx 33\text{pF} \text{ (standard value)}$$

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See TINA-TI™ circuit simulation file, [SBOMAU1](#).

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC, see [TI Precision Labs](#).

Design Featured Op Amp

OPA827	
V_{ss}	8 V to 36 V
V_{inCM}	V _{ee} +3 V to V _{cc} -3 V
V_{out}	V _{ee} +3 V to V _{cc} -3 V
V_{os}	75 μ V
I_q	4.8 mA
I_b	3 pA
UGBW	22 MHz
SR	28 V/ μ s
#Channels	1
OPA827	

Design Alternate Op Amp

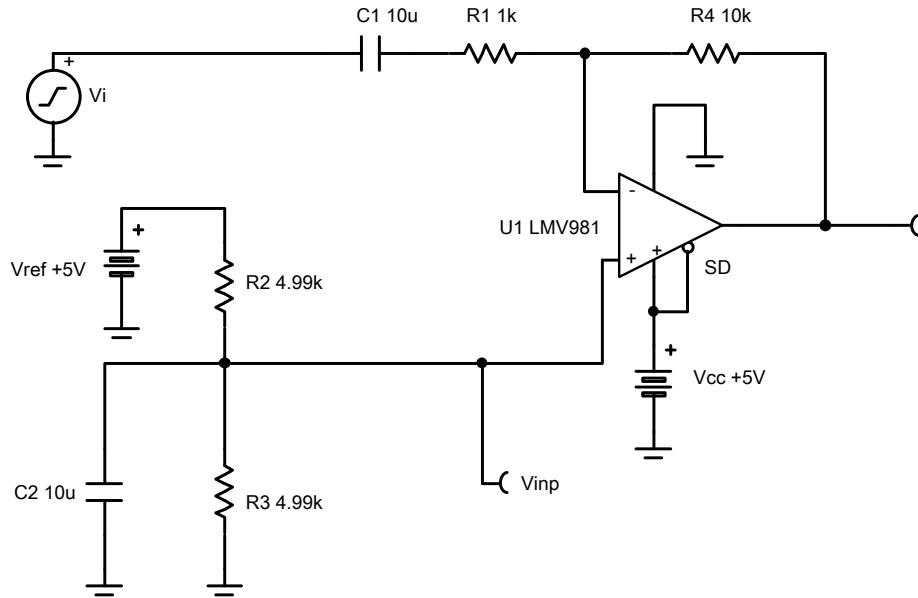
TLC072	
V_{ss}	4.5 V to 16 V
V_{inCM}	V _{ee} +0.5 V to V _{cc} -0.8 V
V_{out}	V _{ee} +350 mV to V _{cc} -1 V
V_{os}	390 μ V
I_q	2.1 mA/Ch
I_b	1.5 pA
UGBW	10 MHz
SR	16 V/ μ s
#Channels	1, 2, and 4
TLC072	

AC Coupled (HPF) Inverting Amplifier Circuit**Design Goals**

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	V_{cc}	V_{ee}	V_{ref}
-240 mV	240 mV	0.1 V	4.9 V	5 V	0 V	5 V

Design Description

This circuit amplifies an AC signal and shifts the output signal so that it is centered at half the power supply voltage. Note that the input signal has zero DC offset so it swings above and below ground. The key benefit of this circuit is that it accepts signals which swing below ground even though the amplifier does not have a negative power supply.

**Design Notes**

1. R_1 sets the AC input impedance. R_4 loads the op amp output.
2. Use low feedback resistances to reduce noise and minimize stability concerns.
3. Set the output range based on linear output swing (see A_{ol} specification).
4. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to R_4 . Adding a capacitor in parallel with R_4 will also improve stability of the circuit if high-value resistors are used.

Design Steps

1. Select R_1 and R_4 to set the AC voltage gain.

$$R_1 = 1 \text{ k}\Omega \text{ (Standard Value)}$$

$$R_4 = R_1 \times |G_{ac}| = 1 \text{ k}\Omega \times |-10\frac{V}{V}| = 10\text{k}\Omega \text{ (Standard Value)}$$

2. Select R_2 and R_3 to set the DC output voltage to 2.5 V.

$$R_3 = 4.99\text{k}\Omega \text{ (Standard Value)}$$

$$R_2 = \frac{R_3 \times V_{ref}}{V_{DC}} - R_3 = \frac{4.99\text{k}\Omega \times 5\text{V}}{2.5\text{V}} - 4.99\text{k}\Omega = 4.99\text{k}\Omega$$

3. Choose a value for the lower cutoff frequency, f_l , then calculate C_1 .

$$f_l = 16\text{Hz}$$

$$C_1 = \frac{1}{2 \times \pi \times R_1 \times f_l} = \frac{1}{2 \times \pi \times 1 \text{ k}\Omega \times 16\text{Hz}} = 9.94\mu\text{F} \approx 10\mu\text{F} \text{ (Standard Value)}$$

4. Choose a value for f_{div} , then calculate C_2 .

$$f_{div} = 6.4\text{Hz}$$

$$R_{div} = \frac{R_2 \times R_3}{R_2 + R_3} = \frac{4.99\text{k}\Omega \times 4.99\text{k}\Omega}{4.99\text{k}\Omega + 4.99\text{k}\Omega} = 2.495\text{k}\Omega$$

$$C_2 = \frac{1}{2 \times \pi \times R_{div} \times f_{div}} = \frac{1}{2 \times \pi \times 2.495\text{k}\Omega \times 6.4\text{Hz}} = 9.96\mu\text{F} \approx 10\mu\text{F} \text{ (Standard Value)}$$

5. The upper cutoff frequency, f_h , is set by the noise gain of this circuit and the gain bandwidth (GBW) of the device (LMV981).

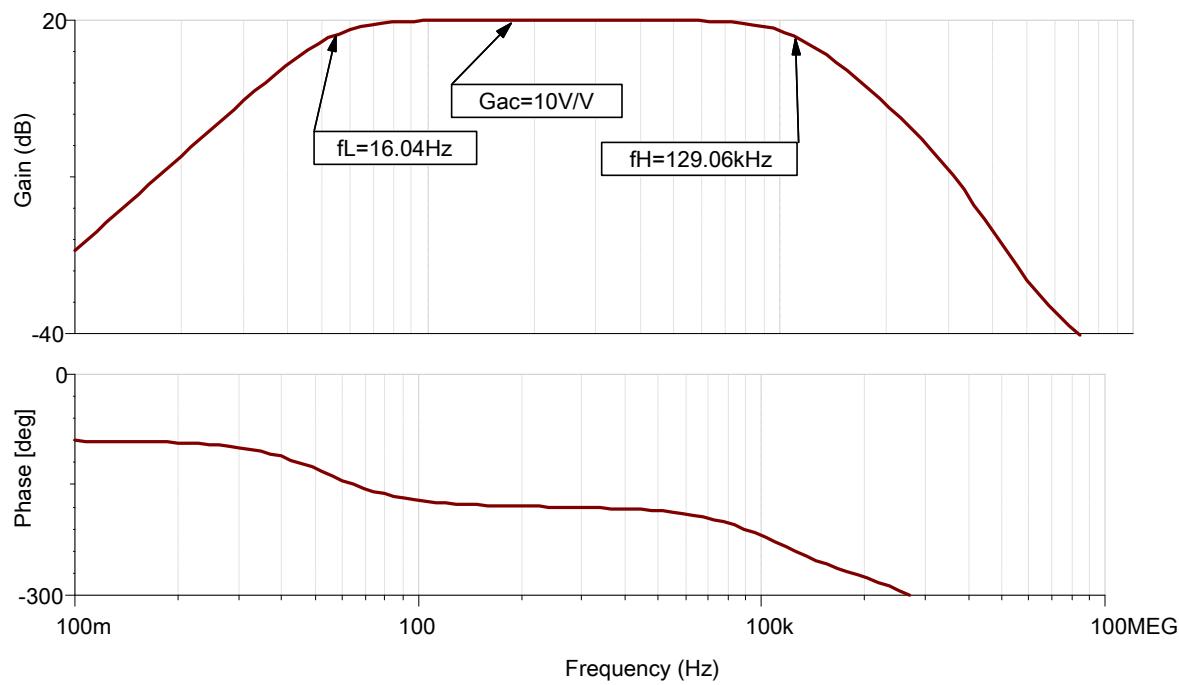
$$\text{GBW} = 1.5\text{MHz}$$

$$G_{noise} = 1 + \frac{R_4}{R_1} = 1 + \frac{10\text{k}\Omega}{1\text{k}\Omega} = 11\frac{V}{V}$$

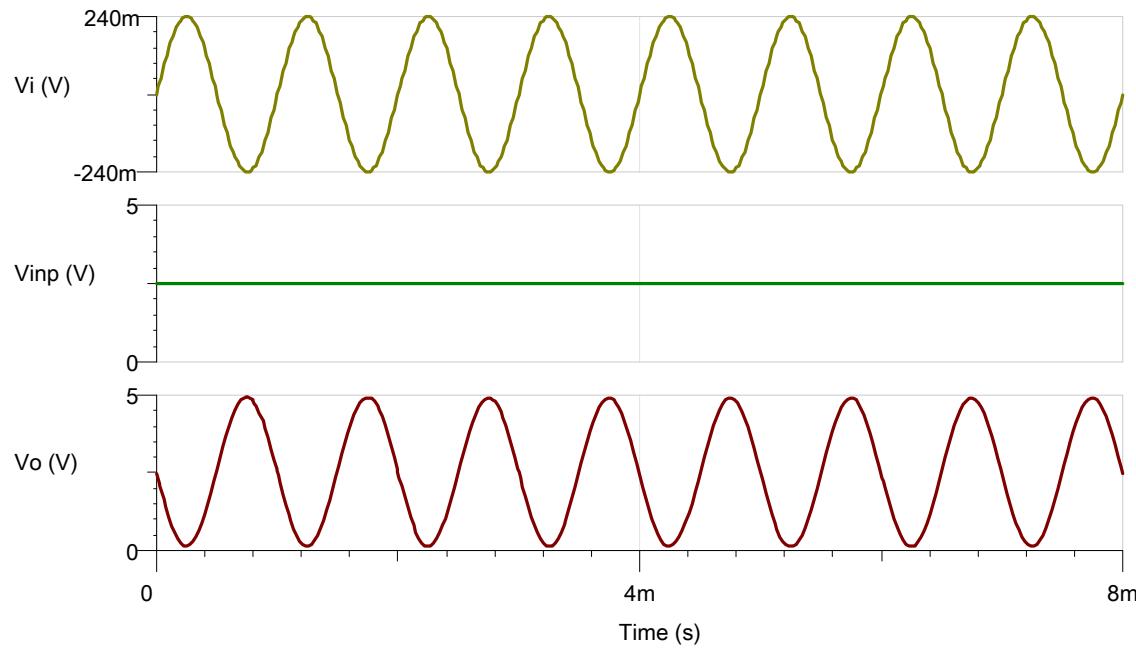
$$f_h = \frac{\text{GBW}}{G_{noise}} = \frac{1.5\text{MHz}}{11\frac{V}{V}} = 136.3\text{kHz}$$

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC504](#).

See [TIPD185](#).

Design Featured Op Amp

LMV981	
V_{cc}	1.8 V to 5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1 mV
I_q	116 μ A
I_b	14 nA
UGBW	1.5 MHz
SR	0.42 V/ μ s
#Channels	1 and 2
LMV981	

Design Alternate Op Amp

LMV771	
V_{cc}	2.7 V to 5 V
V_{inCM}	V_{ee} to (V_{cc} -0.9 V)
V_{out}	Rail-to-rail
V_{os}	0.25 mV
I_q	600 μ A
I_b	-0.23 pA
UGBW	3.5 MHz
SR	1.5 V/ μ s
#Channels	1 and 2
LMV771	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 1, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.....[1](#)

Band Pass Filtered Inverting Attenuator Circuit

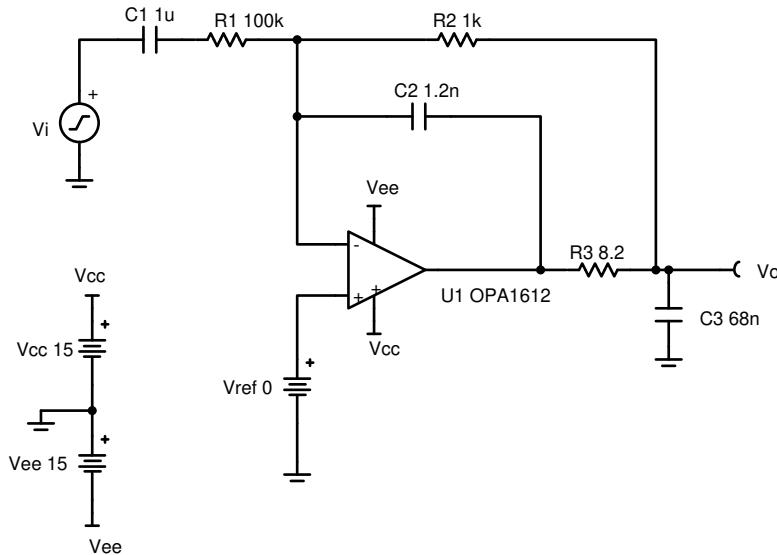


Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	V_{cc}	V_{ee}	V_{ref}
100 mV _{pp}	50 V _{pp}	1m V _{pp}	500 mV _{pp}	15 V	-15 V	0 V

Design Description

This tunable band-pass attenuator reduces signal level by -40 dB over the frequency range from 10 Hz to 100 kHz. It also allows for independent control of the DC output level. For this design, the pole frequencies were selected outside the pass band to minimize attenuation within the specified bandwidth range.



Design Notes

1. If a DC voltage is applied to V_{ref} be sure to check common mode limitations.
2. Keep R_3 as small as possible to avoid loading issues while maintaining stability.
3. Keep the frequency of the second pole in the low-pass filter (f_{p3}) at least twice the frequency of the first low-pass filter pole (f_{p2}).

Design Steps

- Set the passband gain.

$$\text{Gain} = -\frac{R_2}{R_1} = -0.01 \frac{V}{V} (-40\text{dB})$$

$$R_1 = 100\text{k}\Omega$$

$$R_2 = 0.01 \times R_1 = 1 \text{ k}\Omega$$

- Set high-pass filter pole frequency (f_{p1}) below f_l .

$$f_l = 10\text{Hz}, f_{p1} = 2.5 \text{ Hz}$$

- Set low-pass filter pole frequency (f_{p2} and f_{p3}) above f_h .

$$f_h = 100\text{kHz}$$

$$f_{p2} = 150\text{kHz}$$

$$f_{p3} \geq 2 \times f_{p2} = 300\text{kHz}$$

$$f_{p3} = 300\text{kHz}$$

- Calculate C_1 to set the location of f_{p1} .

$$C_1 = \frac{1}{2\pi \times R_1 \times f_{p1}} = \frac{1}{2\pi \times 100\text{k}\Omega \times 2.5\text{Hz}} = 0.636 \mu\text{F} \approx 1 \mu\text{F} \text{ (Standard Value)}$$

- Select components to set f_{p2} and f_{p3} .

$$R_3 = 8.2\Omega \text{ (provides stability for cap loads up to } 100\text{nF})$$

$$C_2 = \frac{1}{2\pi \times (R_2 + R_3) \times f_{p2}} = \frac{1}{2\pi \times 1008.2\Omega \times 150\text{kHz}} \\ = 1052\text{pF} \approx 1200\text{pF} \text{ (Standard Value)}$$

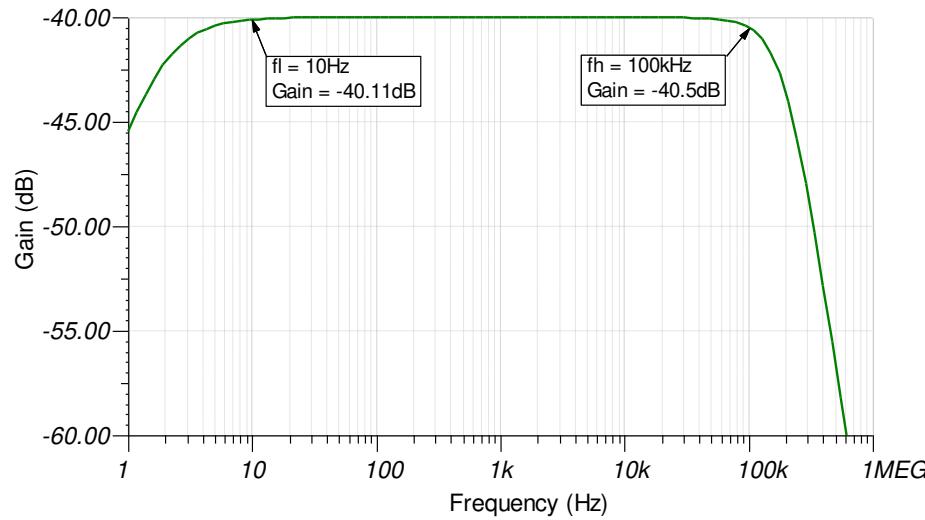
$$C_3 = \frac{1}{2\pi \times R_3 \times f_{p3}} = \frac{1}{2\pi \times 8.2\Omega \times 300\text{kHz}} = 64.7 \text{ nF} \approx 68\text{nF} \text{ (Standard Value)}$$

Design Simulations

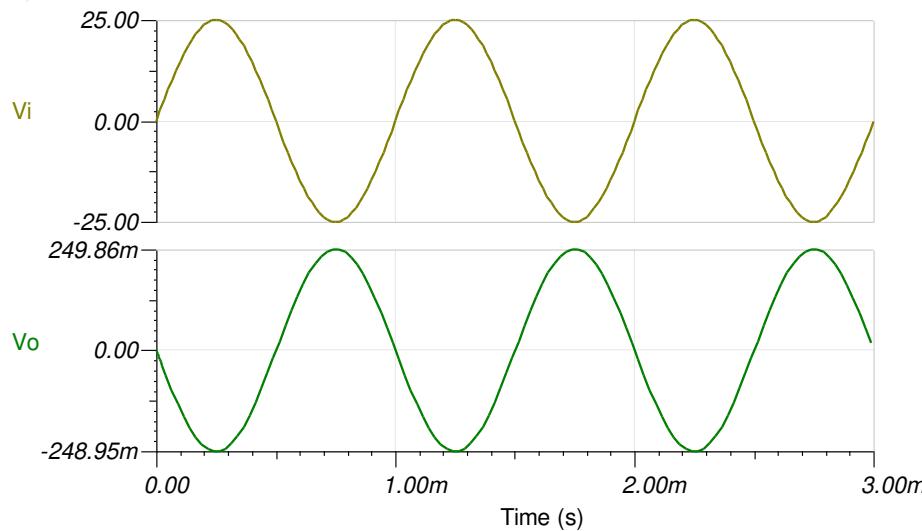
DC Simulation Results

The amplifier will pass DC voltages applied to the noninverting pin up to the common mode limitations of the op amp (± 13 V in this design)

AC Simulation Results



Transient Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC503](#).

See [TIPD118](#).

Design Featured Op Amp

OPA1612	
V_{ss}	4.5 V to 36 V
V_{inCM}	V _{ee} +2 V to V _{cc} -2 V
V_{out}	V _{ee} +0.2 V to V _{cc} -0.2 V
V_{os}	100 μ V
I_q	3.6 mA/Ch
I_b	60 nA
UGBW	40 MHz
SR	27 V/ μ s
#Channels	1 and 2
OPA1612	

Design Alternate Op Amp

OPA172	
V_{ss}	4.5 V to 36 V
V_{inCM}	V _{ee} -100 mV to V _{cc} -2 V
V_{out}	Rail-to-rail
V_{os}	200 μ V
I_q	1.6 mA/Ch
I_b	8 pA
UGBW	10 MHz
SR	10 V/ μ s
#Channels	1, 2, and 4
OPA172	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from July 31, 2017 to February 1, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.....[1](#)

Analog Engineer's Circuit

Circuit to measure multiple redundant source currents with singled-ended signal

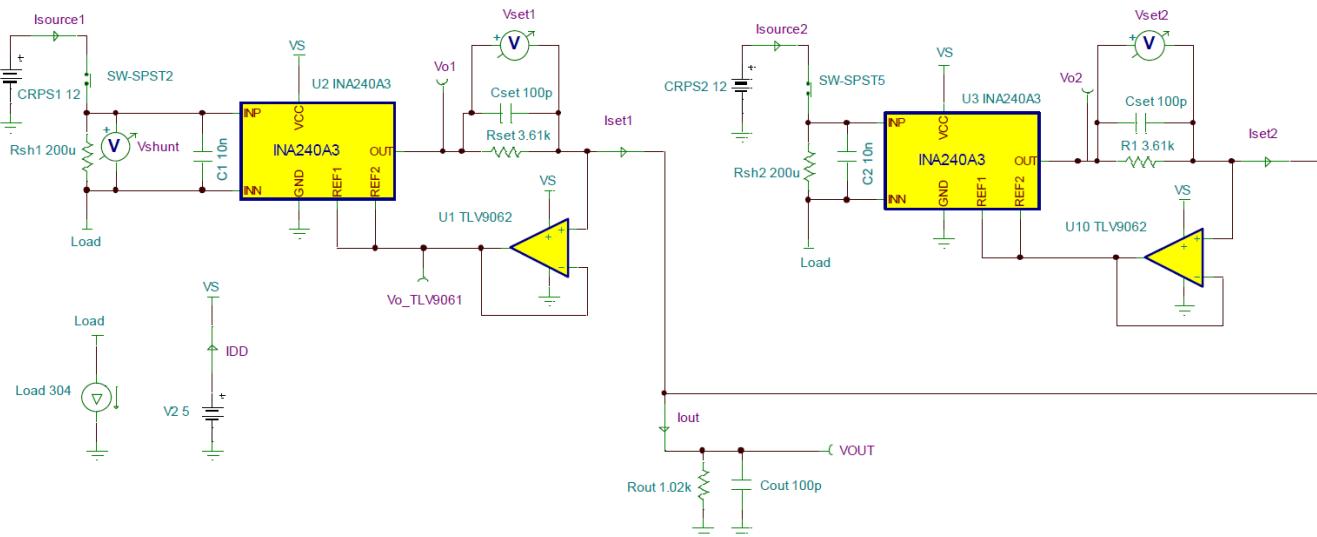


Amplifiers

Input			Output			Error	Supply		
I _{LOAD} Min	I _{LOAD} Max	V _{CM}	I _{OUT} Min	I _{OUT} Max	Bandwidth	I _{LOAD} > 45 A	I _{DD}	V _S	V _{ee}
5A	304A	12V	42.1 μ A	1.6842mA	400kHz	2.1% maximum at full-scale range	$N \times (2.4\text{mA} + 750\mu\text{A}) + I_{\text{OUT}}$		5V GND (0V)

Design Description

This circuit demonstrates how to convert a voltage-output, current-sense amplifier (CSA) into a current-output circuit using the Howland Current Pump method and operational amplifier (op amp). Furthermore, this circuit demonstrates how to design two separate circuits to measure two separate, but redundant supplies powering one load.



Design Notes

1. The [Getting Started with Current Sense Amplifiers](#) video series introduces implementation, error sources, and advanced topics for using current sense amplifiers.
2. Choose precision 0.1% resistors to limit gain error at higher currents.
3. The output current (I_{OUT}) is sourced from the VS supply, which adds to the I_Q of the current sense amplifier.
4. Use the V_{OUT} versus I_{OUT} curve ("claw-curve") of the CSA (INA240A3) to set the I_{OUT} limit during maximum power. If a higher signal current is needed, then add an op amp buffer to the output of the current sense amplifier. A buffer on the output allows for smaller R_{OUT} .
5. For applications with higher bus voltages, simply substitute in a bidirectional current sense amplifier with a higher rated input voltage.
6. The V_{OUT} voltage is the input common-mode voltage (V_{CM}) for the op amp.
7. Offset errors can be calibrated out with one-point calibration given that a known sense current is applied and the circuit is operating in the linear region. Gain error calibration requires a two-point calibration.
8. Include a small feed-forward capacitor (C_{SET}) to increase BW and decrease V_{OUT} settling time to a step response in current. Increasing C_{SET} too much introduces gain peaking in the system gain curve, which results in output overshoot to a step response.
9. Follow best practices for printed-circuit board (PCB) layout according to the data sheet: place the decoupling capacitor close to the VS pin, routing the input traces for IN+ and IN- as a differential pair, and so forth.

Design Steps

1. Choose an available current-sense amplifier (CSA) that meets the common-mode voltage requirement. For this design the INA240A3 is selected.
 - Note that choosing the most optimal CSA for the system requires balancing tradeoffs in CSA offset, CSA gain error, shunt resistor power rating and thus total circuit design could require multiple iterations to achieve the satisfactory error over the entire dynamic range of the load.
2. Determine the maximum output current ($I_{SET_100\%}$) and maximum output swing ($V_{O_ISYS_MAX}$) of the INA240A3. Use the output current vs output voltage curve in the data sheet. For this design, choose the maximum I_{SET} to be 850 μ A with a maximum output swing of $\{Vs - 0.2V\} = 4.8V = V_{O_ISYS_MAX}$.
3. Given the ADC full-scale range ($V_{ADC_FSR} = 1.8V$), the number of sources to measure ($N = 2$), and the maximum CSA output current when the source is at 100% power ($I_{SET_100\%} = 850\mu A$), calculate the maximum allowable R_{OUT} which converts signal current to signal voltage for ADC. For this design $R_{OUT} = 1020 \Omega$ is selected.

$I_{OUT_ISYS_MAX}$ = Total signal current from all N channels when system/load current is at its maximum (304-A).

$I_{SET1_100\%}$ = Signal current from INA240A3 channel 1 when Source 1 is at 100% power (152-A).

$$V_{ADC_FSR} = V_{OUT_ISYS_MAX} < 1.8V$$

$$I_{OUT_ISYS_MAX} = I_{SET1_100\%} + I_{SET2_100\%} = I_{SET_100\%} \times N$$

$$V_{OUT_ISYS_MAX} = I_{OUT_ISYS_MAX} \times R_{OUT}$$

$$\therefore R_{OUT} < \frac{V_{OUT_ISYS_MAX}}{I_{OUT_ISYS_MAX}} = \frac{1.8V}{850\mu A \times 2} = 1058.82\Omega$$

$$\rightarrow R_{OUT} = 1020\Omega, 0.1\%$$

$$\rightarrow V_{OUT_ISYS_MAX} = 1.734V < 1.8V$$

4. Using the following system of equations, we can solve for the minimum allowable R_{SET} . For this design, $R_{SET} = 3610 \Omega$ is selected.

$$\begin{aligned} V_{OUT_I_{SYS_MAX}} &= I_{OUT_I_{SYS_MAX}} \times R_{OUT} \\ V_{OUT_I_{SYS_MAX}} &= V_{O_I_{SYS_MAX}} - V_{SET_100\%} \\ V_{SET_100\%} &= I_{SET_100\%} \times R_{SET} \\ \therefore R_{SET} &\geq \frac{V_{O_I_{SYS_MAX}} - I_{SET_100\%} \times R_{OUT} \times N}{I_{SET_100\%}} \\ \therefore R_{SET} &\geq \frac{V_{O_I_{SYS_MAX}}}{I_{SET_100\%}} - \left(R_{OUT} \times N \right) = 3607.06\Omega \\ \rightarrow R_{SET} &= 3610\Omega, 0.1\% \end{aligned}$$

5. Using the following system of equations, solve for the maximum allowable shunt resistor. For this design, choose $R_{SHUNT} = 200 \mu\Omega$.

$$\begin{aligned} V_{SET1_100\%} &= R_{SET} \times I_{SET1_100\%} = 3610\Omega \times 850\mu A = 3.0685V \\ V_{SHUNT_100\%} &= \frac{V_{SET1_100\%}}{\text{Gain}_{INA240A3}} = \frac{3.0685V}{100V/V} = 30.685mV \\ R_{SHUNT} &\leq \frac{V_{SHUNT_100\%}}{I_{SOURCE_100\%}} = \frac{30.685mV}{152A} \\ \therefore R_{SHUNT} &\leq 201.88\mu\Omega \\ \rightarrow R_{SHUNT} &= 200\mu\Omega, 1\% \end{aligned}$$

6. Check that the common-mode voltage (V_{CM}) and output voltage ($V_{O_TLV9061}$) of the TLV9061 are in the operational region when the circuit is sensing the minimum required 5% source current. The TLV9061 device is a rail-to-rail-input-output (RRIO) op amp so it can operate with very small V_{CM} and output voltages, but A_{OL} will vary. Testing conditions from the data sheet for CMRR and A_{OL} show that choosing $V_{OUT_5\%} \geq 40mV$ provides sufficient A_{OL} when circuit sensing minimum load current.

- If a lower operational V_{CM} is needed, then consider providing a small negative voltage source to the negative supply pin to extend the range of the op amp or current-sense amplifier.

$$\begin{aligned} V_{O_MIN_TLV9061} &= 40mV \\ V_{SHUNT_5\%} &= 5\% \times I_{SOURCE_MAX} \times R_{SHUNT} = 7.6A \times 200\mu\Omega \\ \therefore V_{SHUNT_5\%} &= 1.52mV \\ V_{OUT_5\%} &= V_{SHUNT_5\%} \times \text{Gain} \times \frac{R_{OUT}}{R_{SET}} \\ \therefore V_{OUT_5\%} &= 42.94mV > V_{O_MIN_TLV9061} \end{aligned}$$

7. Using the following equations, calculate and tabulate the total, worst-case RSS error over the dynamic range of the source.

$$\begin{aligned} RE_{MAX_P} &= \text{Max Positive Relative Error} = \frac{V_{OUT_MAX} - V_{OUT_TYP}}{V_{OUT_TYP}} \\ RE_{MAX_N} &= \text{Max Negative Relative Error} = \frac{V_{OUT_MIN} - V_{OUT_TYP}}{V_{OUT_TYP}} \\ E_{RSS} &= \sqrt{e_{V_{OS_CSA}}^2 + e_{V_{OS_OPA}}^2 + e_{R_{SHUNT}}^2 + e_{\text{Gain}_{CSA}}^2 + e_{R_{OUT}}^2 + e_{R_{SET}}^2} \\ V_{OUT_TYP} &= I_{SOURCE1} \times R_{SHUNT_TYP} \times G_{TYP} \times \frac{R_{OUT_TYP}}{R_{SET_TYP}} \\ V_{OUT_MAX} &= \left[\left(I_{SOURCE1} \times R_{SHUNT_MAX} + V_{OS_CSA_MAX} \right) \times G_{MAX_CSA} + V_{OS_OPA_MAX} \right] \times \frac{R_{OUT_MAX}}{R_{SET_MIN}} \\ V_{OUT_MIN} &= \left[\left(I_{SOURCE1} \times R_{SHUNT_MIN} - V_{OS_CSA_MAX} \right) \times G_{MIN_CSA} - V_{OS_OPA_MAX} \right] \times \frac{R_{OUT_MIN}}{R_{SET_MAX}} \end{aligned}$$

$$T_{MAX} = 80^{\circ}C$$

$$\Delta T_{MAX} = 80^{\circ}C - 25^{\circ}C = 55^{\circ}C$$

$$R_{SHUNT} = 200\mu\Omega, 0.1\%, 175 \frac{ppm}{^{\circ}C}$$

$$V_{VS} = 5V; V_{CM} = 12V$$

$$V_{OSI_OPA} = \pm 2mV$$

$$V_{OS_OPA_CMRR} = |V_{OUT} - 2.5V| \times 10^{(-80dB/20dB)}$$

$$V_{OS_OPA_MAX} = V_{OSI_OPA} + V_{OS_OPA_CMRR} + \Delta T_{MAX} \times (530 \frac{nV}{^{\circ}C})$$

$$V_{OSI_CSA_MAX} = \pm 25\mu V$$

$$V_{OS_CSA_CMRR_MAX} = |12V - V_{CM}| \times 10^{(-CMRR_{MIN}/20dB)} = 0$$

$$V_{OS_CSA_PSRR_MAX} = |5V - V_{VS}| \times PSRR_{MAX} = 0$$

$$V_{OS_Drift_MAX} = \Delta T_{MAX} \times \left(\frac{\Delta V_{OS}}{\Delta T} \right) = 55^{\circ}C \times (250 \frac{nV}{^{\circ}C}) = \pm 13.75\mu V$$

$$V_{OS_CSA_MAX} = V_{OSI_MAX} + V_{OS_CMRR} + V_{OS_PSRR} + V_{OS_Drift}$$

$$V_{OS_CSA_MAX} = \pm 38.75\mu V$$

$$e_{V_{OS_CSA}} = V_{OS_CSA_MAX} / V_{SHUNT_IDEAL} \times 100$$

$$e_{V_{OS_OPA}} = V_{OS_OPA_MAX} / V_{SET_IDEAL} \times 100$$

$$e_R = e_{R_{TOLERANCE}} + e_{R_{DRIFT}}$$

$$e_{R_{SHUNT}} = 1\% + \Delta T_{MAX} \times TC = 1\% + 55^{\circ}C \times (175 \frac{ppm}{^{\circ}C}) \times 10^{-4} = 1.963\%$$

$$e_{R_{SET}} = e_{R_{OUT}} = 1\% + 55^{\circ}C \times (50 \frac{ppm}{^{\circ}C}) \times 10^{-4} = 1.275\%$$

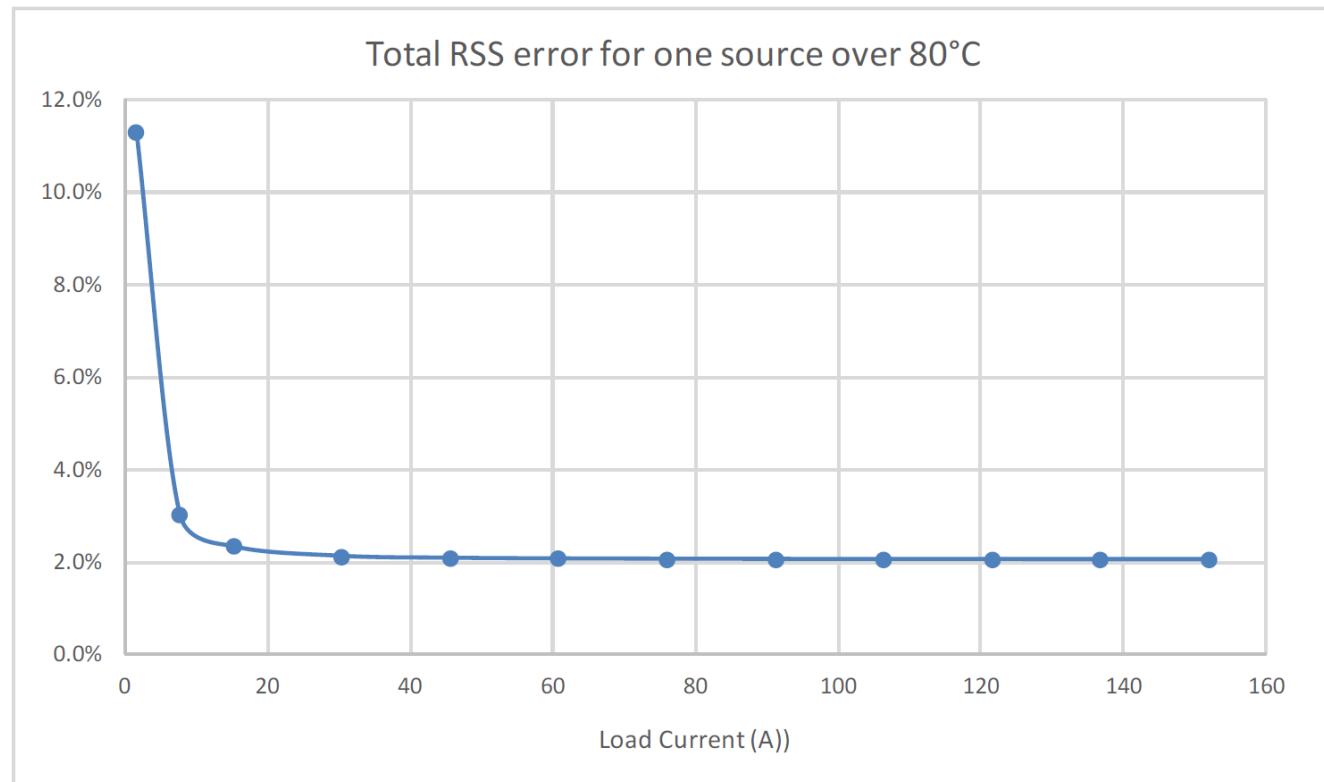
$$e_{GAIN_CSA_25C} = \pm 0.2\%$$

$$e_{GAIN_Drift_CSA_MAX} = \Delta T_{MAX} \times (2.5 \frac{ppm}{^{\circ}C}) \times 10^{-4} = \pm 0.01375\%$$

$$G_{MAX} = G_{TYP} \times (1 + e_{25C_MAX} + e_{Drift_MAX}) = 100 \frac{V}{V} \times (1.002138) = 100.2138 \frac{V}{V}$$

$$G_{MIN} = G_{TYP} \times (1 - e_{25C_MAX} - e_{Drift_MAX}) = 100 \frac{V}{V} \times (0.997862) = 99.7862 \frac{V}{V}$$

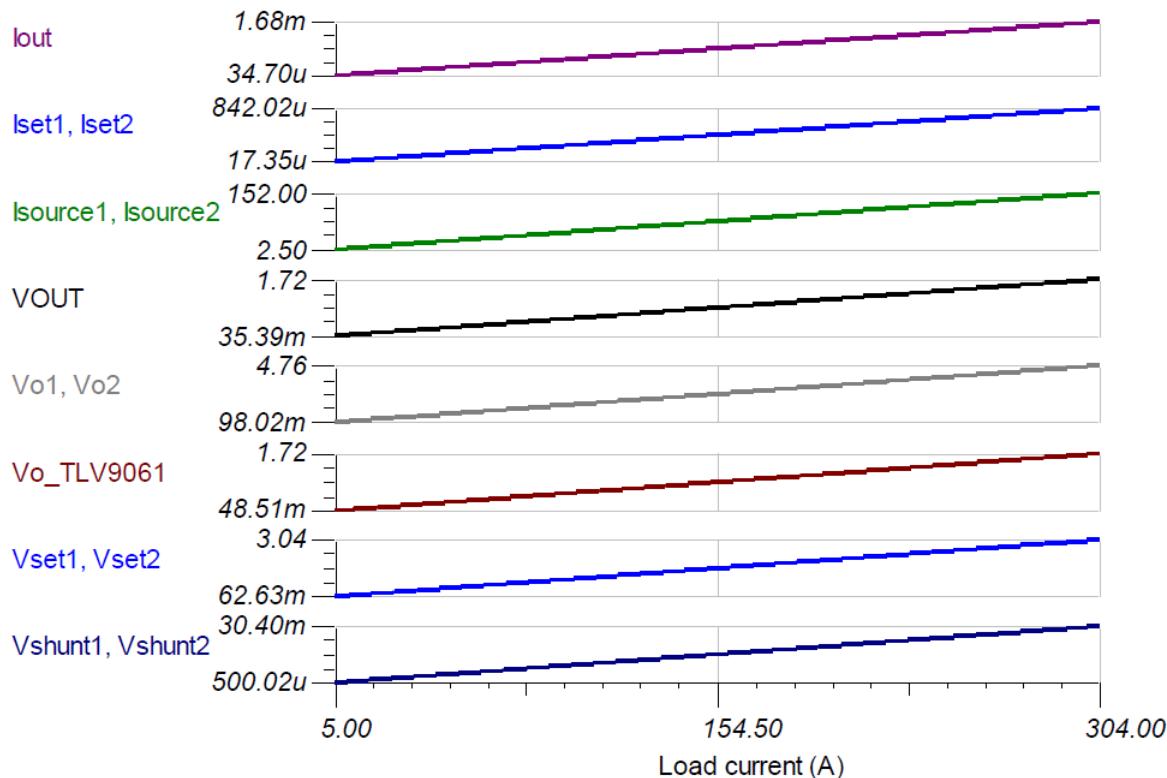
8. Plot the total error as a function of load current



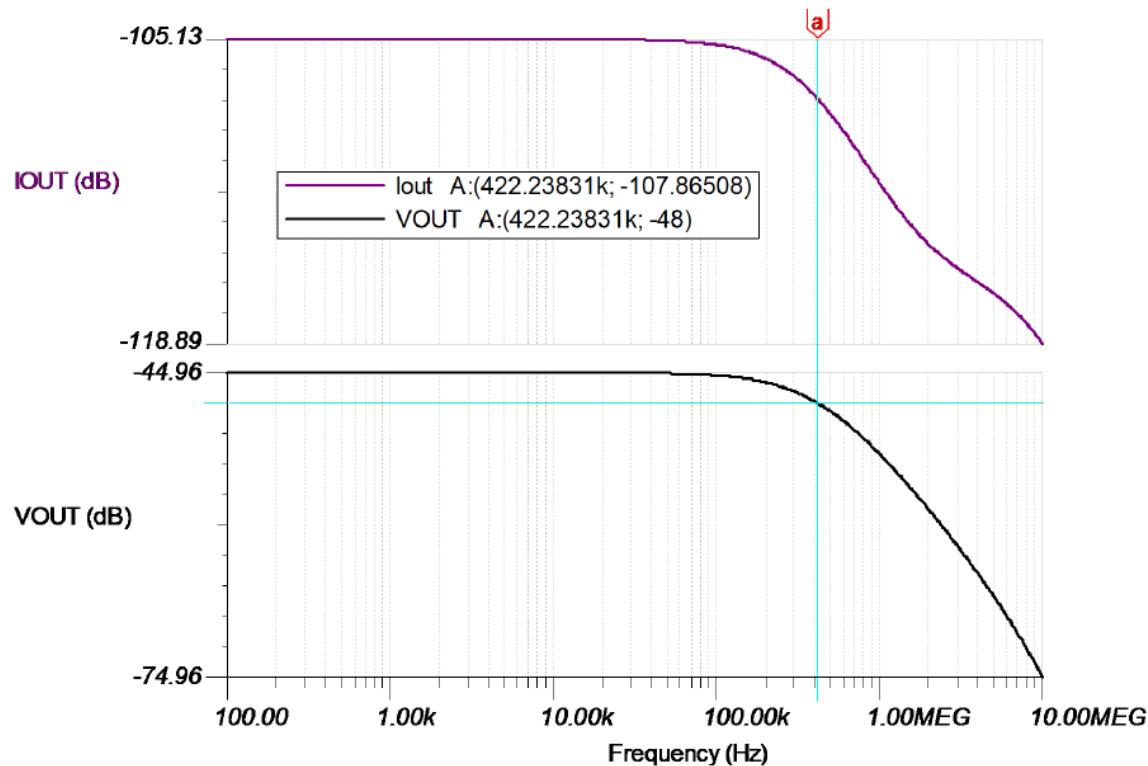
Design Simulations

DC Simulation Results

The following graph shows a linear output response for load currents from 5A to 304A.



AC Simulation Result – I_{LOAD} to I_{OUT} (V_{OUT}) circuit gain



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

Getting Started with Current Sense Amplifiers video series

<https://training.ti.com/getting-started-current-sense-amplifiers>

Current Sense Amplifiers on TI.com

<http://www.ti.com/amplifier-circuit/current-sense/products.html>

Comprehensive Study of the Howland Current Pump

[http://www.ti.com/analog/docs/litabsmultiplefilelist.tsp?
literatureNumber=snoa474a&docCategoryId=1&familyId=78](http://www.ti.com/analog/docs/litabsmultiplefilelist.tsp?literatureNumber=snoa474a&docCategoryId=1&familyId=78)

For direct support from TI Engineers use the E2E community

<http://e2e.ti.com>

Design Featured Current Sense Amplifier

INA240A3	
V_S	2.7V to 5.5V (operational)
V_{CM}	-4V to 80V
Swing to V_S (V_{SP})	$V_S - 0.2V$
V_{OS}	$\pm 25\mu V$ at 12V V_{CM}
I_Q_{MAX}	2.4mV
I_{IB}	90 μA at 12V
BW	400kHz
# of channels	1
Body size (including pins)	4mm × 3.91mm
www.ti.com/product/ina240	

Design Featured Operational Amplifier

TLV9061 (TLV9061S is shutdown version)	
V_S	1.8V to 5.5V
V_{CM}	(V_-) - 0.1V < V_{CM} < (V_+) + 0.1V
CMRR	103dB
A_{OL}	130dB
V_{OS}	$\pm 1.6mV$ maximum
I_Q	750 μA maximum
I_B (input bias current)	$\pm 0.5pA$
GBP (gain bandwidth product)	10MHz
# of channels	1 (2 and 4 channel packages available)
Body size (including pins)	0.80mm × 0.80mm
www.ti.com/product/tlv9061	

Analog Engineer's Circuit

Half-Wave Rectifier Circuit

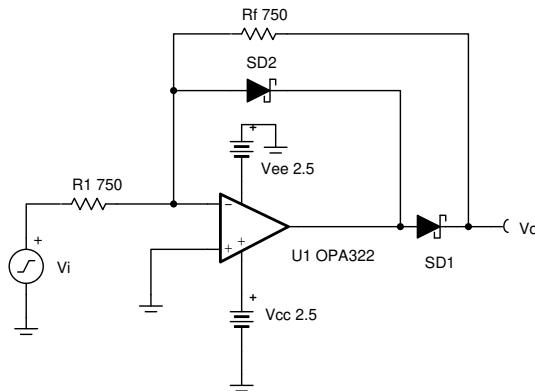


Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
$\pm 0.2 \text{ mV}_{pp}$	$\pm 4 \text{ V}_{pp}$	0.1 V_p	2 V_p	2.5 V	-2.5 V

Design Description

The precision half-wave rectifier inverts and transfers only the negative-half input of a time varying input signal (preferably sinusoidal) to its output. By appropriately selecting the feedback resistor values, different gains can be achieved. Precision half-wave rectifiers are commonly used with other op amp circuits such as a peak-detector or bandwidth limited non-inverting amplifier to produce a DC output voltage. This configuration has been designed to work for sinusoidal input signals between 0.2 mV_{pp} and 4V_{pp} at frequencies up to 50 kHz.



Design Notes

1. Select an op amp with a high slew rate. When the input signal changes polarities, the amplifier output must slew two diode voltage drops.
2. Set output range based on linear output swing (see A_{ol} specification).
3. Use fast switching diodes. High-frequency input signals will be distorted depending on the speed by which the diodes can transition from blocking to forward conducting mode. Schottky diodes might be a preferable choice, since these have faster transitions than pn-junction diodes at the expense of higher reverse leakage.
4. The resistor tolerance sets the circuit gain error.
5. Minimize noise errors by selecting low-value resistors.

Design Steps

- Set the desired gain of the half-wave rectifier to select the feedback resistors.

$$V_o = \text{Gain} \times V_i$$

$$\text{Gain} = -\frac{R_f}{R_1} = -1$$

$$R_f = R_1 = 2 \times R_{eq}$$

- Where R_{eq} is the parallel combination of R_1 and R_f
- Select the resistors such that the resistor noise is negligible compared to the voltage broadband noise of the op amp.

$$E_{nr} = \sqrt{4 \times k_b \times T \times R_{eq}}$$

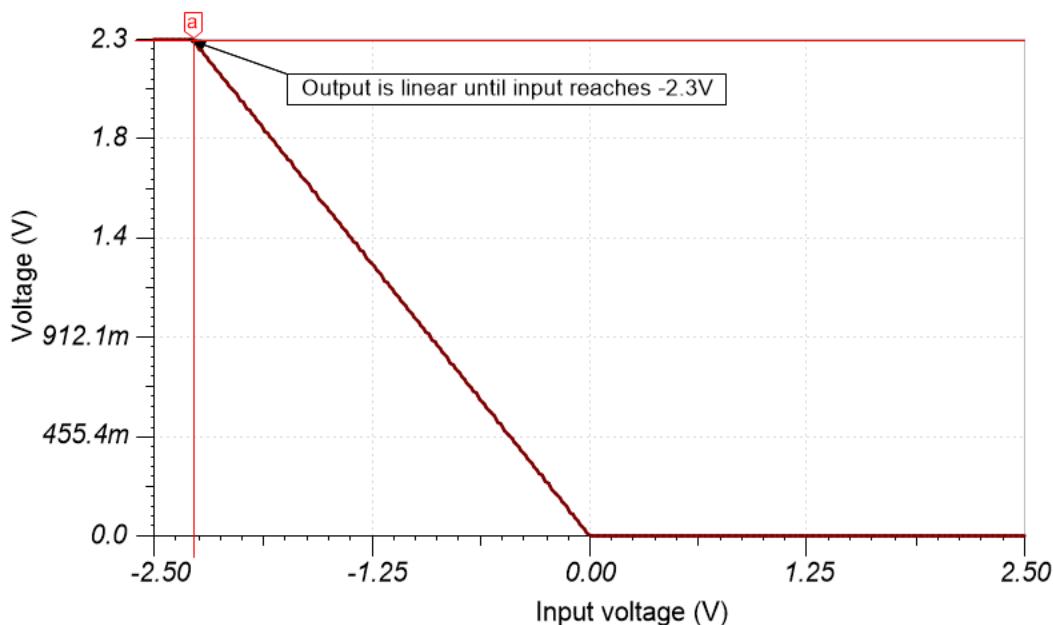
$$R_{eq} \leq \frac{E_{nbb}^2}{4 \times k_b \times T \times 3^2} = (E_{nbb})$$

$$= 7.5 \frac{nV}{\sqrt{\text{Hz}}} = \frac{(7.5 \times 10^{-9})^2}{4 \times 1.381 \times 10^{-23} \times 298 \times 3^2} = 380\Omega$$

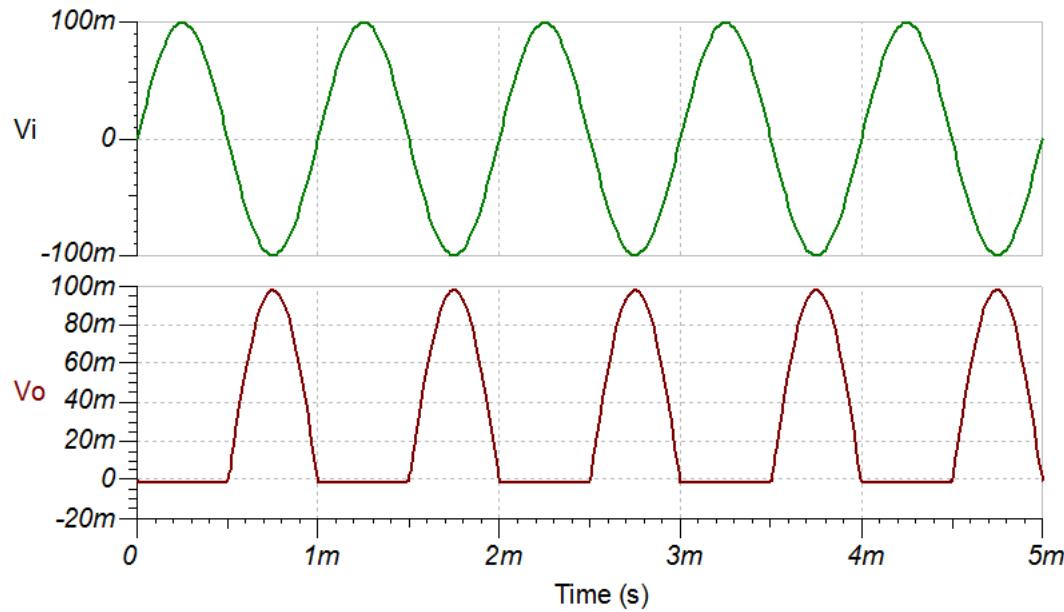
$$R_f = R_1 \leq 760\Omega \rightarrow 750\Omega \text{ (Standard Value)}$$

Design Simulations

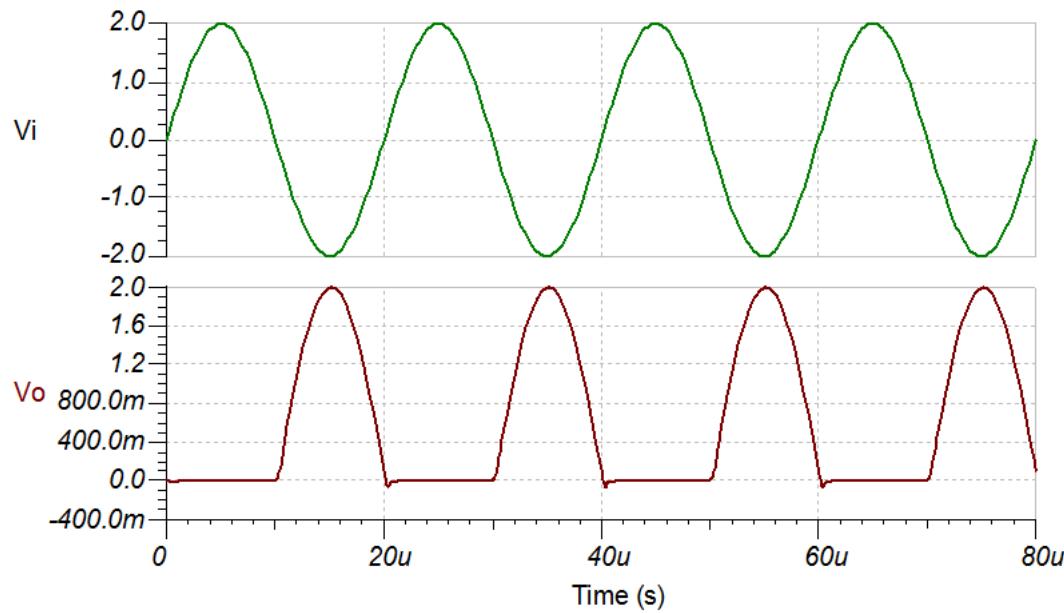
DC Simulation Results



Transient Simulation Results



200 mV_{pp} at 1 kHz



2 V_{pp} at 50 kHz

Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC509](#).

Design Featured Op Amp

OPA322	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	500 μ V
I_q	1.6 mA/Ch
I_b	0.2 pA
UGBW	20 MHz
SR	10 V/ μ s
#Channels	1, 2, and 4
OPA322	

Design Alternate Op Amp

OPA2325	
V_{ss}	2.2 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	40 μ V
I_q	0.65 mA/Ch
I_b	0.2 pA
UGBW	10 MHz
SR	5 V/ μ s
#Channels	2
OPA2325	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from August 2, 2017 to February 1, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page and link to Spice simulation file..... 1

Analog Engineer's Circuit

Slew Rate Limiter Circuit

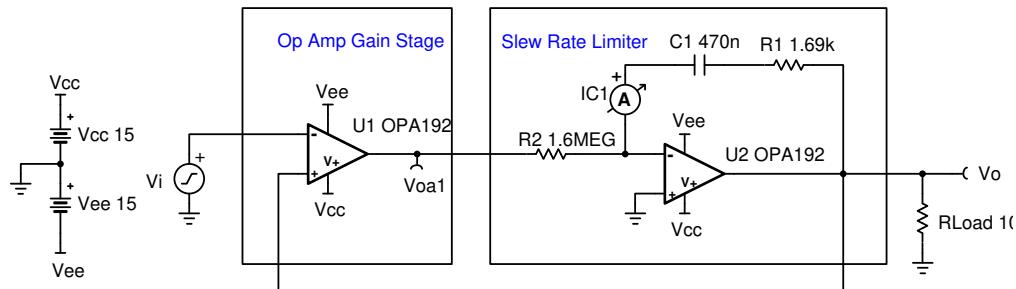


Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	V_{cc}	V_{ee}	V_{ref}
-10 V	10 V	-10 V	10 V	15 V	-15 V	0 V

Design Description

This circuit controls the slew rate of an analog gain stage. This circuit is intended for symmetrical slew rate applications. The desired slew rate must be slower than that of the op amp chosen to implement the slew rate limiter.



Design Notes

1. The gain stage op-amp and slew rate limiting op-amp should both be checked for stability.
2. Verify that the current demands for charging or discharging C_1 plus any load current out of U_2 will not limit the voltage swing of U_2 .

Design Steps

- Set slew rate and choose a standard value for the feedback capacitor, C_1 .

$$C_1 = 470\text{nF}$$

$$\text{SR} = 20 \frac{\text{V}}{\text{s}}$$

- Choose the value of R_2 to set the capacitor current necessary for the desired slew rate.

$$\text{SR} = \frac{I_{C_1}}{C_1}$$

$$20 \frac{\text{V}}{\text{s}} = \frac{I_{C_1}}{470\text{nF}} \text{ where } I_{C_1} = 9.4 \mu\text{A}$$

Gain stage op amp $V_{\text{sat}} = \pm 14.995$ (typical)

$$I_{C_1} = \frac{V_{\text{sat}}}{R_2}$$

$$9.4 \mu\text{A} = \frac{14.995\text{V}}{R_2}, \text{ so } R_2 = 1.595 \text{ M}\Omega \approx 1.6\text{M}\Omega \text{ (Standard Value)}$$

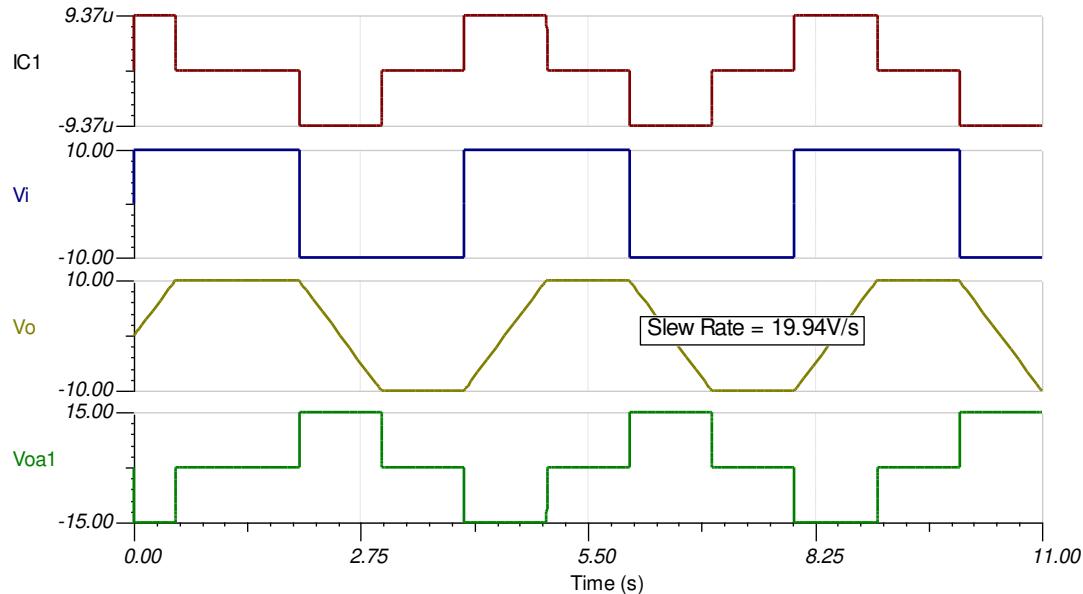
- Compensate feedback network for stability. R_1 adds a pole to the $1/\beta$ network. This pole should be placed so that the $1/\beta$ curve levels off a decade before it intersects the open loop gain curve (200 Hz, for this example).

$$f_p = \frac{1}{2\pi \times R_1 \times C_1} = 200\text{Hz}$$

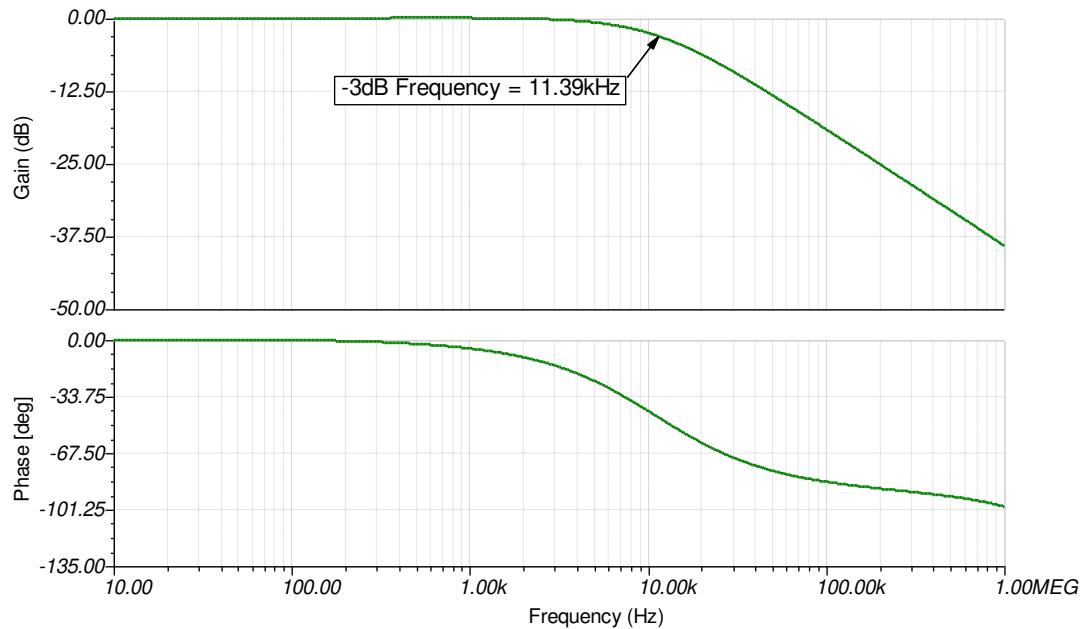
$$200\text{Hz} = \frac{1}{2\pi \times R_1 \times 470\text{nF}}, \text{ so } R_1 = 1.693 \text{ k}\Omega \approx 1.69\text{k}\Omega \text{ (Standard Value)}$$

Design Simulations

Transient Simulation Results



AC Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOC508](#).

See [TIPD140](#).

Design Featured Op Amp

OPA192	
V_{cc}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 μ V
I_q	1 mA/Ch
I_b	5 pA
UGBW	10 MHz
SR	20 V/ μ s
#Channels	1, 2, and 4
OPA192	

Design Alternate Op Amp

TLV2372	
V_{cc}	2.7 V to 16 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	2 mV
I_q	750 μ A/Ch
I_b	1 pA
UGBW	3 MHz
SR	2.1 V/ μ s
#Channels	1, 2, and 4
TLV2372	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.....1

Single-supply, high-input voltage, full-wave rectifier circuit



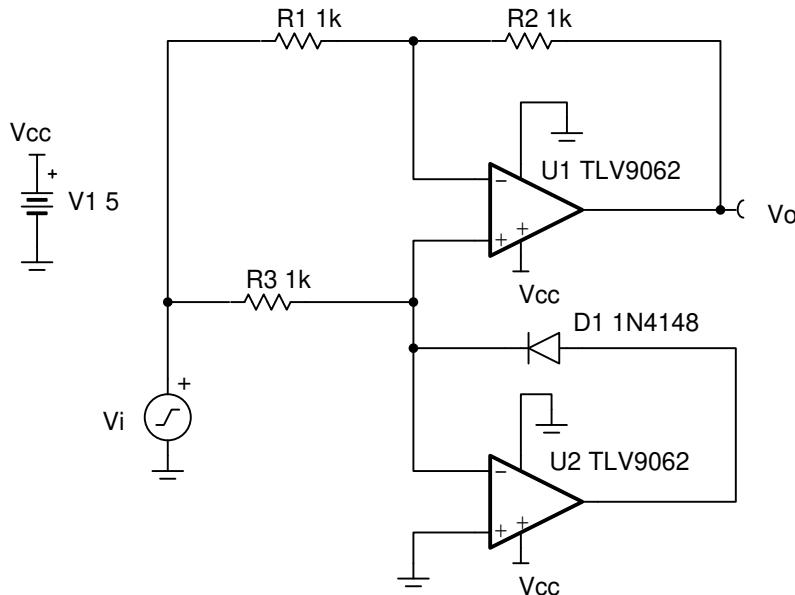
Amplifiers

Design Goals

Input	Output	Frequency	Supply	
$V_{i\text{Max}}$	$V_{o\text{Max}}$	f_{Max}	V_{cc}	V_{ee}
9Vpp	4.5Vpp	50kHz	5V	0V

Design Description

This single-supply precision full-wave rectifier is optimized for high-input voltages. When $V_i > 0V$, D_1 is reverse biased and the top part of the circuit, U1, is activated resulting in a circuit with a gain of $1V/V$. When $V_i < 0V$, D_1 is forward biased and the bottom part of the circuit, U2, is activated resulting in an inverting amplifier circuit with a gain of $-1V/V$.

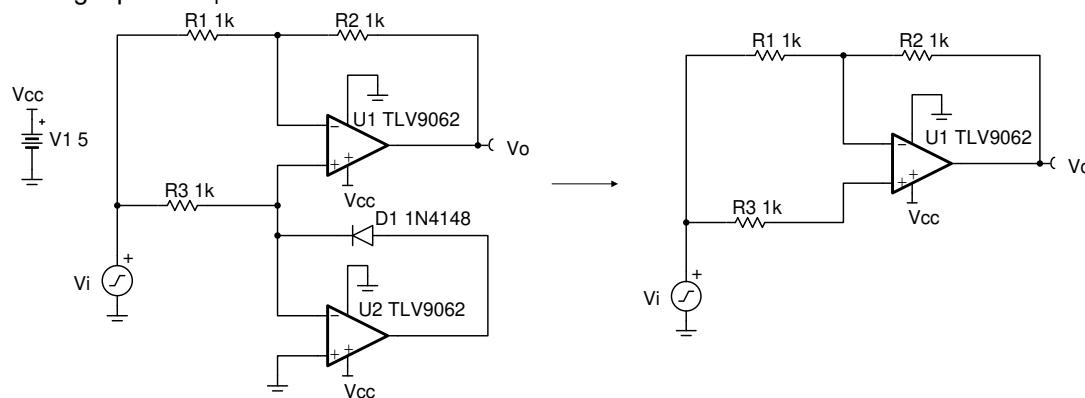


Design Notes

- Observe common-mode and output swing limitations of op amps.
- R_3 should be sized small enough that the leakage current from D_1 does not cause errors for positive input cycles while ensuring the op amp can drive the load.
- Use a fast switching diode for D_1 .
- Resistor tolerance determines the gain error of the circuit.
- Use a negative charge pump (such as the LM7705) for output swing requirements to GND to maintain linearity for output signals near 0V. For additional information, see [Single-supply, low-input voltage, full-wave rectifier circuit](#).
- For more information on op amp linear operating region, stability, capacitive load drive, driving ADCs, and bandwidth please see the [Design References](#) section.

Design Steps

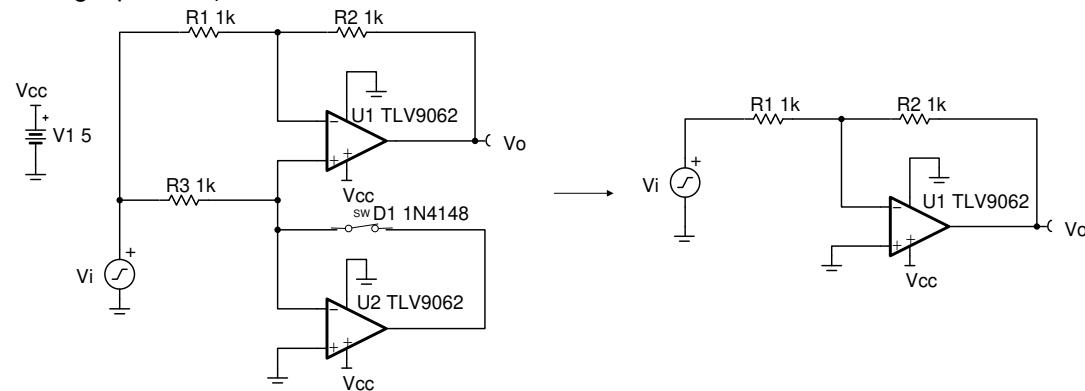
1. Circuit analysis for positive input signals. D₁ is reverse-biased disconnecting the output of U₂ from the non-inverting input of U₁.



$$\frac{V_o}{V_i} = \left(-\frac{R_2}{R_1} \right) + \left(1 + \frac{R_2}{R_1} \right) = 1$$

$$V_o = V_i$$

2. Circuit analysis for negative input signals. D₁ is forward biased, which connects the output of U₂ to the non-inverting input of U₁, which is GND.



$$\frac{V_o}{V_i} = \left(-\frac{R_2}{R_1} \right) = -1$$

$$V_o = -V_i$$

3. Select R₁, R₂, and R₃.

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

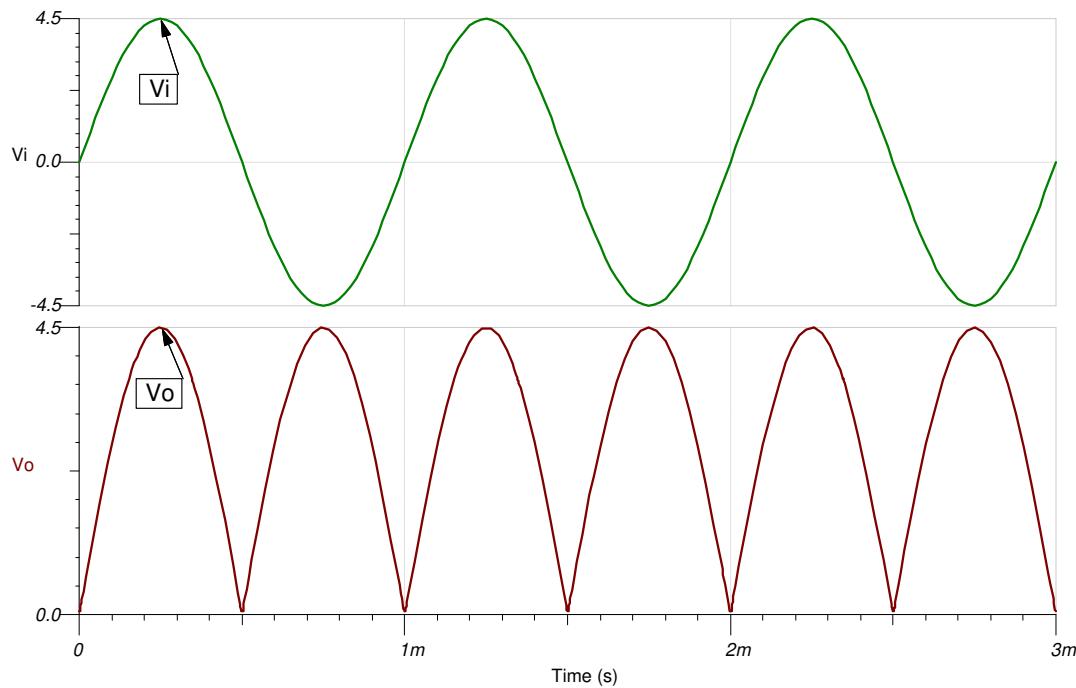
If R₂ = R₁ then V_o = -V_i

Set R₁ = R₂ = R₃ = 1kΩ

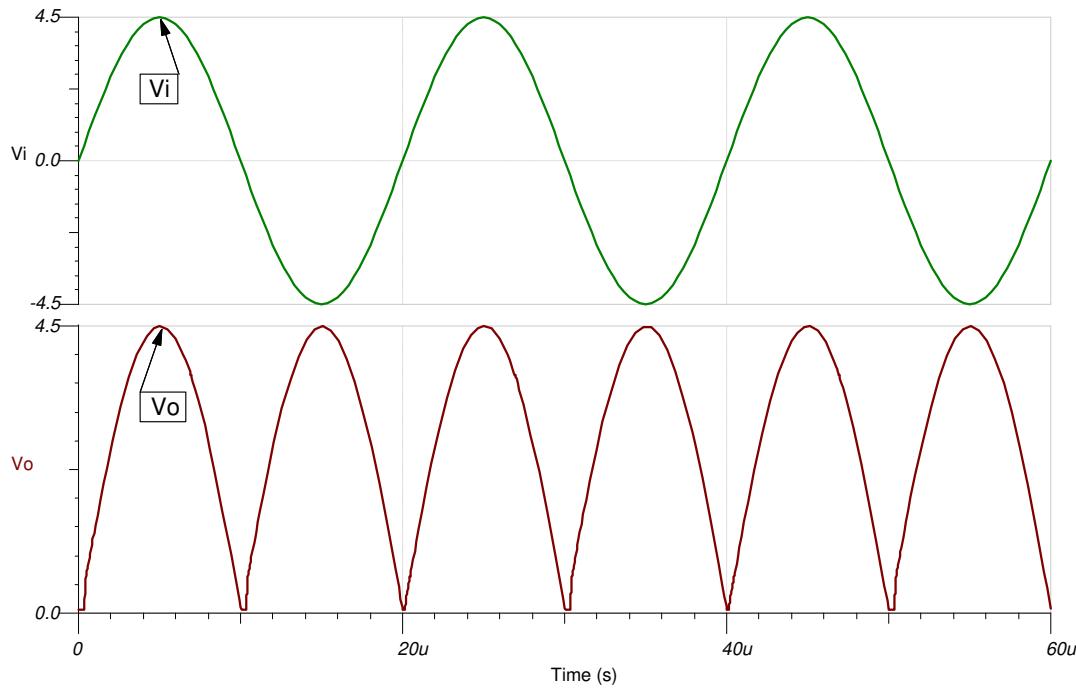
Design Simulations

Transient Simulation Results

A 1-kHz, 9-V_{pp} sine wave yields a 4.5-V_{pp} output sine wave.



A 50-kHz, 9-V_{pp} sine wave yields a 4.5-V_{pp} output sine wave.



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for the comprehensive TI circuit library.
2. SPICE Simulation File [SBOC529](#).
3. [TI Precision Labs](#)
4. See the [Single-Supply Low-Input Voltage Optimized Precision Full-Wave Rectifier Reference Design](#).

Design Featured Op Amp

TLV9062	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.30mV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amps

	OPA322	OPA350
V_{ss}	1.8V to 5.5V	2.7V to 5.5V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{out}	Rail-to-rail	Rail-to-rail
V_{os}	2mV	0.15mV
I_q	1.9mA	5.2mA
I_b	10pA	0.5pA
UGBW	20MHz	38MHz
SR	10V/µs	22V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/OPA322	www.ti.com/product/OPA350

Analog Engineer's Circuit

Full-Wave Rectifier Circuit

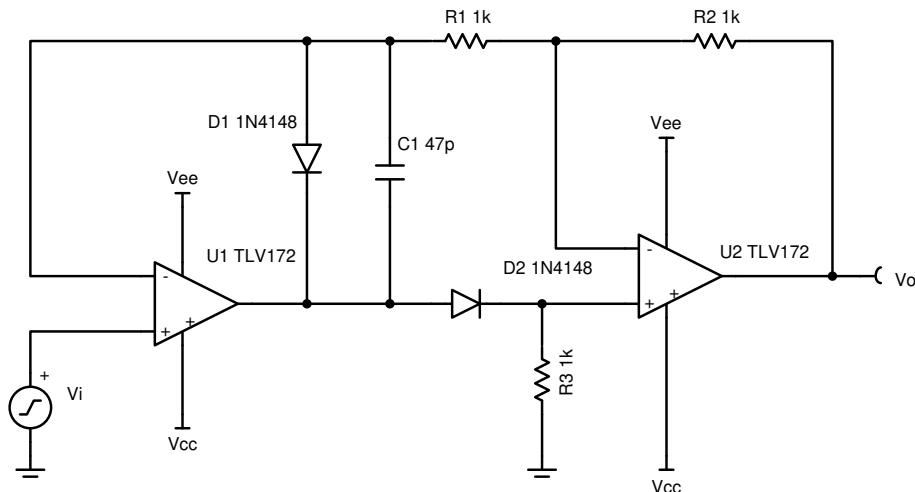


Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	V_{cc}	V_{ee}	V_{ref}
$\pm 25 \text{ mV}$	$\pm 10 \text{ V}$	25 mV	10 V	15 V	-15 V	0 V

Design Description

This absolute value circuit can turn alternating current (AC) signals to single polarity signals. This circuit functions with limited distortion for $\pm 10 \text{ V}$ input signals at frequencies up to 50 kHz and for signals as small as $\pm 25 \text{ mV}$ at frequencies up to 1 kHz.



Design Notes

1. Be sure to select an op amp with sufficient bandwidth and a high slew rate.
2. For greater precision look for an op amp with low offset voltage, low noise, and low total harmonic distortion (THD).
3. The resistors were selected to be 0.1% tolerance to reduce gain error.
4. Selecting too large of a capacitor C_1 will cause large distortion on the transition edges when the input signal changes polarity. C_1 may not be required for all op amps.
5. Use a fast switching diode.

Design Steps

1. Select gain resistors.
 - a. Gain for positive input signals.

$$\frac{V_o}{V_i} = 1 \frac{V}{V}$$

- b. Gain for negative input signals.

$$\frac{V_o}{V_i} = - \frac{R_2}{R_1} = - 1 \frac{V}{V}$$

2. Select R_1 and R_2 to reduce thermal noise and to minimize voltage drops due to the reverse leakage current of the diode. These resistors will appear as loads to U_1 and U_2 during negative input signals.

$$R_1 = R_2 = 1 \text{ k}\Omega$$

3. R_3 biases the non-inverting node of U_2 to GND during negative input signals. Select R_3 to be the same value as R_1 and R_2 . U_1 must be able to drive the R_3 load during positive input signals.

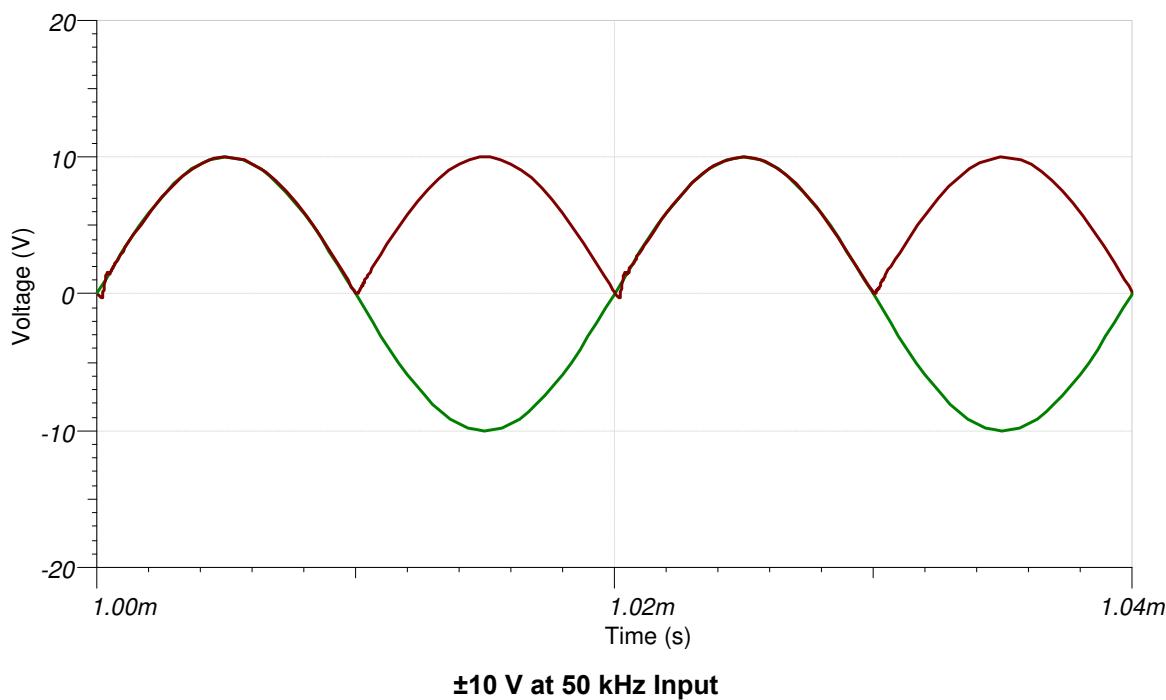
$$R_3 = 1 \text{ k}\Omega$$

4. Select C_1 based on the desired transient response. See the *Design Reference* section for more information.

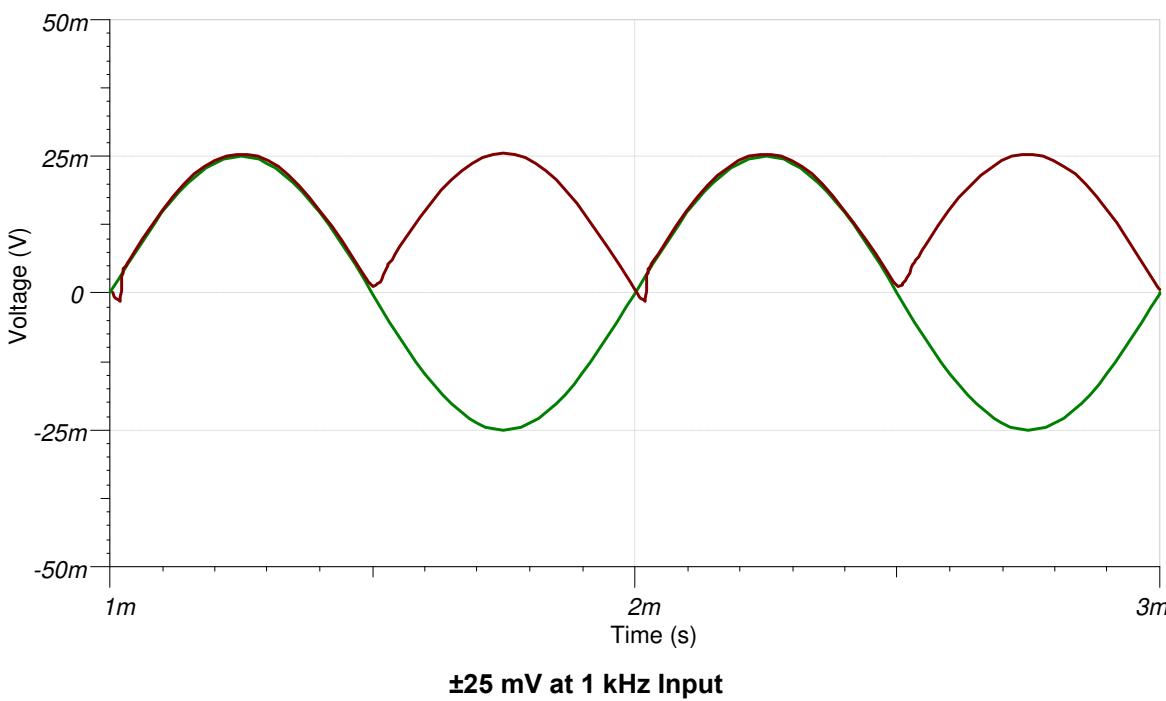
$$C_1 = 47\text{pF}$$

Design Simulations

Transient Simulation Results



±10 V at 50 kHz Input



±25 mV at 1 kHz Input

Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC517](#).

See TIPD139, [Precision Full-Wave Rectifier, Dual-Supply](#).

Design Featured Op Amp

TLV172	
V_{cc}	4.5 V to 36 V
V_{inCM}	V _{ee} to (V _{cc} -2 V)
V_{out}	Rail-to-rail
V_{os}	0.5 mV
I_q	1.6 mA/Ch
I_b	10 pA
UGBW	10 MHz
SR	10 V/μs
#Channels	1, 2, and 4
TLV172	

Design Alternate Op Amp

OPA197	
V_{cc}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	25 μV
I_q	1 mA/Ch
I_b	5 pA
UGBW	10 MHz
SR	20 V/μs
#Channels	1, 2, and 4
OPA197	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 1, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page and Spice simulation file..... [1](#)

Single-Supply, Low-Input Voltage, Full-Wave Rectifier Circuit

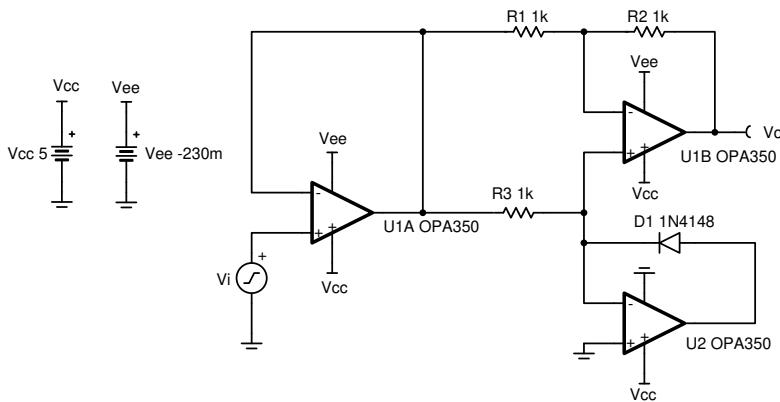


Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
5 mVpp	400 mVpp	2.5 mVpp	200 mVpp	5 V	-0.23 V	0 V

Design Description

This single-supply precision absolute value circuit is optimized for low-input voltages. It is designed to function up to 50 kHz and has excellent linearity at signal levels as low as 5 mVpp. The design uses a negative charge pump (such as LM7705) on the negative op amp supply rails to maintain linearity with signal levels near 0 V.

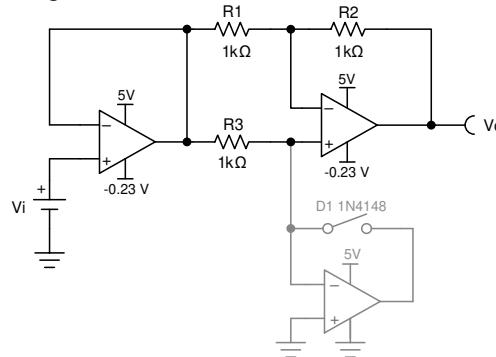


Design Notes

1. Observe common-mode and output swing limitations of op amps.
2. R_3 should be sized small enough that the leakage current from D_1 does not cause errors in positive input cycles while ensuring the op amp can drive the load.
3. Use a fast switching diode for D_1 .
4. Removing the input buffer will allow for input signals with peak-to-peak values twice as large as the supply voltage at the expense of lower input impedance and slight gain error.
5. Use precision resistors to minimize gain error.

Design Steps

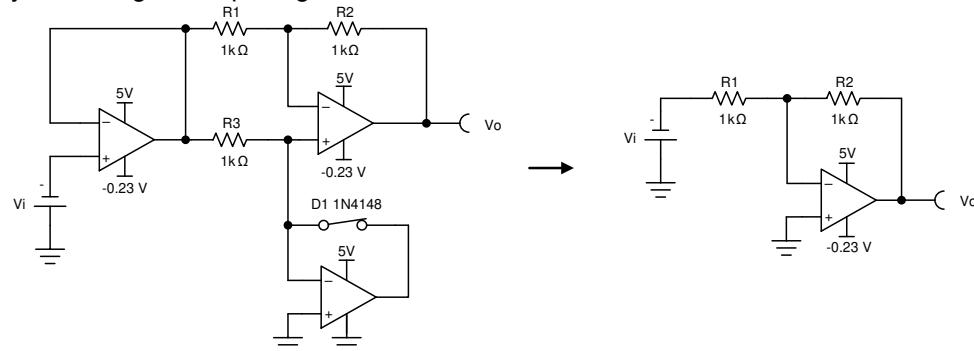
- Circuit analysis for positive input signals.



$$\frac{V_o}{V_i} = \left(-\frac{R_2}{R_1} \right) + \left(1 + \frac{R_2}{R_1} \right) = 1$$

$$V_o = V_i$$

- Circuit analysis for negative input signals.



$$\frac{V_o}{V_i} = \left(-\frac{R_2}{R_1} \right) = -1$$

$$V_o = -V_i$$

- Select R_1 , R_2 , and R_3 .

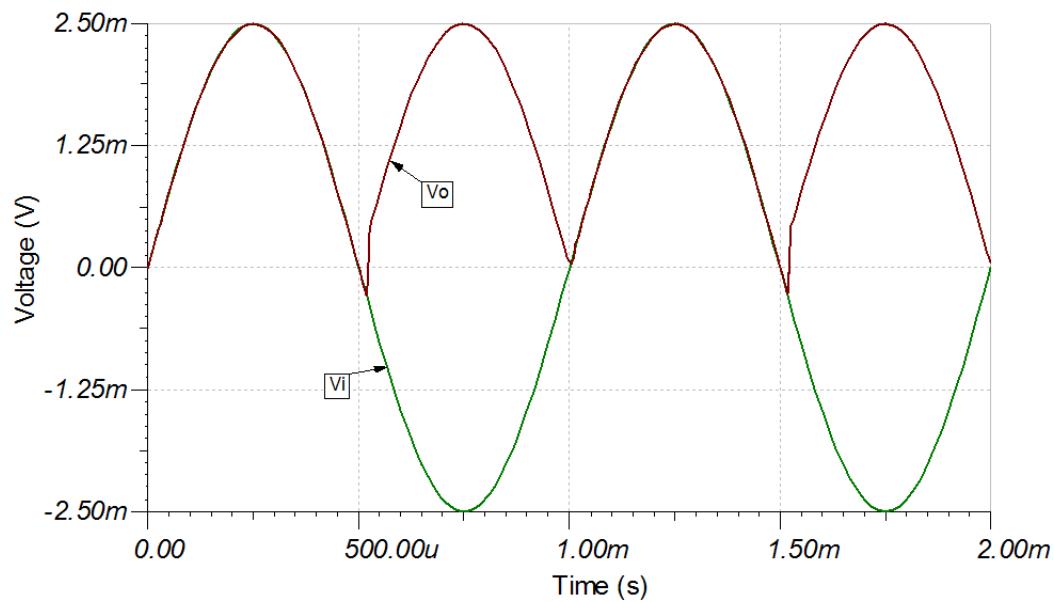
$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

If $R_2 = R_1$ then $V_o = -V_i$

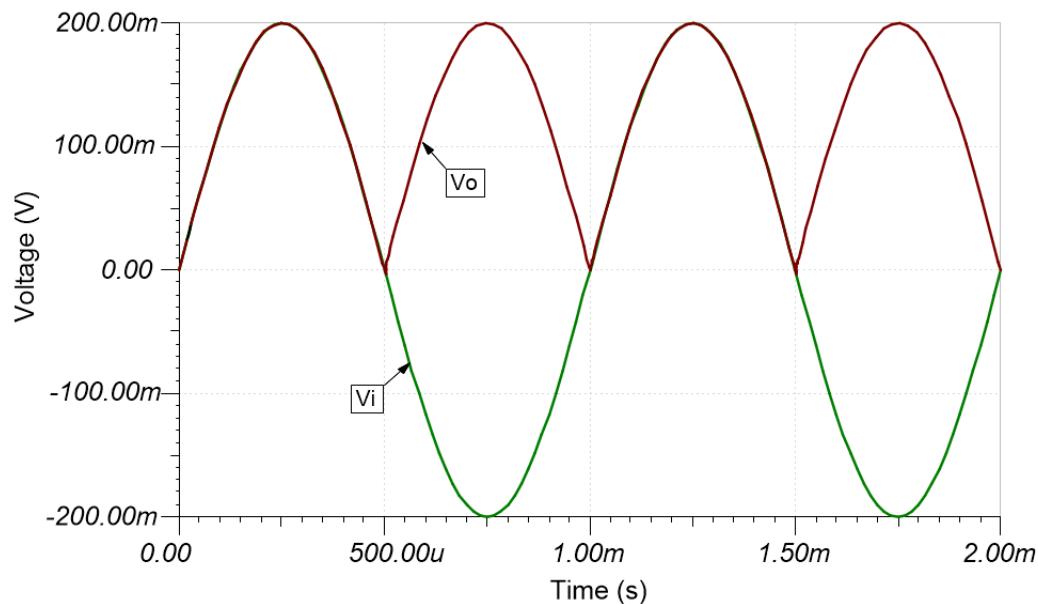
Set $R_1 = R_2 = R_3 = 1 \text{ k}\Omega$

Design Simulations

Transient Simulation Results



5 mVpp at 1 kHz Input



400 mVpp at 1 kHz Input

Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC506](#).

See TIPD124, [Single-Supply Low-Input Voltage Optimized Precision Full-Wave Rectifier Reference Design](#).

Design Featured Op Amp

OPA350	
V_{ss}	2.7 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	150 μ V
I_q	5.2 mA/Ch
I_b	0.5 pA
UGBW	38 MHz
SR	22 V/ μ s
#Channels	1, 2, and 4
OPA350	

Design Alternate Op Amp

OPA353	
V_{ss}	2.7 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	3 mV
I_q	5.2 mA
I_b	0.5 pA
UGBW	44 MHz
SR	22 V/ μ s
#Channels	1, 2, and 4
OPA353	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019

Page

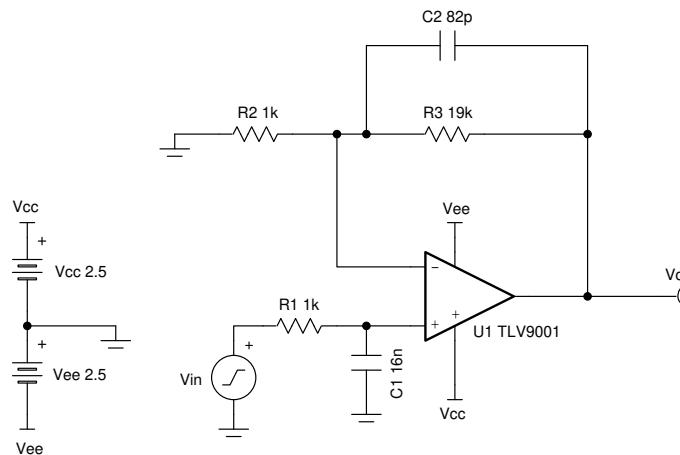
- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file..... [1](#)

Low-pass, filtered, non-inverting amplifier circuit**Amplifiers****Design Goals**

Input		Output		BW	Supply	
V _{iMin}	V _{iMax}	V _{oMin}	V _{oMax}	f _c	V _{cc}	V _{ee}
-0.1V	0.1V	-2V	2V	10kHz	2.5V	-2.5V

Design Description

This low-pass non-inverting circuit amplifies the signal level by 20V/V (26dB) and filters the signal by setting the pole at 10kHz. Components R₁ and C₁ create a low-pass filter on the non-inverting pin. The frequency response of this circuit is the same as that of a passive RC filter, except that the output is amplified by the pass-band gain of the amplifier. Components C₂ and R₃ are used to set the cutoff frequency, f_c, of the non-inverting amplifier.

**Design Notes**

1. The common-mode voltage is equal to the input voltage applied to the non-inverting input of the op amp.
2. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
3. Set the pole frequency created by R₃ / C₂ to be ten times higher than the pole created by R₁ / C₁ to achieve a single pole roll-off that is dominated by R₁ / C₁. If the filter pairs R₁ / C₁ and R₃ / C₂ have the same pole frequency, the gain will be reduced by 6dB at the cutoff frequency. Also the gain decreases at a rate of -40dB/dec until the response reaches 0dB, after which the slope changes to -20dB/dec until the op amp runs out of bandwidth.
4. C₂ limits the bandwidth of the non-inverting gain stage.
5. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on an op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth, see the [Design References](#) section.

Design Steps

The DC transfer function of this circuit follows:

$$V_o = V_{in} \times \left(1 + \frac{R_3}{R_2} \right)$$

1. Calculate the gain.

$$\text{Gain} = \frac{V_{o\text{Max}} - V_{o\text{Min}}}{V_{i\text{Max}} - V_{i\text{Min}}} = \frac{2V - (-2V)}{0.1V - (-0.1V)} = 20 \frac{V}{V}$$

2. Calculate values for R_2 and R_3 .

$$\text{Gain} = 1 + \frac{R_3}{R_2} = 20 \frac{V}{V} \rightarrow (26\text{dB})$$

Choose $R_2 = 1\text{k}\Omega$:

$$R_3 = (\text{Gain} - 1) \times R_2 = 19\text{k}\Omega$$

3. Calculate the component values R_1 and C_1 to set the cutoff frequency, f_c . Pick the value of R_1 and then calculate C_1 to set the location of f_c .

Choose $R_1 = 1\text{k}\Omega$:

$$C_1 = \frac{1}{2\pi \times R_1 \times f_c} = \frac{1}{2\pi \times 1\text{k}\Omega \times 10\text{kHz}} = 15.92\text{nF} \approx 16\text{nF} \text{ (Standard Value)}$$

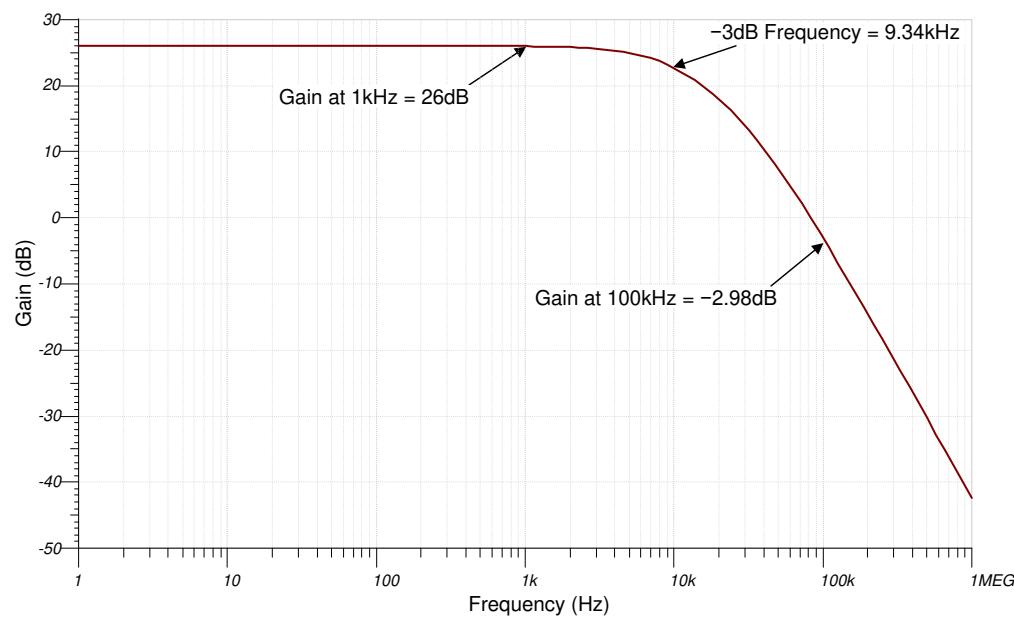
4. Calculate C_2 value to set the cutoff frequency (f_c) of the op amp. Select the corner frequency to be at least ten times larger than f_c .

$$f_c = 10\text{kHz}; 10 \times f_c = 100\text{kHz}$$

$$C_2 = \frac{1}{2\pi \times R_3 \times 100\text{kHz}} = \frac{1}{2\pi \times 19\text{k}\Omega \times 100\text{kHz}} = 83.77\text{pF} \approx 82\text{pF} \text{ (Standard Value)}$$

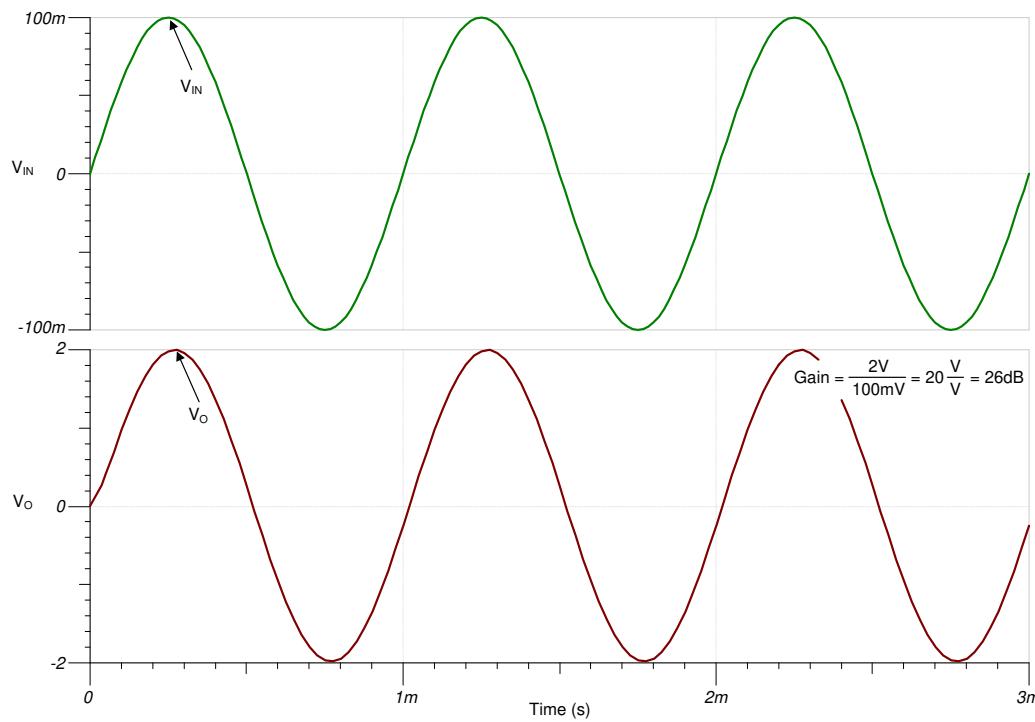
Design Simulations

AC Simulation Results

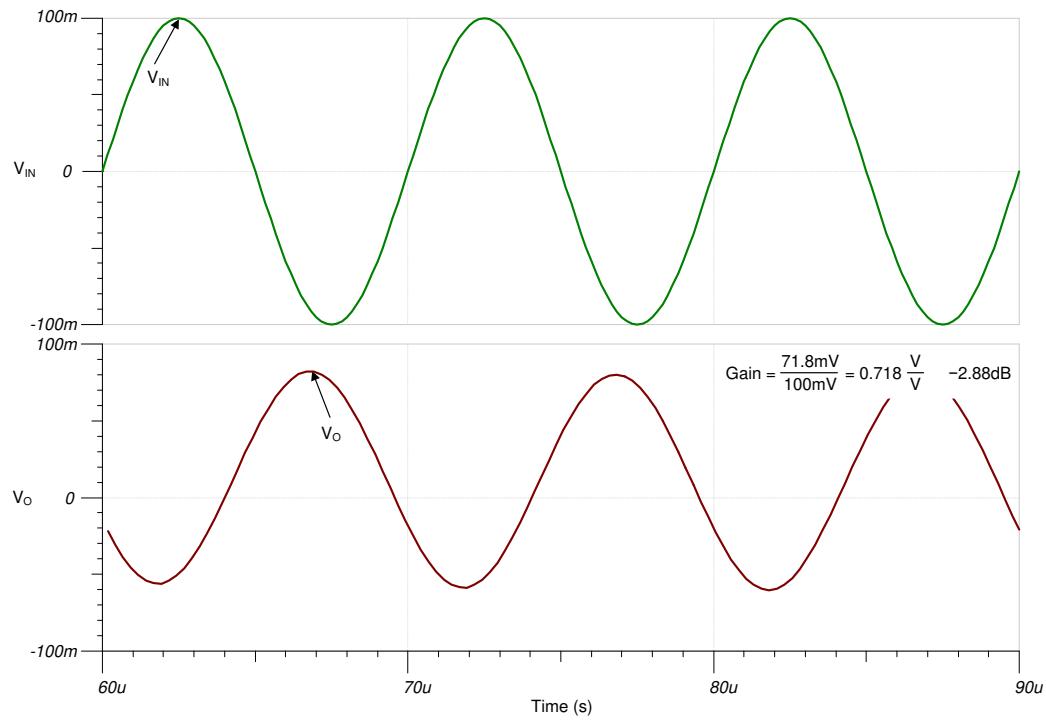


Transient Simulation Results

A 1-kHz, 0.2-V_{PP} sine wave yields a 4-V_{PP} output sine wave.



A 100-kHz, 0.2-V_{PP} sine wave yields a 0.071-V_{PP} output sine wave.



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for the comprehensive TI circuit library.
2. SPICE Simulation File [SBOC528](#).
3. [TI Precision Labs](#)
4. See the [AC Coupled, Single-Supply, Inverting and Non-inverting Amplifier Reference Design](#).

Design Featured Op Amp

TLV9001	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.4mV
I_q	60 μ A
I_b	5pA
UGBW	1MHz
SR	2V/ μ s
#Channels	1,2,4
www.ti.com/product/TLV9001	

Design Alternate Op Amp

OPA375	
V_{ss}	2.25V to 5.5V
V_{inCM}	V_{ee} to V_{cc} – 1.2V
V_{out}	Rail-to-rail
V_{os}	0.15mV
I_q	890 μ A
I_b	10pA
UGBW	10MHz
SR	4.75V/ μ s
#Channels	1,2,4
www.ti.com/product/OPA375	

Non-Inverting Op Amp with Non-Inverting Positive Reference Voltage Circuit

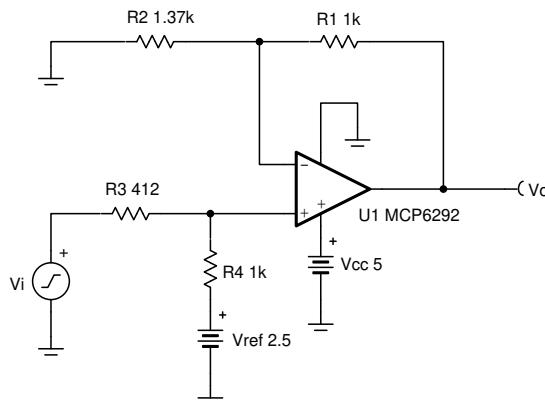


Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	V_{cc}	V_{ee}	V_{ref}
-1 V	3 V	0.05 V	4.95 V	5 V	0 V	2.5 V

Design Description

This design uses a non-inverting amplifier with a non-inverting positive reference to translate an input signal of -1 V to 3 V to an output voltage of 0.05 V to 4.95 V. This circuit can be used to translate a sensor output voltage with a positive slope and negative offset to a usable ADC input voltage range.



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Design Notes

1. Use op amp linear output operating range. Usually specified under A_{OL} test conditions.
2. Check op amp input common mode voltage range.
3. V_{ref} output must be low impedance.
4. Input impedance of the circuit is equal to the sum of R_3 and R_4 .
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100 kΩ. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier.
7. Adding a capacitor in parallel with R_1 will improve stability of the circuit if high-value resistors are used.

Design Steps

$$V_o = V_i \times \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right) + V_{ref} \times \left(\frac{R_3}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right)$$

1. Calculate the gain of the input voltage to produce the desired output swing.

$$G_{input} = \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right)$$

$$V_{o_max} - V_{o_min} = (V_{i_max} - V_{i_min}) \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right)$$

$$\frac{V_{o_max} - V_{o_min}}{V_{i_max} - V_{i_min}} = \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right)$$

$$\frac{4.95V - 0.05V}{3V - (-1V)} = \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right)$$

$$1.225V = \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right)$$

2. Select a value for R_1 and R_4 and insert the values into the previous equation. The other two resistor values must be solved using a system of equations. The proper output swing and offset voltage cannot be calculated if more than two variables are selected.

$$R_1 = R_4 = 1 \text{ k}\Omega$$

$$1.225V = \left(\frac{1 \text{ k}\Omega}{R_3 + 1 \text{ k}\Omega} \right) \left(\frac{1 \text{ k}\Omega + R_2}{R_2} \right)$$

3. Solve the previous equation for R_3 in terms of R_2 .

$$R_3 = \frac{1 \text{ M}\Omega + (1 \text{ k}\Omega \times R_2)}{1.225 \times R_2} - 1 \text{ k}\Omega$$

4. Select any point along the transfer function within the linear output range of the amplifier to set the proper offset voltage at the output (for example, the minimum input and output voltage).

$$V_{o_min} = V_{i_min} \times \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right) + V_{ref} \times \left(\frac{R_3}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right)$$

$$0.05V = -1 \text{ V} \times \left(\frac{1 \text{ k}\Omega}{R_3 + 1 \text{ k}\Omega} \right) \left(\frac{1 \text{ k}\Omega + R_2}{R_2} \right) + 2.5V \times \left(\frac{R_3}{R_3 + 1 \text{ k}\Omega} \right) \left(\frac{1 \text{ k}\Omega + R_2}{R_2} \right)$$

5. Insert R_3 into the equation from step 1 and solve for R_2 .

$$0.05V = -1 \text{ V} \times \left(\frac{\frac{1 \text{ k}\Omega}{\frac{1 \text{ M}\Omega + 1 \text{ k}\Omega \times R_2}{1.225 \times R_2} - 1 \text{ k}\Omega + 1 \text{ k}\Omega}}{\frac{1 \text{ M}\Omega + 1 \text{ k}\Omega \times R_2}{1.225 \times R_2} - 1 \text{ k}\Omega + 1 \text{ k}\Omega} \right) \left(\frac{1 \text{ k}\Omega + R_2}{R_2} \right) + 2.5V \times \left(\frac{\frac{1 \text{ M}\Omega + 1 \text{ k}\Omega \times R_2}{1.225 \times R_2} - 1 \text{ k}\Omega}{\frac{1 \text{ M}\Omega + 1 \text{ k}\Omega \times R_2}{1.225 \times R_2} - 1 \text{ k}\Omega + 1 \text{ k}\Omega} \right) \left(\frac{1 \text{ k}\Omega + R_2}{R_2} \right)$$

$$R_2 = 1360.5\Omega \approx 1370\Omega$$

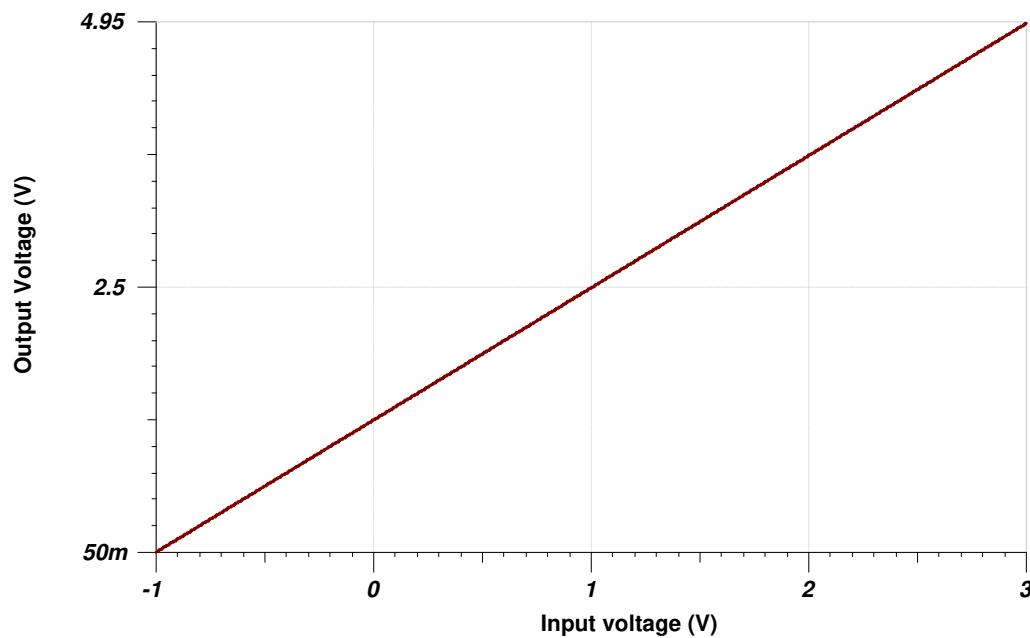
6. Insert R_2 into the equation from step 1 to solve for R_3 .

$$R_3 = \frac{1 \text{ M}\Omega + 1 \text{ k}\Omega \times (1370\Omega)}{1.225 \times (1370\Omega)} - 1 \text{ k}\Omega$$

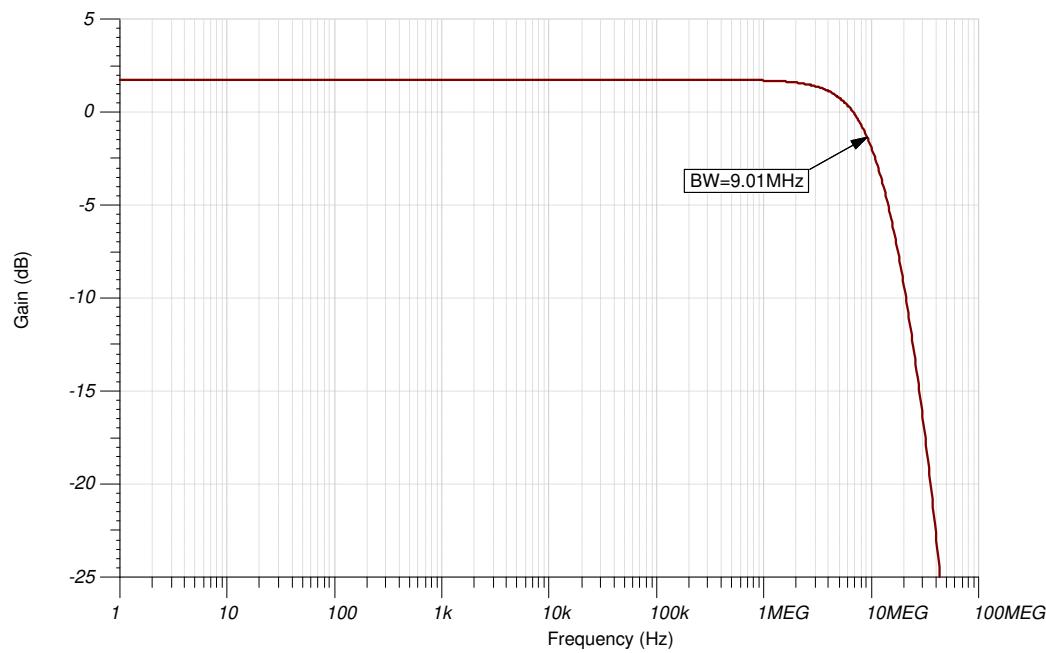
$$R_3 = 412.18\Omega \approx 412\Omega$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOC513](#).

See [Designing Gain and Offset in Thirty Seconds](#).

Design Featured Op Amp

MCP6292	
V_{ss}	2.4 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3 mV
I_q	600 μ A
I_b	1 pA
UGBW	10 MHz
SR	6.5 V/ μ s
#Channels	1, 2, and 4
MCP6292	

Design Alternate Op Amp

OPA388	
V_{ss}	2.5 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.25 μ V
I_q	1.9 mA
I_b	30 pA
UGBW	10 MHz
SR	5 V/ μ s
#Channels	1, 2, and 4
OPA388	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file..... [1](#)

Inverting Amplifier With T-Network Feedback Circuit



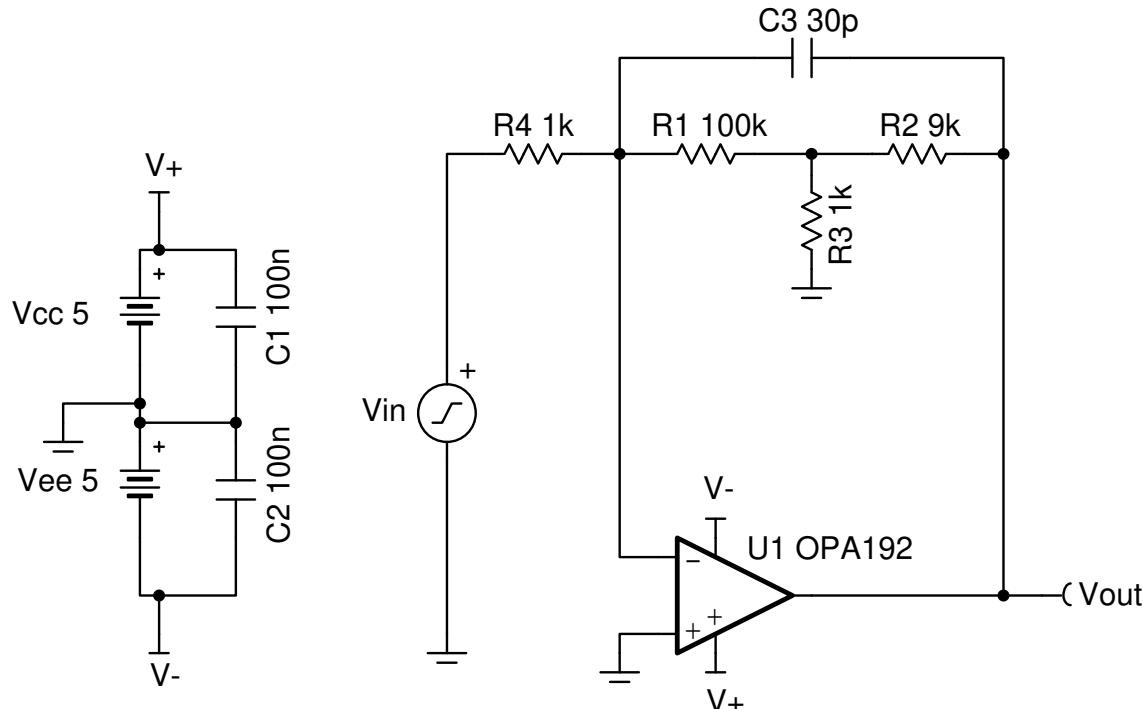
Amplifiers

Design Goals

Input		Output		BW	Supply	
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	f_p	V_{cc}	V_{ee}
-2.5mV	2.5mV	-2.5V	2.5V	5kHz	5V	-5V

Design Description

This design inverts the input signal, V_{in} , and applies a signal gain of $1000V/V$ or $60dB$. The inverting amplifier with T-feedback network can be used to obtain a high gain without a small value for R_4 or very large values for the feedback resistors.



Design Notes

1. C_3 and the equivalent resistance of feedback resistors set the cutoff frequency, f_p .
2. The common-mode voltage in this circuit does not vary with input voltage.
3. Using high-value resistors can degrade the phase margin and increase noise.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Due to the high gain of the circuit, be sure to use an op amp with sufficient gain bandwidth product. Remember to use the noise gain when calculating bandwidth. Use precision, or low offset, devices due to the high gain of the circuit.
6. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth see the [Design References](#) section.

Design Steps

- Calculate required gain.

$$\text{Gain} = \frac{V_{o\text{Max}} - V_{o\text{Min}}}{V_{i\text{Max}} - V_{i\text{Min}}} = \frac{2.5V - (-2.5V)}{2.5mV - (-2.5mV)} = 1000 \frac{V}{V} = 60\text{dB}$$

- Calculate resistor values to set the required gain.

$$\text{Gain} = \left(\frac{\frac{R_2 \times R_1}{R_3} + R_1 + R_2}{R_4} \right)$$

Choose the input resistor R_4 to be $1\text{k}\Omega$. To obtain a gain of 1000V/V , normally a $1-\text{M}\Omega$ resistor would be required. A T-network allows us to use smaller resistor values in the feedback loop. Selecting R_1 to be $100\text{k}\Omega$ and R_2 to be $9\text{k}\Omega$ allows calculation of the value for R_3 . R_2 is in the $10\text{k}\Omega$ range so the op amp can easily drive the feedback network.

$$R_3 = \left(\frac{R_2 \times R_1}{(\text{Gain} \times R_4) - R_1 - R_2} \right) = \left(\frac{9\text{k}\Omega \times 100\text{k}\Omega}{(1000 \times 1\text{k}\Omega) - 100\text{k}\Omega - 9\text{k}\Omega} \right) = 1\text{k}\Omega$$

- Calculate C_3 using the equivalent resistance of the feedback resistors, R_{eq} , to set the location of f_p .

$$R_{eq} = \left(\frac{R_2 \times R_1}{R_3} + R_1 + R_2 \right) = \left(\frac{9\text{k}\Omega \times 100\text{k}\Omega}{1\text{k}\Omega} + 100\text{k}\Omega + 9\text{k}\Omega \right) = 1.009\text{M}\Omega$$

$$f_p = \frac{1}{2\pi \times R_{eq} \times C_3} = 5\text{kHz}$$

$$C_3 = \frac{1}{2\pi \times R_{eq} \times f_p} = \frac{1}{2\pi \times 1.009\text{M}\Omega \times 5\text{kHz}} = 31.55\text{pF} \approx 30\text{pF} \text{ (Standard Value)}$$

- Calculate the small signal circuit bandwidth to ensure it meets the 5 kHz requirement. Be sure to use the noise gain, NG, or non-inverting gain of the circuit.

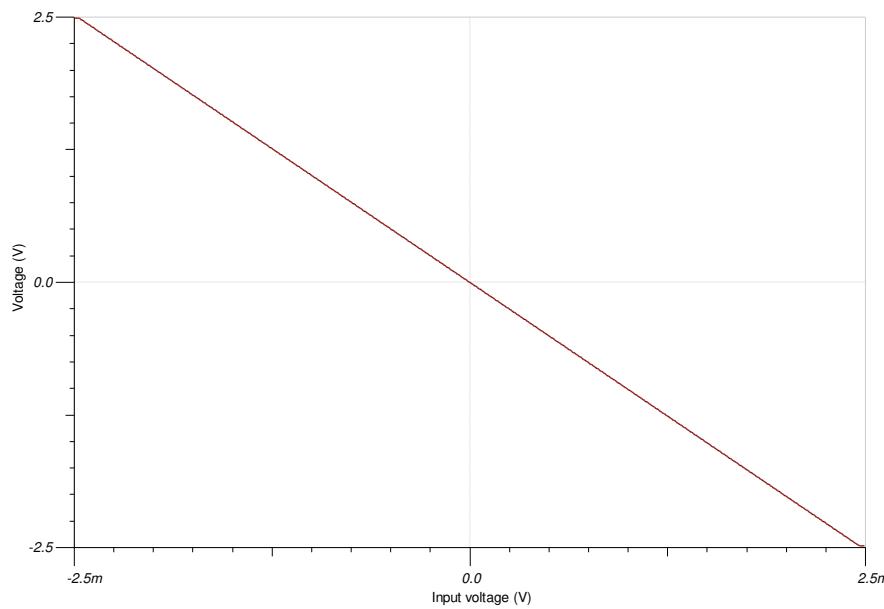
$$NG = 1 + \frac{R_{eq}}{R_4} = 1 + 1009 = 1010 \frac{V}{V}$$

$$BW = \frac{GBP}{NG} = \frac{10\text{MHz}}{1010 \frac{V}{V}} = 9.9\text{kHz}$$

- $BW_{OPA192} = 10\text{MHz}$; therefore this requirement is met.

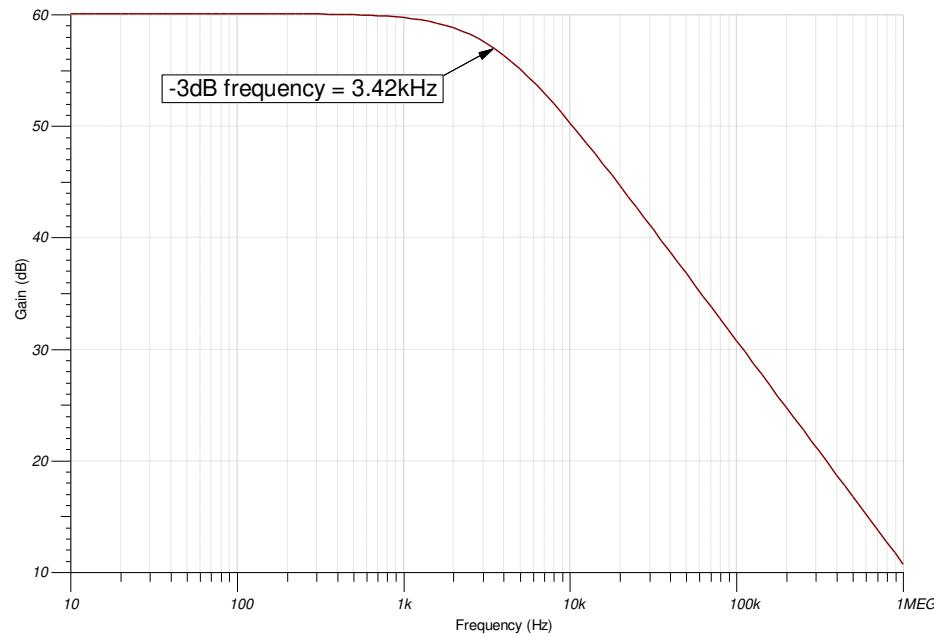
Design Simulations

DC Simulation Results

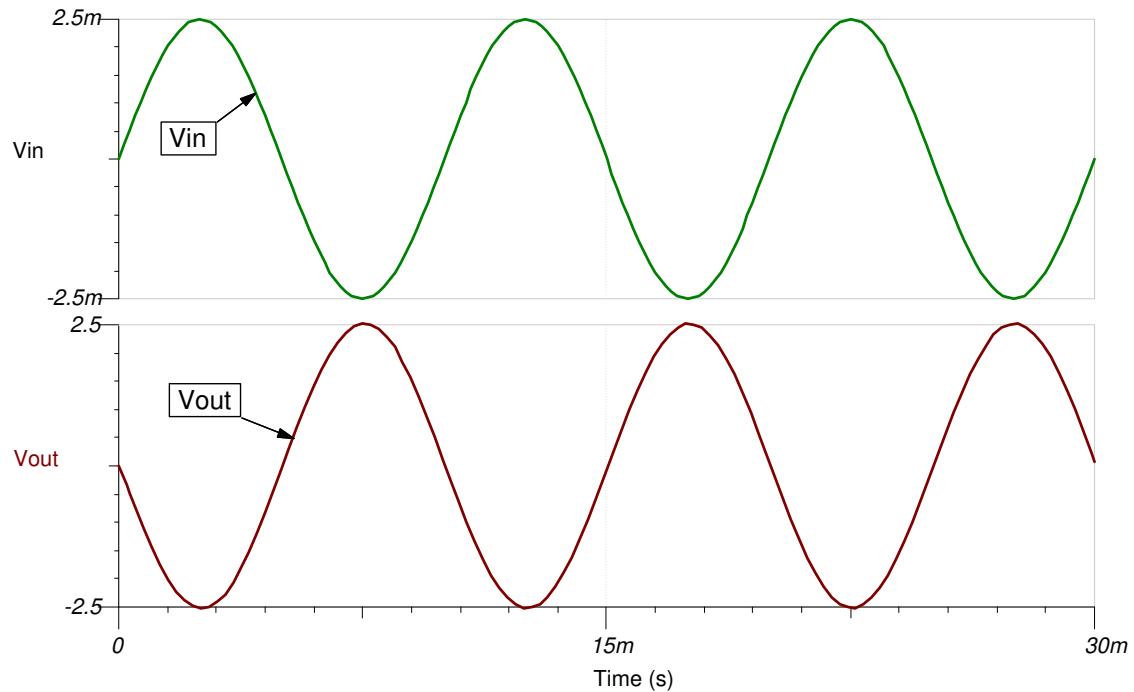


AC Simulation Results

The simulation is very close to the calculation.



Transient Simulation Results



Design References

1. See [Analog Engineer's Circuit Cookbooks](#) for the comprehensive TI circuit library.
2. [TI Precision Labs](#)
3. See the [1 MHz, Single-Supply, Photodiode Amplifier Reference Design](#).

Design Featured Op Amp

OPA192	
V_{ss}	$\pm 2.25V$ to $\pm 18V$
V_{inCM}	Rail-to-Rail
V_{out}	Rail-to-Rail
V_{os}	5 μV
I_q	1mA
I_b	5pA
UGBW	10MHz
SR	20V/ μs
#Channels	1, 2, 4
www.ti.com/product/OPA192	

Design Alternate Op Amp

TLV9062	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-Rail
V_{out}	Rail-to-Rail
V_{os}	0.3mV
I_q	538 μA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/ μs
#Channels	1,2,4
www.ti.com/product/TLV9062	

Inverting Op Amp with Non-Inverting Positive Reference Voltage Circuit

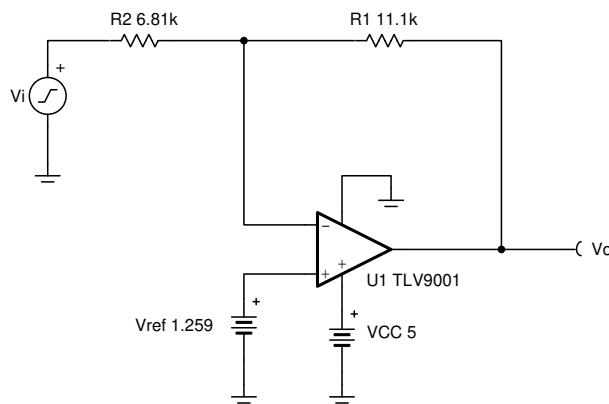


Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	V_{cc}	V_{ee}	V_{ref}
-1 V	2 V	0.05 V	4.95 V	5 V	0 V	1.259 V

Design Description

This design uses an inverting amplifier with a non-inverting positive reference voltage to translate an input signal of -1 V to 2 V to an output voltage of 0.05 V to 4.95 V. This circuit can be used to translate a sensor output voltage with a positive slope and negative offset to a usable ADC input voltage range.



Design Notes

1. Use op amp linear output operating range. Usually specified under A_{OL} test conditions.
2. Amplifier common mode voltage is equal to the reference voltage.
3. V_{ref} can be created with a voltage divider.
4. Input impedance of the circuit is equal to R_2 .
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100 kΩ. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to R_1 . Adding a capacitor in parallel with R_1 will also improve stability of the circuit, if high-value resistors are used.

Design Steps

$$V_o = -V_i \times \left(\frac{R_1}{R_2} \right) + V_{ref} \times \left(1 + \frac{R_1}{R_2} \right)$$

1. Calculate the gain of the input signal.

$$G_{input} = -\frac{R_1}{R_2}$$

$$V_{o_max} - V_{o_min} = (V_{i_max} - V_{i_min}) \left(-\frac{R_1}{R_2} \right)$$

$$-\frac{R_1}{R_2} = -\frac{V_{o_max} - V_{o_min}}{V_{i_max} - V_{i_min}} = -\frac{4.95V - 0.05V}{2V - (-1V)} = -1.633 \frac{V}{V}$$

2. Select R_2 and calculate R_1 .

$$R_2 = 6.81 \text{ k}\Omega$$

$$R_1 = G_{input} \times R_2 = 1.633 \frac{V}{V} \times 6.81 \text{ k}\Omega = 11.123 \text{ k}\Omega \approx 11.1 \text{ k}\Omega \text{ (Standard Value)}$$

3. Calculate the reference voltage.

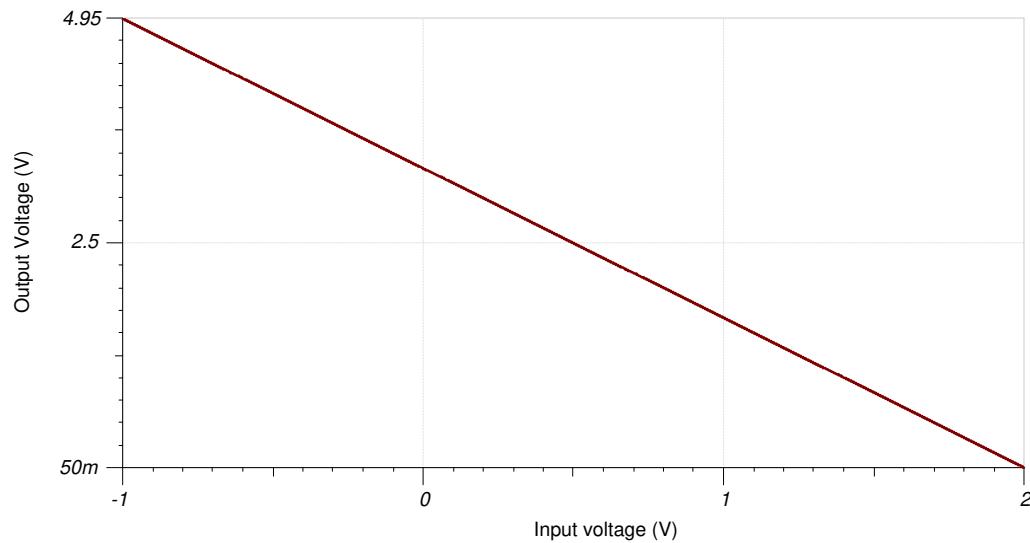
$$V_{o_min} = -V_{i_max} \times \left(\frac{R_1}{R_2} \right) + V_{ref} \times \left(1 + \frac{R_1}{R_2} \right)$$

$$0.05V = -2V \times \left(\frac{11.11 \text{ k}\Omega}{6.81 \text{ k}\Omega} \right) + V_{ref} \times \left(1 + \frac{11.11 \text{ k}\Omega}{6.81 \text{ k}\Omega} \right)$$

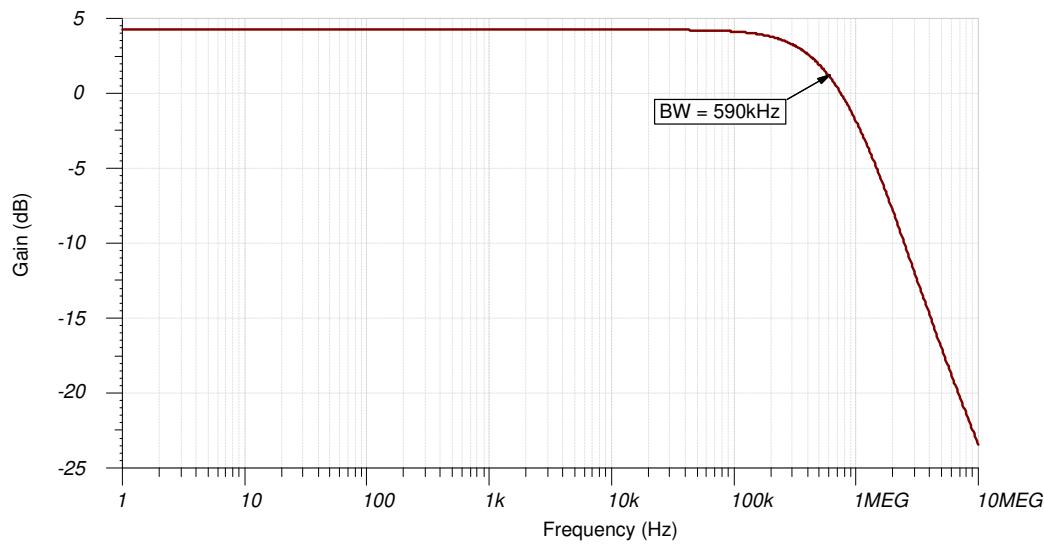
$$V_{ref} = \frac{V_{o_min} + V_{i_max} \times \left(\frac{R_1}{R_2} \right)}{\left(1 + \frac{R_1}{R_2} \right)} = \frac{0.05V + 2V \times \left(\frac{11.11 \text{ k}\Omega}{6.81 \text{ k}\Omega} \right)}{\left(1 + \frac{11.11 \text{ k}\Omega}{6.81 \text{ k}\Omega} \right)} = 1.259V$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOC514](#).

See [Designing Gain and Offset in Thirty Seconds](#).

Design Featured Op Amp

TLV9001	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.4 mV
I_q	60 μ A
I_b	5 pA
UGBW	1 MHz
SR	2 V/ μ s
#Channels	1, 2, and 4
TLV9001	

Design Alternate Op Amp

OPA376	
V_{ss}	2.2 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 μ V
I_q	760 μ A
I_b	0.2 pA
UGBW	5.5 MHz
SR	2 V/ μ s
#Channels	1, 2, and 4
OPA376	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.....

1

Single-Ended Input to Differential Output Circuit Using a Fully-Differential Amplifier



Sean Cashin

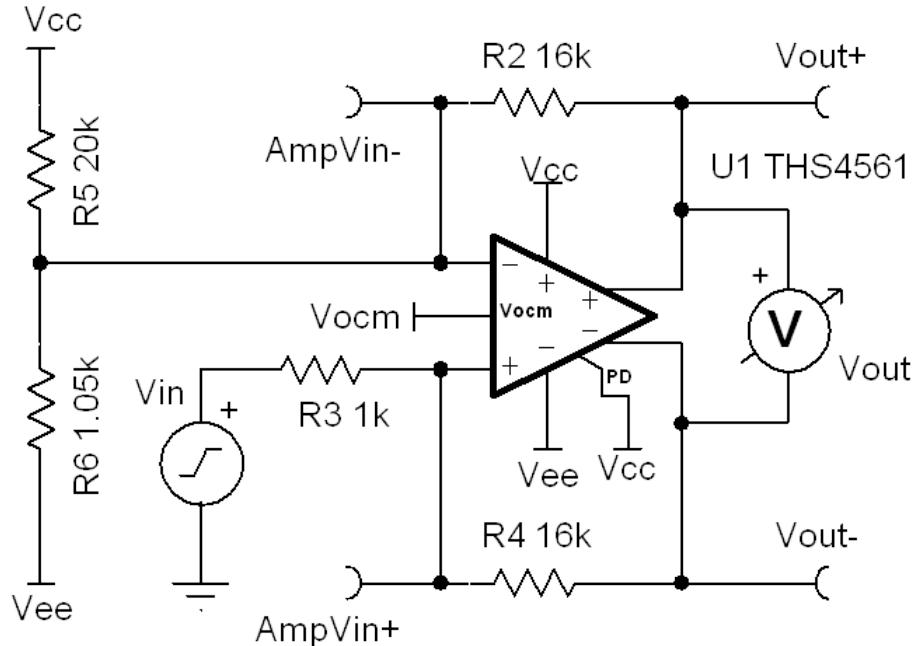
Design Goals

Input	Output	Supply	
Single-Ended	Differential	V_{cc}	V_{ee}
0 V to 1 V	16 Vpp	10 V	0 V

Output Common-Mode	3 dB Bandwidth	AC Gain (Gac)
5 V	3 MHz	16 V/V

Design Description

This design uses a fully-differential amplifier (FDA) as a single-ended input to differential output amplifier.



Design Notes

1. The ratio R_4/R_3 , equal to $R_2/(R_5||R_6)$, sets the gain of the amplifier.
2. The main difference between a single-ended input and a differential input is that the available input swing is only half. This is because one of the input voltages is fixed at a reference.
3. It is recommended to set this reference to mid-input signal range, rather than the min-input, to induce polarity reversal in the measured differential input. This preserves the ability of the outputs to crossover, which provides the doubling of output swing possible with an FDA.
4. The impedance of the reference voltage must be equal to the signal input resistor. This can be done by creating a resistor divider with a Thevenin equivalent of the correct reference voltage and impedance.

Design Steps

- Find the resistor divider with that produces a 0.5V, 1-kΩ reference from $V_s = 10V$.

$$\frac{R_6}{R_5 + R_6} F \quad \frac{0.5V}{10V} \quad \frac{R_5 \cdot R_6}{R_5 + R_6} E = 1k\Omega$$

$$R_6 = FR_5 + FR_6$$

$$R_6(1-F) = FR_5$$

$$R_5 = \frac{R_6(1-F)}{F}$$

$$\frac{R_6(1-F)/F \cdot R_6}{R_6(1-F)/F + R_6} E$$

$$\frac{R_6^2 \cdot (1-F)/F}{(R_6/F - R_6) + R_6} E$$

$$\frac{R_6^2 \cdot (1-F)/F}{R_6/F} E$$

$$R_6 \cdot (1-F) E$$

$$R_6 = \frac{E}{1-F} \frac{1k\Omega}{1-0.05} = 1.05k\Omega$$

$$R_5 = \frac{1.05\Omega(1-0.05)}{0.05} 20k\Omega$$

- Verify that the minimum input of 0 V and the maximum input of 1 V result in an output within the 9.4 V range available for $V_{ocm} = 5 V$.

Since the resistor divider acts like a 0.5 V reference, the measured differential input for a 0 V V_{IN} is:

$$V_{IN} = 0V - 0.5V = -0.5V$$

- The output is:

$$-0.5V \cdot \frac{16V}{V} = -8V > -9.8V$$

- Likewise, for a 1 V input:

$$V_{IN} = 1V - 0.5V = 0.5V$$

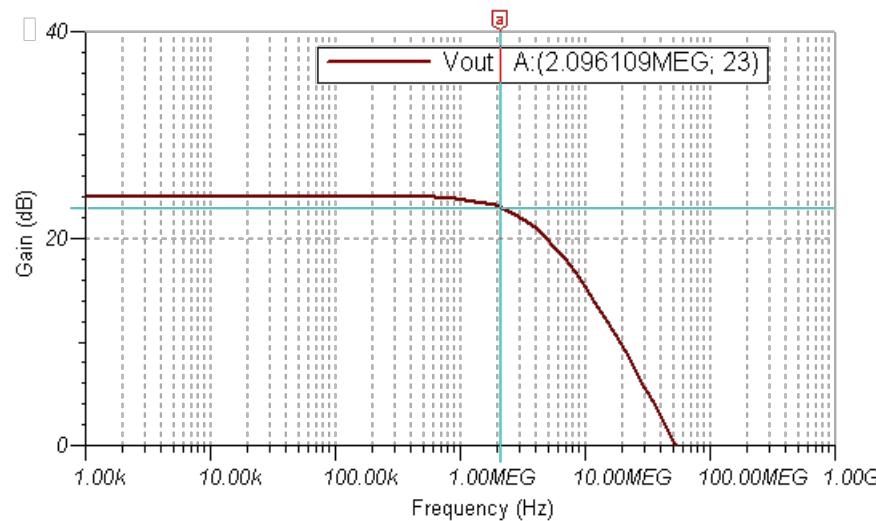
$$0.5V \cdot \frac{16V}{V} = 8V < 9.8V$$

Note

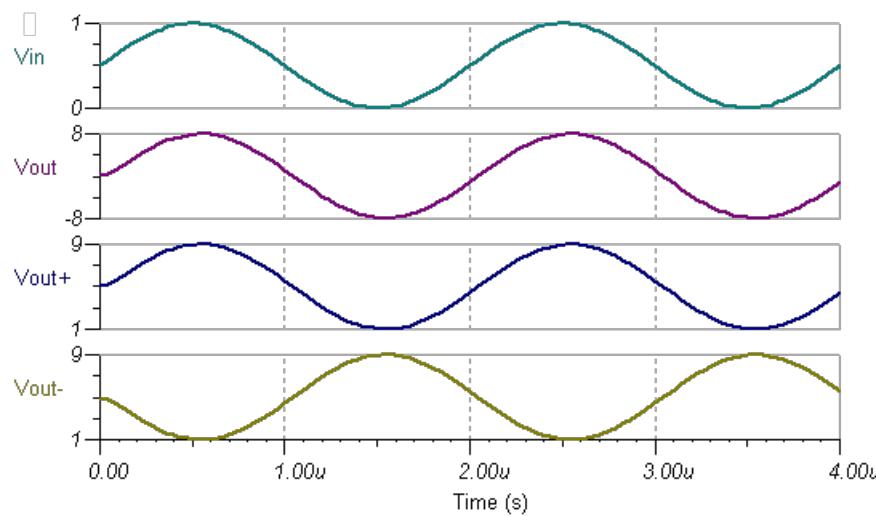
With a reference voltage of 0 V, a 1 V input results in an output voltage greater than the maximum output range of the amplifier.

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the TI Precision Labs video – [Op Amps: Fully Differential Amplifiers – Designing a Front-End Circuit for Driving a Differential Input ADC](#), for more information.

Design Featured Op Amp

THS4561	
V_{ss}	3 V to 13.5 V
V_{inCM}	$V_{ee}-0.1$ V to $V_{cc}-1.1$ V
V_{out}	$V_{ee}+0.2$ V to $V_{cc}-0.2$
V_{os}	TBD
I_q	TBD
I_b	TBD
UGBW	70 MHz
SR	4.4 V/ μ s
#Channels	1
THS4561	

Design Alternate Op Amp

THS4131	
V_{ss}	5 V to 33 V
V_{inCM}	$V_{ee}+1.3$ V to $V_{cc}-0.1$ V
V_{out}	Varies
V_{os}	2 mV
I_q	14 mA
I_b	2 μ A
UGBW	80 MHz
SR	52 V/ μ s
#Channels	1
THS4131	

Non-Inverting Op Amp with Inverting Positive Reference Voltage Circuit

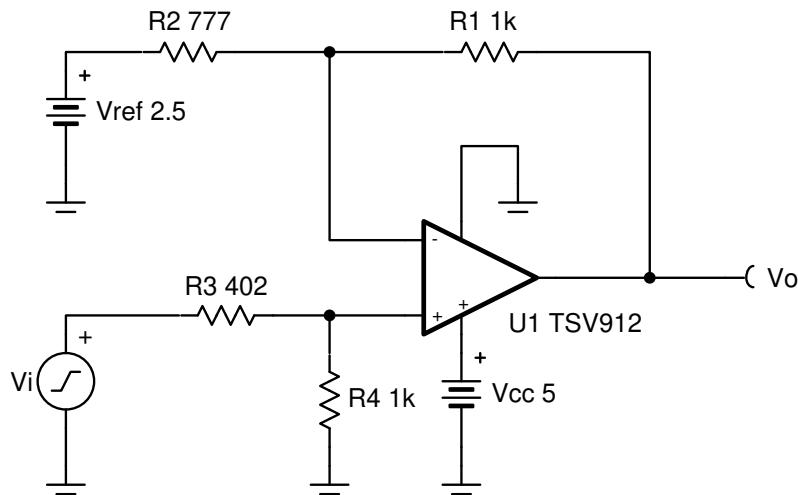


Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
2 V	5 V	0.05 V	4.95 V	5 V	0 V	2.5 V

Design Description

This design uses a non-inverting amplifier with an inverting positive reference to translate an input signal of 2 V to 5 V to an output voltage of 0.05 V to 4.95 V. This circuit can be used to translate a sensor output voltage with a positive slope and offset to a usable ADC input voltage range.



Design Notes

1. Use op amp linear output operating range. Usually specified under A_{OL} test conditions.
2. Check op amp input common mode voltage range. The common mode voltage varies with the input voltage.
3. V_{ref} must be low impedance.
4. Input impedance of the circuit is equal to the sum of R_3 and R_4 .
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100 k Ω . Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier.
7. Adding a capacitor in parallel with R_1 will improve stability of the circuit if high-value resistors are used.

Design Steps

$$V_o = V_i \times \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right) - V_{ref} \times \left(\frac{R_1}{R_2} \right)$$

1. Calculate the gain of the input to produce the largest output swing.

$$\begin{aligned} V_{o_max} - V_{o_min} &= (V_{i_max} - V_{i_min}) \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right) \\ \frac{V_{o_max} - V_{o_min}}{V_{i_max} - V_{i_min}} &= \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right) \\ \frac{4.95V - 0.05V}{5V - 2V} &= \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right) \\ 1.633 \frac{V}{V} &= \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right) \end{aligned}$$

2. Select a value for R_1 and R_4 and insert the values into the previous equation. The other two resistor values must be solved using a system of equations. The proper output swing and offset voltage cannot be calculated if more than two variables are selected.

$$\begin{aligned} R_1 &= R_4 = 1 \text{ k}\Omega \\ 1.633 \frac{V}{V} &= \left(\frac{1 \text{ k}\Omega}{R_3 + 1 \text{ k}\Omega} \right) \left(\frac{1 \text{ k}\Omega + R_2}{R_2} \right) \end{aligned}$$

3. Solve the previous equation for R_3 in terms of R_2 .

$$R_3 = \frac{1 \text{ M}\Omega + (1 \text{ k}\Omega \times R_2)}{1.633 \times R_2} - 1 \text{ k}\Omega$$

4. Select any point along the transfer function within the linear output range of the amplifier to set the proper offset voltage at the output (for example, the minimum input and output voltage).

$$\begin{aligned} V_{o_min} &= V_{i_min} \times \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_2} \right) - V_{ref} \times \left(\frac{R_1}{R_2} \right) \\ 0.05V &= 2V \times \left(\frac{1 \text{ k}\Omega}{R_3 + 1 \text{ k}\Omega} \right) \left(\frac{1 \text{ k}\Omega + R_2}{R_2} \right) - V_{ref} \times \left(\frac{1 \text{ k}\Omega}{R_2} \right) \end{aligned}$$

5. Insert R_3 from step 3 into the equation from step 4 and solve for R_2 .

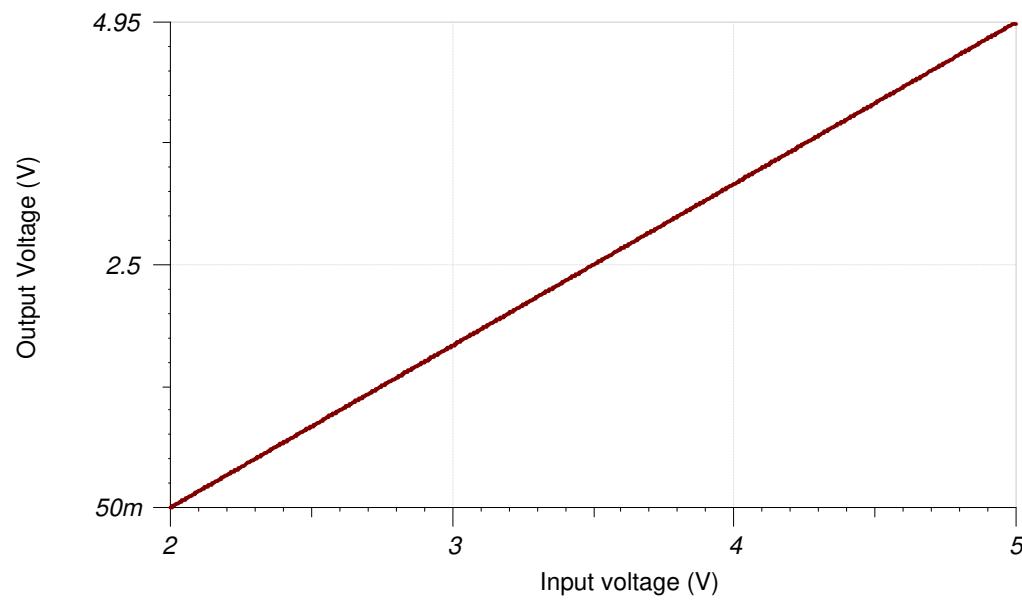
$$\begin{aligned} 0.05V &= 2V \times \left(\frac{\frac{1 \text{ k}\Omega}{\frac{1 \text{ M}\Omega + 1 \text{ k}\Omega \times R_2}{1.633 \times R_2} - 1 \text{ k}\Omega + 1 \text{ k}\Omega}}{1.633 \times R_2} \right) \left(\frac{1 \text{ k}\Omega + R_2}{R_2} \right) - V_{ref} \times \left(\frac{1 \text{ k}\Omega}{R_2} \right) \\ R_2 &= 777.2\Omega \approx 777\Omega \end{aligned}$$

6. Insert R_2 calculation from step 5, and solve for R_3 .

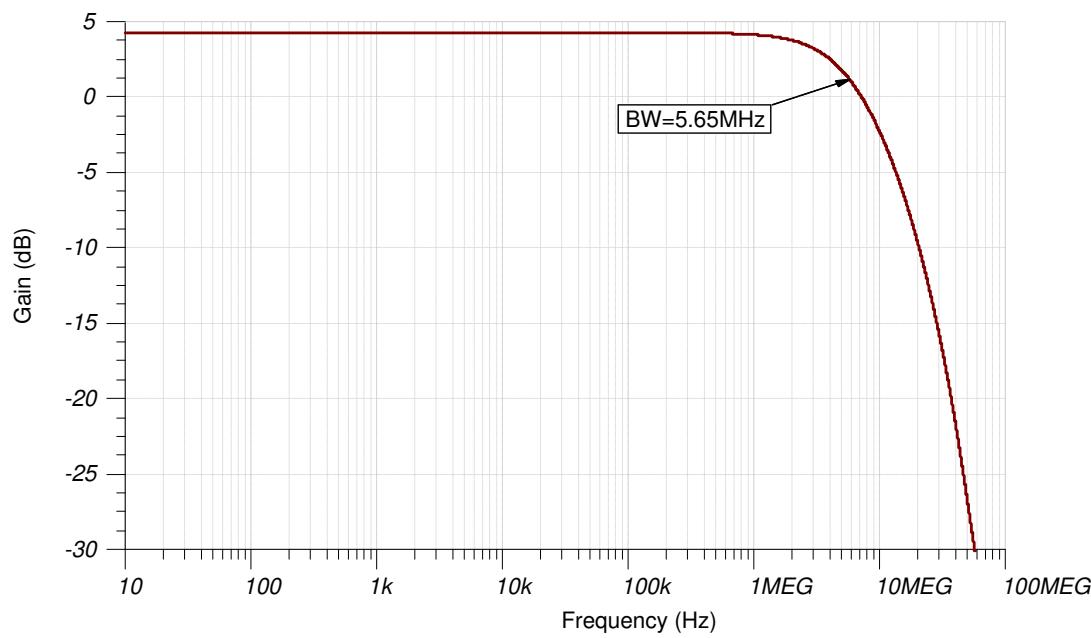
$$\begin{aligned} R_3 &= \frac{1 \text{ M}\Omega + (1 \text{ k}\Omega \times R_2)}{1.633 \times R_2} - 1 \text{ k}\Omega \\ R_3 &= \frac{1 \text{ M}\Omega + 1 \text{ k}\Omega \times (777\Omega)}{1.633 \times (777\Omega)} - 1 \text{ k}\Omega = 400.49\Omega \approx 402\Omega \end{aligned}$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See circuit SPICE simulation file [SBOC512](#).

See [TI Precision Lab Videos on Input and Output Limitations](#).

Design Featured Op Amp

TSV912	
V_{ss}	2.5 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3 mV
I_q	550 μ A
I_b	1 pA
UGBW	8 MHz
SR	4.5 V/ μ s
#Channels	1, 2, and 4
TSV912	

Design Alternate Op Amp

OPA191	
V_{ss}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 μ V
I_q	140 μ A/Ch
I_b	5 pA
UGBW	2.5 MHz
SR	5.5 V/ μ s
#Channels	1, 2, and 4
OPA191	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 4, 2019 to February 5, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file..... [1](#)

Single-Ended Input to Differential Output Circuit

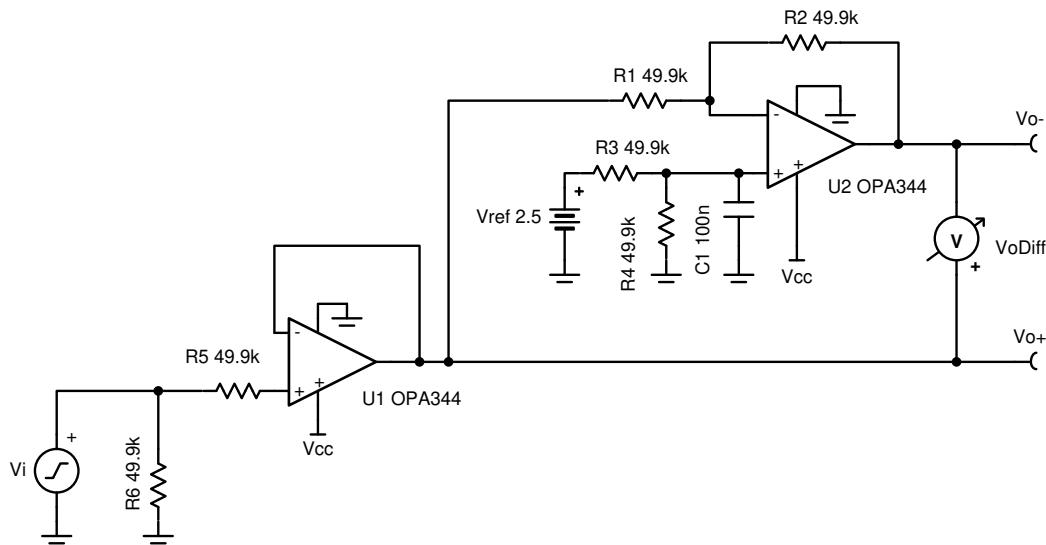


Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{DiffMin}}$	$V_{o\text{DiffMax}}$	V_{cc}	V_{ee}	V_{ref}
0.1 V	2.4 V	-2.3 V	2.3 V	2.7 V	0 V	2.5 V

Design Description

This circuit converts a single ended input of 0.1 V to 2.4 V into a differential output of ± 2.3 V on a single 2.7 V supply. The input and output ranges can be scaled as necessary as long as the op amp input common-mode range and output swing limits are met.



Design Notes

1. Op amps with rail-to-rail input and output will maximize the input and output range of the circuit.
2. Op amps with low V_{os} and offset drift will reduce DC errors.
3. Use low tolerance resistors to minimize gain error.
4. Set output range based on linear output swing (see A_{ol} specification).
5. Keep feedback resistors low or add capacitor in parallel with R_2 for stability.

Design Steps

1. Buffer V_i signal to generate V_{o+} .

$$V_{o+} = V_i$$

2. Invert and level shift V_{o+} using a difference amplifier to create V_{o-} .

$$V_{o-} = (V_{ref} - V_{o+}) \times \left(\frac{R_2}{R_1} \right)$$

3. Select resistances so that the resistor noise is smaller than the amplifier broadband noise.

$$E_{nv} = 30 \frac{nV}{\sqrt{Hz}} \text{ (Voltage noise from op amp)}$$

If $R_1 = R_2 = R_3 = R_4 = 49.9k\Omega$ then

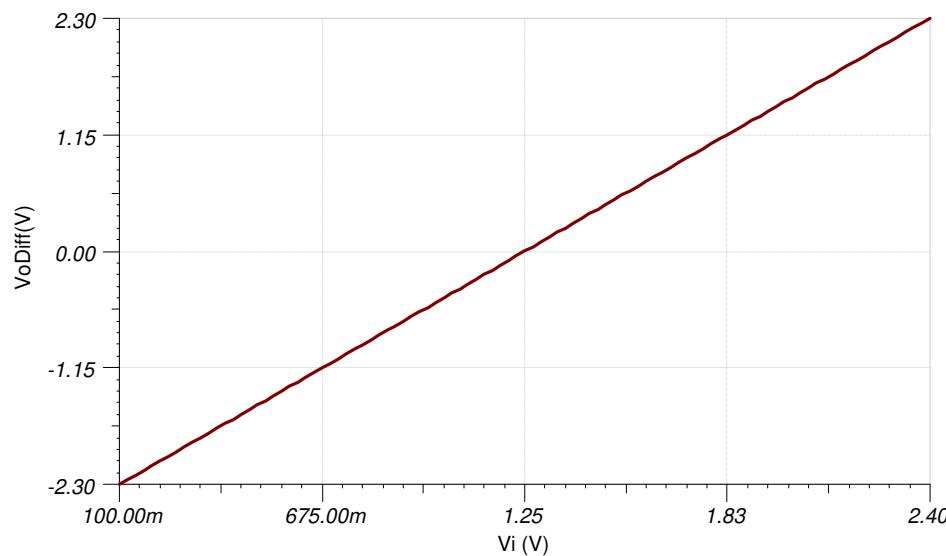
$$E_{nr} = \sqrt{\left(\sqrt{4 \times k_B \times T \times (R_1 || R_2)}\right)^2 + \left(\sqrt{4 \times k_B \times T \times (R_3 || R_4)}\right)^2} = 28.7 \frac{nV}{\sqrt{Hz}} (< E_{nv})$$

4. Select resistances that protect the input of the amplifier and prevents floating inputs. To simplify the bill of materials (BOM), select $R_5 = R_6$.

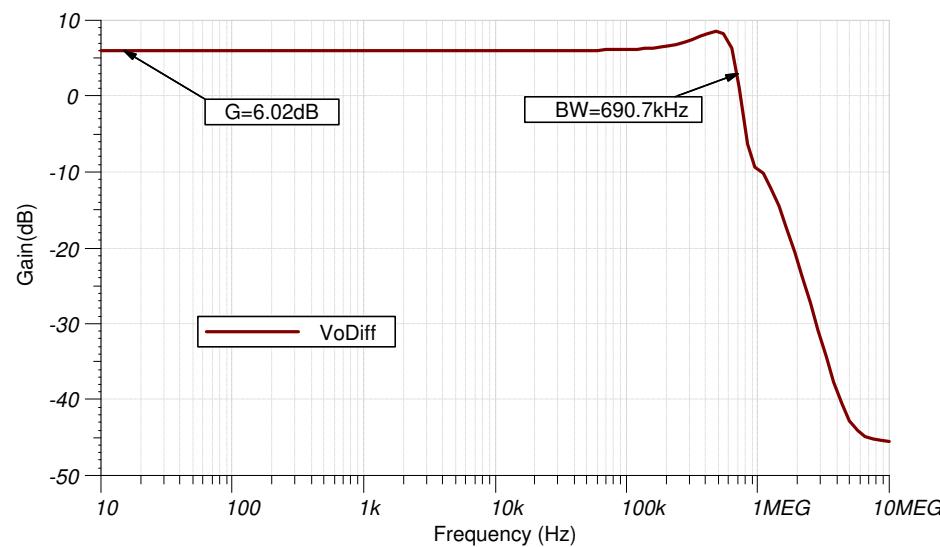
$$R_5 = R_6 = 49.9k\Omega$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOC510](#).

See TIPD131, [Single-Ended Input to Differential Output Conversion Circuit Reference Design](#).

Design Featured Op Amp

OPA344	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.2 mV
I_q	150 μ A
I_b	0.2 pA
UGBW	1 MHz
SR	0.8 V/ μ s
#Channels	1, 2, and 4
OPA344	

Design Alternate Op Amp

OPA335	
V_{ss}	2.7 V to 5.5 V
V_{inCM}	$V_{ee}-0.1$ V to $V_{cc}-1.5$ V
V_{out}	Rail-to-rail
V_{os}	1 μ V
I_q	285 μ A/Ch
I_b	70 pA
UGBW	2 MHz
SR	1.6 V/ μ s
#Channels	1 and 2
OPA335	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.....

1

Differential Input to Differential Output Circuit Using a Fully-Differential Amplifier



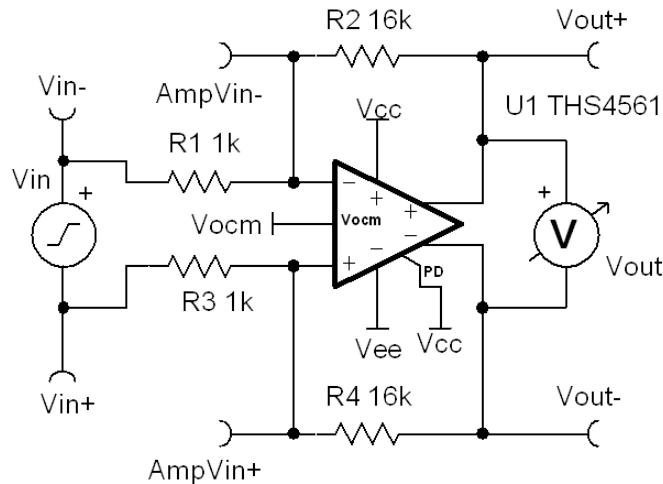
Sean Cashin

Design Goals

Input	Output	Supply	
Differential	Differential	V_{cc}	V_{ee}
1 Vpp	16 Vpp	10 V	0 V
Output Common-Mode		3 dB Bandwidth	AC Gain (Gac)
5 V		3 MHz	16 V/V

Design Description

This design uses a fully differential amplifier (FDA) as a differential input to differential output amplifier.



Design Notes

1. The ratio $R2/R1$, equal to $R4/R3$, sets the gain of the amplifier.
2. For a given supply, the output swing for an FDA is twice that of a single ended amplifier. This is because a fully differential amplifier swings both terminals of the output, instead of swinging one and fixing the other to either ground or a V_{ref} . The minimum voltage of an FDA is therefore achieved when $Vout+$ is held at the negative rail and $Vout-$ is held at the positive rail, and the maximum is achieved when $Vout+$ is held at the positive rail and $Vout-$ is held at the negative rail.
3. FDAs are useful for noise sensitive signals, since noise coupling equally into both inputs will not be amplified, as is the case in a single ended signal referenced to ground.
4. The output voltages will be centered about the output common-mode voltage set by $Vocm$.
5. Both feedback paths should be kept symmetrical in layout.

Design Steps

- Set the ratio R₂/ R₁ to select the AC voltage gain. To keep the feedback paths balanced,

$$R_1 = R_3 = 1\text{k}\Omega \text{ (Standard Value)}$$

$$R_2 = R_4 = R_1 \cdot (G_{AC}) = 1\text{k}\Omega \cdot \left(16 \frac{\text{V}}{\text{V}}\right) = 16\text{k}\Omega \text{ (Standard Value)}$$

- Given the output rails of 9.8 V and 0.2 V for V_s = 10 V, verify that 16 V_{pp} falls within the output range available for V_{ocm} = 5 V.

In normal operation:

$$\text{Amp}V_{IN+} = \text{Amp}V_{IN-}$$

$$V_{OUT+} - V_{ocm} = V_{ocm} - V_{OUT-}$$

$$V_{OUT} = V_{OUT+} - V_{OUT-}$$

- Rearrange to solve for each output voltage in edge conditions

$$V_{OUT-} = 2V_{ocm} - V_{OUT+}$$

$$V_{OUT-} = V_{OUT+} - V_{OUT}$$

$$2V_{OUT+} = 2V_{ocm} + V_{OUT}$$

$$V_{OUT+} = V_{ocm} + \frac{V_{OUT}}{2}$$

$$V_{OUT-} = V_{ocm} - \frac{V_{OUT}}{2}$$

- Verifying for Vout = +8 V and V_{ocm} = +5 V,

$$V_{OUT+} = 5 + \frac{8}{2} = 9\text{V} < 9.8\text{V}$$

$$V_{OUT-} = 5 - \frac{8}{2} = 1\text{V} > 0.2\text{V}$$

- Verifying for Vout = -8 V and V_{ocm} = +5 V,

$$V_{OUT+} = 5 + \frac{-8}{2} = 1\text{V} > 0.2\text{V}$$

$$V_{OUT-} = 5 - \frac{-8}{2} = 9\text{V} > 9.8\text{V}$$

Note that the maximum swing possible is:

$$(9.8\text{V} - 0.2\text{V}) - (0.2\text{V} - 9.8\text{V}) = 18.4\text{V}_{pp}, \text{ or } \pm 9.4\text{V}$$

- Use the input common mode voltage range of the amplifier and the feedback resistor divider to find the signal input range when the output range is 1 V to 9 V. Due to symmetry, calculation of one side is sufficient.

$$\text{Min}(\text{AmpV}_{\text{IN}_+}) = \text{Min}(\text{AmpV}_{\text{IN}_-}) = \text{Vee} - 0.1\text{V} = -0.1\text{V}$$

$$\text{Max}(\text{AmpV}_{\text{IN}_+}) = \text{Max}(\text{AmpV}_{\text{IN}_-}) = \text{Vcc} - 1.1\text{V} = 8.9\text{V}$$

$$\frac{\text{AmpV}_{\text{IN}_-} - \text{V}_{\text{IN}_-}}{R_1} = \frac{\text{V}_{\text{OUT}_+} - \text{AmpV}_{\text{IN}_-}}{R_2}$$

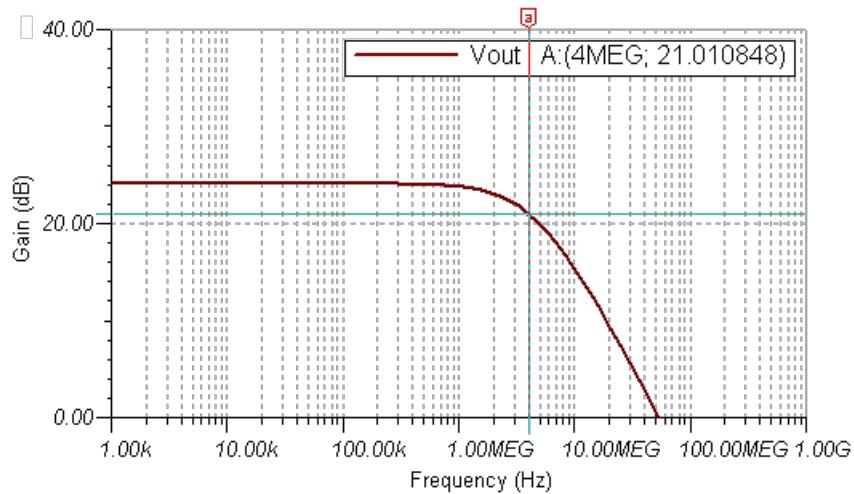
$$\text{V}_{\text{IN}_-} = \text{AmpV}_{\text{IN}_-} - \frac{\text{V}_{\text{OUT}_+} - \text{AmpV}_{\text{IN}_-}}{\frac{R_2}{R_1}}$$

$$\text{Min}(\text{V}_{\text{IN}_-}) = -0.1\text{V} - \frac{9\text{V} - (-0.1\text{V})}{16 \frac{\text{V}}{\text{V}}} = -0.65\text{V}$$

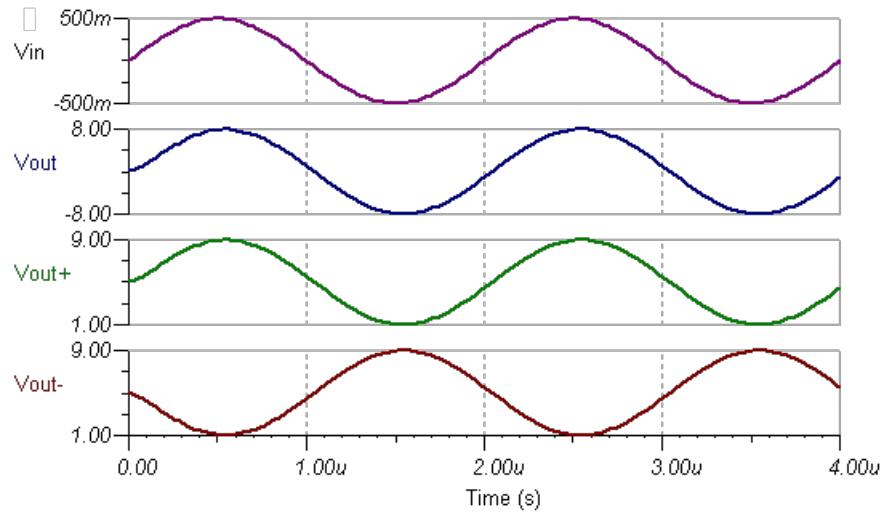
$$\text{Max}(\text{V}_{\text{IN}_-}) = 8.9\text{V} + \frac{8.9\text{V} - 1\text{V}}{16 \frac{\text{V}}{\text{V}}} = 9.4\text{V}$$

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the [TIDA-01036](#) tool folder for more information.

Design Featured Op Amp

THS4561	
V_{ss}	3 V to 13.5 V
V_{inCM}	V _{ee} -0.1 V to V _{cc} -1.1 V
V_{out}	V _{ee} +0.2 V to V _{cc} -0.2
V_{os}	TBD
I_q	TBD
I_b	TBD
UGBW	70 MHz
SR	4.4 V/μs
#Channels	1
THS4561	

Design Alternate Op Amp

THS4131	
V_{ss}	5 V to 33 V
V_{inCM}	V _{ee} +1.3 V to V _{cc} -0.1 V
V_{out}	Varies
V_{os}	2 mV
I_q	14 mA
I_b	2 μA
UGBW	80 MHz
SR	52 V/μs
#Channels	1
THS4131	

AC Coupled Instrumentation Amplifier Circuit

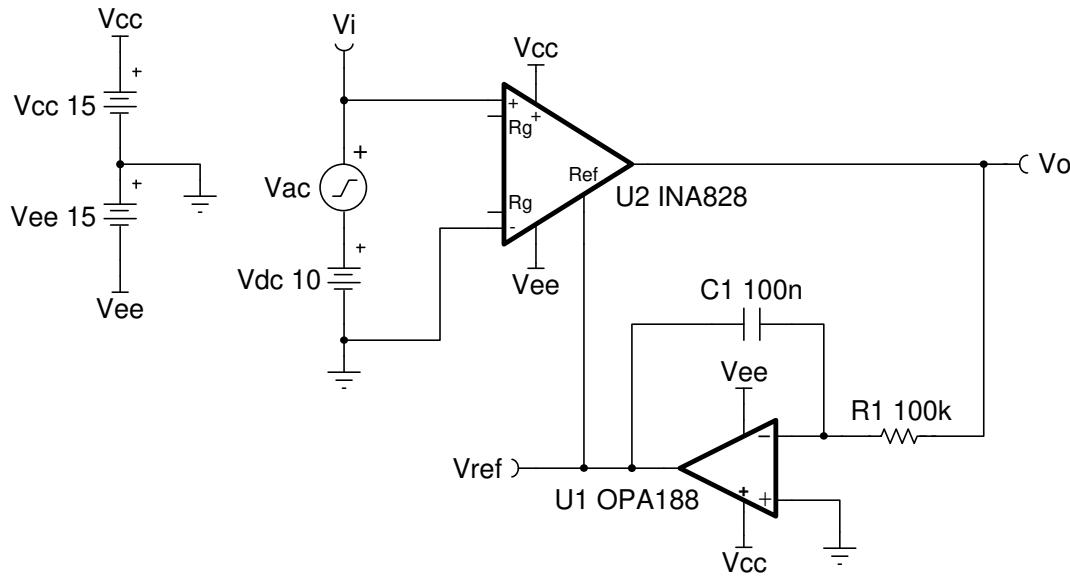


Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
-13 V	13 V	-14.85 V	14.85	15	-15
Lower Cutoff Frequency (f_L)		Gain		Input	
16 Hz		1		$\pm 2\text{VAC}; +10\text{VDC}$	

Design Description

This circuit produces an AC-coupled output from a DC-coupled input to an instrumentation amplifier. The output is fed back through an integrator, and the output of the integrator is used to modulate the reference voltage of the amplifier. This creates a high-pass filter and effectively cancels the output offset. This circuit avoids the need for large capacitors and resistors on the input, which can significantly degrade CMRR due to component mismatch.



Design Notes

1. The DC correction from output to reference is unity-gain. U_1 can only correct for a signal within its input/output limitations, thus the magnitude of DC voltage that can be corrected for will degrade with increasing instrumentation amplifier gain. See the table in Design Steps for more information.
2. Large values of R_1 and C_1 will lower the cutoff frequency, but increase startup transient response time. Startup behavior can be observed in the Transient Simulation Results.
3. When AC-coupling this way, the total input voltage must remain within the common-mode input range of the instrumentation amplifier.

Design Steps

- Set the lower cutoff frequency for circuit (integrator cutoff frequency). The upper cutoff frequency will be dictated by the gain and instrumentation amplifier bandwidth.

$$f_L = \frac{1}{2\pi \times R_1 \times C_1} = 16 \text{ Hz}$$

- Choose a standard value for R_1 and C_1 .

$$C_1 = 100 \text{ nF}$$

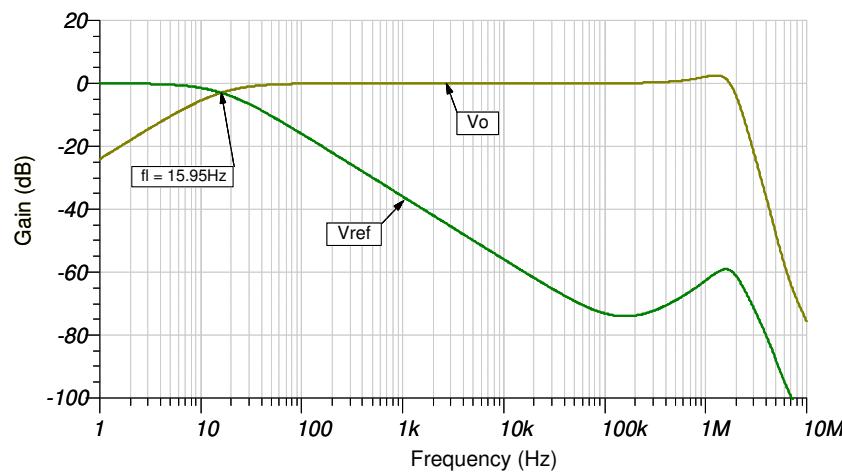
$$R_1 = \frac{1}{2\pi \times 100 \text{ nF} \times 16 \text{ Hz}} = 99.47 \text{ k}\Omega \approx 100 \text{ k}\Omega \text{ (standard value)}$$

- The DC rejection capabilities of the circuit will degrade with gain. The following table provides a good estimate of the DC correction range for higher gains.

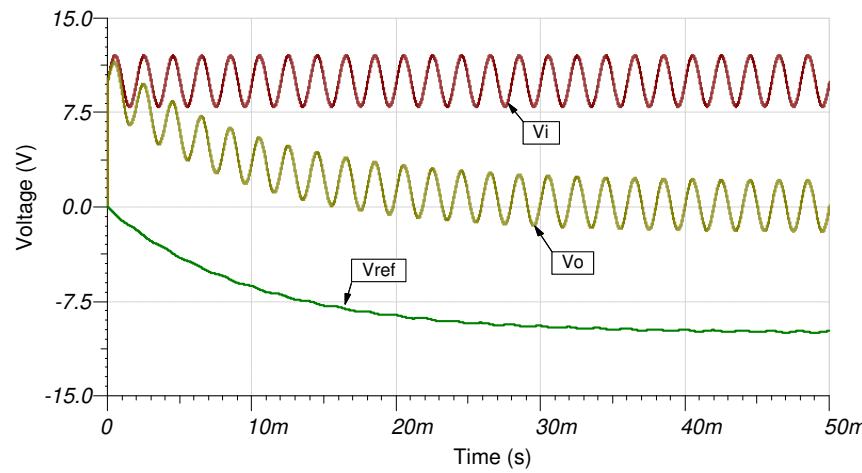
Gain	DC Correction Range
1 V/V	$\pm 10 \text{ V}$
10 V/V	$\pm 1 \text{ V}$
100 V/V	$\pm 0.1 \text{ V}$
1000 V/V	$\pm 0.01 \text{ V}$

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See TINA-TI™ circuit simulation file, [SBOMAU0](#).

See TIPD191, [Instrumentation Amplifier with DC Rejection Reference Design](#).

Design Featured Instrumentation Amplifier

INA828	
V_{ss}	4.5 V to 36 V
V_{inCM}	V _{ee} +2 V to V _{cc} -2 V
V_{out}	V _{ee} +150 mV to V _{cc} -150 mV
V_{os}	20 μ V
I_q	600 μ A
I_b	150 pA
UGBW	2 MHz
SR	1.2 V/ μ s
#Channels	1
INA828	

Design Featured Op Amp

OPA188	
V_{ss}	8 V to 36 V
V_{inCM}	V _{ee} to V _{cc} -1.5 V
V_{out}	Rail-to-rail
V_{os}	6 μ V
I_q	450 μ A
I_b	\pm 160 pA
UGBW	2 MHz
SR	0.8 V/ μ s
#Channels	1, 2, and 4
OPA188	

Design Alternate Op Amp

TLV171	
V_{ss}	2.7 V to 36 V
V_{inCM}	V _{ee} -0.1 V to V _{cc} -2 V
V_{out}	Rail-to-rail
V_{os}	750 μ V
I_q	525 μ A
I_b	\pm 10 pA
UGBW	3 MHz
SR	1.5 V/ μ s
#Channels	1, 2, and 4
TLV171	

Analog Engineer's Circuit

Inverting attenuator circuit



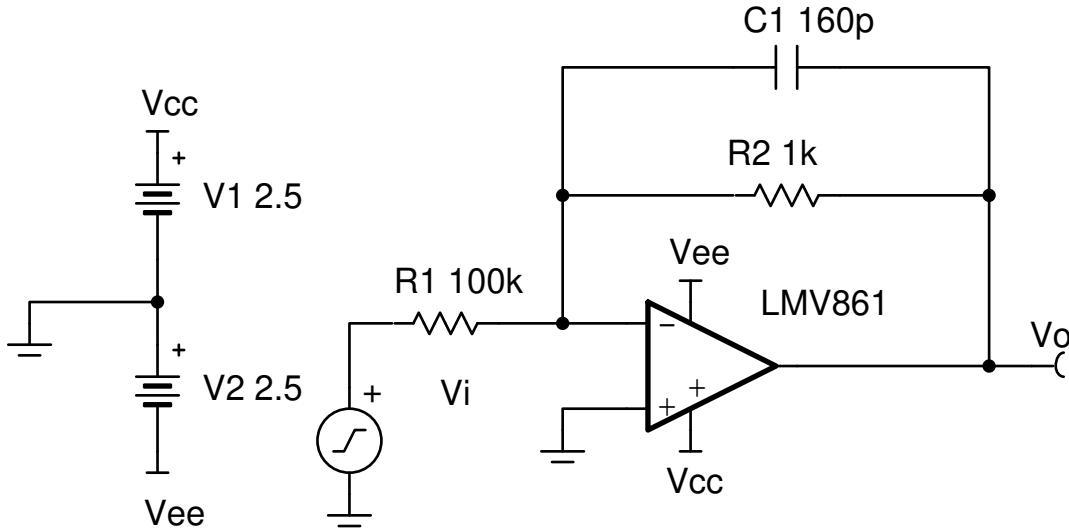
Amplifiers

Design Goals

Input		Output		BW	Gain	Supply	
V _{iMin}	V _{iMax}	V _{oMin}	V _{oMax}	f _p	G	V _{cc}	V _{ee}
-200V	200V	-2V	2V	1MHz	-40dB	2.5V	-2.5V

Design Description

This circuit inverts the input signal, V_i , and applies a signal gain of -40dB. The common-mode voltage of an inverting amplifier is equal to the voltage applied to the non-inverting input, which is ground in this design.



Design Notes

1. The common-mode voltage in this circuit does not vary with input voltage.
2. The input impedance is determined by the input resistor. Make sure this value is large when compared to the output impedance of the source.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit. The capacitor in parallel with R_2 provides filtering and improves stability of the circuit if high-value resistors are used for both the input and feedback resistances.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP).
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth see the [Design References](#) section.
8. Note that higher input voltage levels may require the use of multiple resistors in series to help reduce the voltage drop across the individual resistors. For more information, see the [Design References](#) section.

Design Steps

The transfer function of this circuit follows:

$$V_o = V_i \times \left(-\frac{R_2}{R_1} \right)$$

1. Calculate the gain required for the circuit.

$$G = \frac{V_{oMax} - V_{oMin}}{V_{iMax} - V_{iMin}} = \frac{2V - (-2V)}{200V - (-200V)} = 0.01 \frac{V}{V} = -40\text{dB}$$

2. Choose the starting value of R_1 .

$$R_1 = 100\text{k}\Omega$$

3. Calculate for a desired signal attenuation of 0.01 V/V.

$$G = \frac{R_2}{R_1} \rightarrow R_2 = R_1 \times G = 0.01 \frac{V}{V} \times 100\text{k}\Omega = 1\text{k}\Omega$$

4. Select the feedback capacitor, C_1 , to meet the circuit bandwidth.

$$C_1 \leq \frac{1}{2\pi \times R_2 \times f_p} \rightarrow C_1 \leq \frac{1}{2\pi \times 1\text{k}\Omega \times 1\text{MHz}} \leq 159.15\text{pF} \approx 160\text{pF} \text{ (Standard Value)}$$

5. Calculate the minimum slew rate required to minimize slew-induced distortion.

$$V_p < \frac{SR}{2\pi \times f_p} \rightarrow SR > 2\pi \times f \times V_p \rightarrow SR > 2\pi \times 1\text{MHz} \times 2\text{V} = 12.6 \frac{\text{V}}{\mu\text{s}}$$

- $SR_{LMV861} = 18\text{V}/\mu\text{s}$; therefore, it meets this requirement.

6. Calculate the circuit bandwidth to ensure it meets the 1-MHz requirement. Be sure to use the noise gain, NG, or non-inverting gain, of the circuit.

$$NG = 1 + \frac{R_2}{R_1} = 1.01 \frac{V}{V} \rightarrow BW = \frac{GBP}{NG} = \frac{30\text{MHz}}{1.01 \frac{V}{V}} = 29.7\text{MHz}$$

- $BW_{LMV861} = 30\text{MHz}$; therefore, it meets this requirement.

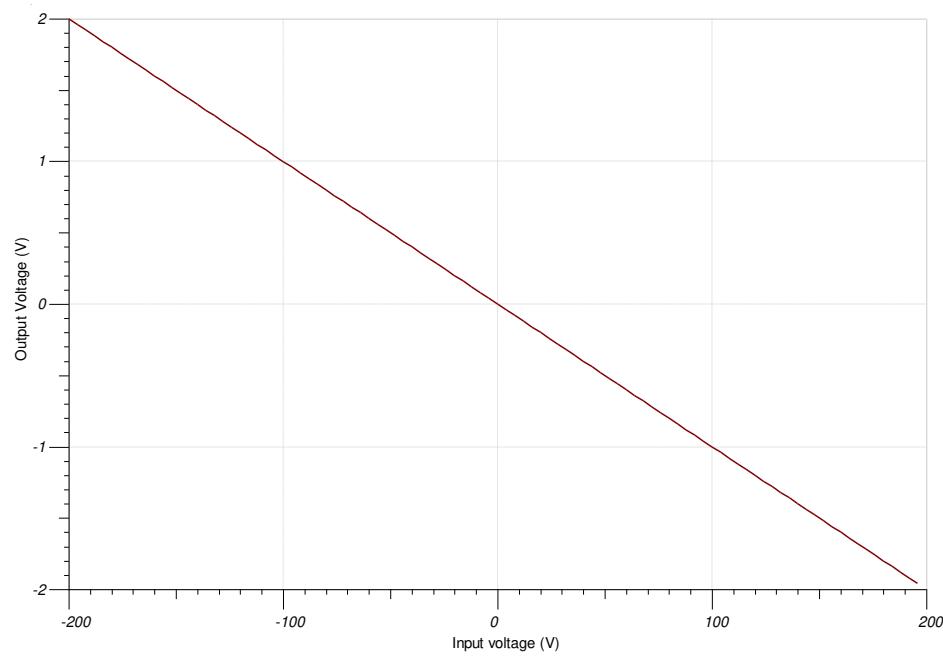
7. If C_1 is not used to limit the circuit bandwidth, to avoid stability issues ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

$$\frac{1}{2\pi \times (C_{cm} + C_{diff}) \times (R_2 \parallel R_1)} > \frac{GBP_{LMV861}}{NG}$$

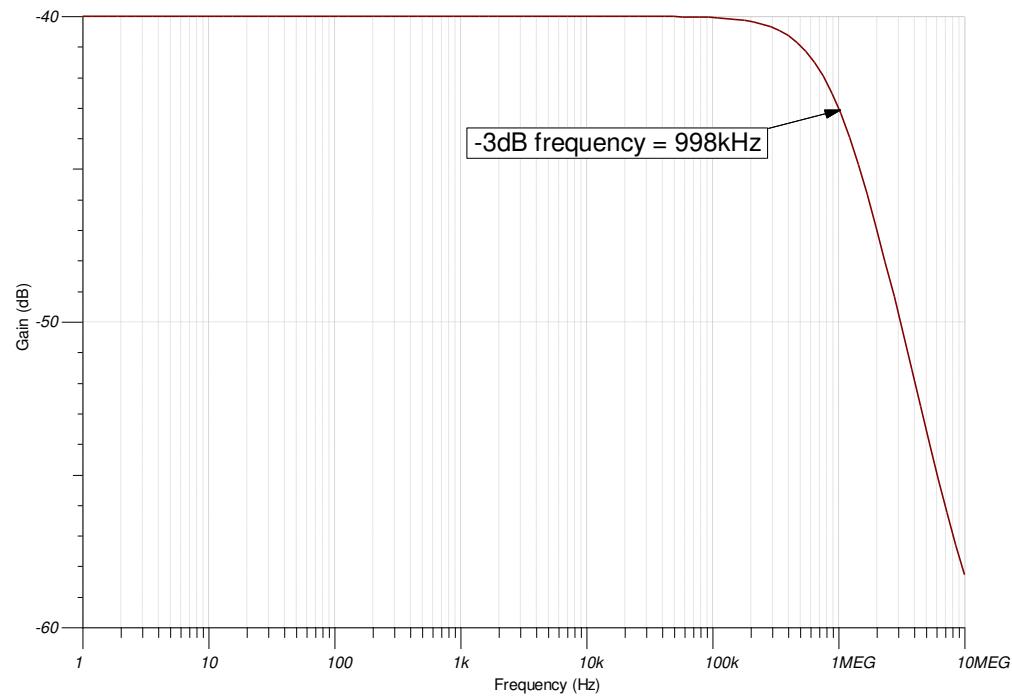
- C_{cm} and C_{diff} are the common-mode and differential input capacitance of the LMV861, respectively.

Design Simulations

DC Simulation Results

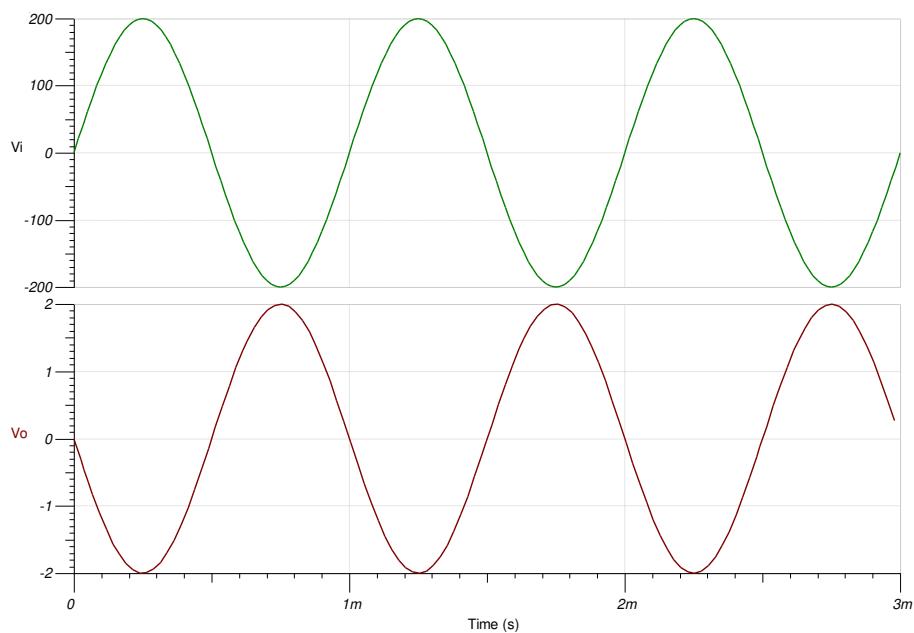


AC Simulation Results



Transient Simulation Results

A 1-kHz, 400-Vpp input sine wave yields a 4-Vpp output sine wave.



Design References

1. See *Analog Engineer's Circuit Cookbooks* for the comprehensive TI circuit library.
2. SPICE Simulation File SBOC522.
3. [TI Precision Labs](#)
4. For more information on circuits with larger input voltages, see *Considerations for High-Voltage Measurements*.

Design Featured Op Amp

LMV861	
V_{ss}	2.7V to 5.5V
V_{inCM}	(Vee – 0.1V) to (Vcc – 1.1V)
V_{out}	Rail-to-rail
V_{os}	0.273mV
I_q	2.25mA
I_b	0.1pA
UGBW	30MHz
SR	18V/µs
#Channels	1, 2
www.ti.com/product/LMV861	

Design Alternate Op Amp

	TLV9002	OPA377
V_{ss}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{out}	Rail-to-rail	Rail-to-rail
V_{os}	0.4mV	0.25mV
I_q	0.06mA	0.76mA
I_b	5pA	0.2pA
UGBW	1MHz	5.5MHz
SR	2V/µs	2V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/TLV9002	www.ti.com/product/OPA377

Analog Engineer's Circuit Amplifiers

Discrete Wide Bandwidth INA Circuit

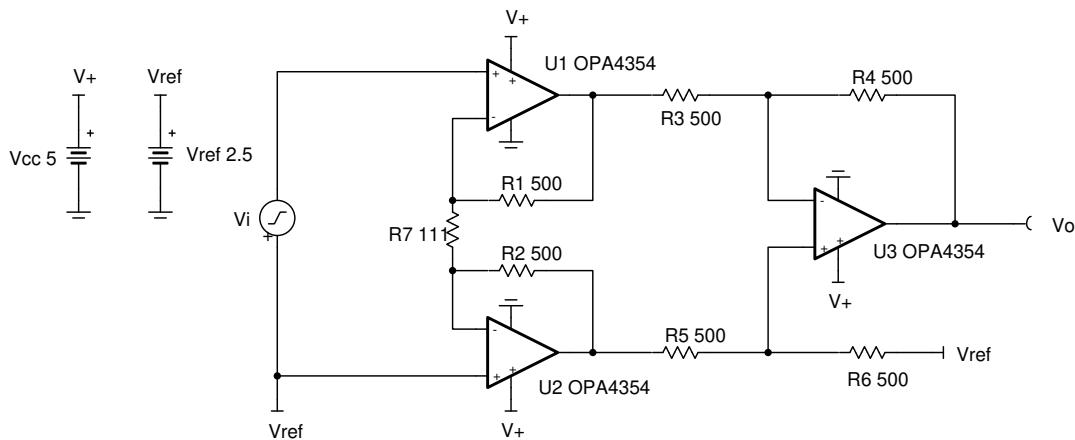


Design Goals

Input		Output		Bandwidth	Supply		
V _{iMin}	V _{iMax}	V _{oMin}	V _{oMax}	BW	V _{cc}	V _{ee}	V _{ref}
-0.24V	+0.24V	+0.1V	+4.9V	10MHz	+2.5V	0V	2.5V

Design Description

This design uses 3 op-amps to build a discrete wide bandwidth instrumentation amplifier. The circuit converts a differential, high frequency signal to a single-ended output.



Design Notes

1. Reduce the capacitance on the output of each op amp to avoid stability issues.
2. Use low gain configurations to maximize the bandwidth of the circuit.
3. Use precision resistors to achieve high DC CMRR performance.
4. Use small resistors in op-amp feedback to maintain stability.
5. Set the reference voltage, V_{ref} , at mid-supply to allow the output to swing to both supply rails.
6. Phase margin of 45° or greater is required for stable operation.
7. R_7 sets the gain of the instrumentation amplifier.
8. Linear operation depends upon the input common-mode and the output swing ranges of the discrete op amps used. The linear output swing ranges are specified under the A_{ol} test conditions in the op amps datasheets.
9. V_{ref} also sets the common-mode voltage of the input, V_i , to ensure linear operation.

Design Steps

1. The transfer function of the circuit is given below.

$$V_o = V_i \times \left(1 + \frac{2 \times R_1}{R_7}\right) \times \left(\frac{R_6}{R_5}\right)$$

where V_i is the differential input voltage

V_{ref} is the reference voltage provided to the amplifier

$$Gain = \left(1 + \frac{2 \times R_1}{R_7}\right) \times \left(\frac{R_6}{R_5}\right)$$

2. To maximize the usable bandwidth of design, set the gain of the diff amp stage to 1V/V. Use smaller value resistors to minimize noise.

Choose $R_3 = R_4 = R_5 = R_6 = 500 \Omega$ (Standard value)

3. Choose values for resistors R_1 and R_2 . Keep these values low to minimize noise.

$R_1 = R_2 = 500 \Omega$ (Standard value)

4. Calculate resistor R_7 to set the gain of the circuit to 10V/V

$$G = \left(1 + \frac{2 \times R_1}{R_7}\right) = 10 \frac{V}{V} \rightarrow \frac{2 \times 500\Omega}{R_7} = 9 \frac{V}{V}$$

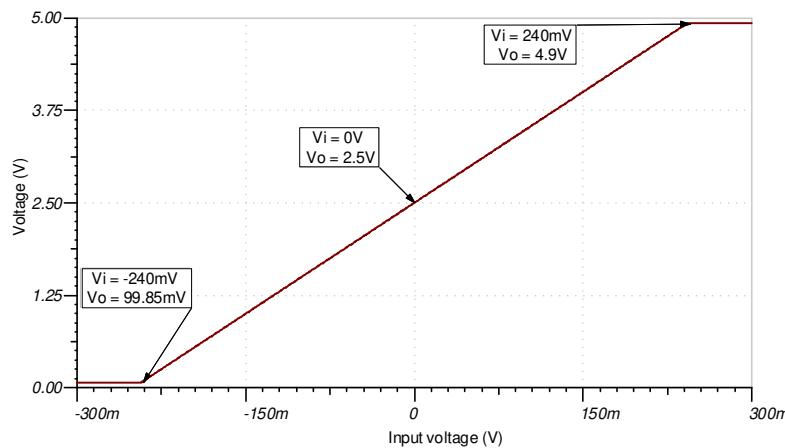
$$R_7 = \frac{1000\Omega}{9 \frac{V}{V}} = 111.11\Omega \rightarrow R_7 = 111\Omega \text{ (Standard Value)}$$

5. Calculate the reference voltage to bias the input to mid-supply. This will maximize the linear output swing of the instrumentation amplifier. See References for more information on the linear operating region of instrumentation amplifiers.

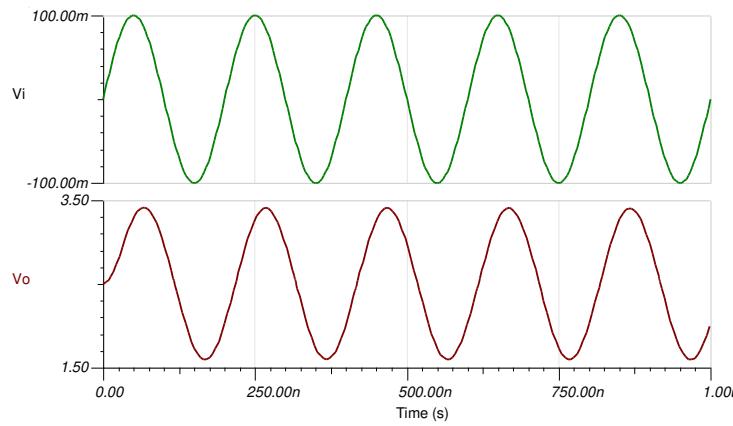
$$V_{ref} = \frac{V_s}{2} = \frac{5 \text{ V}}{2} = 2.5 \text{ V}$$

Design Simulations

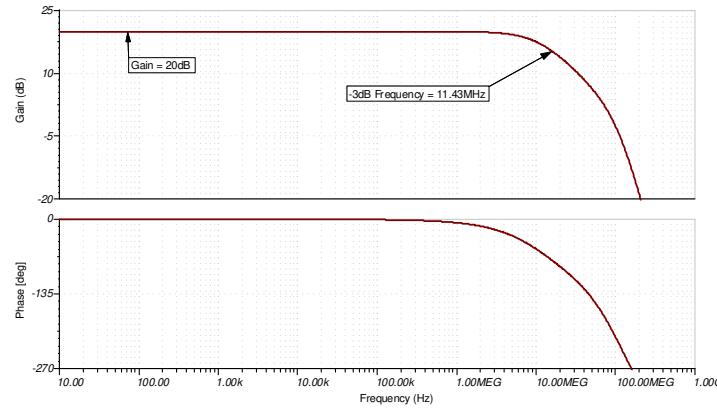
DC Simulation Results



Transient Simulation Results



AC Simulation Results



References

1. [Analog Engineer's Circuit Cookbooks](#)
2. [SPICE Simulation File SBOMAU6](#)
3. [TI Precision Labs](#)
4. [Instrumentation Amplifier \$V_{CM}\$ vs. \$V_{OUT}\$ Plots](#)
5. [Common-mode Range Calculator for Instrumentation Amplifiers](#)

Design Featured Op Amp

OPA354	
V_{ss}	2.5V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	2mV
I_q	4.9mA/Ch
I_b	3pA
UGBW	250MHz
SR	150V/ μ s
#Channels	1,2,4
www.ti.com/product/opa354	

Design Alternate Op Amp

OPA322	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	500 μ V
I_q	1.6mA/Ch
I_b	0.2pA
UGBW	20MHz
SR	10V/ μ s
#Channels	1,2,4
www.ti.com/product/opa322	

Revision History

Revision	Date	Change
A	December 2020	Updated R11 to R7 for resistor number consistency

Inverting Op Amp with Inverting Positive Reference Voltage Circuit

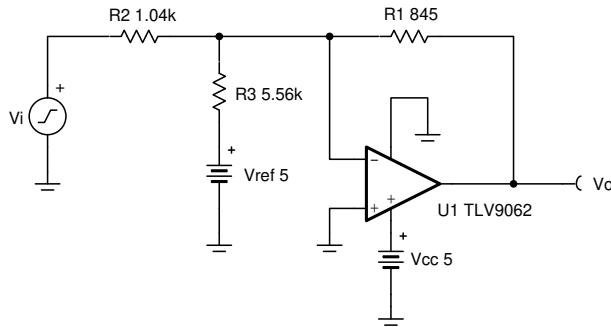


Design Goals

Input		Output		Supply		
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	V_{cc}	V_{ee}	V_{ref}
-5 V	-1 V	0.05 V	3.3 V	5 V	0 V	5 V

Design Description

This design uses an inverting amplifier with an inverting positive reference to translate an input signal of -5 V to -1 V to an output voltage of 3.3 V to 0.05 V. This circuit can be used to translate a negative sensor output voltage to a usable ADC input voltage range.



Design Notes

1. Use op amp linear output operating range. Usually specified under A_{OL} test conditions.
2. Common mode range must extend down to or below ground.
3. V_{ref} output must be low impedance.
4. Input impedance of the circuit is equal to R_2 .
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100 kΩ. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to R_1 . Adding a capacitor in parallel with R_1 will also improve stability of the circuit if high-value resistors are used.

Design Steps

$$V_o = -V_i \times \left(\frac{R_1}{R_2} \right) - V_{ref} \times \left(\frac{R_1}{R_3} \right)$$

1. Calculate the gain of the input signal.

$$G_{input} = \frac{V_{o_max} - V_{o_min}}{V_{i_max} - V_{i_min}} = \frac{3.3V - 0.05V}{-1V - (-5\text{ V})} = 0.8125 \frac{V}{V}$$

2. Calculate R_1 and R_2 .

Choose $R_1 = 845\Omega$

$$R_2 = \frac{R_1}{G_{input}} = \frac{R_1}{0.8125 \frac{V}{V}} = 1.04 \text{ k}\Omega$$

3. Calculate the gain of the reference voltage required to offset the output.

$$G_{ref} = \frac{R_1}{R_3}$$

$$-V_{i_min} \times \left(\frac{R_1}{R_2} \right) - V_{ref} \times \left(\frac{R_1}{R_3} \right) = V_{o_min}$$

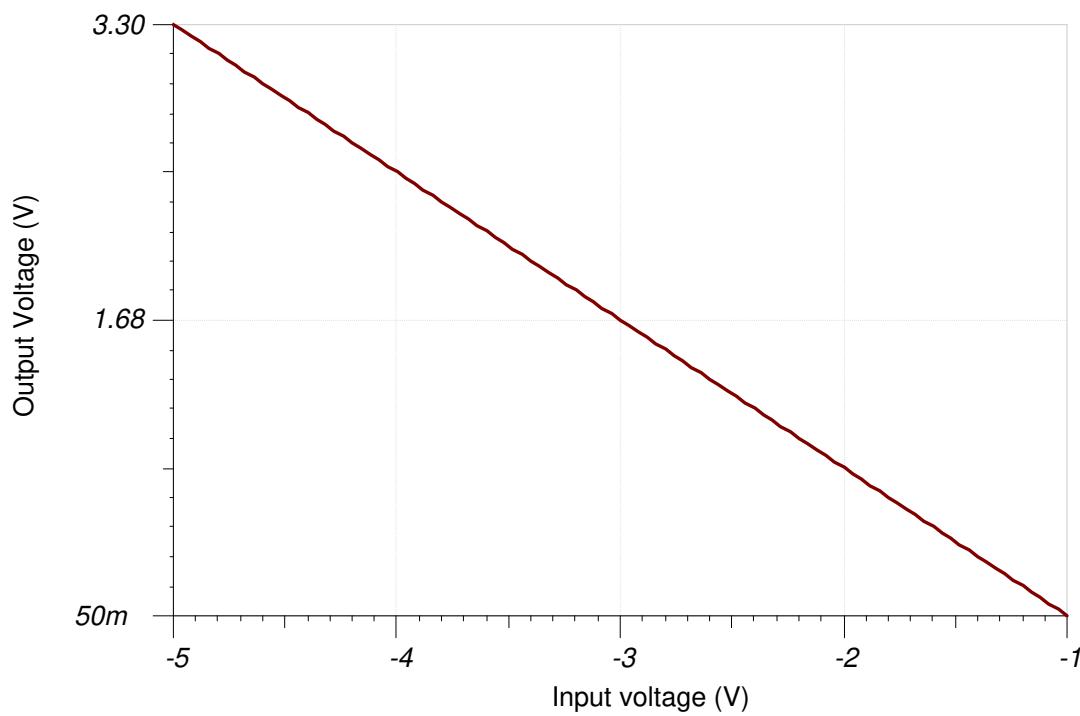
$$\frac{R_1}{R_3} = \frac{V_{o_min} + V_{i_min} \times \left(\frac{R_1}{R_2} \right)}{-V_{ref}} = \frac{0.05V + (-1\text{ V}) \left(\frac{845\Omega}{1.04\text{k}\Omega} \right)}{-5} = 0.1525 \frac{V}{V}$$

4. Calculate R_3 .

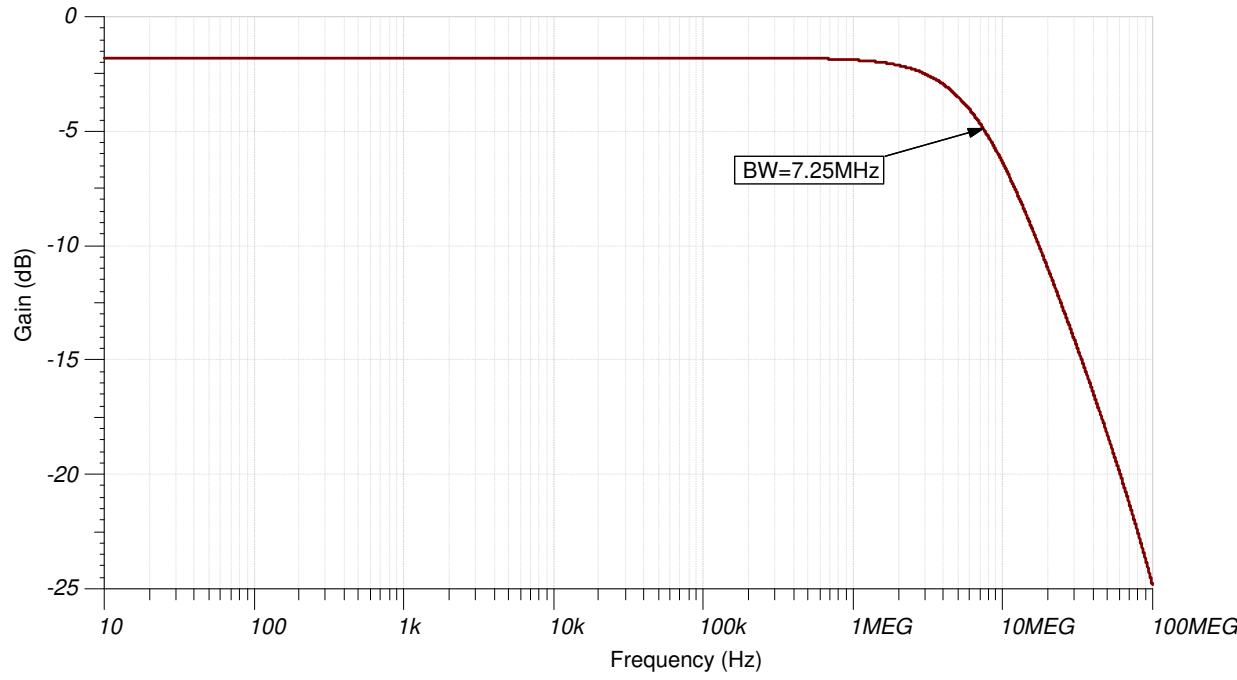
$$R_3 = \frac{R_1}{G_{ref}} = \frac{845\Omega}{0.1525 \frac{V}{V}} = 5.54 \text{ k}\Omega \approx 5.56 \text{ k}\Omega$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

See the circuit SPICE simulation file [SBOC511](#).

See [Designing Gain and Offset in Thirty Seconds](#).

Design Featured Op Amp

TLV9062	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3 mV
I_q	538 μ A
I_b	0.5 pA
UGBW	10 MHz
SR	6.5 V/ μ s
#Channels	1, 2, and 4
TLV9062	

Design Alternate Op Amp

OPA197	
V_{ss}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	25 μ V
I_q	1 mA
I_b	5 pA
UGBW	10 MHz
SR	20 V/ μ s
#Channels	1, 2, and 4
OPA197	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019

Page

- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.....

1

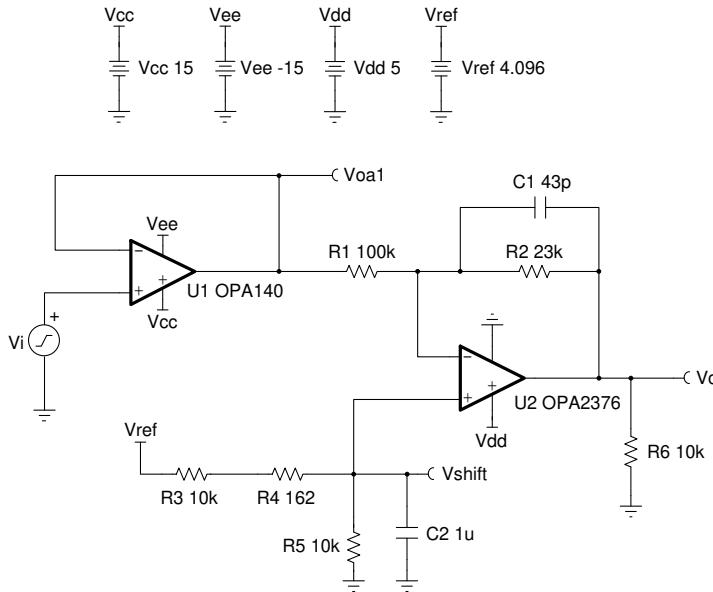


Design Goals

Input		Output		Supply			
$V_{i\text{Min}}$	$V_{i\text{Max}}$	$V_{o\text{Min}}$	$V_{o\text{Max}}$	V_{cc}	V_{ee}	V_{dd}	V_{ref}
-10 V	+10 V	+0.2 V	+4.8 V	+15 V	-15 V	+5 V	+4.096 V

Design Description

This inverting dual-supply to single-supply amplifier translates a ± 10 V signal to a 0 V to 5 V signal for use with an ADC. Levels can easily be adjusted using the given equations. The buffer can be replaced with other ± 15 V configurations to accommodate the desired input signal, as long as the output of the first stage is low impedance.



Design Notes

1. Observe common-mode limitations of the input buffer.
2. A high-impedance source will alter the gain characteristics of U_2 if buffer amplifier U_1 is not used.
3. R_6 provides a path to ground for the output of U_1 if the ± 15 V supplies come up before the 5 V supply. This limits the voltage at the inverting pin of U_2 through the voltage divider created by R_1 , R_2 , and R_6 and prevents damage to U_2 as well as to any converter that may be connected to its output. To best protect the devices a transient voltage suppressor (TVS) should be used at the power pins of U_2 .
4. A capacitor across R_5 will help filter V_{ref} and provide a cleaner V_{shift} .

Design Steps

The transfer function for this circuit follows:

$$V_o = -\frac{R_2}{R_1} \times V_i + \left(1 + \frac{R_2}{R_1}\right) \times V_{shift}$$

1. Set the gain of the amplifier.

$$\frac{\Delta V_o}{\Delta V_i} = \frac{V_{oMax} - V_{oMin}}{V_{iMax} - V_{iMin}} = \frac{4.8V - 0.2V}{10V - (-10V)} = 0.23$$

$$\frac{\Delta V_o}{\Delta V_i} = \frac{R_2}{R_1}$$

$$R_2 = 0.23 \times R_1$$

Choose $R_1 = 100k\Omega$ (standard value)

$R_2 = 23k\Omega$ (for standard values use $22k\Omega$ and $1k\Omega$ in series)

2. Set V_{shift} to translate the signal to single supply.

At midscale, $V_{in} = 0V$

$$\text{Then } V_o = \left(1 + \frac{R_2}{R_1}\right) \times V_{shift}$$

$$V_{shift} = \frac{V_o}{\left(1 + \frac{R_2}{R_1}\right)} = \frac{2.5V}{1.23} = 2.033V$$

3. Select resistors for reference voltage divider to achieve V_{shift} .

$$V_{ref} = 4.096V$$

$$V_{shift} = V_{ref} \times \frac{R_5}{(R_3 + R_4) + R_5}$$

$$\frac{V_{shift}}{V_{ref}} = \frac{2.033V}{4.096V} = \frac{R_5}{(R_3 + R_4) + R_5}$$

$$R_3 + R_4 = 1.0161 \times R_5$$

Select a standard value for R_5

$$R_5 = 10k\Omega$$

$$R_3 + R_4 = 10.161k\Omega$$

$$R_3 = 10k\Omega$$

$R_4 = 162\Omega$ (standard 1% value)

4. Large feedback resistors can interact with the input capacitance and cause instability. Choose C_1 to add a pole to the transfer function to counteract this. The pole must be lower in frequency than the effective bandwidth of the op amp.

$$C_1 = 43\text{pF}$$

$$f_p = \frac{1}{2\pi \times R_2 \times C_1} = 160.3\text{kHz}$$