UNIVERSITY OF LIVERPOOL

Department of Electrical Engineering and Electronics

ELEC373

Digital Systems Design
Assignments 1 and 2
Random Number Generator

Module	ELEC373
Coursework name	Assignment 1 and Assignment 2
Component weight	Assignment 1 = 15%, Assignment 2 = 25%
Semester	1
HE Level	6
Lab location	By simulation, but if the EEE Building opens for general access PC labs 301, 304 as timetabled, at other times for private study
Work	Individually
Timetabled time	12 hours (3 hours per week – Wednesday 2pm – 5pm)
Suggested private study	10 hours including report writing
Assessment method	Individual, formal word-processed reports (Block diagrams and ASMs can be hand drawn and scanned into the report)
Submission format	Online via VITAL
Submission deadline	Assignment 1: 23:59 on Friday 20th November 2020 Assignment 2: TBC
Late submission	Standard university penalty applies
Resit opportunity	August resit period (if total module failed)
Marking policy	Marked and moderated independently
Anonymous marking	Yes
Feedback	Via comments on Vital submission on-line
Learning outcomes	LO1: Ability to design digital systems using the ASM design method LO2: Ability to implement digital systems using the Verilog Hardware Description Language

Marking Criteria

Section	Marks available	Indicative characteristics	
		Adequate / pass (40%)	**Very good / Excellent**
Presentation and structure	10%	• Contains cover page information, table of contents, sections with appropriate headings. • Comprehensible language; punctuation, grammar and spelling accurate. • Equations legible, numbered and presented correctly. • Appropriately formatted reference list.	• Appropriate use of technical, mathematic and academic terminology and conventions. • Word processed with consistent formatting. • Pages numbered, figures and tables captioned. • All sections clearly signposted. • Correct cross-referencing (of figures, tables, equations) and citations.
Introduction, Method and Design	50%	• Problem background introduced clearly. • Evidence of a Top Down Design approach • Conceptual Design Choices introduced. • Design of each module follows a logical sequence. • ASMs correspond to designs for required blocks.	• Appropriate range of references used. • Design decisions justified with alternatives given. • Calculations shown in full, justifying and explaining any decisions. • Correct ASM Syntax used. • Well-structured Verilog Code • Fully synchronous design
Results	30%	• Simulation results present for each block and well annotated. • Results of full system in both simulation and experimentally presented. • Results for each task accompanied by a commentary. • Screen shots of results presented.	• Simulations demonstrate that every pathway in each ASM is functioning correctly. • Tests indicate that there are no problems caused by asynchronous inputs.
Discussion	10%	• Discussion on what worked and what didn't. • Critical assessment on the design – strength and weaknesses	• Discussion on how the system was fully tested.

ELEC 373 Verilog Assignments 1 & 2 (2020-2021)

Assignment Overview

These assignments have been set to get you familiar with designing digital systems and synthesising them from a Verilog description. You should develop your design using Altera's Quartus II V13.0-SP1.

The first assignment is for you to undertake the first two stages of the design process i.e. the conceptual design, communicated by block diagrams, and the embodiment design communicated by ASM charts. You will also be coding some blocks in Verilog and simulating them to prove they function correctly.

The second assignment will require you to develop the full system in Verilog to prove that it works, although you can use a "bdf" file to connect your blocks together. You will be allowed to modify your design based on the feedback from the first assignment. Depending on access to the building, it may be possible that, for the second assignment, you can test your design on a DE2 board in the EEE Department. This will be decided closer to the submission date of assignment 2.

Assignments Outline

Many games of chance require a random number as input, be it from the throw of a dice or a ball on a roulette wheel. Your objective is to develop a design which will display random decimal numbers on the 7 segment displays of the DE2 board. For this example we will use the numbers as our selection for the national lottery where the choice of numbers starts at 1 and goes up to the last two digits of your University ID (add 20 to this number if the last two digits of your number are less than 30).

Your system operation should be as follows:

1. The operator presses KEYV[1] to start the sequence.
2. The operator then presses KEYW[1] and the first number is displayed on HEXX[1] for Y[1] seconds.
3. The system then starts counting again and the operator repeats stage 2. However note that a number previously selected can't be selected again.
4. The process is repeated until the number of numbers selected is equal to Z[1].

Remember that you should be careful about how you handle asynchronous inputs.

Report – Assignment 1

Your report should include the following.

1. Description of Architecture(s) and Controller(s) (with block diagrams showing interconnections).
2. ASM Charts for all Algorithmic State Machines. (1 page per ASM)
3. Commented Verilog code for each module for the Seven Segment Decoder and any counters you have in your design.

[1] See table 1 to identify which key, display, time etc. this is.

4. Full simulations of the Seven Segment Decoder and any counters you have in your design, with annotations indicating what the simulation proves.
5. Discussion and Conclusions about the design choices made.

You should also submit your design and report via VITAL. Make sure all the files need to compile, simulate and test the modules under Quartus 13.0SP1 are included in a single zip file. The report should be attached as a separate Word file. You should structure your report about each module, i.e. include ASM, then, where appropriate, Verilog code, then simulation results consecutively for each module rather than grouping all the ASMs together.

Report – Assignment 2

Your report should include the following.

1. Description of Architecture(s) and Controller(s) (with block diagrams showing interconnections).
2. ASM Charts for all Algorithmic State Machines. (1 page per ASM)
3. Commented Verilog code for each module.
4. Full simulations for each module you have in your design, with annotations indicating what the simulation proves.
5. RTL Schematic of the full system.
6. Simulation of the full system. (With annotations and maximum ½ page on any comments)
7. Explanation of experimental test results. (Max 1 page) Is it truly random ?
8. Conclusion (Maximum ½ page)
9. If we have access to the laboratory - signed demonstrators check sheet

You should also submit your design and report via VITAL. Make sure all the files need to compile, simulate and test the design under Quartus 13.0SP1 are included in a single zip file. The report should be attached as a separate Word file. You should structure your report about each module, i.e. include ASM, then Verilog code, then simulation results consecutively for each module rather than grouping all the ASMs together.

Warning

When marking the reports I will be looking very closely for any signs of collusion, as this is unacceptable. I need to assess your own ability not that of your friend or colleague. If I find any evidence of collusion then the formal University rules will be followed which may result in your suspension.

Assignment 1 Submission Deadline

You only need to submit an Electronic copy: Friday 20th November 2020 @ 11:59pm.
You also need to submit a ZIP file of your modules by the same date and time.

Assignment 2 Submission Deadline

To be confirmed.

Hint

The challenging part to this assignment is preventing duplicate numbers being generated. However, you will get more marks for a working system that does generate duplicate numbers than for one that fails to work whilst attempting to eliminate duplicate numbers.

J.S. Smith
27th October 2020

Table 1 – Assignment parameters

ELEC373	Name	KEYV	KEYW	HEXX	Y Seconds	Z Numbers
201360923	Aveni, Olawale Solomon	KEY0	KEY1	HEX1-0	4	5
201447264	Bai, Jie	KEY1	KEY0	HEX2-1	5	5
201315796	Brown, Connor	KEY1	KEY0	HEX5-4	6	5
201447455	Ding, Qiyang	KEY2	KEY0	HEX3-2	6	5
201447513	Fang, Zhaoyan	KEY3	KEY0	HEX5-4	7	5
201357067	Glowacki, Jakub	KEY0	KEY1	HEX7-6	8	5
201309197	Hankinson, Thomas	KEY3	KEY2	HEX2-1	9	6
201447621	He, Jiayi	KEY1	KEY2	HEX1-0	9	5
201375874	Huang, Yiming	KEY2	KEY1	HEX2-1	4	5
201447715	Huang, Zhongling	KEY3	KEY1	HEX3-2	5	6
201447717	Huo, Kairun	KEY0	KEY2	HEX5-4	6	6
201275074	Ike, Nnadozie Jason	KEY1	KEY2	HEX7-6	7	6
201447758	Jiang, Ziyi	KEY2	KEY3	HEX1-0	8	6
201447759	Jiao, Jian	KEY3	KEY2	HEX2-1	9	6
201447777	Jing, Jiaxi	KEY0	KEY3	HEX3-2	4	6
201347216	Kovvuri, Sandeep Reddy	KEY1	KEY3	HEX5-4	5	7
201447803	Lei, Jiaheng	KEY2	KEY3	HEX7-6	6	7
201305681	Lewis, Oliver Emlyn	KEY3	KEY0	HEX1-0	7	7
201447904	Li, Yang	KEY0	KEY1	HEX2-1	8	7
201447912	Li, Yu	KEY1	KEY0	HEX3-2	9	7
201447973	Lin, Yu-Cheng	KEY2	KEY0	HEX5-4	4	4
201447999	Liu, Jiacheng	KEY3	KEY0	HEX7-6	5	4
201298366	Liu, Jie	KEY0	KEY3	HEX1-0	6	4
201448055	Liu, Yimian	KEY1	KEY3	HEX2-1	7	4
201448053	Liu, Yinhang	KEY2	KEY3	HEX3-2	8	4
201448076	Liu, Zheyu	KEY3	KEY2	HEX5-4	4	4
201448082	Long, Heyang	KEY0	KEY2	HEX7-6	5	5
201448190	Niu, Yusen	KEY1	KEY2	HEX1-0	6	5
201261946	Parhar, Jai Singh	KEY2	KEY1	HEX2-1	7	5
201448219	Qi, Kexin	KEY3	KEY1	HEX3-2	8	5
201290370	Schlaefli Morales, Fernando Rafael	KEY0	KEY1	HEX5-4	4	5
201448466	Wang, Kefan	KEY1	KEY0	HEX7-6	5	5
201219640	Wang, Xuesong	KEY2	KEY0	HEX1-0	6	5
201448540	Wang, Zhaoyang	KEY3	KEY0	HEX2-1	7	6
201376946	Xiang, Li	KEY0	KEY3	HEX3-2	8	6
201376978	Xiong, Jiangao	KEY1	KEY3	HEX5-4	4	6
201376988	Xu, Congyi	KEY2	KEY3	HEX7-6	5	6
201448708	Xue, Chunyan	KEY3	KEY2	HEX1-0	6	6
201448725	Yan, Yujie	KEY0	KEY2	HEX2-1	7	6
201448759	Yang, Xintong	KEY1	KEY2	HEX3-2	8	7
201448812	Yin, Ruihong	KEY2	KEY1	HEX5-4	4	7
201448839	Yu, Tiehan	KEY3	KEY1	HEX7-6	5	7
201448855	Yuan, Lixiang	KEY0	KEY1	HEX1-0	6	7
201448922	Zhang, Jinhao	KEY1	KEY0	HEX2-1	7	7
201449028	Zhang, Zhanhua	KEY2	KEY0	HEX3-2	8	7
201449062	Zhao, Tiange	KEY3	KEY0	HEX5-4	4	4
201449111	Zhou, Hang	KEY0	KEY3	HEX7-6	5	4