UNIVERSITY OF LIVERPOOL

Department of Electrical Engineering and Electronics

ELEC373

Digital Systems Design
Assignment 4
NIOS-II Custom Instructions

Module	ELEC373
Coursework name	Assignment 4
Component weight	20%
Semester	2
HE Level	6
Lab location	PC labs 301, 304 as timetabled, at other times for private study
Work	Individually
Timetabled time	9 hours (3 hours per week – Wednesday 2pm – 5pm)
Suggested private study	10 hours including report writing
Assessment method	Individual, formal word-processed reports (Block diagrams and ASMs can be hand drawn and scanned into the report)
Submission format	Online via VITAL
Submission deadline	23:59 on Friday 14th May 2021
Late submission	Standard university penalty applies
Resit opportunity	August resit period (if total module failed)
Marking policy	Marked and moderated independently
Anonymous marking	No
Feedback	Via printed annotated copy showing corrections
Learning outcomes	LO1: Ability to design digital systems using the ASM design method LO2: Ability to implement digital systems using the Verilog Hardware Description Language LO4: Ability to implement a SOPC System using Quartus Nios-II

Marking Criteria

Section	Marks available	Indicative characteristics	
		Adequate / pass (40%)	**Very good / Excellent**
Presentation and structure	20%	• Contains cover page information, table of contents, sections with appropriate headings. • Comprehensible language; punctuation, grammar and spelling accurate. • Equations legible, numbered and presented correctly. • Appropriately formatted reference list.	• Appropriate use of technical, mathematic and academic terminology and conventions. • Word processed with consistent formatting. • Pages numbered, figures and tables captioned. • All sections clearly signposted. • Correct cross-referencing (of figures, tables, equations) and citations.
Introduction, Method and Design	40%	• Problem background introduced clearly. • Evidence of a Top Down Design approach • Conceptual Design Choices introduced. • Design of each module follows a logical sequence. • ASMs correspond to designs for each block. • Software is clearly commented	• Appropriate range of references used. • Design decisions justified with alternatives given. • Calculations shown in full, justifying and explaining any decisions. • Correct ASM Syntax used. • Well-structured Verilog Code
Results	30%	• Simulation results present for each block and well annotated. • Results of full system in both simulation and experimentally presented. • Results for each task accompanied by a commentary. • Screen shots of results presented.	• Tests indicate that there are no problems caused by asynchronous inputs. • Clear explanation of how the instructions operate correctly
Discussion	10%	• Discussion on what worked and what didn't. • Critical assessment on the design – strength and weaknesses	• Discussion on how the system was fully tested.

ELEC 373 Assignment 4 (2020-2021)
Synthesising the NIOS II Processor

Assignment Outline

In Assignment 3 you added some extra instructions to a MIPS processor which was then synthesised and executed on the DE2 board. This assignment aims to introduce you to a commercial synthesised processor targeted for Altera FPGAs, which allows the easy importing of peripherals and the use of an industry standard IDE for software development.

The challenge, this year, is that you don't have access to the DE2 Boards so everything will be done in simulation. However this is still realistic because, as indicated in the lectures, the software development can happen in parallel with the hardware development.

To start with you should complete the Nios II Hardware Development Tutorial, found on Vital, that will walk you through building a basic NIOS-II system to which you can then add your Custom Instruction.

You will find some screencasts in the Vital module, under the NIOS-II section, that walks you through setting up a custom instruction and simulating its operation in the NIOS processor, however you will need to modify this for your specific custom instruction. You will find Session 15 – Loops in Verilog helpful in developing the Verilog for your Custom Instruction.

Custom Instruction

This requires you to develop a Custom Instruction to count the number of leading 1s (or 0s – see Table 1) in the 32 bit number passed to the instruction. You should write a program to test your Custom Instruction. You should also develop a test routine in C or assembler that performs the same function as the Custom Instruction and compare the speed of the Custom Instruction against your software implementation.

Submission

You report should include the following:

1. ASM(s) and Verilog code for your custom instruction
2. C/C++ for your test program
3. Screen dump showing the results of your program
4. Results showing a speed comparison between the Custom Instruction (i.e. in Hardware) and your software implementation (i.e. a C function that calculates the result).
5. Explanation of your results.

Submission Deadline

Vital: Friday 14th May 2021 @ 11:59pm

Table 1 Custom Instruction Task

ID	Name	Counting
201360923	Ayeni, Olawale Solomon	Leading 0s
201447264	Bai, Jie	Leading 0s
201315796	Brown, Connor	Leading 1s
201447455	Ding, Qiyang	Leading 1s
201447513	Fang, Zhaoyan	Leading 0s
201357067	Glowacki, Jakub	Leading 0s
201309197	Hankinson, Thomas	Leading 1s
201447621	He, Jiayi	Leading 1s
201375874	Huang, Yiming	Leading 0s
201447715	Huang, Zhongling	Leading 0s
201447717	Huo, Kairun	Leading 1s
201275074	Ike, Nnadozie Jason	Leading 1s
201447758	Jiang, Ziyi	Leading 0s
201447759	Jiao, Jian	Leading 0s
201447777	Jing, Jiaxi	Leading 1s
201347216	Kovvuri, Sandeep Reddy	Leading 1s
201447803	Lei, Jiaheng	Leading 0s
201305681	Lewis, Oliver Emlyn	Leading 0s
201447904	Li, Yang	Leading 1s
201447912	Li, Yu	Leading 1s
201447973	Lin, Yu-Cheng	Leading 0s
201447999	Liu, Jiacheng	Leading 0s
201298366	Liu, Jie	Leading 1s
201448055	Liu, Yimian	Leading 1s
201448053	Liu, Yinhang	Leading 0s
201448076	Liu, Zheyu	Leading 0s
201448082	Long, Heyang	Leading 1s
201448190	Niu, Yusen	Leading 1s
201261946	Parhar, Jai Singh	Leading 0s
201448219	Qi, Kexin	Leading 0s
201290370	Schlaefli Morales, Fernando Rafael	Leading 1s
201448466	Wang, Kefan	Leading 1s
201219640	Wang, Xuesong	Leading 0s
201448540	Wang, Zhaoyang	Leading 0s
201376946	Xiang, Li	Leading 1s
201376978	Xiong, Jiangao	Leading 1s
201376988	Xu, Congyi	Leading 0s
201448708	Xue, Chunyan	Leading 0s
201448725	Yan, Yujie	Leading 1s
201448759	Yang, Xintong	Leading 1s
201448812	Yin, Ruihong	Leading 0s
201448839	Yu, Tiehan	Leading 0s
201448855	Yuan, Lixiang	Leading 1s
201448922	Zhang, Jinhao	Leading 1s
201449028	Zhang, Zhanhua	Leading 0s
201449062	Zhao, Tiange	Leading 0s
201449111	Zhou, Hang	Leading 1s

J.S. Smith 27/4/21