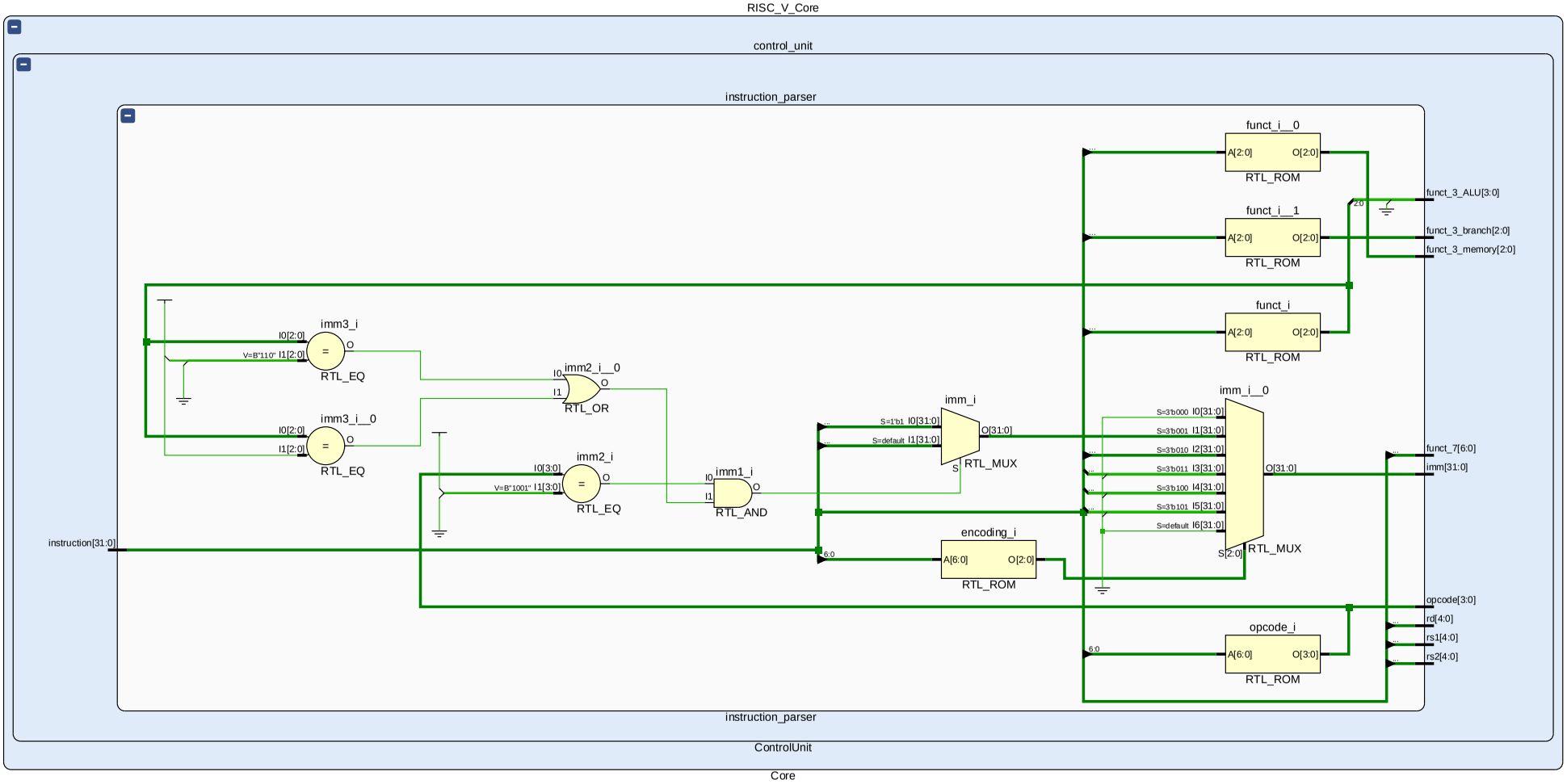
RISC_V_Core
control_unit
instruction_parser
funct_i__0
A[2:0]
O[2:0]
RTL_ROM
funct_i__1
A[2:0]
O[2:0]
RTL_ROM
funct_i
A[2:0]
O[2:0]
RTL_ROM
funct_3_ALU[3:0]
funct_3_branch[2:0]
funct_3_memory[2:0]
imm3_i
I0[2:0]
V=B"110"
I1[2:0]
O
RTL_EQ
imm3_i__0
I0[2:0]
I1[2:0]
O
RTL_EQ
imm2_i__0
I0
I1
O
RTL_OR
imm2_i
I0[3:0]
V=B"1001"
I1[3:0]
O
RTL_EQ
imm1_i
I0
I1
O
RTL_AND
imm_i
S=1'b1
I0[31:0]
S=default
I1[31:0]
O[31:0]
S
RTL_MUX
imm_i__0
S=3'b000
I0[31:0]
S=3'b001
I1[31:0]
S=3'b010
I2[31:0]
S=3'b011
I3[31:0]
S=3'b100
I4[31:0]
S=3'b101
I5[31:0]
S=default
I6[31:0]
O[31:0]
S[2:0]
RTL_MUX
funct_7[6:0]
imm[31:0]
instruction[31:0]
6:0
encoding_i
A[6:0]
O[2:0]
RTL_ROM
opcode[3:0]
rd[4:0]
rs1[4:0]
rs2[4:0]
6:0
opcode_i
A[6:0]
O[3:0]
RTL_ROM
instruction_parser
ControlUnit
Core