

RISC V RV32I

BASE INSTRUCTION SET



REFERENCE

www.riscv.org

The RISC-V Instruction Set Manual

Volume I: User-Level ISA

Document Version 2.2



R-FORMAT

funct7 rs2 rs1 funct3 rd opcode

- ADD Addition
- SUB Subtraction
- SLL Logical Left Shift
- SLT Set Less Than
- SLTU Set Less Than Unsigned
- XOR Xor operation
- SRL Logical Right Shift
- SRA Arithmetic Right Shift
- OR or operation
- AND and operation



I -FORMAT

imm[11:0] rs1 funct3 rd opcode

- •LB Load Byte
- LH Load Half Word
- LW Load Word
- LBU Load Byte Unsigned
- LHU Load Half Word Unsigned
- ADDI Add Immediate
- SLTI Set Less Than Immediate
- SLTIU Set Less Than Immediate Unsigned
- XORI Xor with immediate
- ORI OR with immediate
- ANDI AND immediate
- SLLI Logical Left Shift with immediate
- SRLI Logical Right Shift with immediate
- SRAI Arithmetic Right Shift with immediate
- JALR Jump and Link register



I -FORMAT

Continue...

imm[11:0]	rs1	funct3	rd	opcode
_				-

- CSRRW Atomic Read / Write CSR
- CSRRS Atomic Read and Set Bits in CSR
- CSRRC Atomic Read and Clear Bits in CSR
- CSRRWI Atomic Read / Write CSR with unsigned immediate
- CSRRSI Atomic Read and Set Bits in CSR with unsigned immediate
- CSRRCI Atomic Read and Clear Bits in CSR with unsigned immediate
- ECALL Environmental call
- EBREAK Environmental break
- FENCE Fence
- FENCE.I Fence with immediate



S-FORMAT

Imm[11:5]rs2rs1funct3Imm[4:0]opcode

- SB Store Byte
- SH Store Half Word
- SW Store Word



B-FORMAT

 Imm[11:5]
 rs2
 rs1
 funct3
 Imm[4:1] imm[11]
 opcode

- BEQ Branch Equality
- BNE Branch Not Equal
- BLT Branch Less Than
- BGE Branch Greater Than
- BLTU Branch Less Than Unsigned
- BGEU Branch Greater Than Unsigned



U-FORMAT

Imm[31:12] rd opcode

- LUI Load Upper Immediate
- AUIPC Add Upper Immediate with PC



J-FORMAT

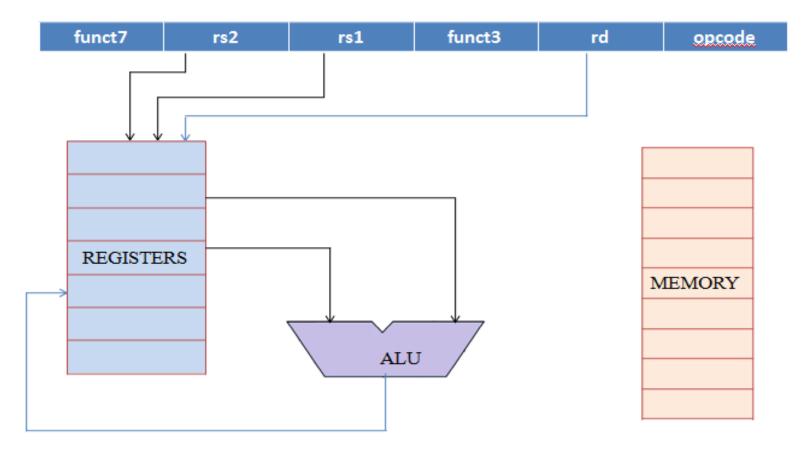
Imm[20] imm[10:1]imm[11] imm[19:12] rd opcode

• JAL - Jump And Link



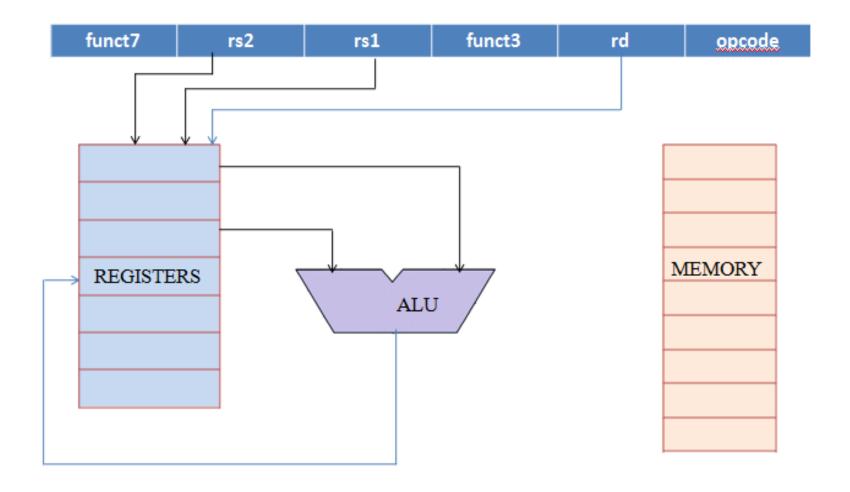
EXECUTION OF OPERATIONS IN R-FORMAT

ADD (Addition)



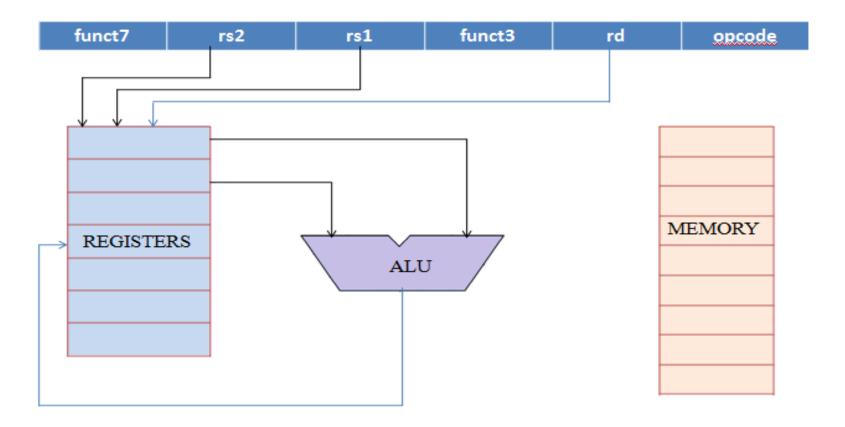
funct7=0000000;funct3=000;opcode =0110011





funct7=0100000;funct3=000;opcode =0110011

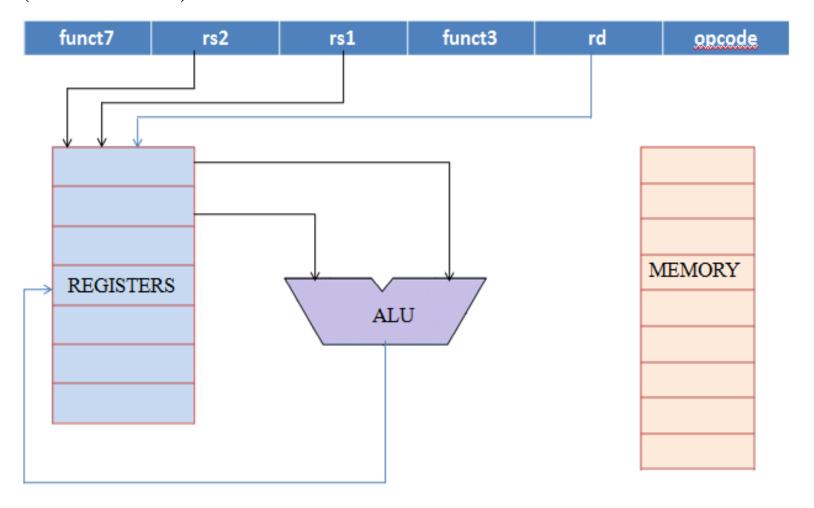




funct7=0000000;funct3=001;opcode=0110011

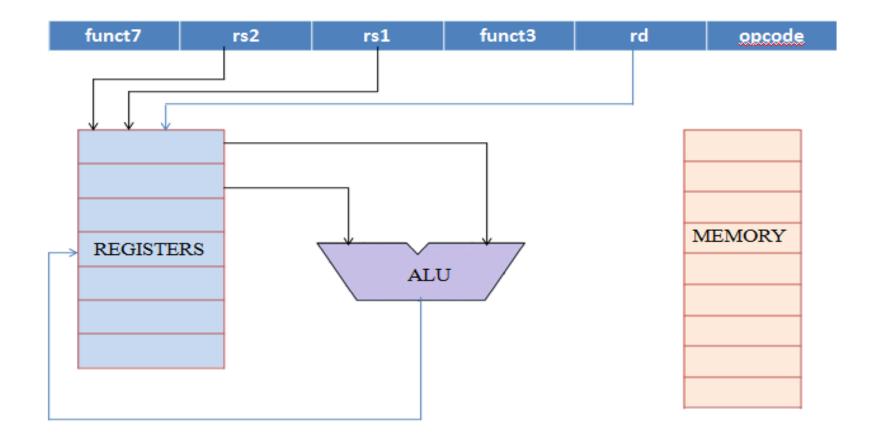


R-FORMAT



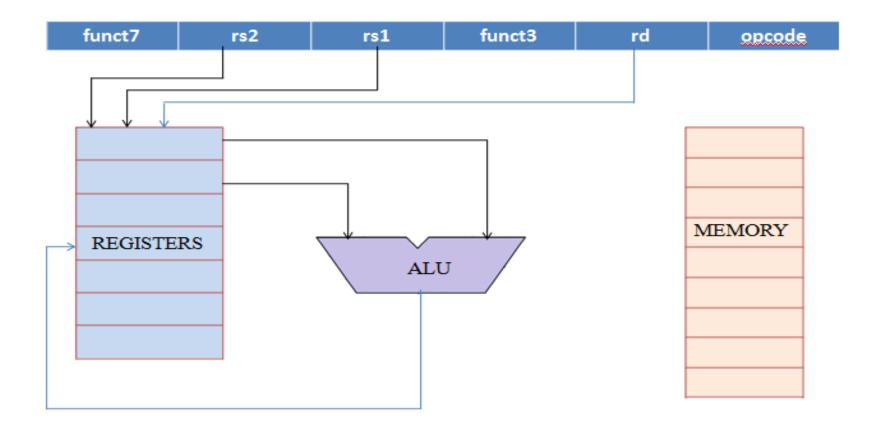
funct7=0000000;funct3=010;opcode=0110011





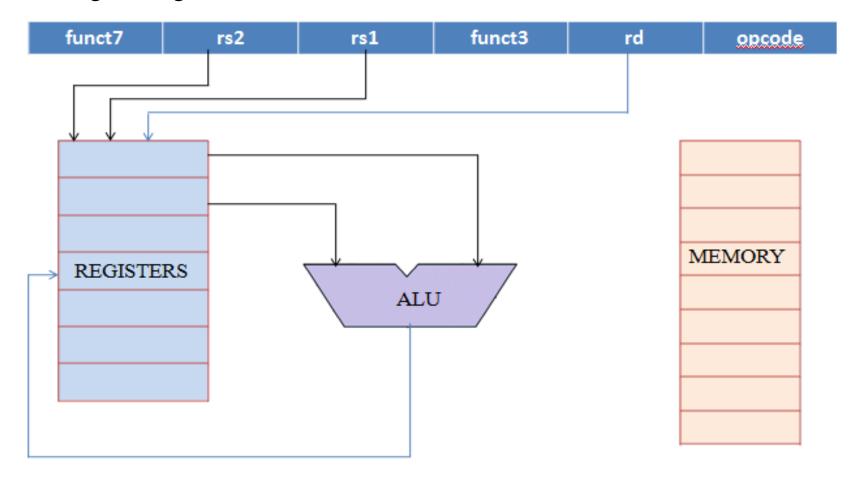
funct7=0000000;funct3=011;opcode=0110011





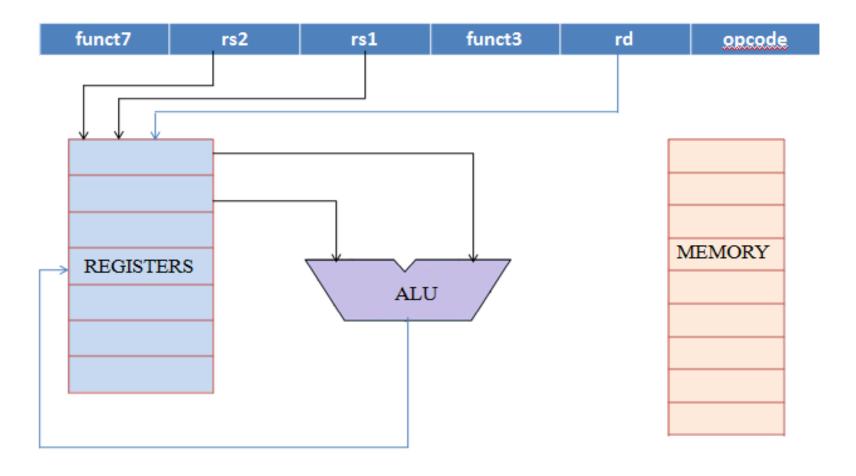
funct7=0000000;funct3=100;opcode=0110011





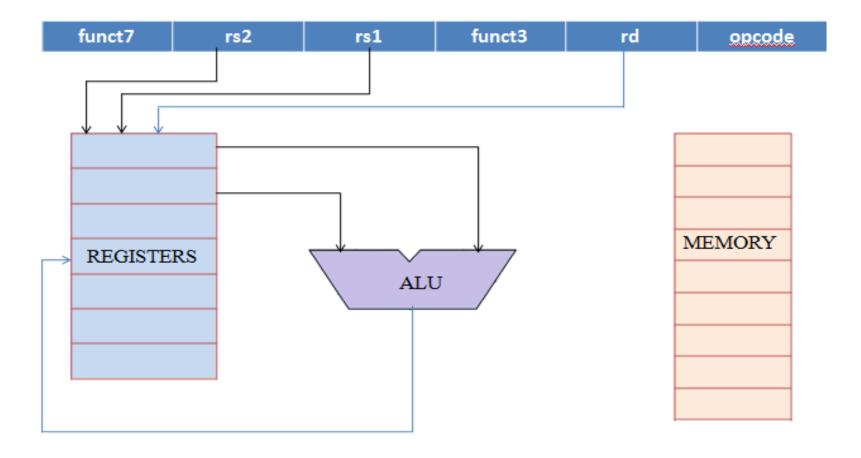
funct7=0000000;funct3=101;opcode=0110011





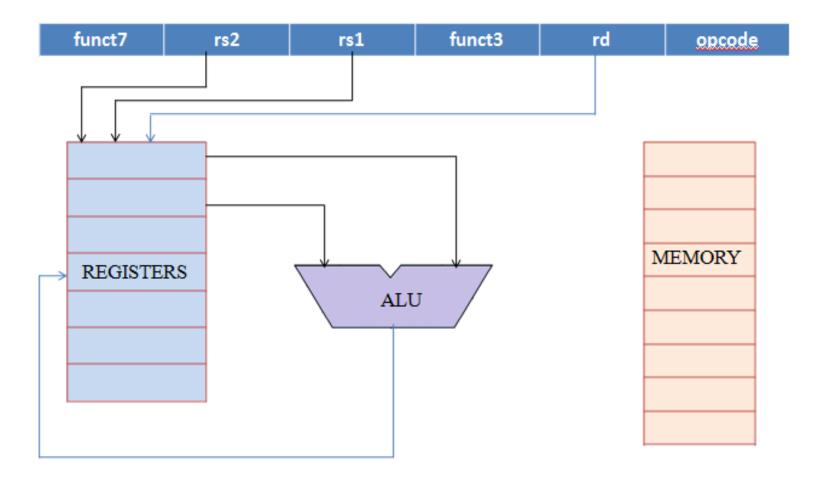
funct7=0100000;funct3=101;opcode=0110011





funct7=0000000;funct3=110;opcode=0110011



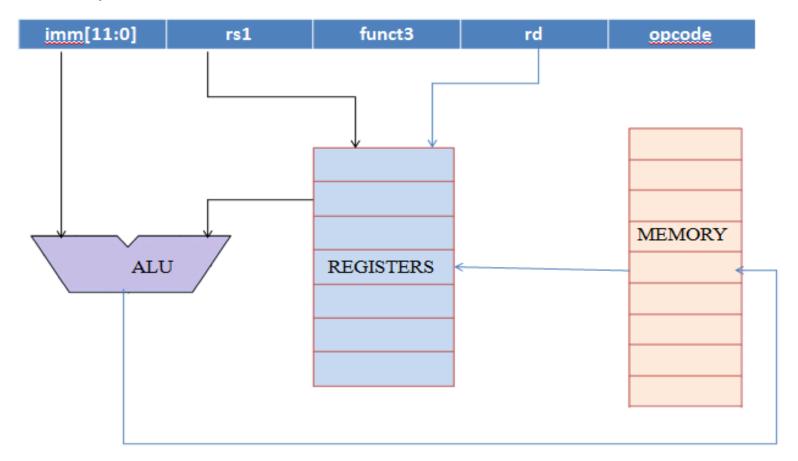


funct7=0000000;funct3=111;opcode=0110011



EXECUTION OF INSTRUCTIONS IN I-FORMAT

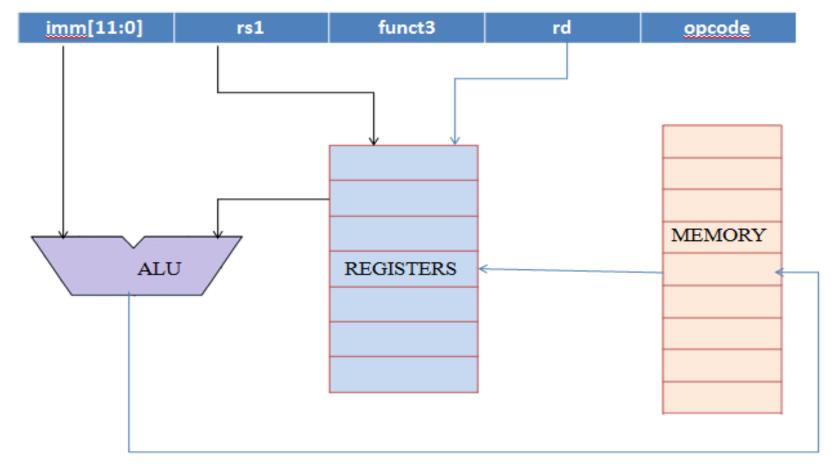
LB (Load Byte)



funct3=000;opcode =0000011

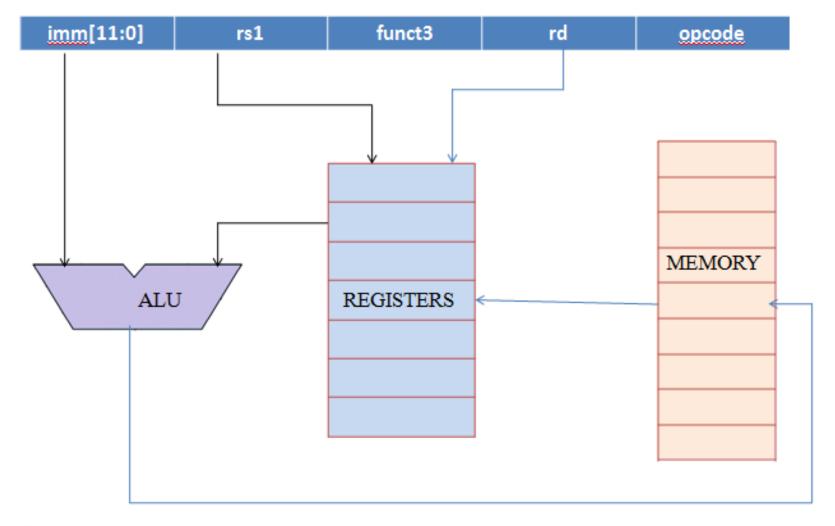


LH (Load Halfword)



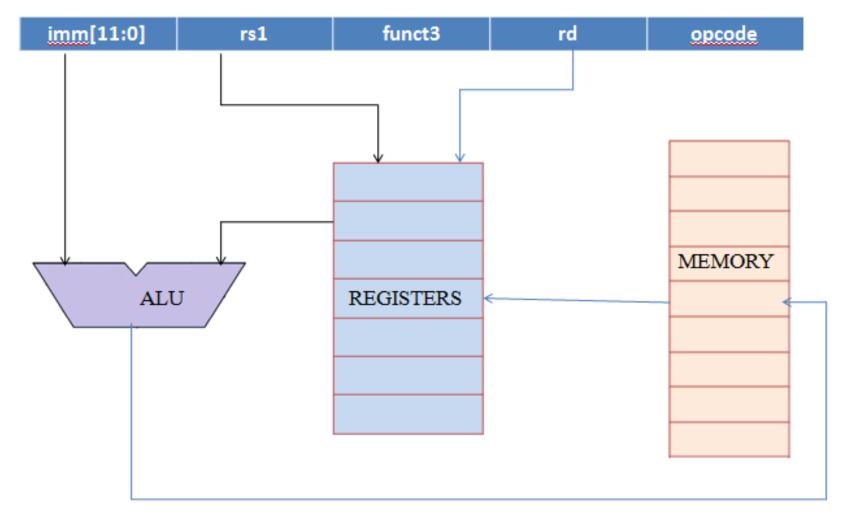
funct3=001;opcode =0000011





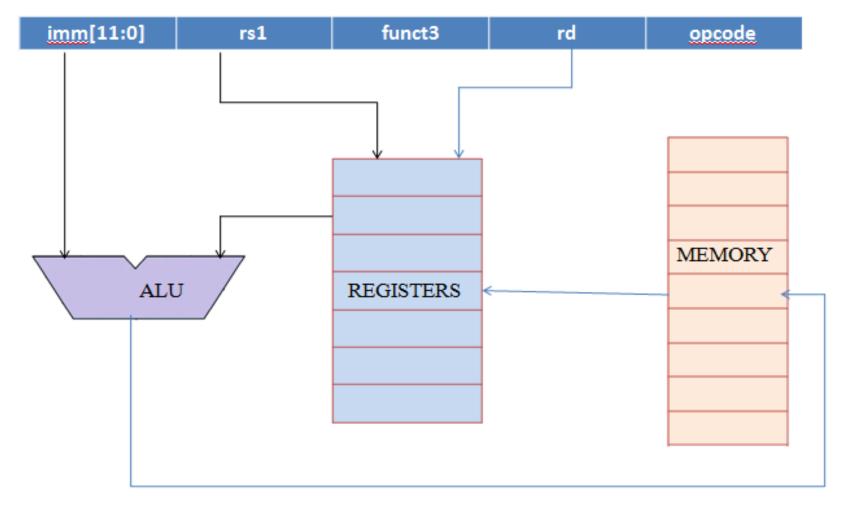
funct3=010;opcode =0000011





funct3=100;opcode=0000011



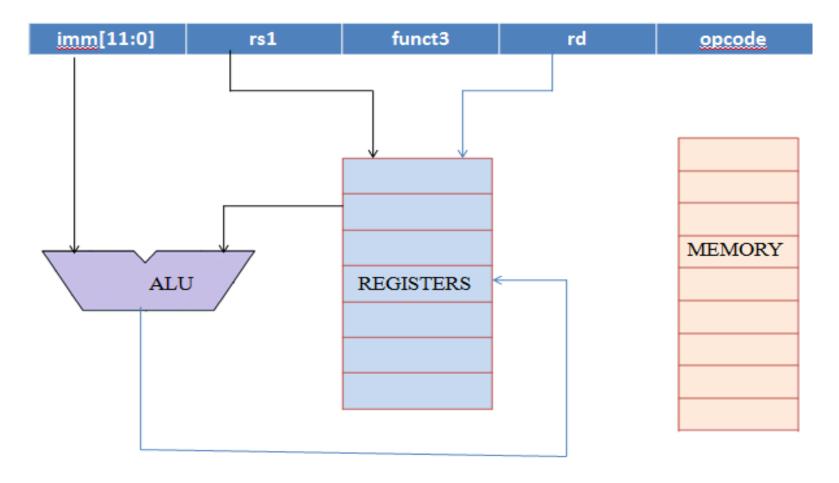


funct3=101;opcode =0000011



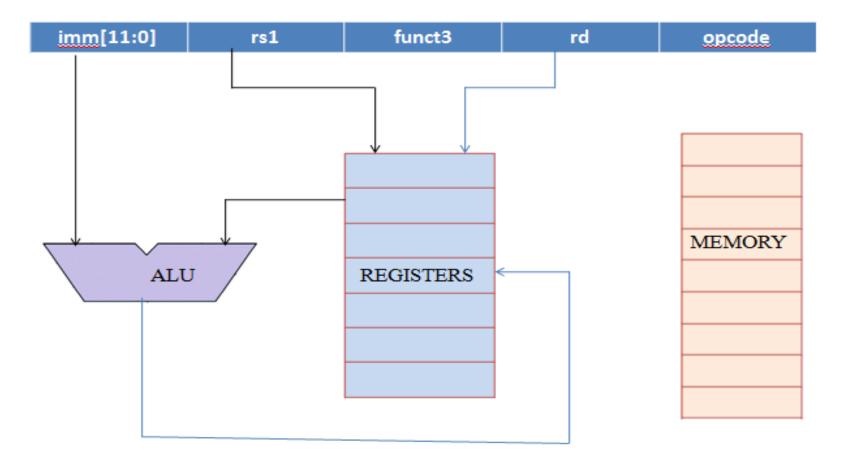
ADDI (Addition Immediate)

I-FORMAT



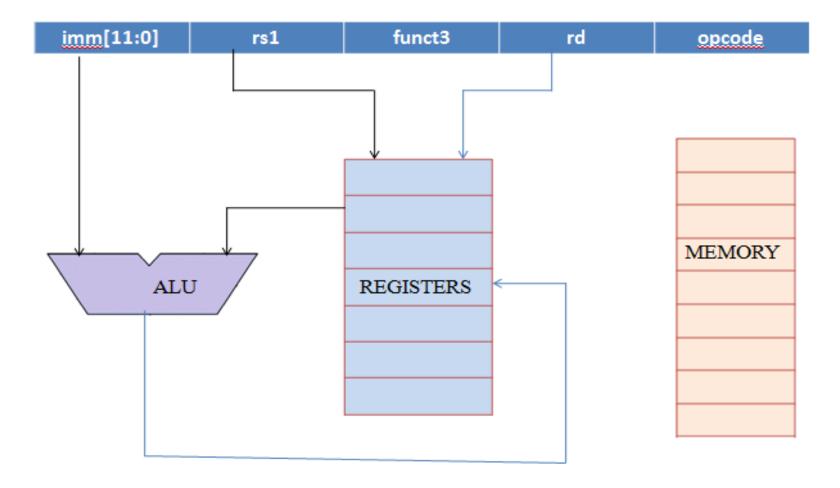
funct3=000;opcode=0010011





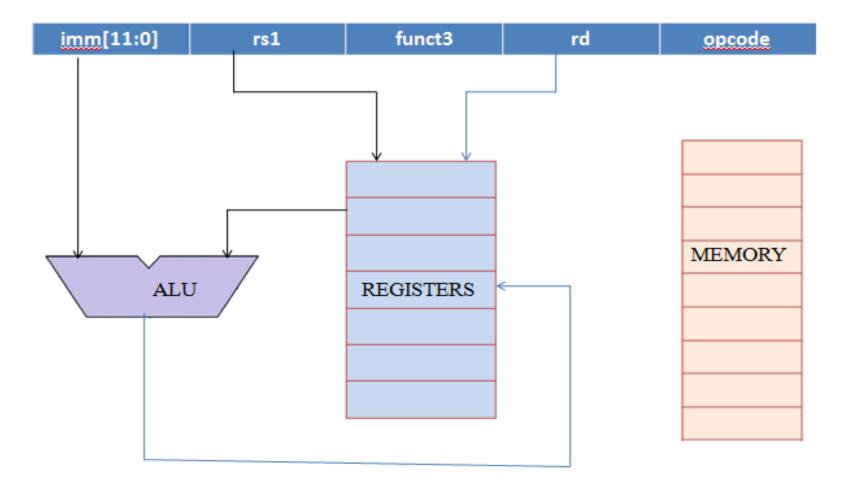
funct3=010;opcode=0010011





funct3=011;opcode =0010011

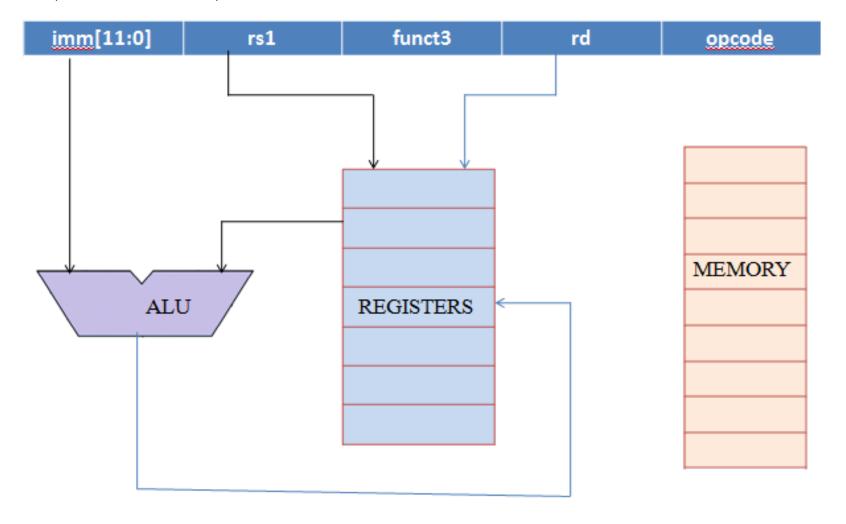




funct3=100;opcode=0010011



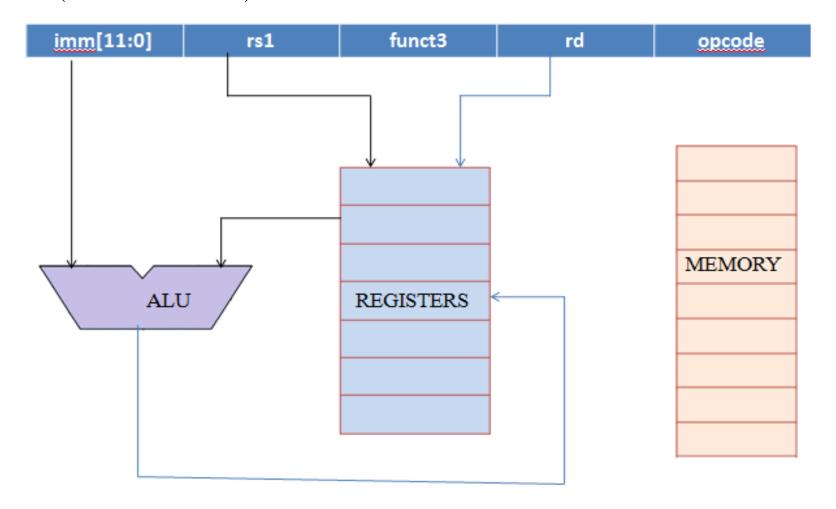
ORI (OR Immediate)



funct3=110;opcode=0010011



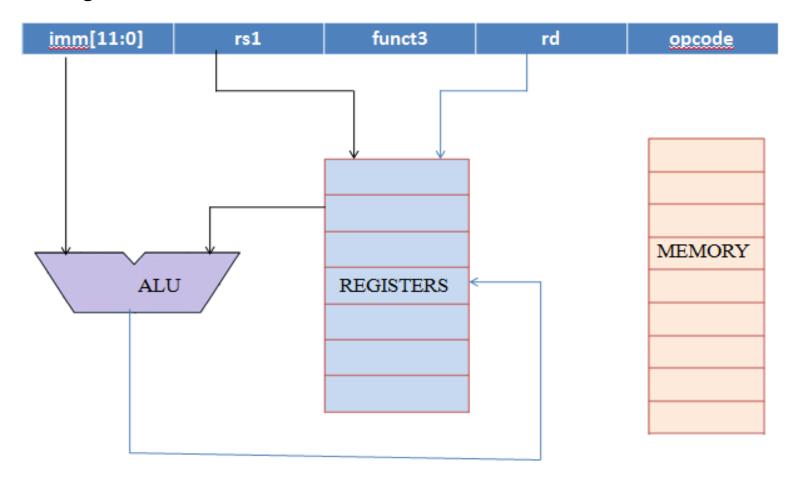
ANDI (AND Immediate)



funct3=111;opcode =0010011



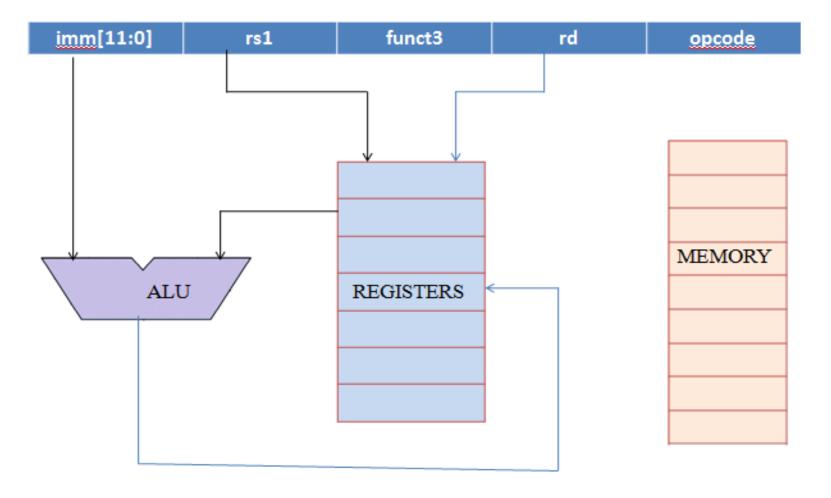
SLLI(Logical Left Shift With Immediate)



imm[11:5]=0000000; funct3=001; opcode =0010011

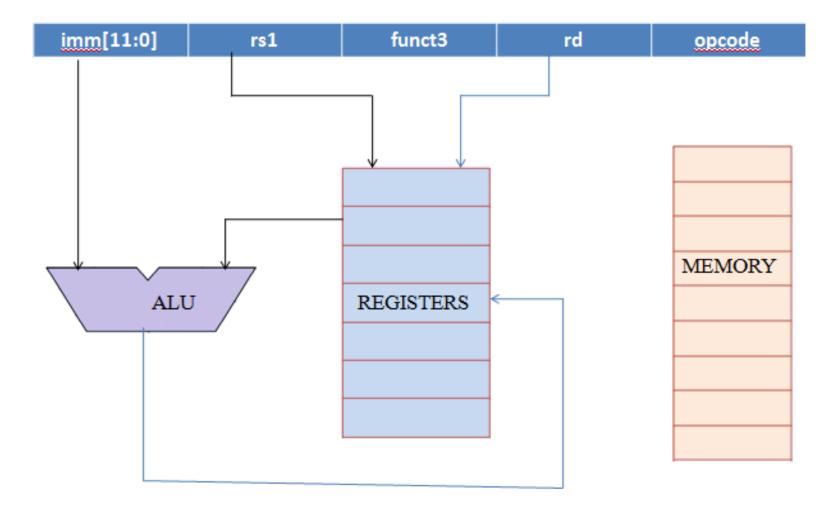


SRLI (Logical Right Shift with Immediate)



imm[11:5]=0000000; funct3=101; opcode =0010011



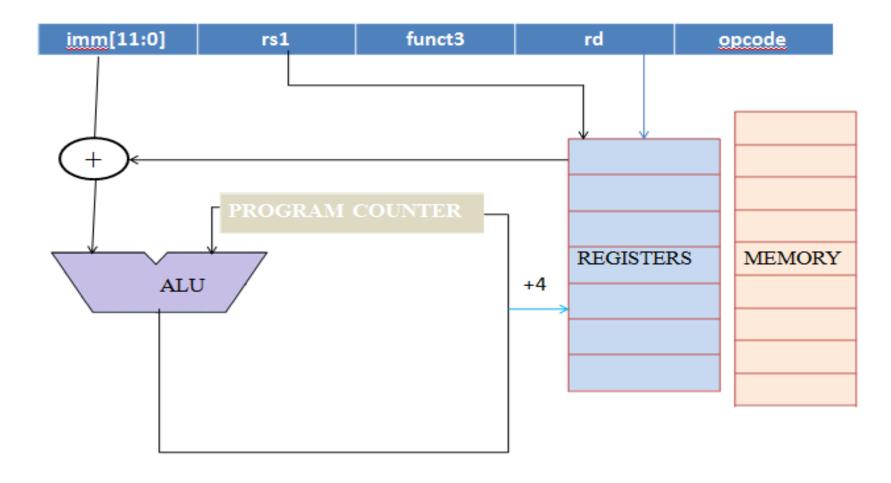


imm[11:5]=0100000; funct3=101; opcode =0010011



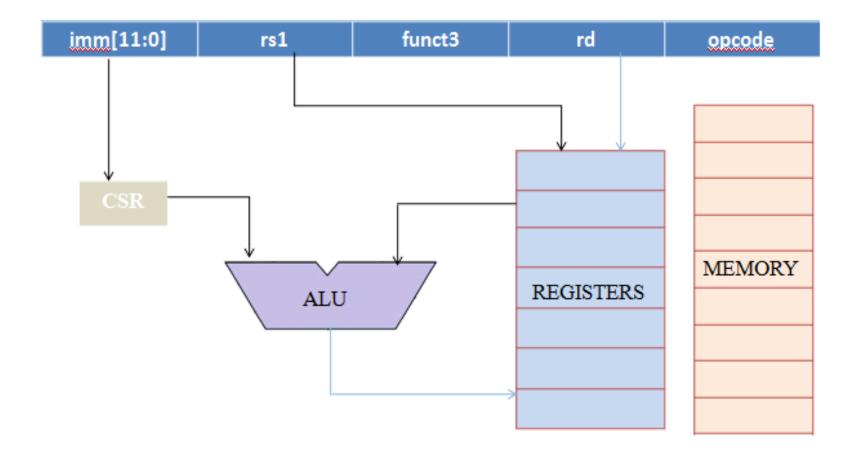
JALR(Jump And Link Register)

I-FORMAT



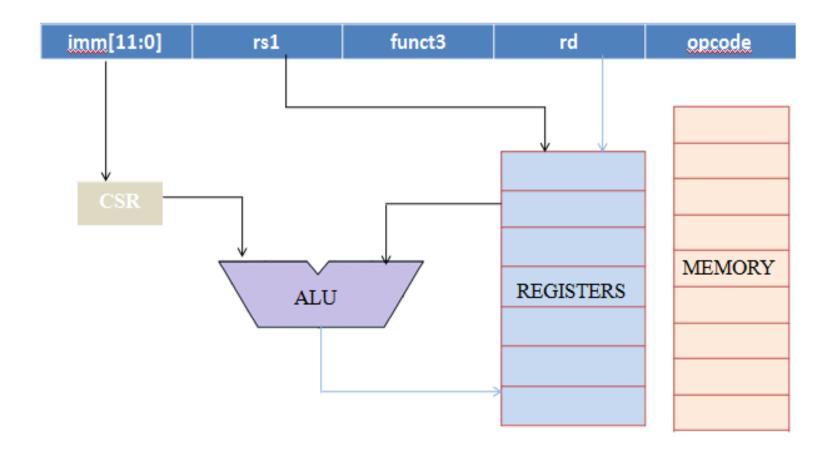
funct3=000;opcode =1100111





opcode = 1110011; funct3 = 001

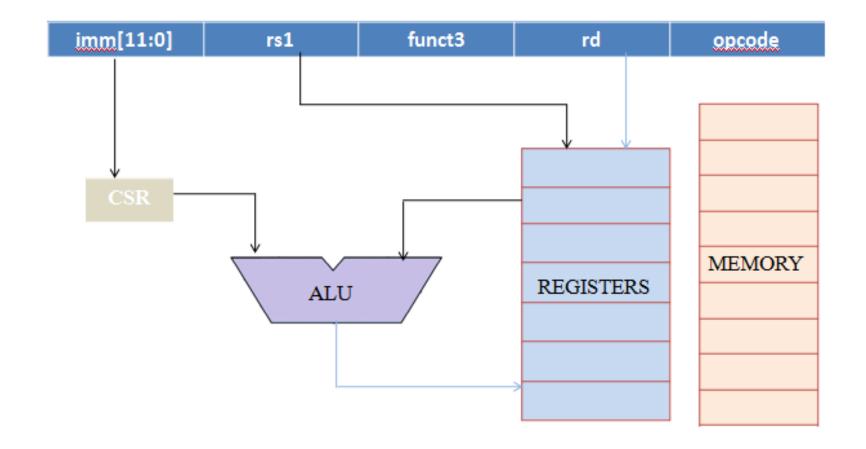




opcode = 1110011; funct3 = 010

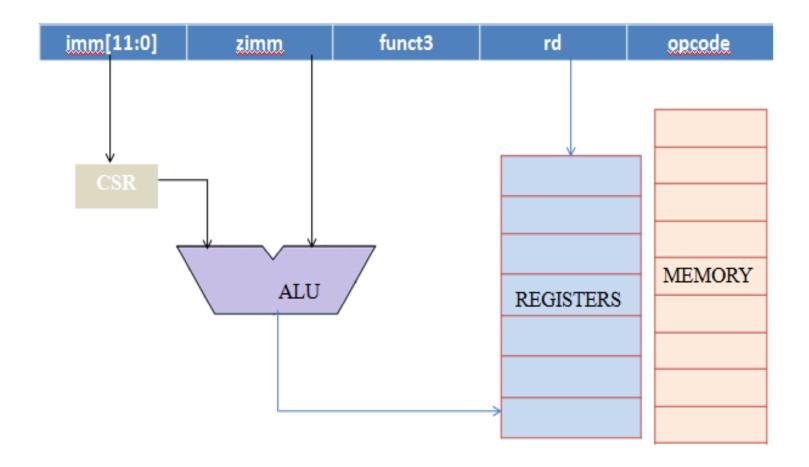


I-FORMAT



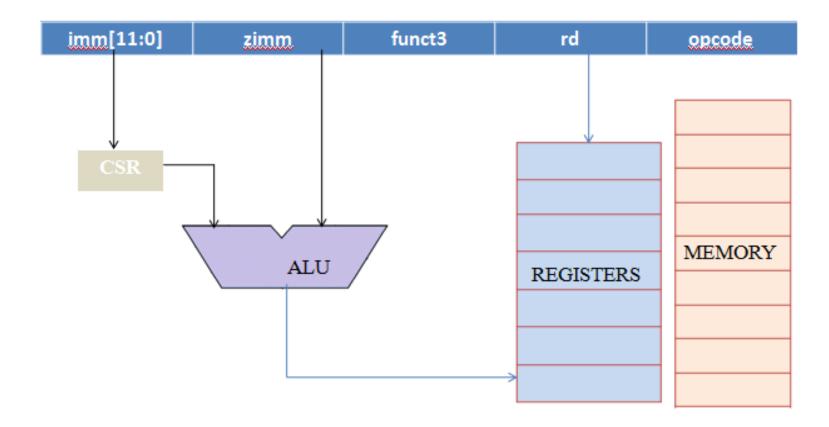
opcode = 1110011; funct3 = 011





opcode = 1110011;funct3 = 101



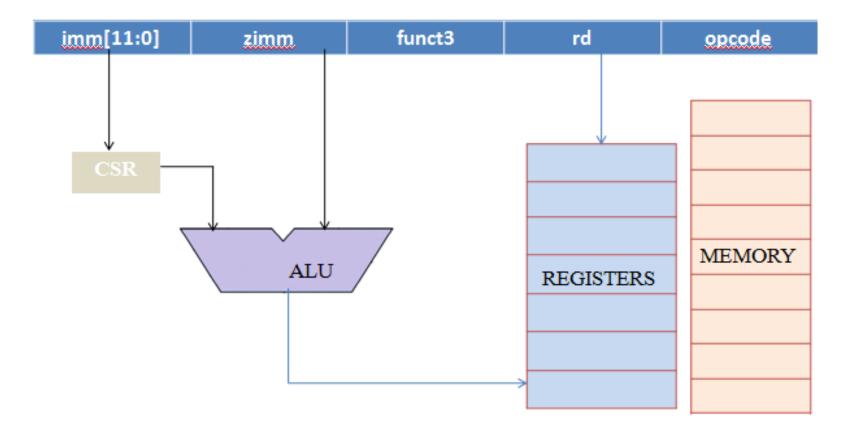


opcode = 1110011;funct3 = 110



CSRRCI (Atomic Read Write Clear Bit with Immediate)

I-FORMAT



opcode = 1110011;funct3 = 111



I- FORMAT

imm[11:0] rs1 funct3 rd opcode

ECALL – Transfer control to the operating system

EBREAK – Transfer control to the debugger

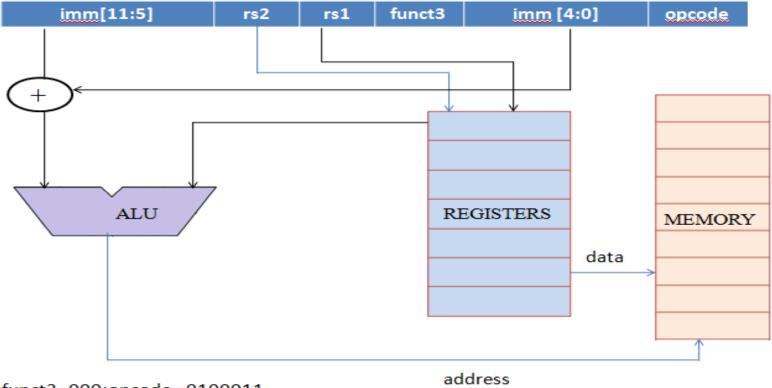
FENCE – Synchronizes thread

FENCE.I- Synchronizes write to the instruction stream.



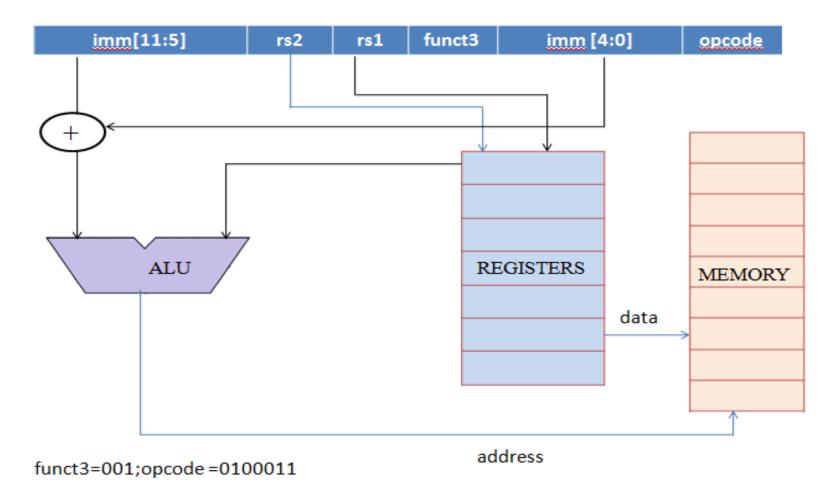
EXECUTION OF INSTRUCTIONS IN S-FORMAT

SB (Store Byte)



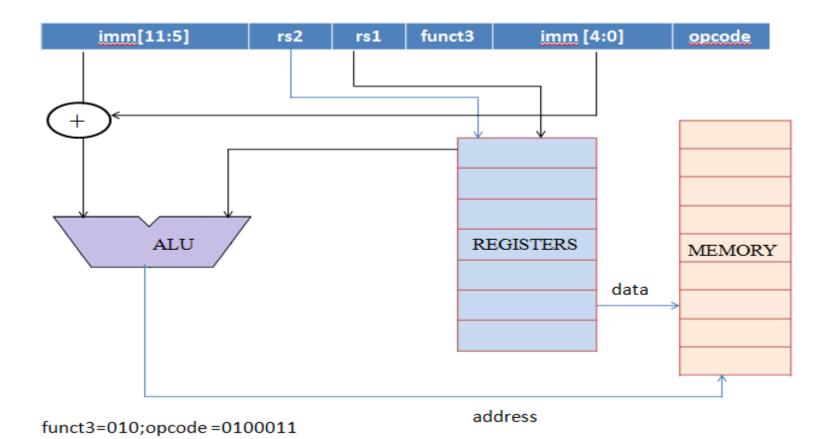
funct3=000;opcode=0100011







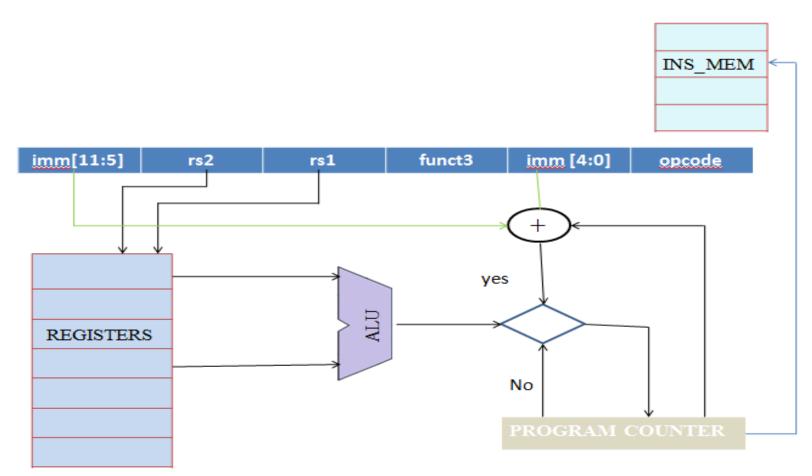
SW (Store Word) S-FORMAT





EXECUTION OF INSTRUCTION IN B-FORMAT

BEQ (Branch Equality)

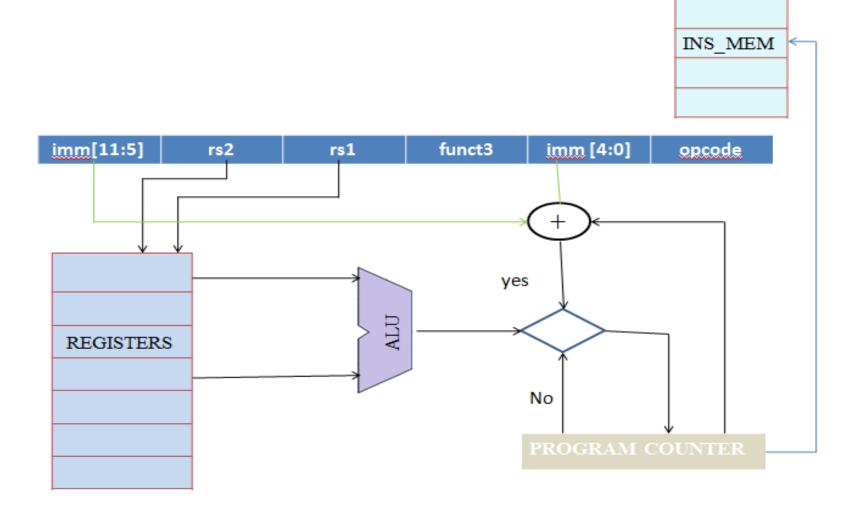


funct3=000;opcode =1100011



BNE (Branch Not Equal)

B-FORMAT

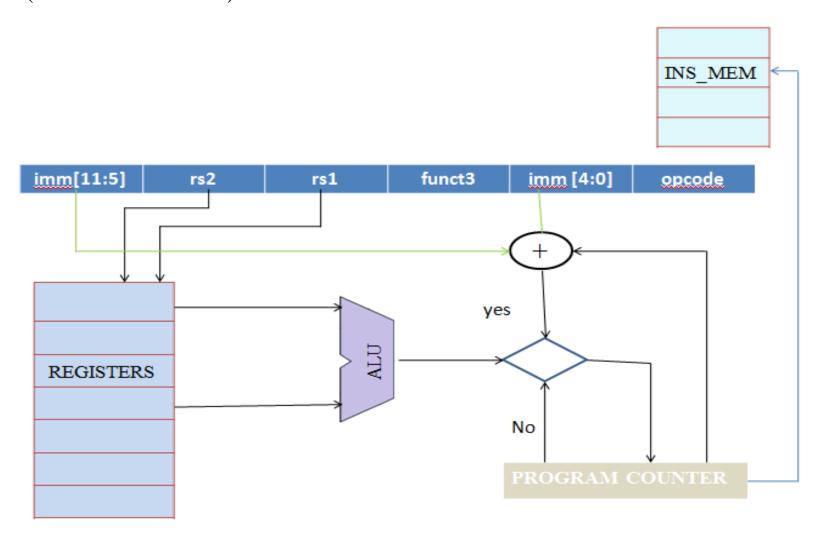


funct3=001;opcode =1100011



BLT(Branch Less Than)

B-FORMAT

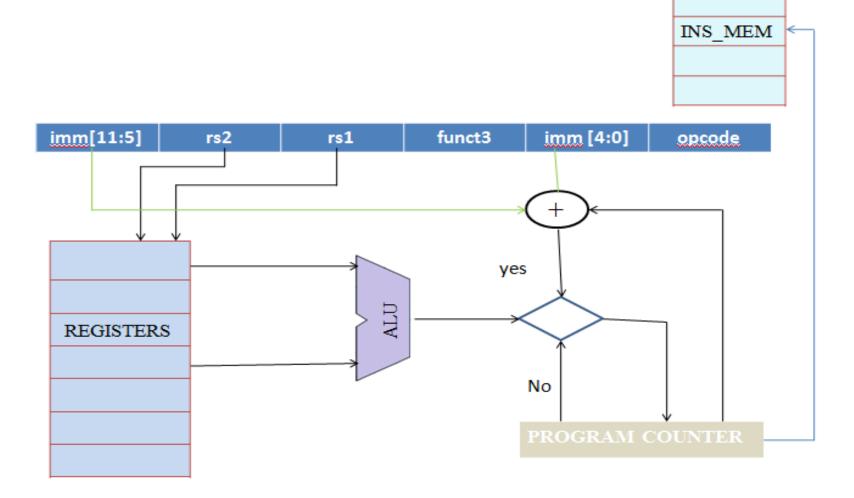


funct3=100;opcode =1100011



BGE (Branch Greater Than)

B-FORMAT

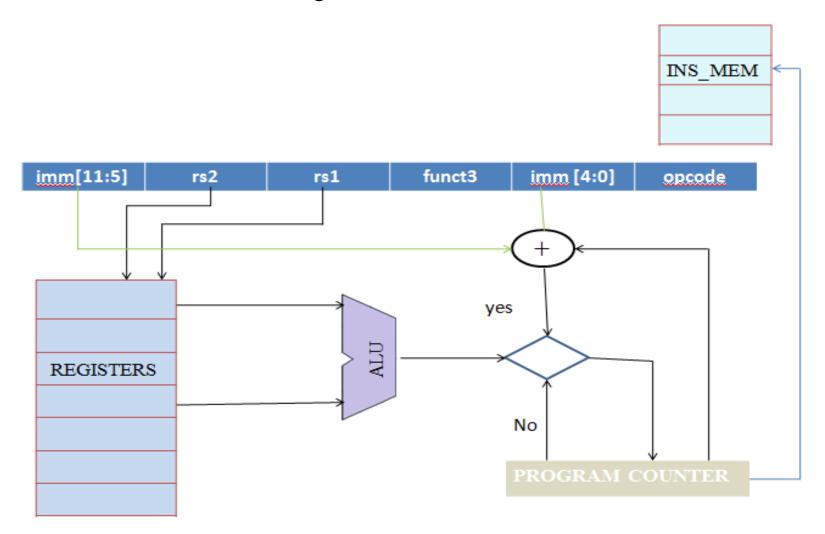


funct3=101;opcode =1100011



BLTU(Branch Less Than Unsigned)

B-FORMAT

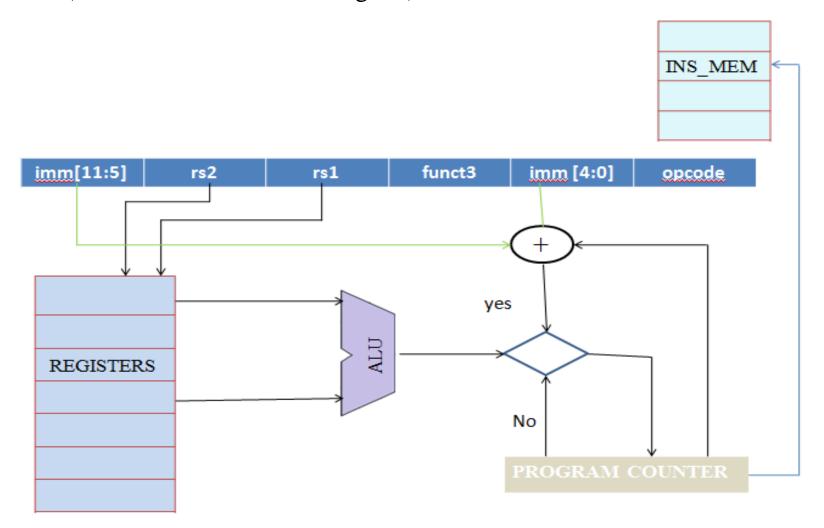


funct3=110;opcode =1100011



BGEU(Branch Greater Than Unsigned)

B-FORMAT



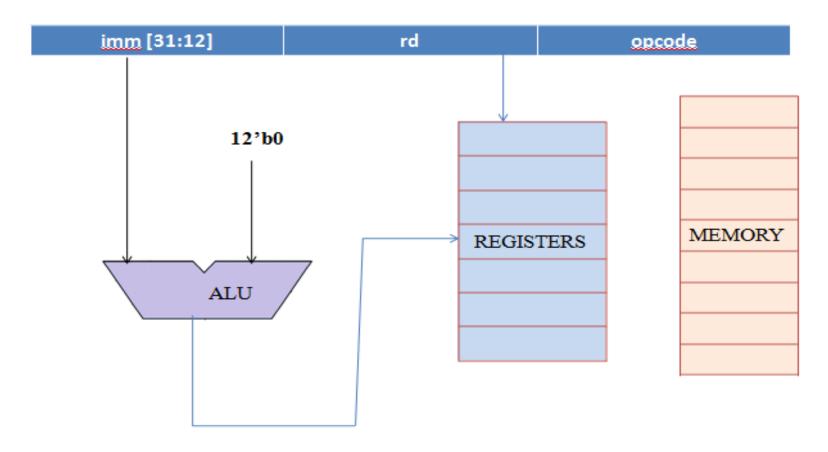
funct3=111;opcode =1100011



EXECUTION OF INSTRUCTIONS IN U-FORMAT

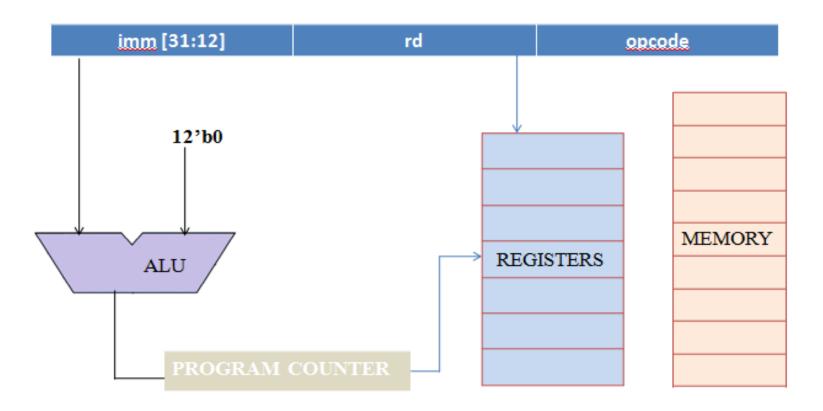
LUI (Load Upper Immediate)

U-FORMAT



opcode = 0110111





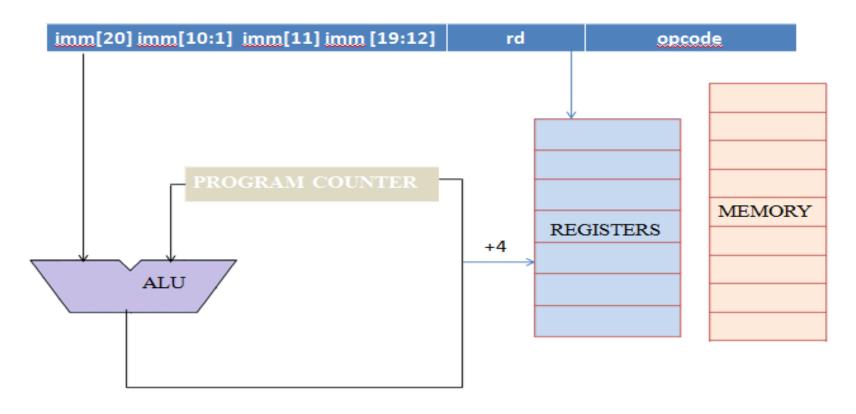
opcode = 0010111



EXECUTION OF INSTRUCTIONS IN J-FORMAT

JAL (Jump and Link)

J-FORMAT



opcode = 1101111

