Synchronous Buck Converter with Output Impedance Correction Circuit

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***Abstract*—This work is related to the improvement of the output impedance of the Buck converter by means of introducing an additional power path that virtually increases the output capacitance during transients. It is well known that in VRM applications, with wide load steps, voltage overshoots and undershoots may lead to undesired performance of the load. To solve this problem, high-bandwidth high-switching frequency power converters can be applied to reduce the transient time or a big output capacitor can be applied to reduce the output impedance. The first solution can degrade the efficiency by increasing switching losses of the MOSFETS, and the second solution is penalizing the cost and size of the output filter. The Output Impedance Correction Circuit (OICC), as presented here, is used to inject or extract a current n-1 times larger than the output capacitor current, thus virtually increasing n times the value of the output capacitance during the transients. This feature allows the usage of a low frequency Buck converter with smaller capacitor but satisfying the dynamic requirements.**

I. INTRODUCTION

The ongoing research trend in Voltage Regulation Module (VRM) design is directed to improve the dynamic response of the Buck converter by means of improving the controller [1]-[5] or by introducing an additional energy path to compensate the charge perturbation in the output capacitor [6]-[18].

Increasing the bandwidth of the classical regulator may lead to instability of the system due to the tolerances of the regulator components, temperature variations both of the converter and regulator and due to aging effects, as well due to the parasitics. In order to achieve higher robustness of the control, integration of low bandwidth linear loop and high bandwidth nonlinear loop may be applied. These solutions can be applied on the fast Buck converter with high switching frequency. The well-known nonlinear V2 control is presented [1]-[2], but it relies on sensing the output voltage ripple, which is very small compared to the DC value of the output voltage. Control techniques presented in [3]-[5] reduce the transient time utilizing the capacitor current which contains information of load behavior, thus reducing the response time of the control. The output capacitor current measurement is based on the noninvasive current sensor presented in [19].

On the other hand, the second possibility is to introduce another energy path to compensate the charge unbalance of the output capacitor [6]-[18], thus reducing the transient time and output voltage overshoot/undershoot. Most of the currently proposed solutions rely on charge-balance control techniques [6], [7], [14]-[18]. The solution presented in [6] introduces two additional resistive paths in order to inject/extract the charge from the output node. Similarly, in [7] the proposed circuit is injecting/extracting charge through auxiliary switches. Solutions from [14]-[16] utilize the auxiliary Boost converter in order to remove the additional charge from the output capacitor during the load step-down transient. The Synchronous Buck converter is used in [17] and [18] in a similar manner like the Boost from [14]-[16] for both load step-up and step-down transients.

References [8] and [9] are introducing the hybrid power system concept. In [8], the auxiliary path, implemented with a Linear Regulator (LR), behaves like high-frequency filter, suppressing the high-frequency components of the load current, thus reducing the output impedance in the high-frequency area. On the other hand, the solution in [9] combines two energy paths, implemented with LR and the Buck converter, in that manner that LR is regulating the output voltage, providing the energy only during the transients, while the Buck converter control is canceling the LR output current, thus redirecting the energy flow through the Buck converter. In [10] a non-linear trans-conductance amplifier is introduced in the system to provide an alternative energy path when the output voltage goes out of the predefined band. The solution presented in [11] utilizes the auxiliary Buck converter when the output voltage error exceeds the threshold. Both main and auxiliary converters duty cycles are saturated in order to stop further deviation of the output voltage. The synchronous Buck converter is used in [12] and [13] as a wide bandwidth voltage source connected in parallel with the main converter during the transients. When the output voltage error is outside the predefined band the auxiliary converter is connected in [12], while in [13], the auxiliary converter is connected when the output capacitor current exceeds its threshold.

Analyzing the existing solutions based on the additional energy path, the following limitations are observed:

1. The behavior of the system depends on the information from the load [6], [7].

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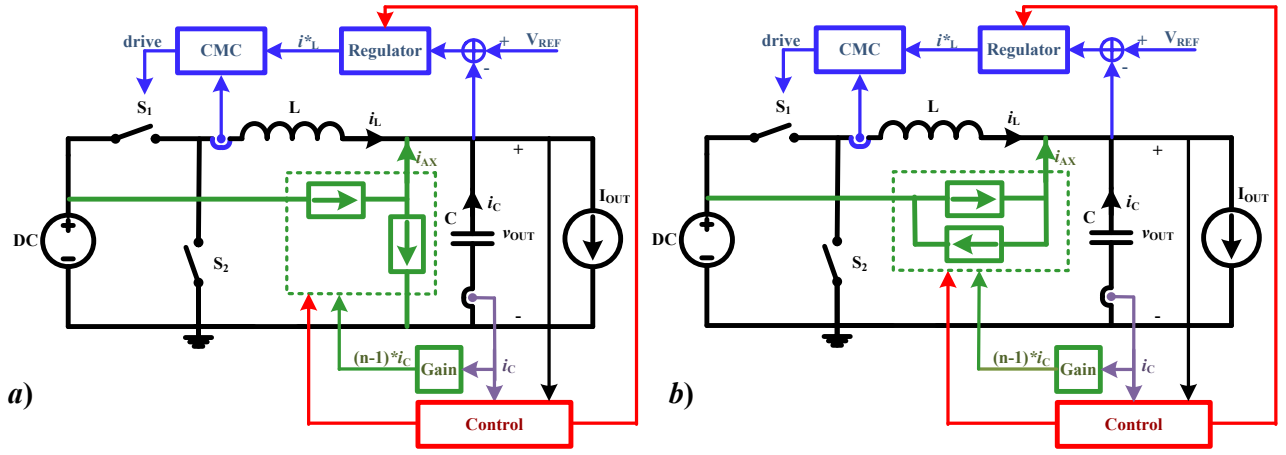

Figure 1. Synchronous BUCK converter with CMC and Output Impedance Correction Circuit a) without and b) with energy recovery path

2. The additional energy path is activated with the output voltage error in [10]-[12], [14]-[18]. The reaction of the auxiliary path is delayed and the deviation is already present.
3. Solutions based on the charge balance technique, presented in [6], [7], [14]-[18], control the system in open loop, thus their performance will be degraded on other types of the load perturbations than a step function. Additionally, the performance of the system is unknown under consecutive load steps if the transient routine is not terminated. Furthermore, perturbations in the input voltage and the tolerances of the components can affect the system behavior.
4. The LR is active all the time in [8], [9] which increases the losses, since the LR may try to compensate the inductor current ripple in the steady state.
5. The current provided by the auxiliary path is not controlled, which may lead to unpredicted and potentially damaging currents [11]-[13], [17], [18].
6. Solutions in [14]-[16] depend on the estimation of the amplitude of the load step based on the output voltage behavior which may lead to the unpredicted behavior of the system if the prediction is not performed correctly.
7. Solutions in [15], [17] and [18] rely on the prediction of the timings for the charge balance of the output capacitor, which are dependent on converter parameters and tolerances. If the timings are estimated wrongly it may cause undesired behavior of the system.
8. The output capacitor current measurements in [17], [18] are performed with a shunt resistor placed in series with the output capacitor, thus degrading the performance of the output capacitor.

The solution presented in this paper utilize additional energy path, provided by the Output Impedance Correction Circuit (OICC), in that manner that auxiliary current, injected/extracted trough this path is controlled to have n-1 times higher value than the output capacitor current with appropriate directions. In order to measure the output capacitor current, noninvasive current sensor from [19] is used. The auxiliary current is controlled, so undesired current peaks are avoided and, additionally, transient time behavior is initialized by observing measured output capacitor current and it is terminated when the error of the output voltage reaches zero. In this way the problems with the transient time estimation error are also avoided.

II. The Output Impendance Correction Circuit (OICC) – Ideal Operation

A Synchronous Buck converter with current mode control (CMC) and with the OICC is shown on Fig. 1. Depending on how the OICC is implemented, the energy transfer can be unidirectional (Fig. 1a) or bidirectional (Fig. 1b). The first, unidirectional solution corresponds to a LR implementation of the current source, while the second corresponds to bidirectional Buck converter implementation with current mode control. Both solutions penalize the overall efficiency compared with the same converter with large output capacitance, but it depends on the periodicity of the transients. The solution based on the LR as a current source is more inefficient compared with the Bidirectional Buck solution, but the current source sub-system is less complex and it is possible to obtain higher bandwidth than with the Bidirectional Buck solution (limited by the switching frequency of the Bidirectional Buck converter). On the other hand, the Bidirectional Buck converter has a higher efficiency with possibility of energy recovery, but it needs an additional inductor that cannot be easily integrated.

The system utilizes the OICC in a manner that the OICC injects/extracts a current in the output node that is n-1 times bigger than the output capacitor current with corresponding directions. This behavior of the OICC virtually increases the output capacitance n times during the transients, thus reducing the output impedance by the same factor. The main advantage of this approach is that a smaller capacitance can be used, which means lower cost and the possibility to use capacitors with a higher resonant frequency. Furthermore, allows the possibility of integration of the capacitor on the same chip together with power converter and the OICC. On the other hand, main drawbacks are increased complexity of the system and a lower overall efficiency.

From the control point of view, the implementation of the OICC does not have a big influence. As it is shown on Fig. 1, the system is composed of the main Buck converter with

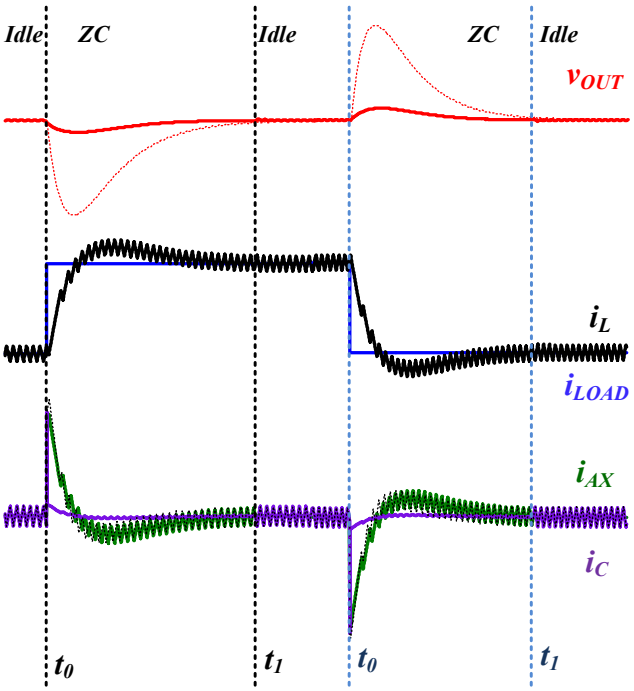

Figure 2. Ideal system waveforms: load step transitions with (solid) and without (dotted) the OICC

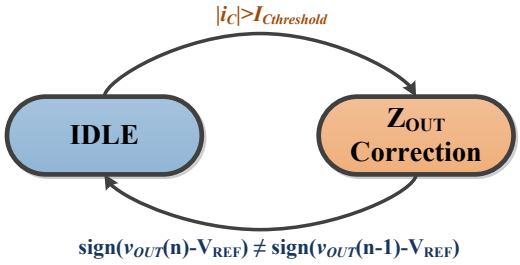

Figure 3. The State machine of the system control

a slow regulator that can be dynamically modified, the OICC that behaves like a controlled current source and the system control. The control is divided into the analog part that gives the reference to the OICC and the digital part that observes the state variables of the system and controls the main converter regulator and the OICC. Since the goal is to virtually increase the output capacitance by a factor n, the analog reference is the value of the capacitor current multiplied by n-1. The control block will allow the OICC to inject/extract that current only in the certain states of the transient routine. At the same time, in order to maintain the stability of the system, the control modifies the main converter regulator.

During the steady-state, the OICC is inactive; all energy is transferred trough the main Buck converter and it is behaving like a voltage source while the system control is observing the output capacitor current in order to initialize the transient routine when a load step occurs. In this manner, by observing the output capacitor current, the system reacts nearly instantaneously on a load perturbation, since the output capacitor current is the fastest variable in the system that sees this perturbation. If the load step has small amplitude (in both directions), the system control will ignore this transient and the main Buck regulator will cancel the disturbance. On the other hand, if the amplitude is sufficiently high, the transient routine will start. This behavior of the system is achieved by defining the band of the output capacitor current in which the main Buck regulator can control the output voltage without assistance of the OICC.

In Fig. 2 the ideal transition routine behavior is presented. The waveforms of the system variables with OICC are presented with the solid line and without the OICC are presented with dotted line. In the steady state operation, the OICC is turned off and the small load variations are regulated by the low bandwidth regulator. The system controller observes the output capacitor current and, when the amplitude of the load current, thus the output capacitor current is out of the predefined band, OICC is activated and correction of the output impedance starts. The system controller, which is implemented like the state machine, presented in Fig. 3, is triggered by the output capacitor current in moment t_0 and the system goes to the Z_{OUT} *Correction* state (*ZC* in Fig. 2). In this state, the OICC is providing n-1 times more current than output capacitor, thus reducing the amount of charge extracted/injected from/to the output capacitor. As a result the voltage perturbation is smaller. In order to end the Z_{OUT} *Correction* state, the system controller is observing the output voltage error signal. When the error changes the sign in t_1, the output voltage is equal or close to the reference voltage and that event triggers the system controller which returns the system back to the *Idle* state.

During the *Idle* state, the output capacitance is C, but during the Z_{OUT} *Correction* state, the equivalent capacitance is n·C. This affects the CMC Buck converter averaged model by moving the pole closer to the origin with the factor 1/n. Therefore, in order to maintain stability of the system in both states of operation, it is necessary to modify the regulator. The regulator is modified so the bandwidth of the Buck converter loop-gain remains the same with similar phase margin.

The average models of the main Buck converter with CMC in both states are derived and they are presented in Fig. 4. Depending on which CMC control is applied (average, peak or hysteretic window), the model will behave differently in high frequency part of the spectrum, but in the low frequency part the model can be simplified to the first order system where the reference, given by the regulator, is the current injected by a controlled current source, as shown in Fig. 4.

The averaged model presented in Fig. 4a corresponds to the system during the *Idle* state. The loop gain is given by

$$L(s) = \frac{1}{sC} R(s), \qquad (1)$$

where $R(s)$ is regulator transfer function and C is the output capacitance. The regulator needs to be designed to maintain the stability of the system.

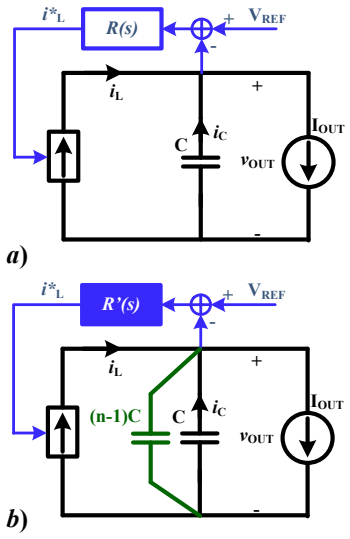

Figure 4. Avraged models of the system during *a*) the *Idle* state and *b*) Z_{OUT} *Correction* state

The second averaged model presented in Fig. 4b corresponds to the system during the Z_{OUT} *Correction* state. The loop gain is given by

$$L'(s) = \frac{1}{s\,nC} R'(s), \tag{2}$$

where $R'(s)$ is modified regulator transfer function.

In order to maintain the same dynamic characteristics of the loop gain in both cases, it is necessary to satisfy

$$R'(s) = nR(s). \tag{3}$$

By satisfying (3), the duration of the transients will be the same for the systems with and without the OICC, but the initial output impedance is reduced. Initial output impedance is given with

$$Z_{OUT}(s) = \frac{1/sC}{1+L(s)}, \tag{4}$$

while the output impedance with OICC is

$$Z'_{OUT}(s) = \frac{1/snC}{1+L(s)} = \frac{Z_{OUT}(s)}{n}. \tag{5}$$

III. Simulations

In order to verify the concept, three prototypes have been designed and simulated using *SIMetrix/SIMPLIS* software. For all simulations performed in this chapter, the OICC has been modeled like controlled current source with limited bandwidth. The transfer function of the OICC from the capacitor current i_C to the auxiliary current i_{AX}, injected by the OICC is given with

$$F(s) = \frac{i_{AX}(s)}{i_C(s)} = \frac{n-1}{1+s/2\pi f_{OICCc}}, \tag{6}$$

where n is the output capacitor multiplication factor and f_{OICCc} is the frequency up to which the OICC has constant gain n-1.

A. Prototype A

The design specifications of the Prototype A are shown in Table I. The Synchronous Buck converter is controlled with Hysteretic-Window Current-Mode-Control (HWCMC) in order to have switching frequency of 300 kHz in steady state. The bandwidth (BW) of the loop in both states is ~30 kHz, while the phase margin (PM) is higher than 65°.

TABLE I. Prototype A – Design Specification

Input voltage, V_{IN}	5 V
Output voltage, V_{OUT}	2 V
Inductance, L	5.6 µH
Output Capacitance, C_{OUT}	22 µF, 3.32 mΩ, 1.32 nH
Switching frequency, f_{SW}	~ 300 kHz
Load step	4 A, 40 A/µs
Output Capacitor multiplication factor, n	10
The OICC corner frequency, f_{OICCc}	~ 50 kHz

The system has been tested without and with the OICC on the load step of 4 A with slew rate of 40 A/µs. Since the duty cycle is close to 50%, only the load step-up transient is presented in Fig. 5, while the summary of the simulation results are shown in Table II. It shows that both overshoot and undershoot of the output voltage are reduced by factor 10 even with the limited BW of the OICC (undershoot has been reduced from initial -1580 mV to -150 mV and overshoot has been reduced from initial 1560 mV to 150 mV).

In Fig. 5 the main waveforms of the system variables without (red) and with (blue) the OICC are shown. The reduction of output voltage undershoot can be seen. Additionally, the output capacitor current is presented for both cases (with and without the OICC). It can be seen when the OICC concept is applied, that after initial spike, the output capacitor current is significantly reduced, thus the amount of charge taken from the output capacitor is reduced.

When the end of the transient is detected by the control, system enters an additional settling transient due to the regulator modification and non-zero auxiliary current.

In order to show the system robustness, the system has been tested with pulsating load during the transient routine. The waveforms of the system variables are shown in Fig. 6. The system enters in Z_{OUT} *Correction* state after initial load step-up in moment t_0 = 1 ms. After 100 µs the load current starts pulsating with period of 20 µs, amplitude of 4 A and

TABLE II. Prototype A – Simulation Results

	Load step-up		Load step-down	
	Δ V_{OUT}	***duration***	***Δ V_{OUT}***	***duration***
Basic	-1580 mV	~ 300 µs	1560 mV	~ 300 µs
OICC	-155 mV	~ 300 µs	150 mV	~ 300 µs

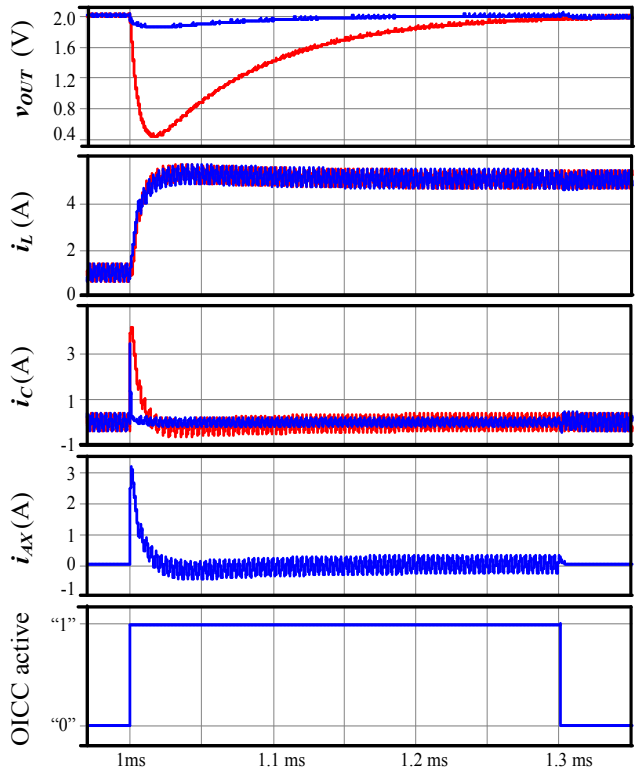

Figure 5. Main system waveforms without (red) and with (blue) OICC

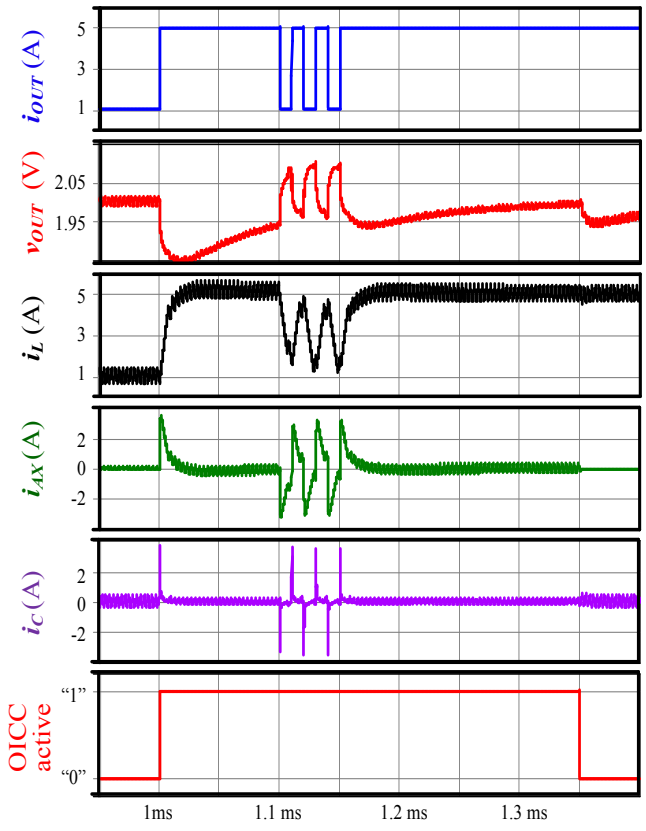

Figure 6. Main system waveforms with OICC under pulsating load

duty cycle of 50%, as shown in Fig. 6. The output voltage remains controlled, while inductor current is trying to cancel the disturbance in the system. The period of operation of the OICC has been extended by 50 µs from the initial case with single load step.

The OICC concept is maintaining the control over the system variables in both states, which is not the case with most of the solutions in the state-of-the-art, since they are compensating the disturbance in open-loop mode.

B. Prototype B

The OICC concept has been compared with the solution proposed in [6], which has been selected for the comparison since it provides a generic concept based on the charge balance technique with auxiliary energy path. In the system [6], when the transient is initialized, the duty cycle is saturated so the inductor current reaches the new value in minimum time. The auxiliary path is injecting/extracting constant current with amplitude equal to 50% of the load step. The auxiliary current has non-zero value until the inductor current reaches the new load current.

The design specifications of the Prototype B are shown in Table II. The Synchronous Buck converter is controlled with a Voltage Mode Control (VMC) during the steady-state in solution from [6] with a switching frequency of 100 kHz. In the case of the OICC approach, HWCMC control has been applied to the same converter and it is designed to have switching frequency of 100 kHz in steady state. The BW of the main Buck loop in both states of the system with the OICC is ~3.5 kHz, while the phase margin (PM) is higher than 65°.

The system has been simulated under the load step of 3 A, with infinitive slew-rate (equivalent series inductance (ESL) of the output capacitor is ignored). The simulation results are summarized in Table IV, while the waveforms of the system variables are shown in Fig. 7. The system implemented with the OICC has smaller amplitude of the output voltage undershoot and overshoot (approximately 40% smaller). On the other hand the transient is shorter in system proposed in [6] approximately 7.5 times.

TABLE III. PROTOTYPE B – DESIGN SPECIFICATION

Input voltage, V_{IN}	12 V
Output voltage, V_{OUT}	5 V
Inductance, L	100 µH
Output Capacitance, C_{OUT}	250 µF, 0.2 mΩ
Switching frequency, f_{SW}	100 kHz
Load step	3 A
Output Capacitor multiplication factor, n	10
The OICC corner frequency, f_{OICCc}	~ 300 kHz

TABLE IV. PROTOTYPE B – SIMULATION RESULTS

	Load step-up		**Load step-down**	
	Δ V_{OUT}	***duration***	***Δ V_{OUT}***	***duration***
Solution [6]	-76 mV	46 µs	71 mV	57 µs
OICC	-42 mV	385 µs	42 mV	383 µs

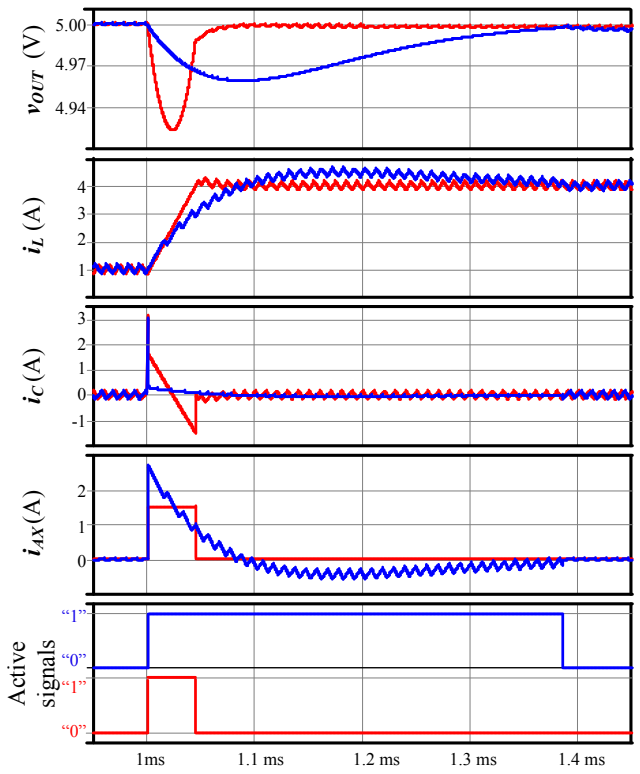

Figure 7. Main system waveforms of the system proposed in [6] (red) and with the OICC (blue)

C. *Prototype C*

Prototype C has been developed in order to compare the OICC concept with the VRM design Demo Circuit 449-A from Linear Technology presented in [20]. The VRM is implemented as a 2-Phase Synchronous Buck converter which utilizes 5.5 mF output capacitance in order to satisfy the dynamic specification for AMD HAMMER CPU. The goal of the comparison is to show that the same system can be used with smaller capacitance if the OICC concept is applied.

The design specifications of the Prototype C are shown in Table V. The 2-Phase Synchronous Buck converter is controlled with Peak-Current-Mode-Control (PCMC) with switching frequency of 150 kHz per phase. The bandwidth (BW) of the main Buck loop in both states is ~20 kHz, while the phase margin (PM) is higher than 65°.

Simulation results are summarized in Table VI, while the step-down transient waveforms are shown in Fig. 8. It can be seen both from Table VI, as well as from Fig.8 that the system has nearly the same response on the same load perturbation.

Also, it can be seen that the ripple (~7 mV) of the output capacitor voltage is bigger in the case of OICC implementation during the *Idle* state. This shows that a significant amount of area can be saved, since the output capacitor in the OICC design is ten times smaller. The cost is paid in area consumed by the OICC, which could be integrated in one chip, even in the same chip with the control and switches of the VRM.

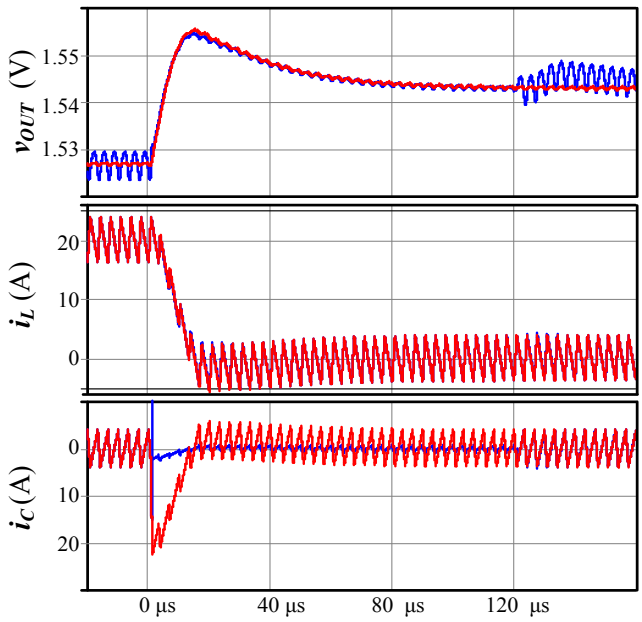

Figure 8. Main system waveforms of the Demo Circuit 449-A (red) and the system with the OICC (blue)

TABLE V. PROTOTYPE C – DESIGN SPECIFICATION

	Design [20]	**OICC**
Input voltage, V_{IN}	12 V	12 V
Output voltage, V_{OUT}	1.55 V	1.55 V
Load Line	1 mΩ	1 mΩ
Inductance, L	1 µH	1 µH
Equivalent Output Capacitance, C_{OUT}	5.5 mF, 2 µΩ, 1.1 pH	550 µF, 20 µΩ, 1.1 pH
Switching frequency, f_{SW}	150 kHz	150 kHz
Load step	20 A, 30A/µs	20 A, 30A/µs
Output Capacitor multiplication factor, n	-	10
The OICC corner frequency, f_{OICCc}	-	~ 300 kHz

TABLE VI. PROTOTYPE C – SIMULATION RESULTS

	Load step-up		**Load step-down**	
	Δ V_{OUT}	***duration***	***Δ V_{OUT}***	***duration***
Design [20]	-10 mV	~ 130 µs	12 mV	~ 130 µs
OICC	-11 mV	~ 130 µs	11 mV	~ 130 µs

IV. IMPLEMENTATION AND EXPERIMENTAL VERIFICATION

In order to validate the OICC concept, the system based on Prototype A with LR as the OICC has been build and it is presented in Fig. 9. The 20 W Synchronous Buck converter utilizes IRL3402 power switches from International Rectifier and IR2010 synchronous driver. The OICC uses three NPN transistors (ZTX1053A) and three PNP transistors (ZTX951) for the current capacity. For all operation amplifiers LM6172 has been used, except for non-invasive current sensor, which is based on AD8061.

The experimental results are presented in Fig. 10-12, while the summary of the results is presented in Table VII. In Fig.10 the load step-up transition is presented without the OICC, while in Fig.11 and Fig.12 the OICC is active. When the system is operating without the OICC (Fig.10), the output voltage undershoot is 780 mV, while the overshoot is 1.4 V. When the OICC is active, with the same load steps, the voltage undershoot is reduced to 228 mV (Fig 11-12), while the overshoot is reduced to 284 mV. The differences in the simulated results and the experimental are due to the fact that the simulations are performed with an ideal current source, while the experimental verification is performed with a resistive load which is connected/disconnected in the output node. When the output voltage deviation starts to increase (in both directions), the resistive load modifies its current, so the difference between the load current and the inductor current is not as big as in the case with the current source. In the case of the load step-up, the current source would take the constant current of 5 A, but in the case of the resistive load with deviation of 50%, the load current is reduced by double, thus the amount of charge taken from the output capacitor is smaller.

Also, the measured auxiliary current is presented (in the Fig. 11-12 the measurement of the auxiliary current is plotted with gain 1/9). Fig. 11 shows the additional settling transients due to the Buck converter regulator change when the end of transient routine is detected (84 mV for load step-up and 244 mV for load step-down).

V. Conclusions

In this paper the Output Impedance Correction Circuit (OICC) concept is presented. It allows the utilization of low switching frequency Synchronous Buck converter with small

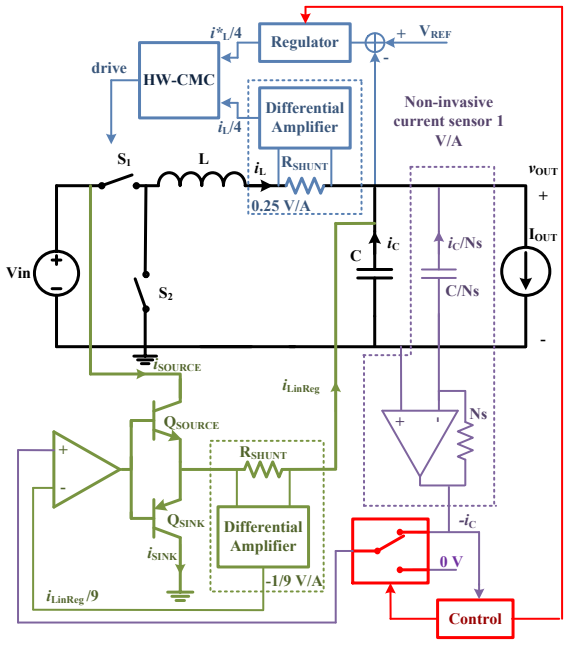

Figure 9. Schematic the OICC concept with Linear regulator like OICC – Synchronous BUCK converter (black), the inductor current measurement, driving signal generation and the regulator (blue), non-invasive current sensor (purple), the OICC (green) and system control (red)

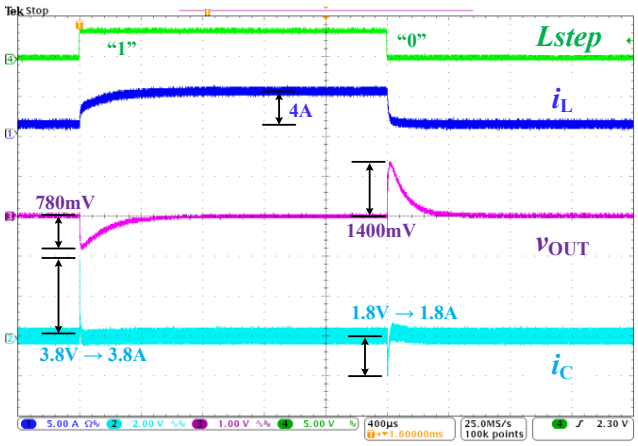

Figure 10. Experimental results – load step transients without the OICC: the load driving signal (green 5V/div), the inductor current i_L (blue 5A/div), the output voltage v_{OUT} (pink 1V/div) and measured output capacitor current i_C (light blue 2V/div), time 400µs/div

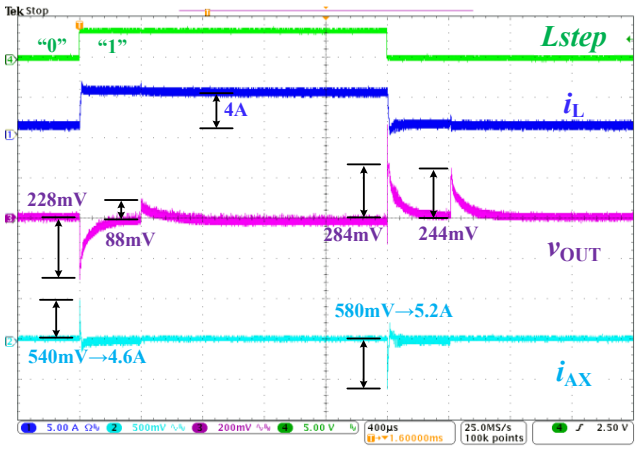

Figure 11. Experimental results – load step transients with the OICC: the load driving signal (green 5V/div), the inductor current i_L (blue 5A/div), the output voltage v_{OUT} (pink 200mV/div) and measured auxiliary current $i_{AX}/9$ (light blue 500mV/div), time 400µs/div

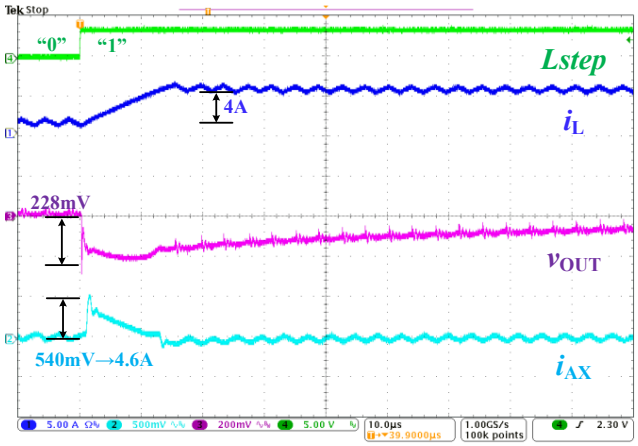

Figure 12. Experimental results – the first load step-up transient with the OICC: the load driving signal (green 5V/div), the inductor current i_L (blue 5A/div), the output voltage v_{OUT} (pink 200mV/div) and measured auxiliary current $i_{AX}/9$ (light blue 500mV/div), time 10µs/div

TABLE VII. PROTOTYPE A – SIMULATION VS. EXPERIMENTAL RESULTS

			Basic	OICC
Simulation	***Load step-up***	ΔV_{OUT}	-1580 mV	-155 mV
		duration	~ 300 µs	~ 300 µs
	Load step-down	ΔV_{OUT}	1560 mV	150 mV
		duration	~ 300 µs	~ 300 µs
Experimental results	***Load step-up***	ΔV_{OUT}	-780 mV	-228 mV (88mV)
		duration	~ 400 µs	~ 400 µs
	Load step-down	ΔV_{OUT}	1400 mV	284 mV (244 mV)
		duration	~ 400 µs	~ 400 µs

output capacitor to supply fast-dynamic high amplitude loads in VRM applications. By introducing the additional energy path in the system with controlled current, virtual increment of the output capacitor is achieved during the transients of the load. To validate the OICC concept, three prototypes have been designed and simulated, while the first one has been built and experimentally verified. The simulation shows the benefits of the OICC concept like robustness on the pulsating load or possibility of applying Adaptive Voltage Positioning (AVP) on the VRM. Furthermore, experimental results, which are in relatively good agreement with simulations, show an improvement of the transient response of the output voltage (228 mV instead of 780 mV for step-up transient and 284 mV instead of 1.4 V for step down) without extension of the transient time (400 µs).

The OICC concept shows significant improvement in dynamic. Furthermore, the reaction time is reduced due to the fact that the system responses almost instantaneously since the output capacitor current is the first system variable that contains the information of the load behavior. Also, the concept does not rely on the transient time estimation, since the transient is finished when the output voltage error reaches zero. The auxiliary current is controlled, thus the undesired peaks in the current are avoided. Furthermore, all the limitations mentioned in the introduction are not present in the proposed concept. The main drawback is that the performance is sensitive on the output capacitor current sensor, but, since the OICC has limited BW, the effects are reduced. The second one is that the OICC introduces additional perturbance in the system when the transient is finished. The overall efficiency is penalized, but it depends on the periodicity of the load transients. The linear regulator solution penalizes efficiency due to large voltage drop between the terminals. On the other hand, the implementation with Bidirectional Buck converter increases efficiency with energy recovery, but penalizes the complexity.

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