A Systematic Approach to DC-Bus Control Design in Single-Phase Grid-Connected Renewable Converters

Masoud Karimi-Ghartemani, *Senior Member, IEEE*, Sayed Ali Khajehoddin, *Member, IEEE*, Praveen Jain, *Fellow, IEEE*, and Alireza Bakhshai, *Senior Member, IEEE*

***Abstract*—This paper presents a method for design and control of dc-bus capacitance and transients in a renewable single-phase grid-connected converter. Conventionally, a proportional (P) or proportional-integrating (PI) controller is commonly used and the design stage is performed using trial-error or using a simplified analysis that does not take the dynamics of the current control loop into consideration. This paper proposes 1) a systematic and efficient method for design of dc-bus PI controller gains; and 2) an accurate method for the design of the dc-bus controller gains without neglecting the dynamics of the current control loop. Two main objectives are to have control over the amount of output current harmonics and over the level of bus fluctuations caused by random input power swings. The proposed method is transparent and it provides a convenient and rigorous insight for the designer to properly select the size of dc-bus component and to determine the controller gains.**

***Index Terms*—DC-bus control, dc-bus design, distributed generation, renewable energy.**

I. Introduction

INTERMITTENT nature of renewable sources such as wind and solar requires employment of power electronic converters with adequate controls to properly respond to the input power transients. A commonly used converter is the two-stage topology [1], [2] where, normally, the first stage performs the power extraction and also provides a suitable voltage level for the second stage; and the second stage generates and injects the stable ac power to the grid at a low level of harmonics. A passive (capacitive or inductive) element is often used between the two stages of a two-stage converter [3]. This element decouples the power pulsation of the grid side from the source side and, thus, prevents deviations from the optimum point [4]. In other words, the passive component will act as an energy storage to supply the oscillatory output power demand. The passive element serves as the dc side for the second-stage inverter and is also called dc bus or dc link.

There are two issues pertaining to the dc bus in a single-phase application: double-frequency (2-f) ripples in the loop and the bus fluctuations. The 2-f ripples are natural byproduct of the single-phase ac application [5]. In the control loop, such ripples distort the reference for the output current. This distortion is mainly in terms of a third harmonic and also a phase shift (which causes reactive current injection). The fluctuations in the bus are caused by random changes in the input power of a renewable energy system. These fluctuations, when cross the limits, activate the protection devices and shut off the input or output stage causing a limit-cycle behavior and they decrease the efficiency. Therefore, in designing the controls for such a converter, the control objectives pertaining to the dc bus may be summarized as follows: 1) regulate the average value of the stored energy at a given value; 2) minimize the fluctuations of the stored energy in response to input power transients; and 3) prevent the two problems of generation of output current harmonics and deviation from unity power factor operation caused by the loop ripples. It is worthwhile mentioning that both aforementioned undesired effects become less pronounced when the size of bus component becomes larger. However, unnecessary increase in the size of bus component increases the cost and also the physical size and weight of the converter and can decrease its lifetime too. Therefore, the aforementioned control objectives are to be achieved without unnecessary increase in the size of the bus component.

For balanced three-phase systems, the 2-f output power oscillations are not reflected on the passive component due to the symmetry of oscillating powers. Moreover, application of *dq*-transformation generates dc signals and facilitates modeling of the converter by linear time invariant (LTI) control loops [6]. As a result, the control objectives listed previously may be addressed using the widely available linear theory tools [7]–[12]. In single-phase topologies, however, the control loops cannot be easily put within the framework of LTI systems and this makes the control objectives more challenging.

There are various converter topologies for single-phase grid-connected renewable applications [3], [13], [14]. Fig. 1 shows a commonly used power converter along with the related control systems for single-phase grid-connected applications. The bus control provides a signal that, after being multiplied with the phase-locked loop (PLL)-synchronized signal of grid voltage, generates a reference for the ac grid current. This reference is then forwarded to the current control loop to generate the actual ac current. Due to the presence of this multiplication

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M. Karimi-Ghartemani is with the Department of Electrical and Computer Engineering, Mississippi State University, MS 39762 USA (e-mail: karimi@ece.msstate.edu).

S. A. Khajehoddin is with the SPARQ Systems Inc., Kingston, ON K7L3N6 Canada (e-mail: akhajehoddin@sparqsys.com).

P. Jain and A. Bakhshai are with the Department of Electrical and Computer Engineering, Queens University, Kingston, ON K7L 3N6 Canada (e-mail: praveen.jain@queensu.ca; alireza.bakhshai@queensu.ca).

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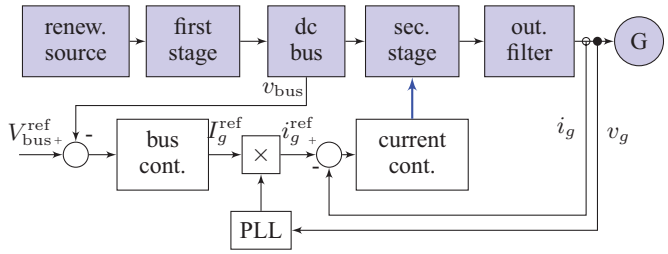

Fig. 1. Commonly used bus-control structure.

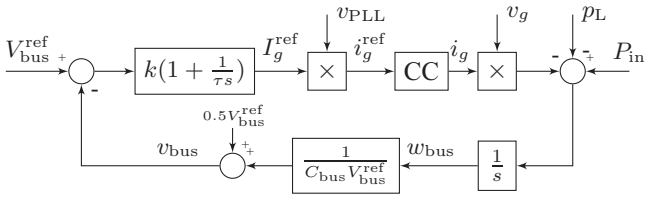

Fig. 2. Model of the bus-voltage control system.

in the control loop, the overall system equations become time varying. Moreover, the system equations are nonlinear due to the nonlinear relationship between bus energy and its voltage. Both effects become more pronounced when the size of the passive component decreases.

The bus controller in its simplest form is a P [15] or a PI controller [16], [17]. When a P controller is used, a feed-forward of the input power is also necessary. However, such a feed-forward path increases the coupling between input and output stages and, thus, any noise or fast oscillation at the input power can create harmonics at the output reference current. The PI controller avoids this shortcoming at the expense of more complicated design stage.

The objective of this paper is to develop a systematic and efficient method to design the PI controller's gains in Fig. 1 to achieve the control objectives aforementioned. To this end, this paper first presents a method without including a model of the current control system. This paper then proceeds to present a complete modeling of the system including the current control system. The proposed approach allows fast design of the bus controller and gives a full picture of the interactions that occur between the two nested loops. The results of the proposed approach are highly useful in an efficient design of a dc-bus controller without unnecessary increase in the size of the bus element.

II. Study System

The study system is based on a voltage-source converter with a capacitor $C_{\rm bus}$ as the bus component. The voltage of the bus is denoted by $v_{\rm bus}$. The instantaneous bus energy is equal to $w_{\rm bus} = \frac{1}{2}C_{\rm bus}v_{\rm bus}^2$. Since the focus of this paper is on bus control, there is little or no discussion on the current control system. It is assumed that the output filter is a first-order inductive filter and the current control loop is a proportional-resonant (PR) controller properly designed to have desirable transient response for the current control loop. The method of designing the PR controller gains presented in [18] is used.

The dc value of the bus voltage is denoted by $V_{\rm bus}$ and the reference value for $V_{\rm bus}$ is available and is denoted by $V_{\rm bus}^{\rm ref}$. This value is provided by the maximum power tracking algorithm (MPTA) [19] in a single-stage converter topology. In this topology, the MPTA simply finds the optimum value of the voltage and forwards it to the bus control. The bus controller should be fast enough to track that command in order to maximize the amount of energy harvested. In a two-stage topology, the bus-voltage reference should properly be selected to ensure linear operation of the inverter. In this case, the bus-voltage reference value does not change by the first stage and there is basically no interaction between the controls for the two stages. However, again the bus control system should be fast enough to prevent large transients on the dc bus.

Let the input power be denoted by $P_{\rm in}$ and its rated value be P. The grid voltage is assumed to be a pure sinusoid voltage $v_g = V_g \sin\omega t$ and the PLL provides a normalized signal synchronous with v_g that is $v_{\rm PLL} = \sin\omega t$. The numerical values for the study system are listed in (1). The bus capacitance $C_{\rm bus}$ is one of the design parameters among the bus-voltage controller gains k and τ in $G_{\rm PI}(s) = k(1+\frac{1}{\tau s})$

$$\begin{aligned} V_g &= 240\sqrt{2}\ \text{V}, \quad \omega = 2\pi 60\ \text{rad/s} \\ V_{\rm bus}^{\rm ref} &= 400\ \text{V}, \quad P = 250\,\text{W}. \end{aligned} \tag{1}$$

III. Modeling of the Bus-Voltage Control Loop

The input power to the bus is $P_{\rm in}$ and the output power is transferred to the grid by the inverter and through the output filter. Neglecting possible losses, the balance of power relationship can be expressed as

$$P_{\rm in} = P_{\rm bus} + P_{\rm out} = C_{\rm bus}v_{\rm bus}\dot{v}_{\rm bus} + P_L + v_g i_g \tag{2}$$

where $P_L = Li_g\frac{\rm di_g}{\rm dt}$ is the instantaneous power of the output inductance and i_g is its current.

Fig. 2 shows a detailed block diagram including an approximate linear model of the bus control system, where CC stands for the current control system. In order to understand the relationship between this diagram and (2), it shall be noticed that the following approximation is used:

$$\begin{aligned} w_{\rm bus} &= \frac{1}{2}C_{\rm bus}v_{\rm bus}^2 \approx C_{\rm bus}V_{\rm bus}^{\rm ref}(v_{\rm bus} - V_{\rm bus}^{\rm ref}) + \frac{1}{2}C_{\rm bus}(V_{\rm bus}^{\rm ref})^2 \\ &= -\frac{1}{2}C_{\rm bus}(V_{\rm bus}^{\rm ref})^2 + C_{\rm bus}V_{\rm bus}^{\rm ref}v_{\rm bus}. \end{aligned} \tag{3}$$

Equation (3) yields that

$$v_{\rm bus} = \frac{w_{\rm bus}}{C_{\rm bus}V_{\rm bus}^{\rm ref}} + \frac{1}{2}V_{\rm bus}^{\rm ref}.$$

The relative error in this approximation may be defined and calculated as

$$\frac{\Delta w_{\rm bus}}{W_{\rm bus}^{\rm ref}} = \frac{\frac{1}{2}C_{\rm bus}v_{\rm bus}^2 - C_{\rm bus}V_{\rm bus}^{\rm ref}(v_{\rm bus}-V_{\rm bus}^{\rm ref}) - \frac{1}{2}C_{\rm bus}(V_{\rm bus}^{\rm ref})^2}{\frac{1}{2}C_{\rm bus}(V_{\rm bus}^{\rm ref})^2} = \left(\frac{v_{\rm bus}-V_{\rm bus}^{\rm ref}}{V_{\rm bus}^{\rm ref}}\right)^2 \quad (4)$$

that reaches a value of 0.01 for 10% of the bus-voltage deviations. Therefore, the approximation is justified.

It is worthwhile mentioning that the control loop may be closed on $w_{\rm bus}$ (or on $v_{\rm bus}^2$) instead of $v_{\rm bus}$. Using w instead of v makes the control loop linear and obviates the need for the aforementioned approximation. This method is adopted in some literature [20], however, we use the voltage variable because it is popular. The achieved results on this paper on efficient design of a controller are equally applicable to both structures.

The block diagram of Fig. 2 shows that, even if the CC and inverter operation is totally linear, the whole loop is not in the form of an LTI loop due to the two multiplications before and after the CC unit. These two multiplications introduce time-varying terms into the equations. Moreover, apart from the aforementioned linear approximation, there are two other points where nonlinearities are introduced in the loop. One is at the inverter point where it multiplies the CC signal into the bus voltage.[1] The second one is caused by the inductance power P_L, that is, multiplication of the grid current with inductance voltage and this introduces a nonlinearity to the loop.

IV. Simplified Modeling, Analysis, and Design of the Bus-Voltage Control Loop

A. Modeling

Different modeling techniques and simplifying assumptions can be used to design a controller for the given system. An accurate modeling takes all modes of the system into consideration at the expense of making it more complicated to analyze. The simplest, but reasonably accurate, analysis of the loop and design of control is first performed in this section. This analysis is based on the assumptions that 1) the CC loop is ideal/fast and its transients are neglected as compared to the bus-voltage control loop; and 2) the nonlinearities are neglected. The simplified diagram is shown in Fig. 3. The CC is substituted with unity gain and then the two multipliers, which generate $v_{\rm PLL}v_g = V_g\sin^2(\omega t) = \frac{V_g}{2} - \frac{V_g}{2}\cos(2\omega t)$, are approximated by $\frac{V_g}{2}$.

The characteristic equation of the LTI loop of Fig. 3 is

$$1 - k\frac{V_g}{2C_{\rm bus}V_{\rm bus}^{\rm ref}}\left(1+\frac{1}{\tau s}\right)\frac{1}{s} = 0. \quad (5)$$

[1]Such nonlinearity can be avoided by incorporating a term $\frac{V_{\rm bus}^{\rm ref}}{v_{\rm bus}}$ in the pulsewidth modulation method [21]. We have adopted this strategy in the whole analysis presented in this paper.

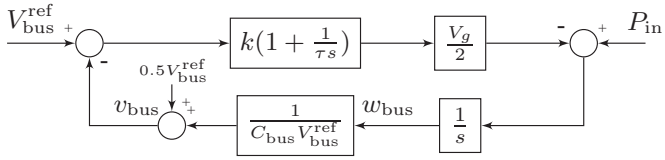

Fig. 3. Simplified model of the bus-voltage control system.

This results the equation $s^2 + 2\zeta\omega_n s + \omega_n^2 = 0$ where

$$2\zeta\omega_n = -k\frac{V_g}{2C_{\rm bus}V_{\rm bus}^{\rm ref}}, \quad \omega_n^2 = -k\frac{V_g}{2C_{\rm bus}V_{\rm bus}^{\rm ref}\tau} = \frac{2\zeta\omega_n}{\tau}. \quad (6)$$

The roots of the characteristic equation are located at $s = \sigma \pm j\omega$ where

$$\sigma = -\zeta\omega_n, \omega = \omega_n\sqrt{1-\zeta^2}.$$

The stability condition requires that $k < 0$ and $\tau > 0$. The design stage involves adjusting the gains k and τ to minimize the bus-voltage transients and the grid current harmonics.

B. Bus-Voltage Fluctuations

To derive a relationship between the bus-voltage transient response and the controller gains, it is noticed that the transfer function from the input power to the bus voltage is

$$G(s) = \frac{V_{\rm bus}(s)}{P_{\rm in}(s)} = \frac{1}{C_{\rm bus}V_{\rm bus}^{\rm ref}}\frac{s}{s^2+2\zeta\omega_n s+\omega_n^2} \quad (7)$$

where definition of ζ and ω_n is given in (6). The response of this function to a step jump of power equal to P is

$$V_{\rm bus}(t) = \frac{P}{C_{\rm bus}V_{\rm bus}^{\rm ref}\omega_n\sqrt{1-\zeta^2}}e^{-\zeta\omega_n t}\sin(\omega_n\sqrt{1-\zeta^2}t).$$

The value of peak is calculated by solving $\dot{V}_{\rm bus}(t) = 0$. The normalized peak fluctuation is defined and calculated as

$$V_p = \frac{V_{\rm bus}^{\rm max}}{V_{\rm bus}^{\rm ref}} = \frac{P}{C_{\rm bus}(V_{\rm bus}^{\rm ref})^2\omega_n}e^{-\frac{\zeta\cos^{-1}\zeta}{\sqrt{1-\zeta^2}}}. \quad (8)$$

C. Output Current Harmonics

In order to derive a relationship between the output current harmonics and the controller gains, it shall be noticed that, as far as the bus control loop is concerned, the harmonics are mainly caused by the 2-f ripple that exists on the bus controller's output signal.[2] This ripple is a result of oscillating component of the output power that has a magnitude of $\frac{V_g I_g}{2}$, where I_g is the magnitude of the output current and satisfies $P_{\rm in} = \frac{V_g I_g}{2}$. The ac pulsating power passes through the $\frac{1}{s}$ block, and then through $1/(C_{\rm bus}V_{\rm bus}^{\rm ref})$ unit to create the bus-voltage ripples. The

[2]This 2-f ripple, when multiplied with the PLL signal, generates a whole range of harmonics in the current reference signal. Assuming that the PLL signal is clean, the 2-f ripple generates a single and a triple-frequency component. The first component manifests as a reactive power injection and the triple-frequency as a third harmonic.

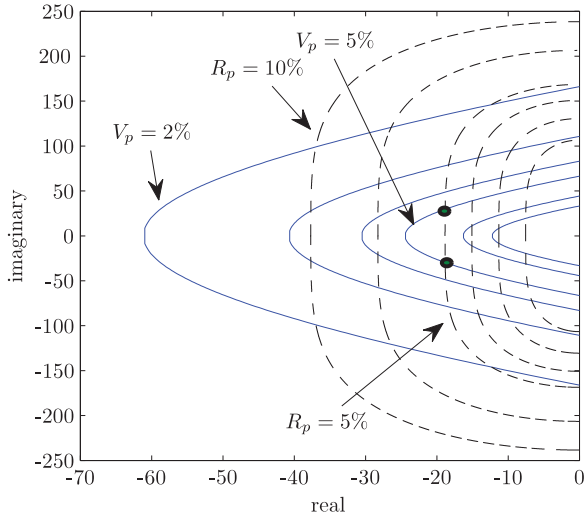

Fig. 4. Loci of V_p = const. and R_p = const. on the complex plane, $s = \sigma + j\omega$, corresponding to the closed-loop poles.

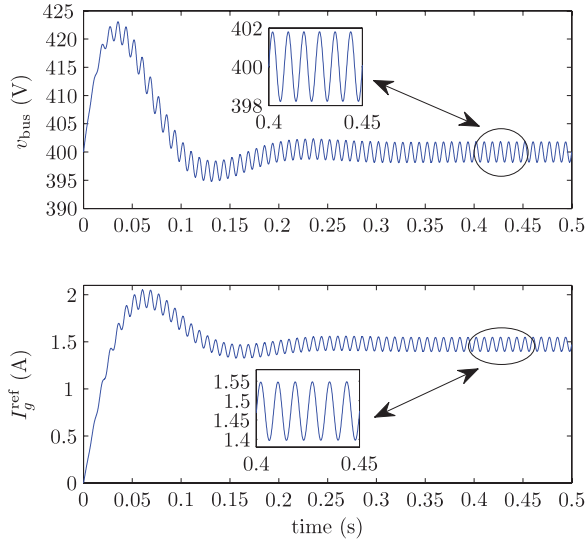

Fig. 5. Bus voltage (on top) and the PI controller's output (at bottom) responses to a 250-W step jump at the input power. Bus capacitance is 470 μF and the controller gains are $k = -0.04, \tau = 0.03$ (that corresponds to $\zeta = 0.54$ and $\omega_n = 35$ obtained by choosing the marked points on Fig. 4).

magnitude of the bus-voltage ripple in full power is then equal to

$$\tilde{V}_{\rm bus} = P\frac{1}{|j2\omega|}\frac{1}{C_{\rm bus}V_{\rm bus}^{\rm ref}} = \frac{P}{2\omega C_{\rm bus}V_{\rm bus}^{\rm ref}}. \tag{9}$$

The magnitude of the 2-f ripple on the reference current is equal to $I_2 = \frac{V_g I_g}{2}|\frac{1}{j2\omega}|\frac{1}{C_{\rm bus}V_{\rm bus}^{\rm ref}}|k(1+\frac{1}{\tau 2j\omega})|$. The normalized current ripple ratio is defined and calculated as

$$R_p = \frac{I_2}{I_g} = \frac{V_g}{8\omega^2 C_{\rm bus}V_{\rm bus}^{\rm ref}}\frac{|k|}{\tau}\sqrt{4\tau^2\omega^2+1}. \tag{10}$$

Using (6), R_p can be expressed in terms of ζ and ω_n as

$$R_p = \frac{I_2}{I_g} = \frac{\omega_n^2}{4\omega^2}\sqrt{\frac{16\zeta^2\omega^2}{\omega_n^2}+1}. \tag{11}$$

Notice that R_p does not depend on the capacitor value. The 2-f ripples on the reference current magnitude cause a third harmonic with magnitude of $0.5R_p$ at the reference point of the CC loop. Assuming that $G_{\rm cc}(s)$ is the closed-loop transfer function of the CC loop, the output current will have a third harmonic with magnitude of $0.5R_p|G_{\rm cc}(j3\omega)|$. This can be considered as an approximate value for the output current total harmonic distortion (THD). In other words

$$h_3 = 50R_p|G_{\rm cc}(j3\omega)|\%, \quad \text{THD} \approx 50R_p|G_{\rm cc}(j3\omega)|\%. \tag{12}$$

D. New Grid for Complex Plane

The loci of $V_p = K$ and $R_p = K$ when drawn on the complex plane for different values of K portray a grid that is highly useful for design purposes. Such a loci for $K = 0.02, 0.03, 0.04$ 0.05, 0.075, and 0.1 are shown in Fig. 4 for $C_{\rm bus} = 470$ μF. It is observed that the loci of $V_p = K$ become smaller and approaches toward the origin as the constant value increases. In other words, in order to have a small voltage fluctuation, the closed-loop poles must lie on curves with small constants, meaning that they must be pushed left and up. On the other hand, the loci of $R_p = K$ become larger as the constant value becomes larger. This means that, in order to have small THD, the poles must be pushed right and down (toward the origin). This shows the tradeoff that exists between the two control objectives. The location of poles must be selected appropriately to satisfy both requirements. For example, the points marked by circles on the graph correspond to $V_p = 0.05$ and $R_p = 0.05$, that is, to 5% bus-voltage fluctuation and 5% 2-f ripple on the reference current magnitude. For this point, $\zeta = 0.54$ and $\omega_n = 35$ and the controller gains are $k = -0.04$ and $\tau = 0.03$ s (for a bus capacitance of $C_{\rm bus} = 470$ μF).

Fig. 5 shows the simulation results for the aforesaid setting of controller. The simulation is performed on a complete model that includes all nonlinearities. The results closely match the analytical results. The voltage fluctuation is 5%, that is, 20 V. The bus-voltage ripples is about 1.75 V, that is, consistent with (9). The input power of $P = 250$ W corresponds to an output current of $I_g = \frac{2P}{V_g} = 1.47$ A. The 2-f ripple is about 75 mA that translates to 5%. All this is consistent with the results of analysis.

It is obvious that decreasing the capacitor value reduces the chance of finding an admissible region for closed-loop poles that satisfies the two control objectives. This fact can serve as a criterion to find the minimum value of capacitance. Assume, for example, that it is desired to have a maximum V_p of 5% and a maximum R_p of 5%. These two curves and the admissible regions for the location of poles of the bus-voltage control loop are shown in Fig. 6 for four values of capacitances equal to 470, 370, 270, and 170 μF. It is observed that the admissible region shrinks and it totally disappears as soon as the capacitance decreases below 200 μF. Notice that an admissible region that corresponds to a very small ζ and/or small ω_n is not desirable

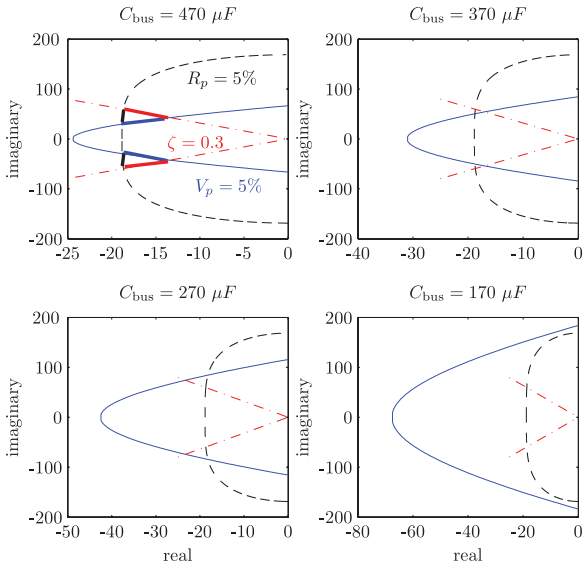

Fig. 6. Admissible regions (below 5% overshoot and below 5% ripple) for the location of poles of the bus-voltage control loop for four values of capacitances equal to 470, 370, 270, and 170 μF. Admissible region is the triangular-shape region marked by highlighted lines and keeps shrinking when the bus capacitor decreases.

because it causes sluggish responses with long oscillations, even though the peak of those oscillations is small and the 2-f ripple is low. It is observed from Fig. 6 that, for $C_{\rm bus} = 270\ \mu$F, the maximum damping ratio in the admissible region is about 0.2. This is already too small and can cause undesirable oscillations. If the condition of $\zeta > 0.3$ is also applied, the capacitor cannot really be chosen below 350 μF.

Based on the aforementioned analysis, the following design algorithm can be proposed.

E. Design Algorithm I

Given: power rating P, reference value for bus voltage $V_{\rm bus}^{\rm ref}$, CC loop is designed and given.

Objective: design the PI controller gains k and τ as well as the bus capacitor $C_{\rm bus}$ to achieve a desired transient response, the bus-voltage fluctuations not exceeding $V_p^{\max}$, and the output current THD not exceeding $\text{THD}_{\max}$.[3]

Pick an initial value for $C_{\rm bus}$ and follow the steps listed below.

Step 1: Grid the complex plane using the curves of $V_p = K$ and $R_p = K$ given by (8) and (11). Also draw the line $\zeta = \zeta_{\min}$. A value of $\zeta_{\min} = 0.3$ is recommended but it may slightly be decreased or increased based on the minimum tolerable damping in the system.

Step 2: Locate the admissible region that satisfy $V_p < V_p^{\max}$, $R_p < R_p^{\max}$, and $\zeta > \zeta_{\min}$:

1) if the admissible region does not exist, it means that $C_{\rm bus}$ is too small, increase $C_{\rm bus}$ and go to Step 1;
2) if the admissible region is large, it means that $C_{\rm bus}$ can be decreased. Reduce $C_{\rm bus}$ and go to Step 1;
3) if the admissible region exists and is not large, choose the location of poles in the admissible region, obtain ζ and ω_n, and go to Step 3.

Step 3: Calculate the controller gains from (6).

The algorithm may complete either at Step 2-2 by selecting the location of poles or at Step 2-3 where the minimum value of capacitance that satisfies the requirements is obtained.

V. Complete Modeling, Analysis, and Design of the Bus-Voltage Control Loop

The analysis method in Section IV is based on the assumption that the CC loop is fast. The interactions between the CC loop and the bus control loop are thus ignored. This assumption may not be valid when attempts are made to increase the speed of the bus control loop (in order to decrease the bus-voltage fluctuations) or equivalently, when the size of bus component is reduced. In such cases, the interactions between the bus control and the CC loops may not be negligible. Therefore, a more accurate analysis can be performed by including the dynamics of the CC loop. This is, however, not a straightforward task because the two multiplications before and after the CC loop make the system equations time varying.

A. LTI Modeling of the CC and Multiplications

Assume that the output filter is an *LCL* filter with components L_1, C_1, and L_2. Define the state variables of this filter x_3, x_4, x_5 as the inverter current, the capacitor voltage, and the grid current, respectively. A full-state feedback plus an output resonant control is used as the current control loop. Therefore, the equations of the CC loop including the multiplications can be expressed in the state-space format

$$\begin{aligned}
\dot{x}_1 &= -\omega x_2 + k_r(u\sin\omega t - x_3)\\
\dot{x}_2 &= \omega x_1\\
L_1\dot{x}_3 &= x_1 - k_p x_5 - k_3 x_3 - k_4 x_4\\
C_1\dot{x}_4 &= x_3 - x_5\\
L_2\dot{x}_5 &= x_4 - V_g\sin\omega t\\
y &= x_5 V_g\sin\omega t
\end{aligned} \tag{13}$$

where $u = I_g^{\rm ref}$ is the input signal, y (the output power) is the output signal, x_1, x_2 are the state variables of the resonant controller, k_r is the gain of a resonant controller, and (k_p, k_3, k_4) are the state feedback gains. Define three new fictitious state variables $x_{3f} = \omega x_3$, $x_{4f} = \omega x_4$, and $x_{5f} = \omega x_5$. Then, with respect to the state vector of $x^T = (x_1, x_2, x_3, x_{3f}, x_4, x_{4f}, x_5, x_{5f})$, (13) can be written as

$$\dot{x} = Ax + Bu - C^T, \quad y = Cx \tag{14}$$

[3] $R_p^{\max}$ is directly related to the $\text{THD}_{\max}$ through (12).

where A and B are, respectively, equal to

$$\begin{pmatrix} 0 & -\omega & -k_r & 0 & 0 & 0 & 0 & 0 \\ \omega & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{L_1} & 0 & -\frac{k_3}{L_1} & 0 & -\frac{k_4}{L_1} & 0 & -\frac{k_p}{L_1} & 0 \\ 0 & 0 & \omega & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_1} & 0 & 0 & 0 & -\frac{1}{C_1} & 0 \\ 0 & 0 & 0 & 0 & \omega & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \omega & 0 \end{pmatrix} \begin{pmatrix} k_r \sin\omega t \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \tag{15}$$

and $C = (0, 0, 0, 0, 0, 0, V_g \sin\omega t, 0)$. Now, consider

$$P_1 = \begin{pmatrix} \sin\omega t & -\cos\omega t \\ \cos\omega t & \sin\omega t \end{pmatrix} P = \begin{pmatrix} P_1 & 0 & 0 & 0 \\ 0 & P_1 & 0 & 0 \\ 0 & 0 & P_1 & 0 \\ 0 & 0 & 0 & P_1 \end{pmatrix}$$

and define the transformation $z = Px$. Applying this transformation to (14) results in

$$\dot{z} = \bar{A}z + \bar{B}u, y = \bar{C}z \tag{16}$$

where

$$\bar{A} = (\dot{P} + PA)P^{-1}, \bar{B} = PB, \bar{C} = CP^{-1}. \tag{17}$$

The matrices $\bar{A}$, $\bar{B}$, and $\bar{C}$ are all time varying. However, they can be represented as a summation of a constant matrix plus a matrix at 2-f. In other words, $\bar{A} = \bar{A}_0 + \bar{A}_2, \bar{B} = \bar{B}_0 + \bar{B}_2, \bar{C} = \bar{C}_0 + \bar{C}_2$. The matrix $\bar{A}_0$ is equal to (18) as shown at the bottom of the next page, and

$$\bar{B}_0^T = \left(\frac{k_r}{2}, 0, 0, 0, 0, 0, 0, 0\right)$$
$$\bar{C}_0 = \left(0, 0, 0, 0, 0, 0, \frac{V_g}{2}, 0\right).$$

The matrices $\bar{A}_2$, $\bar{B}_2$, and $\bar{C}_2$ are 2-f matrices and are not calculate here because we are not using them in this analysis. The LTI eighth-order state-space representation given by $\dot{z}_0 = \bar{A}_0 z_0 + \bar{B}_0 u,\ y = \bar{C}_0 z_0$ models the fifth-order linear time-varying system. This LTI model can be used for the bus control design.

The previous analysis may be performed for the case where the output filter is an L filter. Consider the CC loop comprising a resonant controller $\frac{k_r s}{s^2+\omega^2}$ and a state-feedback gain k_p, that is, equivalent to a PR controller [18] for the L filter. Following the same sequence of derivations performed previously for *LCL*, the following matrices are obtained for $\bar{A}_0$, $\bar{B}_0$, and $\bar{C}_0^T$,

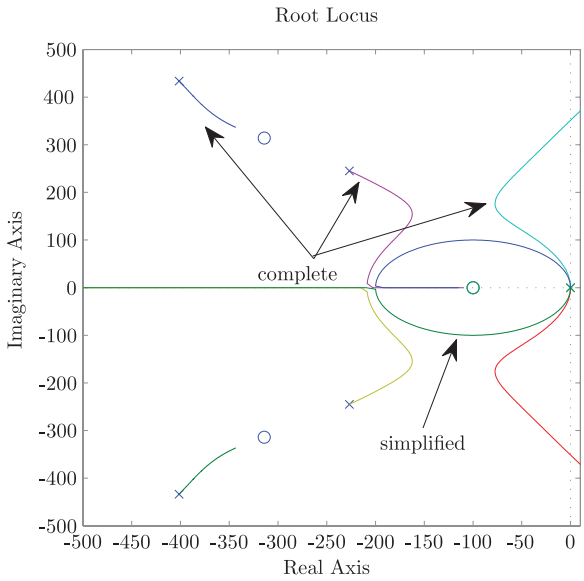

Fig. 7. Accurate loci [the roots of (22)] and simplified loci [the roots of (5)] versus k for $\tau = 10$ ms and $C_{\text{bus}} = 470\ \mu$F.

respectively:

$$\begin{pmatrix} 0 & 0 & -\frac{k_r}{2} & 0 \\ 0 & 0 & 0 & -\frac{k_r}{2} \\ \frac{1}{2L} & 0 & -\frac{k_p}{2L} & \frac{\omega}{2} \\ 0 & \frac{1}{2L} & -\frac{\omega}{2} & -\frac{k_p}{2L} \end{pmatrix} \begin{pmatrix} \frac{k_r}{2} \\ 0 \\ 0 \\ 0 \end{pmatrix} \begin{pmatrix} 0 \\ 0 \\ \frac{V_g}{2} \\ 0 \end{pmatrix}. \tag{19}$$

The aforementioned analysis shows that the system described by dynamics $\dot{x} = Ax + B(t)u, y = C(t)x$ shown in (14) is mathematically equivalent to $\dot{z} = (\bar{A}_0 + \bar{A}_2)z + (\bar{B}_0 + \bar{B}_2)u, y = (\bar{C}_0 + \bar{C}_2)z$. Therefore, thanks to the linearity of equations, it is possible to approximately decompose the system into two subsystems: one representing the dc variations and the other 2-f dynamics.

B. Design of a Bus Controller

The previous linear transformation decomposes the system dynamics into the dc dynamics and the 2-f dynamics. For the design purposes, the system can be substituted by its dc equivalence, that is

$$\dot{z}_0 = \bar{A}_0 z_0 + \bar{B}_0 u, y = \bar{C}_0 z_0 \tag{20}$$

and its transfer function is given by

$$G_0(s) = \bar{C}_o(sI - \bar{A}_0)^{-1}\bar{B}_0. \tag{21}$$

In other words, the (5) is modified to

$$1 - k\frac{1}{C_{\text{bus}}V_{\text{bus}}^{\text{ref}}}\left(1 + \frac{1}{\tau s}\right)\frac{1}{s}G_0(s) = 0. \tag{22}$$

The loci of the roots of (22) versus k is shown in Fig. 7. This is for a selection of $\tau = 10$ ms (and $C_{\text{bus}} = 470\ \mu$F and $V_{\text{bus}}^{\text{ref}} =$

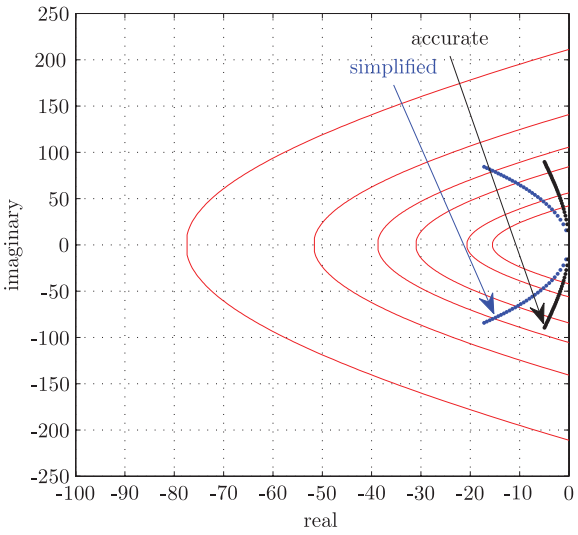

Fig. 8. Accurate loci [the roots of (22)] and simplified loci [the roots of (5)] versus k for $\tau = 10$ ms and $C_{\rm bus} = 370$ μF. (k varies from 0 to -0.03.)

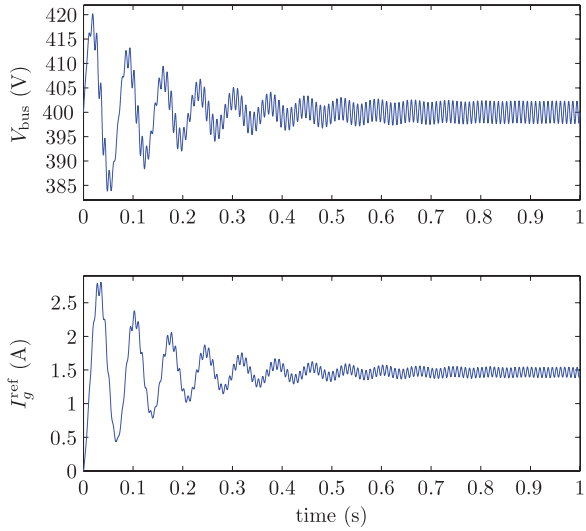

Fig. 9. Bus voltage (on top) and the PI controller's output (at bottom) responses to a 250-W step jump at the input power. Bus capacitance is 370 μF and the controller gains are $k = -0.03, \tau = 0.01$ (that corresponds to the terminal point of root locus of Fig. 8).

400 V). Clearly, the loci shown in Fig. 7 is the most accurate and complete picture of the system poles. It shows that, as compared to the simplified model (also shown in the figure), the dominant poles change direction at some point and start approaching the unstable region. Moreover, a pair of poles of the CC approaches the dominant region.

The deviations between the complete (or accurate) model of this section and the simplified model of Section IV become larger when the bus capacitor becomes smaller. Assume, for example, that a bus capacitor of 370 μF is used. The root-loci of both simplified model and the accurate model for $\tau = 10$ ms and for k varying from 0 to -0.03 are drawn in Fig. 8. The simplified model predicts that the overshoot is just below 4% and the damping of dominant poles is about 0.2. The accurate model indicates that the overshoot is above 4% and the damping is as low as about 0.06. The simulation results showing the response of the real model are shown in Fig. 9. The oscillations of the responses are due to the low damping ratio of the dominant poles. The predictions made by an accurate model of this section are much closer to the real responses than those predictions made by the simplified model.

C. Design Algorithm II

Given: power rating P, reference value for bus voltage $V_{\rm bus}^{\rm ref}$, CC loop is designed and given.

Objective: design the PI controller gains k and τ as well as the bus capacitor $C_{\rm bus}$ to achieve a desired transient response, bus-voltage fluctuations not exceeding $V_p^{\max}$, and the output current THD below a given limit $\text{THD}_{\max}$.

Obtain $R_{p,\max}$ from (12). Pick an initial value for $C_{\rm bus}$ and follow the steps listed below.

$$\begin{pmatrix} 0 & 0 & -\frac{k_r}{2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{k_r}{2} & 0 & 0 & 0 & 0 \\ \frac{1}{2L_1} & 0 & -\frac{k_3}{2L_1} & \frac{\omega}{2} & -\frac{k_4}{2L_1} & 0 & -\frac{k_p}{2L_1} & 0 \\ 0 & \frac{1}{2L_1} & -\frac{\omega}{2} & -\frac{k_3}{2L_1} & 0 & -\frac{k_4}{2L_1} & 0 & -\frac{k_p}{2L_1} \\ 0 & 0 & \frac{1}{2C_1} & 0 & 0 & \frac{\omega}{2} & -\frac{1}{2C_1} & 0 \\ 0 & 0 & 0 & \frac{1}{2C_1} & -\frac{\omega}{2} & 0 & 0 & -\frac{1}{2C_1} \\ 0 & 0 & 0 & \frac{1}{2L_2} & 0 & 0 & \frac{\omega}{2} & \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2L_2} & -\frac{\omega}{2} & 0 \end{pmatrix} \tag{18}$$

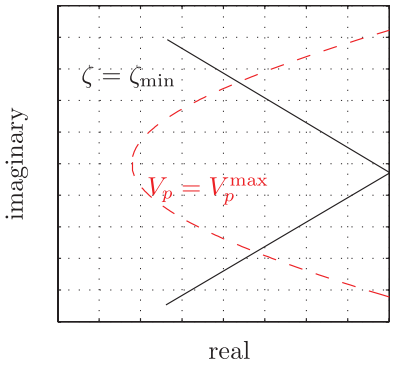

Fig. 10. Curves of $V_p = V_p^{\max}$ given by (8) and $\zeta = \zeta_{\min}$.

Step 1: Select a small positive value for τ.

Step 2: Calculate the maximum value of $-k_{\max}$ from (10).

Step 3: Draw on the complex plane the curves of $V_p = V_p^{\max}$ given by (8) and $\zeta = \zeta_{\min}$. A sketch of such graph is shown in Fig. 10.

Step 4: Draw the root locus of (22) for k varying from 0 to $k_{\max}$.

1) If the terminal point of the locus does not reach the V_p curve, increase τ and go to Step 1. If increasing τ does not help, increase $C_{\rm bus}$ and go to Step 1.
2) If the terminal point of the locus crosses the V_p curve, it means that $C_{\rm bus}$ can be made smaller (if desired). Decrease $C_{\rm bus}$ and go to Step 1.
3) If the terminal point of the locus is close to V_p curve and satisfies the damping condition, algorithm is over. Otherwise, increase $C_{\rm bus}$ and go to Step 1.

The algorithm may complete either at Step 4-2 or at Step 4-3, where the minimum value of capacitance that satisfies the requirements is obtained.

Although the previous design algorithm assumes that the CC is designed and available, it offers the possibility of an interactive design of CC and the bus control thanks to the complete modeling of the whole system. This topic is not studied in this paper.

VI. Experimental Results

The analytical results of this paper are verified using a two-stage 250-W power-electronic conversion system. The renewable source is modeled by a photovoltaic simulator of model Agilent E4360A. The grid voltage magnitude is $240\sqrt{2}$ V and the bus-voltage reference is 400 V. The output filter is an inductance of 10 mH and the current control is a PR controller. The whole control algorithms are implemented in an FPGA series Stratix II and the sampling frequency is 20 kHz. The output current, grid voltage, and bus voltage are sampled using A/D with 12 bits.

The PI controller's gains are set at $k = -0.04$ and $\tau = 0.03$. The following scenarios are implemented and tested.

Scenario I ($C_{\rm bus} = 562\,\mu$F): Consider an input power jump of $P = 200$ W. The theoretical values for the bus-voltage overshoot and the current ripples are $V_p = 4\%$ and $R_p = 4\%$. These correspond to 16-V overshoot in the bus voltage and a THD of $2|G_{\rm cc}(j3\omega)|$ at the output current. The measured bus voltage and the output current are shown in Fig. 11. The bus-voltage fluctuation is just about 16 V and this complies with the analytical results.

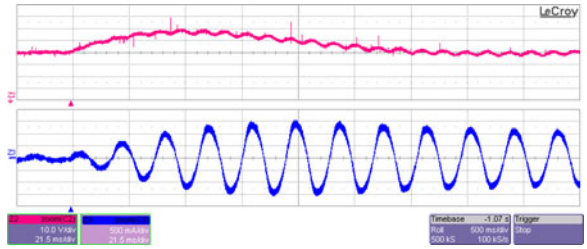

Fig. 11. Bus voltage and the output current responses to an input power jump of 200 W when $C_{\rm bus} = 562\,\mu$F.

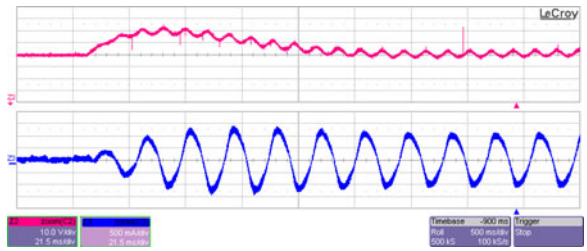

Fig. 12. Bus voltage and the output current responses to an input power jump of 200 W when $C_{\rm bus} = 292\,\mu$F.

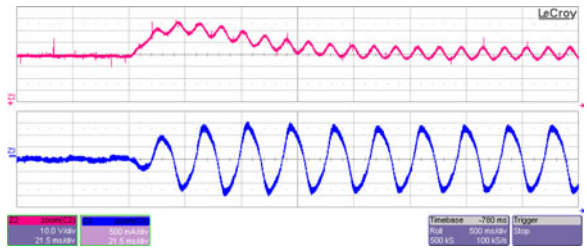

Fig. 13. Bus voltage and the output current responses to an input power jump of 200 W when $C_{\rm bus} = 157\,\mu$F.

Scenario II ($C_{\rm bus} = 292\,\mu$F): The theoretical values for the bus-voltage overshoot and the current ripples are $V_p = 4.6\%$ and $R_p = 7.6\%$. These correspond to 18.5-V overshoot in the bus voltage and a THD of $3.8|G_{\rm cc}(j3\omega)|$ at the output current. The measured bus voltage and the output current are shown in Fig. 12. The bus-voltage fluctuation is slightly above 18 V and this complies with the analytical results.

Scenario III ($C_{\rm bus} = 157\mu$F): The theoretical values for the bus-voltage overshoot and the current ripples are $V_p = 5.3\%$ and $R_p = 14\%$. These correspond to 21-V overshoot in the bus voltage and a THD of $7|G_{\rm cc}(j3\omega)|$ at the output current. The measured bus voltage and the output current are shown in Fig. 13. The bus-voltage fluctuation is slightly above 21 V and this complies with the analytical results.

Scenario IV ($C_{\rm bus} = 112\,\mu$F): The theoretical values for the bus-voltage overshoot and the current ripples are $V_p = 5.6\%$ and $R_p = 20\%$. These correspond to 22-V overshoot in the bus voltage and a THD of $10|G_{\rm cc}(j3\omega)|$ at the output current. The measured bus voltage and the output current are shown in

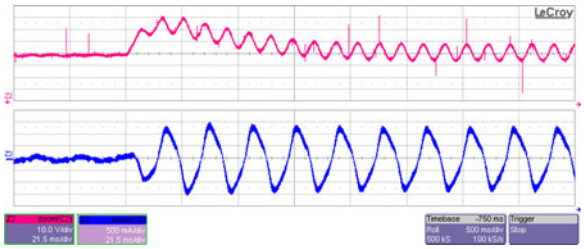

Fig. 14. Bus voltage and the output current responses to an input power jump of 200 W when $C_{\rm bus} = 112\ \mu$F.

TABLE I
HARMONIC CONTENT OF OUTPUT CURRENT FOR DIFFERENT BUS CAPACITORS

$C_{\rm bus}$	h_2	h_3	h_5	h_7	THD %	h_3 (adjusted)
562 μF	0.5	4.5	0.75	0.5	5	2
292 μF	0.4	6.3	1	0.4	6.6	3.8
157 μF	0.5	9.7	1.3	0.7	10	7.2
112 μF	0.8	12.7	1.5	0.6	13	10.2

Fig. 14. The bus-voltage fluctuation is just above 22 V and this complies with the analytical results.

The major harmonic components of the output current (second, third, fifth, and seventh) as well as the THD are shown in Table I for the previous four cases. The harmonics keep increasing as the bus capacitor is decreased. The experimental setup has a background THD of about 2.5% caused by other nonlinearities in the system. Therefore, if the values shown in Table I are accordingly adjusted by subtracting the background harmonic, then the values shown in the last column in Table I will be obtained. This is the contribution to the third harmonic caused by the bus control loop and due to the loop ripples. The last column in Table I closely conforms with the (12) given the fact that for our current control, $|G_{\rm cc}(j3\omega)|$ was about unity.

VII. CONCLUSION

Design of the dc-bus control loop for single-phase grid-connected renewable applications is addressed in this paper. The control objectives of minimizing the bus-voltage fluctuations and minimizing the output harmonics are formulated and quantified using simple-to-use grids on the complex plane. The systematic developments presented in the paper facilitate an efficient design of the bus component size as well as the controller's gains. In order to increase the speed of bus control and reduce the voltage fluctuations without excessively increasing the size of bus component, a complete model is derived that considers the interactions between the bus control loop and the current control loop. Those interactions are neglected in the existing literature and are important for an interactive design of the current control system and the bus control system. Simulation and experimental results confirm effectiveness of the algorithms presented in the paper.

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