A Unifying Approach to Single-phase Synchronous Reference Frame PLLs

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***Abstract*—The three-phase synchronous reference frame phase-locked loop (3ϕ-SRF-PLL) is widely used in three-phase power electronics and power system applications thanks to its desirable performance and its simple yet robust structure. Inspired from the 3ϕ-SRF-PLL and due to the increasing interest in single-phase applications, multiple single-phase SRF-PLL (1ϕ-SRF-PLL) versions have also been proposed in the recent years. This paper presents a unifying approach to the understanding and analysis of the 1ϕ-SRF-PLLs. The paper integrates several 1ϕ-SRF-PLLs having apparently different structures into a single structure. The approach is much useful in understanding various PLLs and also in facilitating further developments in this field.**

***Index Terms*—Phase-locked loop, PLL, EPLL, SRF-PLL, dq PLL, inverse Park PLL.**

I. Introduction

The three-phase synchronous reference frame phase-locked loop (3ϕ-SRF-PLL) is arguably the most commonly-used PLL structure for three-phase applications. It has a simple and robust structure and can estimate the phase angle and frequency of a three-phase balanced, and sinusoidal set of signals with no steady state error, and it is reasonably robust in the presence of signal distortions [1], [2]. Structures which are essentially modified versions of the 3ϕ-SRF-PLL have been reported in order to further improve its performance against unbalance, signal distortions and dc component [3]–[8].

The 3ϕ-SRF-PLL takes advantage of the symmetry that exists in a balanced three-phase system. This is used to transform the sinusoidal signals into dc signals using the abc/dqo (or the Park's) transformation. The 3ϕ-SRF-PLL then regulates the q-component of the transformed signals to zero within a simple PI loop to attain the phase angle and frequency. The phase angle provided by this PLL estimates the phase angle of the positive-sequence component of the input signal that coincides with the phase angle of the phase-a signal for a balanced set of input signals.

The dq signals can also be generated from the $\alpha\beta$ signals rather than the original abc signals. The $\alpha\beta$ signals are two orthogonal sinusoidal signals generated from the abc signals using a constant linear transformation (called the abc/$\alpha\beta\gamma$ or the Clarke's transformation). The α signal is equal to the phase-a signal in balanced situations and the 3ϕ-SRF-PLL estimates the phase angle of this signal. The β signal is 90-degree phase-shifted (or orthogonal or delayed or quadrature) version of the α signal. This fact means that the 3ϕ-SRF-PLL can be used in a single phase application provided that the orthogonal version of the single phase signal, that is the β signal, is also available. This has been the idea behind multiple single-phase PLL structures that have been derived from the 3ϕ-SRF-PLL. We shall call those structures the 1ϕ-SRF-PLLs.

The 1ϕ-SRF-PLLs can be divided into two categories. The first category of 1ϕ-SRF-PLLs generates the orthogonal signal directly from the input signal. The idea is to introduce 90 degrees phase-shift (or one quarter of a cycle time delay) into the input signal. This has been realized using direct time delay, Hilbert transform, Kalman filtering, all-pass filtering, and FIR (finite impulse response) filtering among the others [9]–[12]. These methods usually do not take into account the frequency variations. The concept of using a second-order low-pass filter (LPF) to generate the orthogonal signal is also used in the literature. This method can incorporate frequency variations that are fed back to the orthogonal generator from the main PLL loop [13]. Another method is presented in [14] based on analog calculation of derivative and integral of the input signal and multiplying them together and then taking square root of the result while preserving the sign.

The members in the second category of 1ϕ-SRF-PLLs generate the orthogonal signal using the phase angle information and by applying an inverse transform to the dq signals. Obviously, they require some method to prevent creation of algebraic loops. The well-known representative of this class of 1ϕ-SRF-PLLs is the one called the inverse Park transform PLL (IP-PLL). The IP-PLL uses two LPFs to filter the dq signals and these two filtered signals are used in an inverse transform to generate the orthogonal signal [10], [15], [16]. Another idea is to use a filtered version of u_d as the estimate for the amplitude of the orthogonal signal. Its phase angle can also be synthesized from the PLL angle. This idea has been conceived by different researchers in the filed with very minor differences of presentation [17]–[19]. Several other newly developed single phase PLL structures are also reported in the literature such as [20]–[23] that can be placed within this class of 1ϕ-SRF-PLLs.

Totally independent from the 1ϕ-SRF-PLLs approach, the single phase enhanced PLL (EPLL) was derived from an optimization perspective [24], [25]. Its desirable features and performances are reported in several publications. However, its connection to the 1ϕ-SRF-PLLs has not been studied so far; neither the connections among different members of 1ϕ-SRF-PLLs. Such connections may not always be easy to establish due to the apparently very different presentations.

The objectives of this paper are as follows. 1) To establish the connections among several different 1ϕ-SRF-PLLs. 2) To show that the EPLL is also a member of 1ϕ-SRF-PLLs despite the fact that it is derived differently. 3) To show that multiple newly developed 1ϕ-SRF-PLLs are converging (or have already converged) to the EPLL despite differences of

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presentations. For examples, the methods of [17], [20], [21] are completely equivalent to the EPLL while those of [22], [23] are simplified and incomplete versions of the EPLL.

The results of this paper show the convergence of different approaches adopted by independent researchers (some starting from 3ϕ-SRF-PLL and some adopting an optimization approach) and will thus serve as a confirmation to such approaches. Moreover, the results of this study integrate multiple structures into a simple yet effective representation that offers a great help to understand them and to facilitate further developments in the field.

II. Overview of PLL, EPLL, 3ϕ-SRF-PLL, 1ϕ-SRF-PLLs

A. PLL

Structure of the standard single phase PLL is shown in Fig. 1. The input signal is denoted by $u(t)$. The LF stands for loop filter and VCO stands for voltage-controlled oscillator. The input signal is multiplied by the VCO's output signal $y(t)$, is passed through the LF and the outcome is applied to the VCO. The VCO generates a sinusoidal signal whose phase angle is proportional to the integral of the VCO's input. In other words, $\phi = \int^t \omega(\tau)d\tau$, where ω is the VCO's input and $y(t) = \cos\phi$ is the VCO's output. The main drawback of this structure, as far as many power systems and power electronics applications are concerned, is the presence of double-frequency oscillations in the loop even for a purely sinusoidal input signal.

B. EPLL

The enhanced phase-locked loop (EPLL) enhances the standard PLL by removing its main drawback that is the presence of double-frequency errors. The EPLL achieves this task by means of estimating the amplitude of the input signal. Thus, in addition to removing the ripples, the EPLL also provides an estimate of the input signal magnitude and also provides a filtered version of the input signal. In other words, the EPLL not only operates as a PLL, it functions as a filter and can also operate as a controller [26].

Block diagram of the EPLL is shown in Fig. 2. The EPLL comprises a PLL (the portion in the dashed box in Fig. 2) and also a branch that generates a signal y that is the filtered version of the input signal u. Thus, A estimates the peak value of input signal and ϕ estimates its phase angle. The frequency is estimated at ω; and ω_o is the nominal value of the input frequency. The signals S_1 and S_2 are generated by the VCO (or the trigonometric function shown by "Trig" in Fig. 2) and S_2 is 90 degrees delayed version of S_1. They are

$$(S_1, S_2) = (\cos\phi, \sin\phi) \quad \text{or} \quad (\sin\phi, -\cos\phi). \tag{1}$$

Theses two representations are equivalent due to the fact that any sinusoidal signal, e.g. the input signal u, can be expressed as sine and cosine functions equally. Thus, the signal S_1 is a unity sinusoidal signal that is in-phase with the input signal and this represents a stable reference for synchronization

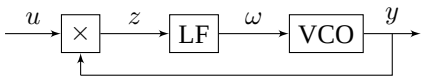

Fig. 1. Structure of the standard PLL

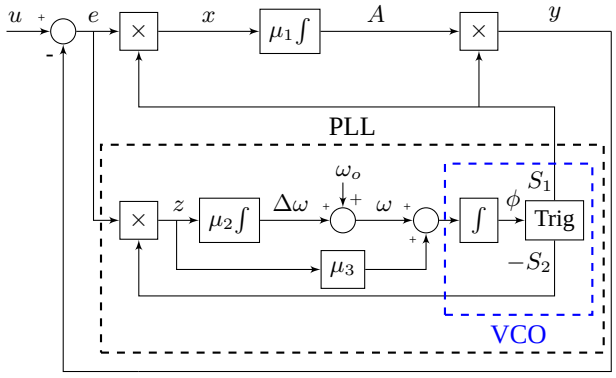

Fig. 2. The EPLL structure

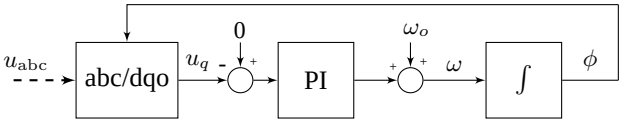

Fig. 3. 3ϕ-SRF-PLL

purposes. The EPLL differential equations can therefore be written by inspecting the block diagram of Fig. 2 as

$$\begin{cases} \dot{A} = \mu_1 e S_1 \\ \dot{\Delta\omega} = -\mu_2 e S_2 \\ \dot{\phi} = \omega_o + \Delta\omega - \mu_3 e S_2 \\ e = u - y = u - AS_1. \end{cases} \tag{2}$$

In the equation set (2) and also in the rest of this paper, the over dot notation is used to denote the time derivative of a function.

C. 3ϕ-SRF-PLL

The structural block diagram of the 3ϕ-SRF-PLL is shown in Fig. 3 where u_{abc} denotes the three-phase input signal and the thick-dashed line shows a three-phase connection as opposed to the thin-solid lines that show single phase connections. The abc/dqo or the Park's transformation is defined by $u_{\text{dqo}} = P u_{\text{abc}}$ where[1]

$$P = \frac{2}{3}\begin{pmatrix} \cos(\phi) & \cos(\phi - \frac{2\pi}{3}) & \cos(\phi + \frac{2\pi}{3}) \\ \sin(\phi) & \sin(\phi - \frac{2\pi}{3}) & \sin(\phi + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix}. \tag{3}$$

For a three-phase balanced set of input signals

$$u_{\text{abc}}^T = \left(U\cos(\theta), U\cos(\theta - \frac{2\pi}{3}), U\cos(\theta + \frac{2\pi}{3})\right), \tag{4}$$

[1]Strictly speaking, the abc/dqo transformation is slightly different from the Park's transformation in the sense that the former is power-invariant. Such a difference is not important in the context of PLL studies presented in this paper.

the dqo signals are

$$u_{\rm dqo}^T = (U\cos(\theta-\phi), -U\sin(\theta-\phi), 0)\,, \tag{5}$$

where T denotes matrix or vector transposition. By regulating u_q to zero, the loop regulates θ to ϕ.

The 3ϕ-SRF-PLL may also be presented in terms of the stationary frame signals $u_{\alpha\beta}$. Such signals are defined as

$$u_{\alpha\beta} = Qu_{\rm abc} = \frac{2}{3}\begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} u_{\rm abc}. \tag{6}$$

For the input signal of (4), it yields that

$$u_{\alpha\beta}^T = (U\cos\theta, U\sin\theta). \tag{7}$$

In other words, α-component signal is the same as the phase-a signal and β-component signal is the 90 degrees delayed version of the phase-a component. With the above definition for the matrices P and Q, the dq signals may be computed from $\alpha\beta$ signals using the rotation matrix as follows.[2]

$$\begin{pmatrix} u_d \\ u_q \end{pmatrix} = \begin{pmatrix} \cos\phi & \sin\phi \\ \sin\phi & -\cos\phi \end{pmatrix} u_{\alpha\beta}. \tag{8}$$

D. 1ϕ-SRF-PLLs

The $\alpha\beta$ representation shows that the 3ϕ-SRF-PLL does not really need to have three input signals to operate. It can operate if it is supplied by a single phase signal and its 90 degrees delayed version. This has been the basic idea for multiple extensions of the 3ϕ-SRF-PLL in order to make it work for single phase applications. The first and simplest approach is to ignore the β signal and set it to zero! By this, the 3ϕ-SRF-PLL reduces to the standard single phase PLL, shown in Fig. 1. This has also been called power-PLL or pPLL in some references [16] although the same term is used for other structures as well [27]. This structure has the problem of double-frequency error and is not of interest unless in very limited number of applications which do not require fast response. In such cases, a LPF with a very short bandwidth is inserted in the loop in order to significantly mitigate the ripples at the cost of very slow transient response.

The second approach is to generate an estimate of the β signal using the α signal. Two methods of time-delay and Hilbert transform have been used to generate the orthogonal signal [10]. These methods do not take into account the frequency variations. The concept of using a second-order LPF (based on the second-order generalized integrator- SOGI) to generate the orthogonal signal is also used in the literature. This method can incorporate frequency variations that are fed back to the SOGI from the SRF-PLL [13]. Another method, called inverse Park transform, uses two LPFs after u_d and u_q to generate u'_d and u'_q. These two new signals are used in an inverse transform to generate the orthogonal signal [15]. Another method is presented in [14] based on analog calculation of derivative and integral of the input signal and multiplying them together and then taking square root of the result while preserving the sign. In other words, $u_\beta = \text{sign}(\dot{u}_\alpha)\sqrt{\dot{u}_\alpha \int u_\alpha}$. There have been several other methods to achieve the task of orthogonal signal generation, such as Kalman filtering [9], all-pass filtering [28], and FIR (finite impulse response) filtering [11].

[2]Alternatively, the input signals may be represented as sine functions too but the matrix P needs to be adjusted accordingly by swapping its first two rows. In this case, the $\alpha\beta/dq$ matrix will be equal to

$$\begin{pmatrix} u_d \\ u_q \end{pmatrix} = \begin{pmatrix} \sin\phi & -\cos\phi \\ \cos\phi & \sin\phi \end{pmatrix} u_{\alpha\beta}.$$

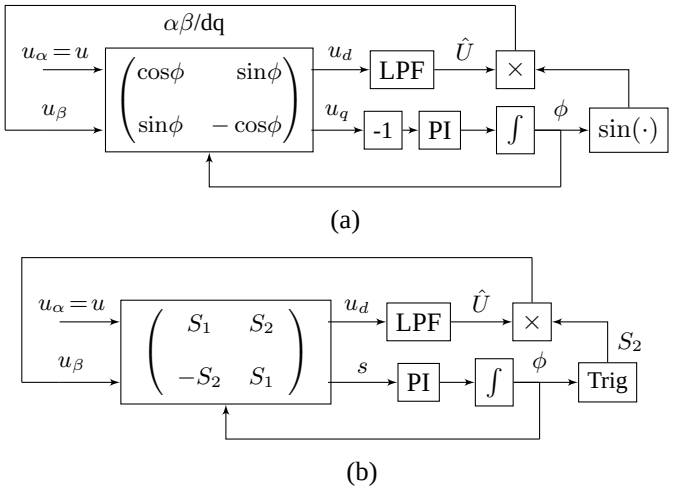

Fig. 4. Simplest 1ϕ-SRF-PLL: (a) one typical implementation (b) general form

As stated in Introduction, these methods may be classified into two groups: those that generate the orthogonal signal directly from the input signal using some sort of operations such as time-delay, Hilbert transform, filtering etc; and those that generate the orthogonal signal using the very information provided by the system such as the d component and the phase angle along with some sort of filtering. The approach adopted by the second group is generally more efficient than the one used by the first group in terms of simplicity and robustness of structure as well as maintaining the frequency-adaptivity of the whole system. Some of these approaches will be reviewed in Section V and their correspondence with the EPLL is also explained.

III. Simplest 1ϕ-SRF-PLL Structure

Based on (5), the regulation of u_q to zero results in convergence of ϕ to θ. Meanwhile, the signal u_d converges to U that is the amplitude of the input signal. Based on this fact, signal u_β can be constructed by simply multiplying u_d by $\sin\theta$. However, this generates an algebraic loop. In order to avoid the algebraic loop, and also to mitigate the high frequency noise and distortions, a simple first-order LPF with unity gain may be used. The achieved 1ϕ-SRF-PLL structure developed based on this strategy is shown in Fig. 4. This is the simplest structure possible within the second category of 1ϕ-SRF-PLL structures. Figure 4(b) shows generalization of Fig. 4(a). The functions S_1 and S_2 are defined in (1).

IV. Equivalence of Simplest 1ϕ-SRF-PLL and EPLL

Despite apparently very different structures, the simplest 1ϕ-SRF-PLL and the EPLL are completely equivalent. This

section proves this equivalence.

Consider the input signal u. Thus, $u_\alpha = u$ and $u_\beta = \hat{U}S_2$. The signal s that is the driving signal of the PI unit in the simplest 1ϕ-SRF-PLL is equal to

$$s = -S_2\ u_\alpha + S_1\ u_\beta = (u - \hat{U}S_1)(-S_2) \tag{9}$$

where $\hat{U}$ is the LPF output.

Now, consider the EPLL system that is supplied by the same input signal u. It is observed from the EPLL structure shown in Fig. 2 that the signal z is the driving signal of the PI controller and it is equal to

$$z = -eS_2 = -(u - AS_1)S_2. \tag{10}$$

Assuming that the PI coefficients for both systems are identical, the two signals, i.e. s and z, become equal if $\hat{U} = A$.

The process of amplitude estimation in the EPLL is shown in Fig. 2 and is also described by the first differential equation in (2). The EPLL estimates the amplitude through the upper branch in Fig. 2 and using

$$\dot{A} = \mu_1 eS_1 = \mu_1(u - AS_1)S_1 = \mu_1\psi(A, \phi), \tag{11}$$

where $\psi(A, \phi) = (u - AS_1)S_1$. Notice that ψ corresponds to the point x shown on Fig. 2.

In the simplest 1ϕ-SRF-PLL shown in Fig. 4, the signal u_d will be equal to

$$u_d = u_\alpha S_1 + u_\beta S_2 = (u - \hat{U}S_1)S_1 + \hat{U} = \psi(\hat{U}, \phi) + \hat{U} \tag{12}$$

where the relationship between $\hat{U}$ and u_d is given by the LPF dynamics. Assume that the LPF has a transfer function $\mathrm{LPF}(s) = \frac{\omega_c}{s+\omega_c}$, then

$$\dot{\hat{U}} + \omega_c\hat{U} = \omega_c u_d \tag{13}$$

where ω_c is the bandwidth of the LPF. Now, substituting u_d from (12) into (13) yields

$$\dot{\hat{U}} = \omega_c\psi(\hat{U}, \phi). \tag{14}$$

Comparison of (14) and (11) shows that the amplitude estimation laws of the EPLL and the simplest 1ϕ-SRF-PLL are equivalent if and only if $\omega_c = \mu_1$. The following theorem summarizes the equivalence study presented above.

Theorem 1. Provided that both systems have identical PI coefficients, the simplest 1ϕ-SRF-PLL of Fig. 4 with the LPF of $\frac{\omega_c}{s+\omega_c}$ is equivalent to the EPLL of Fig. 2 if $\omega_c = \mu_1$.

The proof is already provided in the discussion preceding the theorem. However, a block diagram approach on the amplitude estimation laws may also be given as follows. The two block diagrams shown in Fig. 5 are equivalent if $\tau = \frac{1}{\mu_1}$. The diagram on the left corresponds to the amplitude estimation of the simplest 1ϕ-SRF-PLL of Fig. 4. The diagram on the right shows the amplitude estimation in the EPLL of Fig. 2. The definition for the function ψ is given in (11). Thus, in order for the two systems to be perfectly equivalent, the relationship between the LPF time-constant (or cut-off frequency) and the EPLL parameter is given by $\frac{1}{\tau} = \omega_c = \mu_1$.

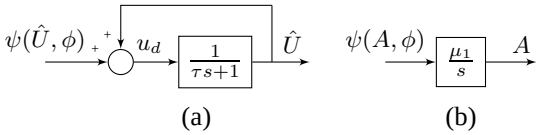

Fig. 5. (a) Amplitude estimation in the simplest 1ϕ-SRF-PLL, (b) Amplitude estimation in EPLL

The synthesis circuit PLL of [17] clearly coincides with the simplest 1ϕ-SRF-PLL of Fig. 4. The improved synthesis circuit PLL of [17] which addresses the harmonics as well, is equivalent to the EPLL extension introduced in [29].

V. Correspondence between EPLL and Several Other 1ϕ-SRF-PLLs

The structure of Fig. 4 is not the only structure that is equivalent to the EPLL but it is the most direct form. Multiple other structures that are derived from the 3ϕ-SRF-PLL have been developed and reported in the recent literature that are also equivalent to the EPLL. Some of such structures are explained and their equivalence to the EPLL is shown in this section.

A. PLL of [21]

The structure presented in [21] defines $u_\alpha = u - \hat{U}\sin\phi$ and sets $u_\beta = 0$ and applies these two signals to the SRF-PLL. Notice that this is not in line with other similar methods where u_β is orthogonal to u_α. Then, the driving signal of the PI controller will be equal to

$$s = (u - \hat{U}\sin\phi)\cos\phi$$

that is identical with (9) and (10) for $(S_1, S_2) = (\sin\phi, -\cos\phi)$. This means that the phase/frequency loop (or the basic SRF-PLL operation) remains unchanged. The amplitude estimation of [21] is done through

$$\dot{\hat{U}} = -K_i(u - \hat{U}\sin\phi)(-\sin\phi)$$

that is identical with the amplitude estimation loop in the EPLL, i.e. the equation (11), for $(S_1, S_2) = (\sin\phi, -\cos\phi)$ and $K_i = \mu_1$. This concludes that the two PLLs are completely equivalent.

B. PLL of [20]

The method of [20] clearly coincides with the EPLL as far as the phase/ frequency loop is concerned. That is because in the method of [20], the driving signal to the PI is selected as

$$-u\sin\phi + \frac{\hat{U}}{2}\sin 2\phi = (u - \hat{U}\cos\phi)(-\sin\phi)$$

that is identical with (9) and (10) for $(S_1, S_2) = (\cos\phi, \sin\phi)$.

The amplitude estimation method adopted in [20] is shown in Fig. 6, left portion. The input signal to the LPF is equal to

$$u\cos\phi - \frac{\hat{U}}{2}\cos(2\phi) = (u - \hat{U}\cos\phi)\cos\phi + \frac{\hat{U}}{2} = \psi(\hat{U}, \phi) + \frac{\hat{U}}{2}.$$

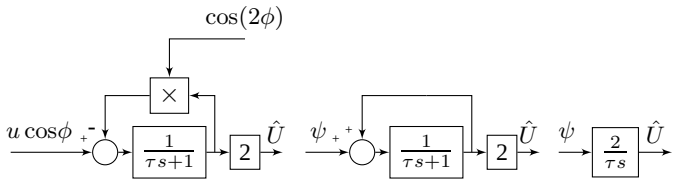

Fig. 6. Three equivalent systems; $\psi = \psi(\hat{U}, \phi) = (u - \hat{U}\cos\phi)\cos\phi$

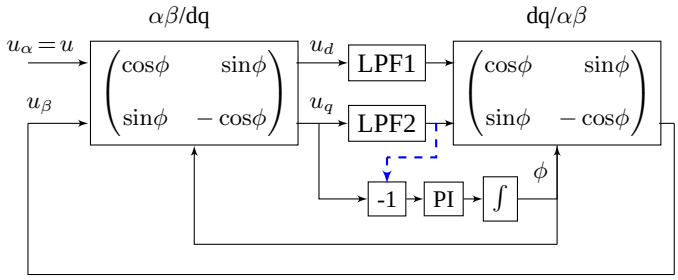

Fig. 7. Inverse Park transform PLL

Therefore, the diagram can be simplified as the one in the middle of Fig. 6. It can further be simplified as the one in the right side of Fig. 6 based on the equivalence previously shown in Fig. 5. Therefore, this PLL will be equivalent to the EPLL for a selection of $\tau = \frac{2}{\mu_1}$ and equal PI coefficients.

The decoupling network in [19] is the same as the method employed in [20].

C. PLL of [22], [23], [30]

The method described in [22], [23] is basically a simplified and incomplete version of EPLL that assumes a fixed/known value for the amplitude (and thus does not employ any amplitude estimation). The method will be applicable to cases that the input signal magnitude is nearly constant and known. It is shown in [22] that the double-frequency ripple can be attenuated at least about 87% for a range of input signal amplitudes between 0.88 to 1.1; this PLL is intended for grid-connected applications where the amplitude is pretty much stable. The same PLL of [22], [23] is furnished with an amplitude estimation strategy based on using two LPFs and a nonlinear operation which signify a complicated structure with no added advantage.

D. Inverse Park Transform PLL

In the inverse Park transform PLL (IP-PLL), [10], [15], [16], the β component is generated using inverse of $\alpha\beta/dq$ transform. The input signals to this transform are obtained by passing the dq signals from two LPFs as shown in Fig. 7. The phase angle loop is driven either by u_q or by its filtered version (after the LPF) for better steady-state operation.

On one hand, it is obvious that the structure of Fig. 7 coincides with Fig. 4 when the second input to the dq/$\alpha\beta$ unit is zero, i.e. when LPF2 is zero. On the other hand, signal u_q converges to zero in the steady state and in the ideal case of sinusoidal input. Therefore, it can be concluded that these two structures (Fig. 7 and Fig. 4) perform very similarly. However, the structure of Fig. 7 requires more computations in order to implement the LPF2 and also to perform the dq/$\alpha\beta$. It seems that this extra branch in Fig. 7 offers no particular advantage when compared to the PLL of Fig. 4 (or the EPLL of Fig. 2).

If the second LPF is considered in the phase/frequency loop (the path shown by the thick-dashed line in Fig. 7), the PLL loop becomes of order three. Methods for design of such LPF within the loop are presented in [31], [32]. It shall be mentioned in passing that the double frequency cancelation block in [31] is also basically the same as IP-PLL. However, since u_β is set to zero in [31], further calculations are needed to cancel all double frequency ripples.

Remark. The loop gain in the SRF-PLL is proportional to the amplitude of the input signal. This means that a proper loop design should consider the tentative range of signal magnitudes. However, it is possible to make the loop adaptive such that it automatically adjusts itself to the possible variations in the amplitude. This is done by dividing the loop gain to the estimated value of the amplitude. Such mechanism is used in various publications such as [31], [32] among several others.

VI. Numerical Results

Three systems of Fig. 2 (the EPLL), Fig. 4 (the simplest 1ϕ-SRF-PLL) and Fig. 7 (the IP-PLL) are simulated for equal values of controllers' gains and the results are shown in this section. The PI controller's gains are selected at $\mu_3 = 260$ and $\mu_2 = 17000$. Moreover, the selection of $\mu_1 = \frac{1}{\tau} = \omega_c = 260$ is also made. The input signal is defined as a sinusoidal signal whose amplitude undergoes a jump of -25% at t=0.1 s, its phase angle experiences a jump of 10 deg at t=0.2 s and its frequency jumps from 60 to 59.5 Hz at t=0.3 s. The EPLL and the simplest 1ϕ-SRF-PLL showed identical results, as expected. The estimated amplitude, the phase angle error and the estimated frequency for the EPLL and the IP-PLL are shown in Fig. 8. The IP-PLL shows slightly longer transient time as compared with the other two PLLs. This is shown in the zoomed portions.

In the second simulation, some harmonic distortions and noise are added to the same input signal. A value of 5% of harmonics 3, 5, 7 and 11 as well as a white Gaussian noise with zero mean and the standard deviation of 0.01 are added to the signal. The estimated amplitude, the phase angle error and the estimated frequency for are shown in Fig. 9. The EPLL and the IP-PLL perform slightly differently at the steady state. The difference is, however, very tiny and is negligible for all practical purposes. Figure 10 shows a zoomed version of Fig. 9 in order to visualize the extents of difference in the responses by the two PLLs in the steady state.

VII. Conclusion

It is observed that several recent and independently conducted research works on the concept of single phase PLL systems have closely converged to one point despite their apparently different structures and presentations. The paper

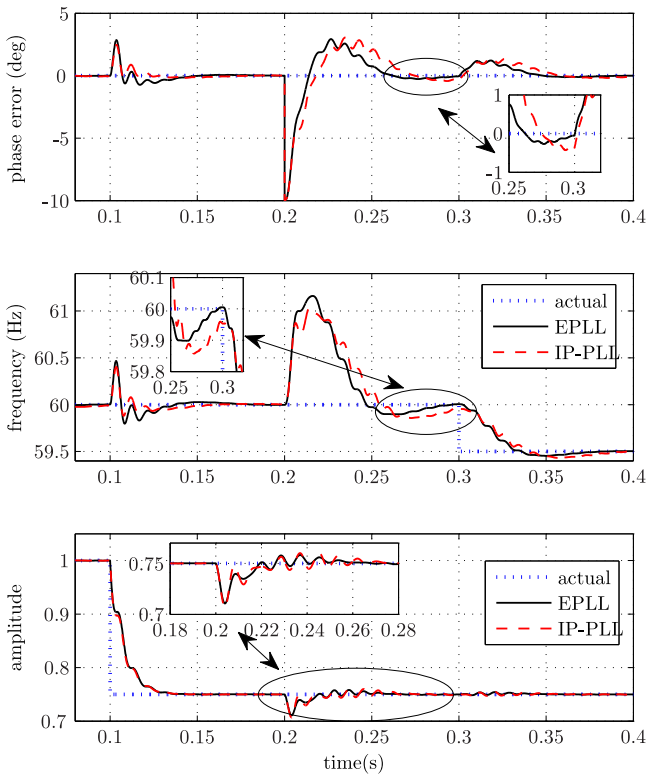

Fig. 8. Performance of the EPLL of Fig. 2 (which coincides with the simplest 1ϕ-SRF-PLL of Fig. 4) and inverse Park PLL of Fig. 7 in tracking input signal transients.

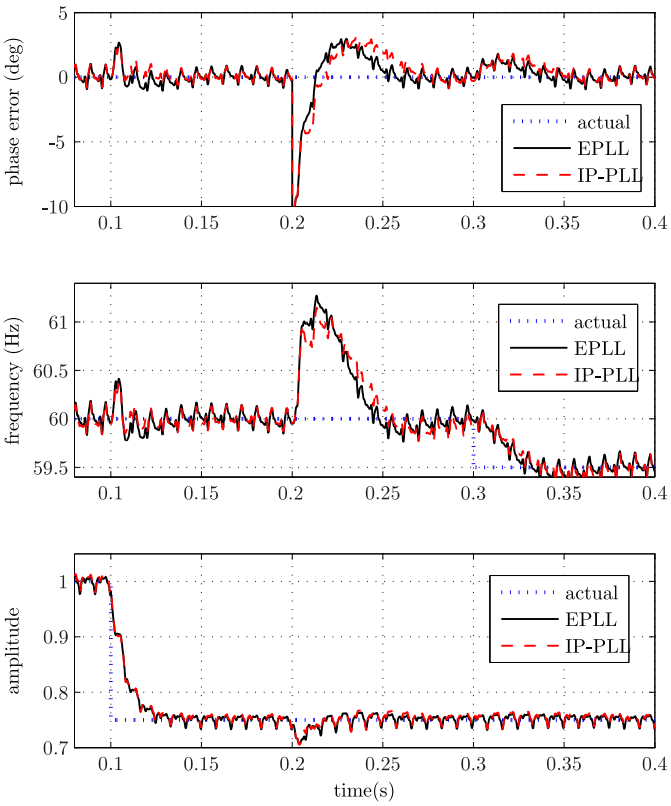

Fig. 9. Performance of the EPLL of Fig. 2 (which coincides with the simplest 1ϕ-SRF-PLL of Fig. 4) and inverse Park PLL of Fig. 7 in tracking input signal transients in noise and distortions.

establishes the analogies between several of those structures and shows that they share the same framework the simplest of which is offered by the EPLL. The convergence discussed in this paper is a confirmation of the advantageous structures that different people have developed using different perspectives. The unifying approach of this paper can be very helpful for deeper understanding of different PLLs. This gives much insight for those who need to select a PLL for their specific application or for those who are new to this area of research and plan to contribute to further developments in the field.

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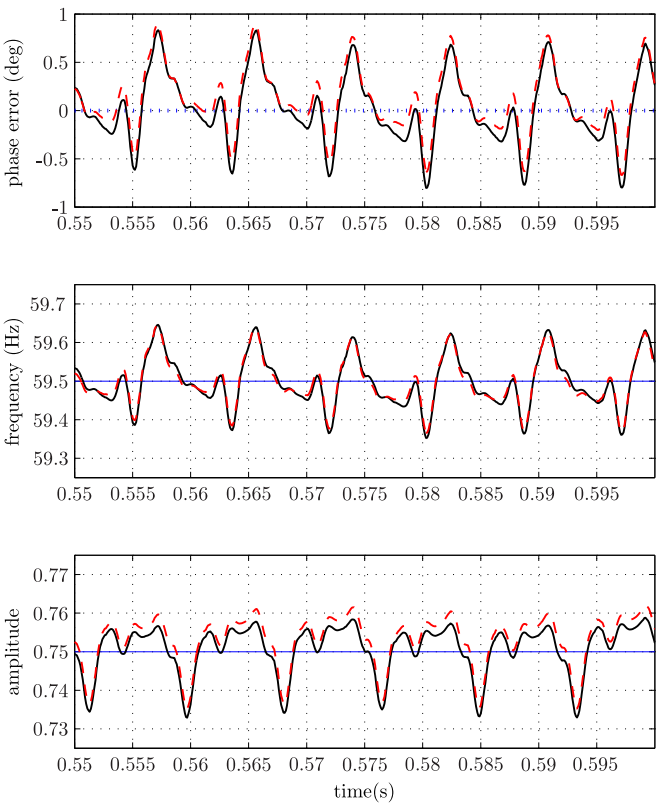

Fig. 10. Zoomed version of Fig. 9 to illustrate the steady state responses.

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