Sinusoid-Locked Loops based on the Principles of Synchronous Machines

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***Abstract*—Phase-locked loops (PLL), which are widely applied to track the phase of a periodic signal, play an important role in modern electrical engineering. For some applications, it is also necessary to track the amplitude and the frequency of a signal (often sinusoidal), in addition to its phase. A strategy/device that is able to track the amplitude, frequency and phase of the fundamental component of a signal is called a sinusoid-locked loop (SLL). For a synchronous machine connected to the utility grid, the real and reactive power exchanged with the grid can be controlled to be zero. In this case, the machine is floating on the grid and the phase, the frequency and the amplitude of the voltage generated by the machine are the same as those of the grid voltage, respectively. In this paper, following the recently-proposed synchronverter concept, a virtual synchronous machine is controlled to implement this function so that it is operated as an SLL to provide the phase, frequency and amplitude of the fundamental component of the signal supplied. Both simulation and experimental results are provided to demonstrate its excellent performance, with comparison made to some major PLLs.**

***Index Terms*—Phase-locked loop (PLL), sinusoid-locked loop (SLL), synchronverters, second-order generalised integrator (SOGI), sinusoidal tracking algorithm (STA), synchronisation, enhanced phase-locked loop (EPLL).**

I. Introduction

More and more renewable energy sources are being connected to the grid. The most important and basic requirement for these applications is to synchronise the generated voltage with the grid voltage [1]–[4]. The information about the phase, the frequency and the amplitude of the fundamental component of the utility grid voltage must be provided quickly and accurately so that grid-connected inverters could be controlled to generate synchronised voltages with the connected grid.

There exist many open-loop and closed-loop phase-detection algorithms. The simplest open-loop method is zero-crossing [5] under the assumption that the voltage frequency is constant at least within half cycle. This method suffers from a slow update rate because the updated phase information is available only every half cycle. It is also unreliable because multiple zero-crossings could happen when the voltage is distorted [6]. More sophisticated open-loop phase-detection algorithms include the space-vector filter (SVF) based method [7], the extended Kalman filter (EKF) method [7] and the weighted least square estimation (WLSE) based method [8]. These techniques are often found to be sluggish with high sensitivity to frequency deviations, voltage distortions and voltage unbalances [5].

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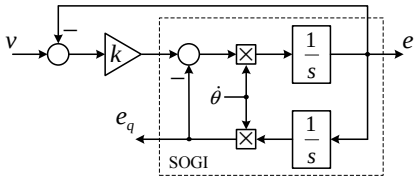
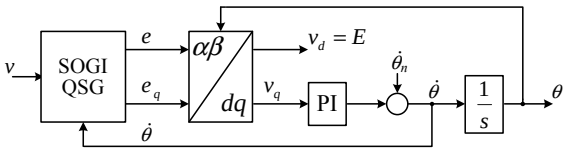
Closed-loop methods often employ a phase-locked loop (PLL) system, where a voltage-controlled oscillator (VCO) is designed to track the phase of the input signal. PLLs have been adopted as a part of the controllers for most of the grid-connected applications nowadays, e.g. in renewable energy applications [9], [10], FACTS devices [11], [12], active power filters [13], UPS applications [14] and power quality control [15]. The robustness and accuracy of the PLL are essential to the operation of these controllers [11], [16].

The most common technique used in three-phase applications is based on the synchronous reference frame (SRF-PLL) [17]–[19]. Similar operating concept can also be found in [20]. Although this technique can achieve excellent performance under ideal grid conditions, its response with unbalanced voltages is unacceptable with second harmonics existing in the PLL output because of the presence of the negative sequence [4], [20]. Reducing the PLL bandwidth could mitigate this problem but with the cost of lowering the dynamic performance [4]. In order to overcome this drawback, several advanced solutions have been proposed recently. In [4], two decoupled synchronous reference frames rotating in opposite directions were proposed to isolate and cancel the negative sequence of the grid voltage. Therefore, only positive sequence signal could pass through the PLL so that the steady-state errors and oscillations could be eliminated. One problem with this is that it does not take into account the effect of harmonics [6], which can be dealt with the delayed signal cancellation (DCS) operators proposed in [6], [21]. Another method was proposed on the stationary reference frame $\alpha\beta$ to isolate the negative sequence by generating a 90-degree shifted signal from the $\alpha\beta$ voltage with the second-order generalised integrator (SOGI) technique [22] [23], [24] and then the positive-sequence can be processed with a traditional SRF-PLL or a frequency-locked loop (FLL). A complex-coefficient filter (CCF) was proposed in [25] to extract the positive sequence to be processed with an SRF-PLL.

Although synchronisation is required in both three- and single-phase applications, the synchronisation in single-phase applications is much more difficult because the instantaneous single-phase voltage could not be treated as an instantaneous space vector [3]. Therefore the common solutions of several recent proposals for single-phase synchronisation are based on three-phase synchronisation, i.e. to generate a quadrature component v_q of the input signal v and then to treat the two perpendicular components as the output v_α and v_β of the Clark transformation from three-phase instantaneous voltage signals v_a, v_b and v_c [3], [22], [26]. The SOGI-based PLL proposed in [26], as shown in Figure 1, is one of such implementations.



(a) Quadrature-signal generator based on a second-order-generalised integrator (SOGI-QSG)



(b) A single phase PLL equipped with the SOGI-QSG

Figure 1. A single phase SOGI-based PLL

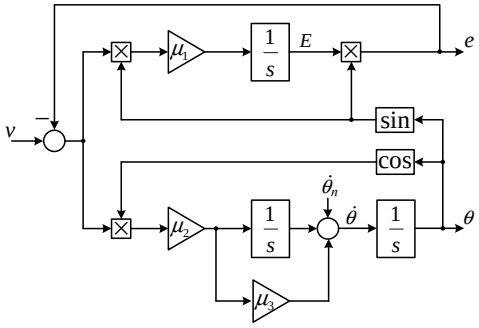


Figure 2. The sinusoidal tracking algorithm (STA) or the EPLL

Similar to its three-phase version [24], the sensitivity to the harmonics of the input signal is controlled by the gain k. A smaller gain offers better noise rejection but leads to a longer settling time. The critically-damped response is obtained when $k = \sqrt{2}$. Similar implementations were also proposed in [3], where filters were used to generate the quadrature version of the input voltage.

Other different single-phase synchronisation methods that are not based on the generation of a quadrature signal were also proposed with good signal tracking, low noise sensitivity and fast dynamic response. In [27], [28], an enhanced PLL (EPLL) was proposed to improve the performance of a conventional PLL, with a new phase-detection scheme that allows the amplitude to be calculated online. It was extended to three-phase applications in [29] with four single-phase EPLLs. The sinusoidal tracking algorithm (STA) proposed in [30], [31], as shown in Figure 2, is actually an equivalent implementation of the EPLL which shows fast frequency tracking performance. A simple single-phase PLL was introduced in [19] based on the principles of Coulon oscillators. Adaptive notch filters (ANF) [32] and the digital implementation of a resonant filter-based frequency tracking method [33] are some other recent developments.

In order to synchronise an inverter with the grid or another power source, it is also necessary for the inverter to be informed with the frequency and the amplitude of the voltage to be connected, in addition to the phase. This requires the synchronisation strategy be able to provide the amplitude and frequency, in addition to the phase, of the signal as well. Such a strategy/device is called a sinusoid-locked loop (SLL). In this paper, a novel approach for single-phase synchronisation is proposed to address this issue by mimicking a grid-connected synchronous machine that does not exchange power with the grid. If such a machine generates the same instantaneous voltage as the grid voltage, which means the voltage amplitude, the phase and the frequency of the generated voltage are the same as those of the grid voltage, then there is no power (real or reactive) exchanged between the synchronous machine and the grid. The other way around is also true. That is, if the power of a synchronous machine exchanged with the grid is zero, then the phase, the frequency and the amplitude of the voltage generated by the synchronous machine are the same as those of the grid voltage and the machine is locked to the grid voltage. Following the idea of synchronverters [34], which are inverters to mimic synchronous generators, the mathematical model of a synchronous machine can be adopted as the core of an SLL to lock the voltage. The control objective of the SLL is then to zero the real power and reactive power exchanged with the input voltage. Both simulation and experimental results are presented to demonstrate its excellent performance.

The rest of the paper is organised as follows. An overview of the synchronverter concept is presented in Section II. The proposed SLL is described and implemented in Section III, together with guidelines for tuning parameters. Simulation results and experimental results are given in Sections IV and V, respectively, followed by conclusions made in Section VI.

II. Overview of the Synchronverter Technology

A synchronverter is an inverter that mimics a conventional synchronous generator [34], which considerably facilitates the grid connection of renewable energy and distributed generation. Figure 3 shows the control strategy for a synchronverter. It includes the mathematical model of a three-phase round-rotor synchronous machine described by

$$\ddot{\theta} = \frac{1}{J}(T_m - T_e - D_p\dot{\theta}),$$

$$T_e = M_f i_f \left\langle i, \widetilde{\sin}\theta \right\rangle, \tag{1}$$

$$e = \dot{\theta} M_f i_f \widetilde{\sin}\theta, \tag{2}$$

$$Q = -\dot{\theta} M_f i_f \left\langle i, \widetilde{\cos}\theta \right\rangle, \tag{3}$$

where T_m, T_e, e, θ and Q are the mechanical torque applied to the rotor, the electromagnetic torque, the three-phase generated voltage, the rotor angle and the reactive power, respectively. J is the imaginary moment of inertia of all the parts rotating with the rotor. i_f is the field excitation current and M_f is the maximum mutual inductance between the stator windings and the field winding. $\dot{\theta}$ is the angular speed of the machine and also the frequency of voltage e and i is the stator current (vector) flowing out of the machine. $\widetilde{\sin}\theta$ and $\widetilde{\cos}\theta$ are defined as

$$\widetilde{\sin}\theta = \begin{bmatrix} \sin\theta \\ \sin\left(\theta - \frac{2\pi}{3}\right) \\ \sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix}, \quad \widetilde{\cos}\theta = \begin{bmatrix} \cos\theta \\ \cos\left(\theta - \frac{2\pi}{3}\right) \\ \cos\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix}.$$

In this paper, it is assumed that the number of pairs of poles for each phase is 1 and hence the mechanical speed of the machine is the same as the electrical speed of the electromagnetic field.

Similarly to the control of a synchronous generator, there are two control channels: one for the real power and the other for the reactive power. The real power is controlled by a frequency droop control loop, using the (imaginary) mechanical friction coefficient D_p as the feedback gain. This loop regulates the (imaginary) speed $\dot{\theta}$ of the synchronous machine and creates the phase angle θ for the generated voltage e. The reactive power is controlled by a voltage droop control loop, using a voltage droop coefficient D_q. This loop regulates the field excitation $M_f i_f$, which is proportional to the amplitude of the voltage generated.

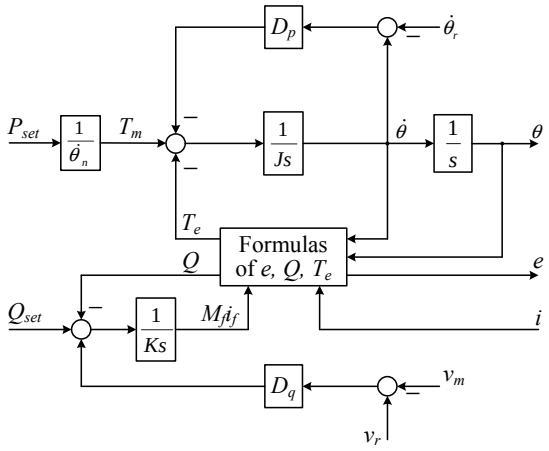


Figure 3. The controller for a synchronverter

III. Design of the Proposed Sinusoid-Locked Loop

A. A single-phase synchronous machine (SSM) connected to the grid

The simplified model of an SSM connected to the grid is depicted in Figure 4, where the grid voltage is denoted as $v = v_m \sin\theta_v$ and the SSM is modelled as a voltage source $e = E\sin\theta$, which represents the generated voltage, in series with the synchronous reactance X_s.

The real power P and reactive power Q flowing out of the SSM are [2], [12]

$$P = \frac{v_m E}{2X_s}\sin\left(\theta - \theta_v\right), \tag{4}$$

and

$$Q = \frac{v_m}{2X_s}\left[E\cos\left(\theta - \theta_v\right) - v_m\right]. \tag{5}$$

The factor 2 in the denominator is because E and v_m are peak amplitude values instead of RMS values. The SSM is considered to be synchronised and floating on the grid [2] if and only if

$$\begin{cases} E = v_m, \\ \theta = \theta_v. \end{cases} \tag{6}$$

In this case, $P = 0$ and $Q = 0$. In other words, if P and Q could be driven to zero then the condition (6) is satisfied and the generated voltage e is the same as the input (terminal) voltage v.

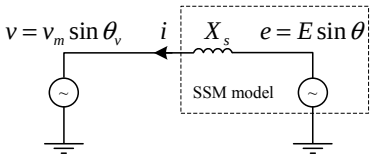
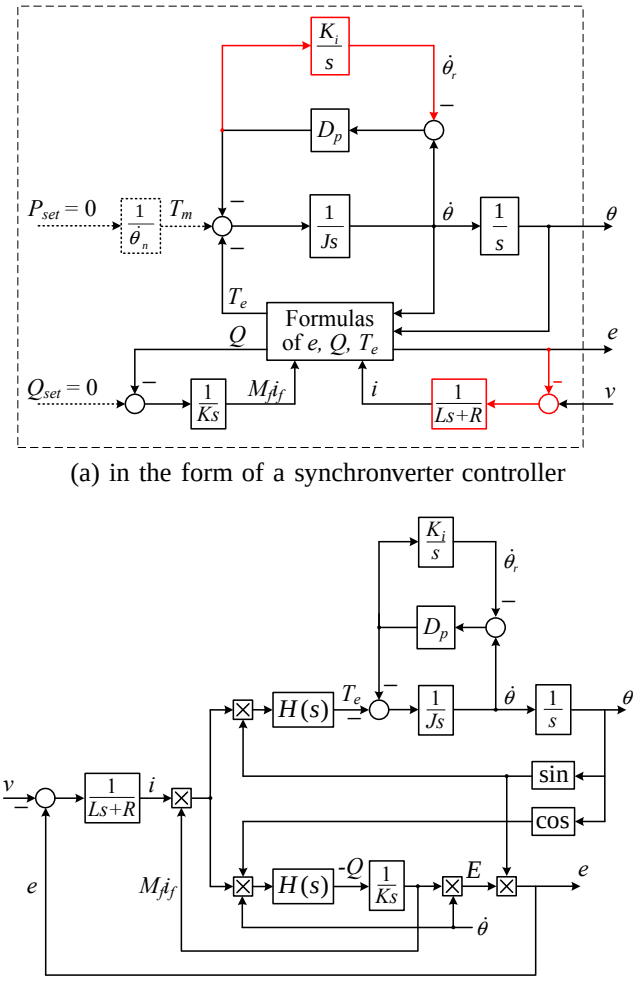


Figure 4. Model of an SSM connected to the grid



(a) in the form of a synchronverter controller

(b) in the conventional form

Figure 5. The proposed sinusoid-locked loop (SLL)

B. Implementation of the SLL

As mentioned above, the idea of the proposed SLL is to operate a virtual (single-phase) synchronous generator with $P = 0$ and $Q = 0$ so that the generated voltage e is the same as the fundamental component of the terminal voltage (or input voltage) v. Hence, the controller of the synchronverter shown in Figure 3 can be adopted to implement it after making necessary changes. The proposed SLL is shown in Figure 5(a), which is able to provide the frequency $\dot{\theta}$, phase θ, voltage amplitude E and a recovered voltage e for the terminal voltage (or input voltage) v.

As discussed above, the desired real power and reactive power should all be set as 0. For single-phase applications, the instantaneous values of T_e and Q given in (1) and (3) are

pulsating. Hence, their average values

$$T_e = \frac{1}{T}\int_{t-T}^{t} M_f i_f i \sin\theta \mathrm{dt}, \tag{7}$$

$$Q = -\frac{1}{T}\int_{t-T}^{t} \dot{\theta} M_f i_f i \cos\theta \mathrm{dt}, \tag{8}$$

where $T = \frac{2\pi}{\dot{\theta}}$ is the period of voltage v, should be used. The amplitude of the generated voltage e is

$$E = \dot{\theta} M_f i_f$$

and the instantaneous value of the generated voltage e is

$$e = \dot{\theta} M_f i_f \sin\theta = E \sin\theta, \tag{9}$$

which should track that of the input signal v.

The stator current i, which is the inductor current in the case of a synchronverter, should be generated internally as the voltage difference between e and v divided by the virtual synchronous reactance $X_s(s) = sL + R$, i.e.,

$$i = \frac{e - v}{sL + R}. \tag{10}$$

This completes the (virtual) current feedback loop, which is crucial for the synchronisation process.

1) Tracking the frequency and the phase: For synchronverters, the reference frequency $\dot{\theta}_r$ is provided and the actual frequency $\dot{\theta}$ is normally not the same as $\dot{\theta}_r$ because of the frequency droop control. For an SLL, $\dot{\theta}$ should track the frequency of voltage v, denoted $\dot{\theta}_v$, in order to drive T_e to 0. Hence, it is expected that $\dot{\theta}_r = \dot{\theta}_v$ and a mechanism should be added to achieve this.

After setting the desired real power to zero for a synchronverter, the electromagnetic torque T_e can be driven to zero only when the output of the frequency droop control block D_p is zero, which means $\dot{\theta}$ should be the same as the reference frequency $\dot{\theta}_r$. This is actually what is expected. Hence, on one hand, the output of the frequency droop control block D_p needs to be zero and, on the other hand, a reference frequency $\dot{\theta}_r$ needs to be generated so that $\dot{\theta}_r = \dot{\theta}_v$. These can be achieved by the integrator $\frac{K_i}{s}$ in Figure 5(a). At the steady state, T_e is driven to zero and the real power generated is

$$P = \dot{\theta} T_e = 0 \tag{11}$$

as well. As a result, $\dot{\theta}$ is the same as the (angular) frequency $\dot{\theta}_v$ of voltage v and the phase θ is the same as the phase θ_v of voltage v as well, i.e.,

$$\begin{cases} \dot{\theta} = \dot{\theta}_v, \\ \theta = \theta_v. \end{cases} \tag{12}$$

The SLL tracks the frequency and phase well.

2) Tracking the voltage amplitude: The voltage droop control in synchronverters is not needed for the SLL because the generated voltage is expected to be the same as the voltage v. The desired reactive power is set to 0 and the loop to drive the reactive power Q to zero is kept. At the steady state, $Q = 0$ in addition to $P = 0$. Hence, (5) is equivalent to

$$E = v_m. \tag{13}$$

Together with (12), the condition (6) is satisfied and the SLL is synchronised with the voltage v.

It is worth noting that one advantage of the SLL is that the frequency, phase, voltage amplitude and the recovered signal are all directly available internally without any extra calculation.

C. Tuning of the parameters

The SLL mainly contains an amplitude loop to regulate the reactive power (and the voltage), a frequency loop to regulate the real power (and the frequency $\dot{\theta}$) and a loop to generate the reference frequency $\dot{\theta}_r$ for the frequency loop.

The time constant of the frequency loop is

$$\tau_f = \frac{J}{D_p}. \tag{14}$$

The choice of τ_f determines the dynamic response of the loop. It is proportional to the moment of inertia J. A large τ_f is equivalent to having a large J, which makes the SLL less sensitive to variations in the grid frequency and also makes the system more stable. However, the response is slow. A small τ_f is equivalent to having a small J, which leads to fast frequency tracking. As a general rule of thumb, τ_f can be chosen much smaller than the period of the voltage v so that the frequency can be tracked very quickly.

The time constant of the amplitude loop is proportional to

$$\tau_q = \frac{K}{\dot{\theta}_n} \tag{15}$$

and the amplitude loop generates $M_f i_f$, which directly affects the amplitude of e in (9). Hence the choice of τ_q affects the dynamic response of the amplitude tracking. Generally, the frequency loop should be tuned much faster than the amplitude loop, which is normally the case because τ_f is often chosen much smaller than the period of the voltage v. This allows the voltage to be established. Otherwise $M_f i_f$ and eventually the voltage amplitude E would be driven to zero, which is also an equilibrium point of the system, before the frequency and phase could be synchronised. However, if a very large τ_q is chosen, it would take long time for the voltage amplitude E to track v_m.

The inductance L and resistance R of the virtual synchronous reactance X_s can be chosen small to enable a large transient current i, which helps speed up the tracking process. However, too small L and R may cause oscillations in the frequency estimated. Moreover, the ratio $\frac{R}{L}$ is the cut-off frequency of the filter $\frac{1}{sL+R}$, which determines the capability of filtering out the harmonics from the voltage v.

The loop to generate the reference frequency $\dot{\theta}_r$ is an outer loop for the frequency loop so it should be tuned much slower than the frequency loop. Its time constant is

$$\tau_{fn} = \frac{1}{D_p K_i}$$

and can be tuned as $\tau_{fn} = (10 \sim 100)\tau_f$.

Table I
PARAMETERS OF THE SLL FOR SIMULATIONS AND EXPERIMENTS

Parameters	Values	Parameters	Values
f_n	50 Hz	J	2.0264×10^{-5}
τ_f	0.0005 s	K	4809.6
τ_{fn}	0.049 s	K_i	100
τ_q	18.37 s	L	0.3 mH
D_p	0.2026	R	0.01 Ω

Table II
PARAMETERS FOR THE SOGI-BASED PLL AND THE STA

For the SOGI-based PLL	Values	For the STA	Values
k	1	μ_1	200
K_p	2.5	μ_2	500
K_i	50	μ_3	0.01

D. An equivalent structure of the SLL

The proposed SLL shown in Figure 5(a) can be redrawn as shown in Figure 5(b) to see the differences from conventional PLLs. The hold filter

$$H(s) = \frac{1 - e^{-Ts}}{Ts}$$

with $T = \frac{2\pi}{\dot{\theta}}$ is adopted to take the average value of the incoming signal.

With comparison to the STA or EPLL shown in Figure 2, the proposed SLL has the following features:

1). the error signal $v - e$ is passed through a low-pass filter $\frac{1}{Ls+R}$, which reduces the impact of the harmonics in v and also amplifies the difference to speed up the tracking process because R and L are often chosen small.

2). the hold filter $H(s)$ is applied to both channels, which removes the ripples in the signal entering the integrators and reduces the variations in frequency $\dot{\theta}$ and amplitude E.

3). the frequency $\dot{\theta}$ is forwarded into the voltage channel, which speeds up the tracking process when frequency changes.

4). $M_f i_f$ is forwarded into the frequency channel, which speeds up the tracking process when voltage changes.

5). a local feedback loop consisting of D_p and $\frac{K_i}{s}$ is added to the frequency loop, which is equivalent to cascading $\frac{s+D_pK_i}{s+D_pK_i+D_p/J} = \frac{s+1/\tau_{fn}}{s+1/\tau_{fn}+1/\tau_f}$ to $\frac{1}{Js}$. Since $\tau_{fn} \gg \tau_f$, $\frac{s+D_pK_i}{s+D_pK_i+D_p/J}$ is a lead compensator. It provides phase lead at high frequencies and enhances the responsiveness and stability of the system.

IV. SIMULATION RESULTS

Extensive simulations were carried out in MATLAB/Simulink to verify the proposed synchronisation method. The parameters of the SLL used in the simulations are given in Table I.

A. Tracking a distorted noisy signal with a non-stationary frequency

In addition to the fundamental component with $v_m = 20\sqrt{2}$, the voltage v contains a noise-added harmonic component

$$v_h(t) = 2\sqrt{2}\sin(3\omega_v t + 1.5) + 2\sqrt{2}\sin(5\omega_v t + 2.5) + n(t), \tag{16}$$

where $n(t)$ is a uniform random noise with the amplitude of $2\sqrt{2}$ V. The frequency $f_v = \frac{\omega_v}{2\pi}$ of the signal, which varied from 40Hz to 60Hz periodically with the cycle of 8 s, is expressed for the first period as

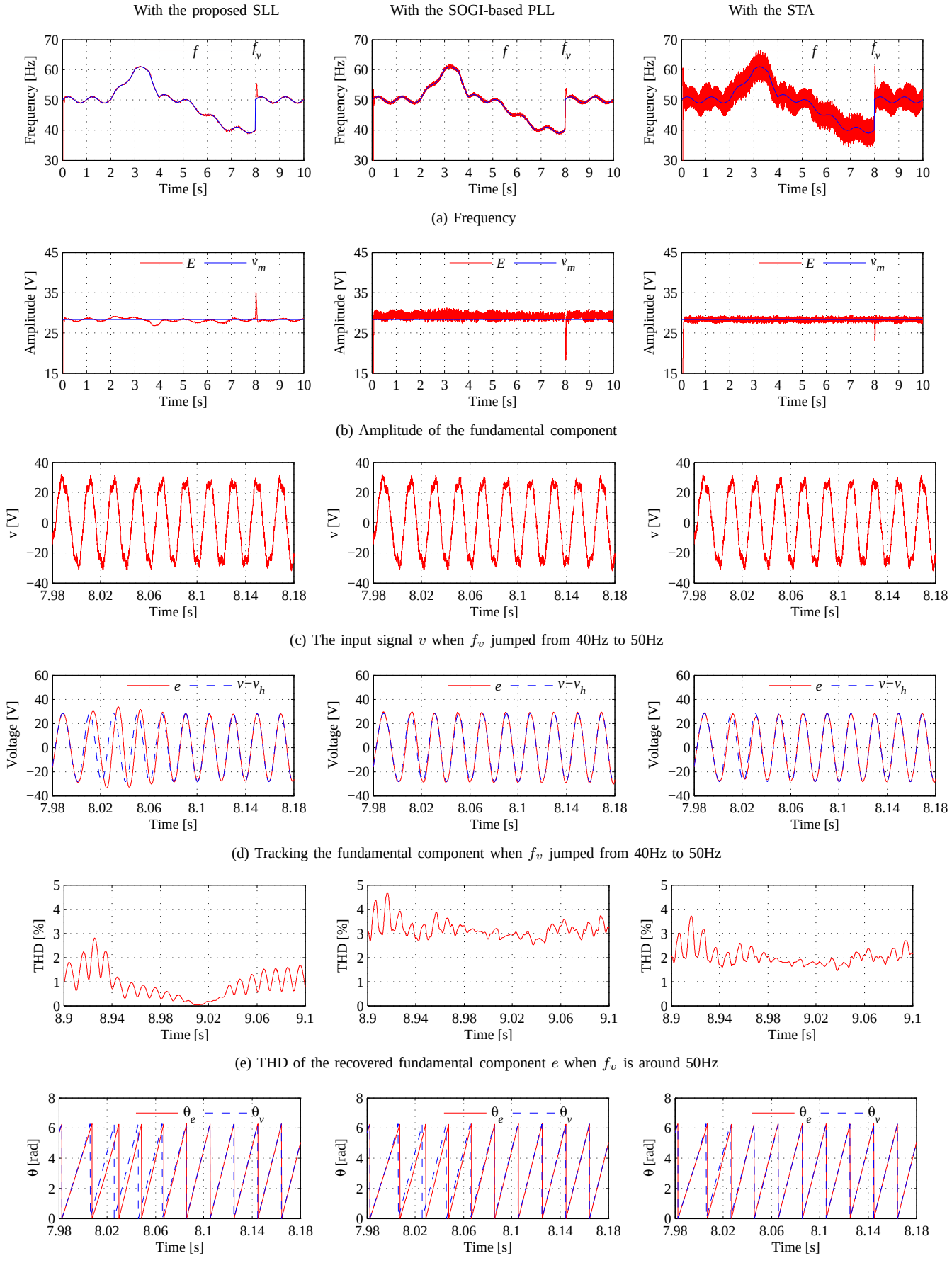
$$f_v = 50 + \sin(2\pi t) + \begin{cases} 0, & (0 < t \le 2) \\ 10(t-2), & (2 < t \le 3) \\ 10, & (3 < t \le 3.5) \\ 10 - 18(t-3.5), & (3.5 < t \le 4) \\ 1 - (t-4), & (4 < t \le 5) \\ -5(t-5), & (5 < t \le 7) \\ -10, & (7 < t \le 8). \end{cases} \tag{17}$$

The relevant signals from the simulation are shown in the left column of Figure 6. It is worth mentioning that, although the amplitude of the fundamental component does not change, the amplitude of v does change because of $v_h(t)$. As a result, the estimated amplitude E is not a straight line. Although there was significant amount of harmonics and noise contained in the signal, the amplitude, frequency and phase of the fundamental component were tracked very well by the proposed SLL without any problem, even when there was a large step change in the frequency from 40Hz to 50Hz at $t = 8$s. The amplitude of the generated voltage e is very close to the reference fundamental amplitude v_m of $v - v_h$. It was insensitive to the amplitude of harmonic components and therefore tracked v_m very well.

For the purpose of comparison, the SOGI-based PLL shown in Figure 1 and the STA shown in Figure 2 were simulated with the parameters given in Table II, which were optimised to compromise the dynamic performance and stability. The relevant signals from the simulations are shown in the middle column of Figure 6 for the SOGI-based PLL and in the right column of Figure 6 for the STA. Although the phase of the reference signal was tracked well with both methods, the frequency variations were much larger than those obtained with the proposed SLL and the THD of the recovered voltages were much higher as well. The ripples in the voltage amplitude were bigger than those in the case with the proposed SLL. The SOGI-based PLL offered better performance than the STA in tracking the frequency (but worse than the proposed SLL). When the frequency jumped from 40Hz to 50Hz, it took slightly longer for the proposed SLL to follow the frequency than the other two methods.

B. Extracting the fundamental component from a noisy distorted square wave

In this simulation, the input signal v, as shown in Figure 7(a), is a clean square wave with the period of 19 ms and the amplitude of $20\sqrt{2}$ V, added with the harmonic signal $v_h(t)$ given in (16). Simulations were carried out with the same parameters used in the previous subsection for the



(a) Frequency

(b) Amplitude of the fundamental component

(c) The input signal v when f_v jumped from 40Hz to 50Hz

(d) Tracking the fundamental component when f_v jumped from 40Hz to 50Hz

(e) THD of the recovered fundamental component e when f_v is around 50Hz

(f) Tracking the phase of the fundamental component when f_v jumped from 40Hz to 50Hz

Figure 6. Simulation results: Tracking a distorted noisy signal with a non-stationary frequency

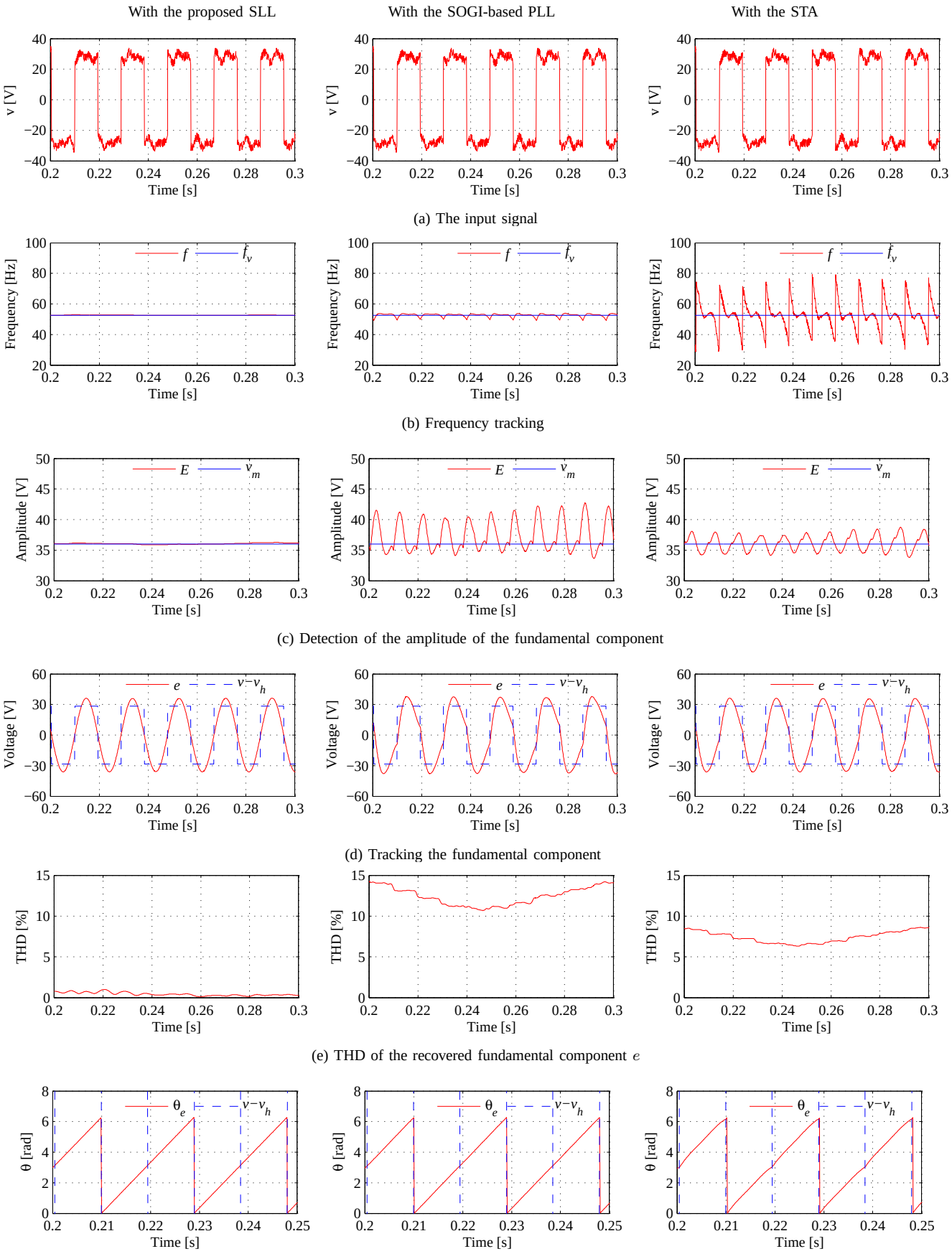


Figure 7. Simulation results: Extracting the fundamental component from a noisy distorted square wave

proposed SLL, the SOGI-based PLL and the STA to extract the fundamental component of v. The relevant signals are shown in Figure 7. The proposed SLL demonstrated excellent performance and is superior to the other two. The SOGI-based PLL caused noticeable frequency variations and the STA was not able to track the frequency while the proposed SLL followed the frequency very well. The STA caused noticeable variations in the amplitude detected and the SOGI-based PLL was not able to track the amplitude while the proposed SLL detected the amplitude very well. The recovered signals e, as shown in the left column of Figure 7(d), is clean and sinusoidal with the THD as low as 0.8% at the fundamental frequency of 52.63Hz but the recovered signals from the other two methods have significant amount of harmonics. The STA had difficulties in tracking the phase as well.

V. Experimental Results

Various experiments were carried out with a TI renewable energy kit, which is equipped with a floating point DSP TMS320F28335, with a sampling frequency of 10 kHz. The voltage signal v was properly conditioned and read by the DSP via the on-chip Analog to Digital Converter (ADC) module. The results of three experiments, for which the same parameters used in simulations were used, will be described below. The time constant of the frequency loop is five times of the sampling frequency and, hence, the frequency is expected to settle down in about 15~20 sampling periods, that is less than one tenth of the grid period. One experiment was carried out with the input signal taken from the utility grid and the other two experiments were carried out with the voltage signals adopted in the simulations, which were generated by the same DSP through a Digital to Analog (DAC) module.

A. Tracking the grid voltage

The grid voltage was scaled down with a single-phase transformer and then shifted and conditioned by op-amps to form a signal that could be read by the ADC module. The same experiment was carried out with the proposed SLL, the SOGI-PLL and the STA with the results shown in the left column, middle column and right column of Figure 8, respectively. The phase was tracked well by all three methods. The proposed SLL tracked the voltage almost immediately, producing accurate frequency, amplitude and phase. Although the grid signal was not clean, the SLL did not have any difficulty in tracking it. Because there is no phase delay, the SLL can also be used as a filter. The SOGI-based PLL took about one cycle to produce the correct amplitude and half cycle to produce the correct frequency while the STA took about two cycles to produce the correct amplitude and one cycle to produce the correct frequency, all with noticeable overshoot. Apparently, the proposed SLL outperforms the other two significantly.

B. Tracking a distorted noisy signal with a non-stationary frequency

The voltage signal used in Section IV-A was generated and sent out via a DAC channel as the voltage signal v. Again, the experiment was carried out for the SLL, the SOGI-based PLL and the STA with the results shown in Figure 9. The experimental results matched very well with the simulation results shown in Figure 6. The proposed SLL tracked the varying frequency and the amplitude very well. The SOGI-based PLL was also able to track the frequency and the amplitude but with much bigger ripples. The frequency produced by the STA varied in a very wide band. The experimental results when the frequency jumped from 40 to 50 Hz are shown in Figure 10. The proposed SLL tracked the frequency jump well and settled down well. The SOGI-PLL tracked the frequency well but there were noticeable variations in the frequency after the jump. The STA was not able to deal with the jump in the frequency.

C. Extracting the fundamental component from a noisy distorted square wave

The voltage signal used in Section IV-B was generated and sent out via a DAC channel as the voltage signal. Again, the experiment was carried out for the SLL, the SOGI-based PLL and the STA with the results shown in Figure 11. The experimental results matched the simulation results well. The proposed SLL was able to track the phase, frequency and amplitude but the SOGI-PLL cannot track the amplitude. The STA was not able to track the amplitude and the frequency well although the phase was tracked well. The voltage recovered by the proposed SLL is very clean but the voltages recovered by the other two methods contain significant harmonics.

VI. Conclusion

Following the idea of synchronverters [34], a sinusoid-locked loop is proposed to track the fundamental component of a periodic signal based on the principles of grid-connected synchronous machines that do not exchange any power with the grid. Both simulation and experimental results have demonstrated its excellent performance in tracking the frequency and amplitude of the fundamental component of the signal, in addition to the phase. The response is much faster than the SOGI-based PLL and the STA, which are commonly used synchronisation methods for grid-connected inverters. The recovered voltage is very clean with a very low THD and the detected frequency and amplitude contain very small ripples. Some guidelines for tuning the parameters are also provided.

Acknowledgements

The authors would like to thank Robert Owen for the generous donation of TI kits under the TI's European University Programme.

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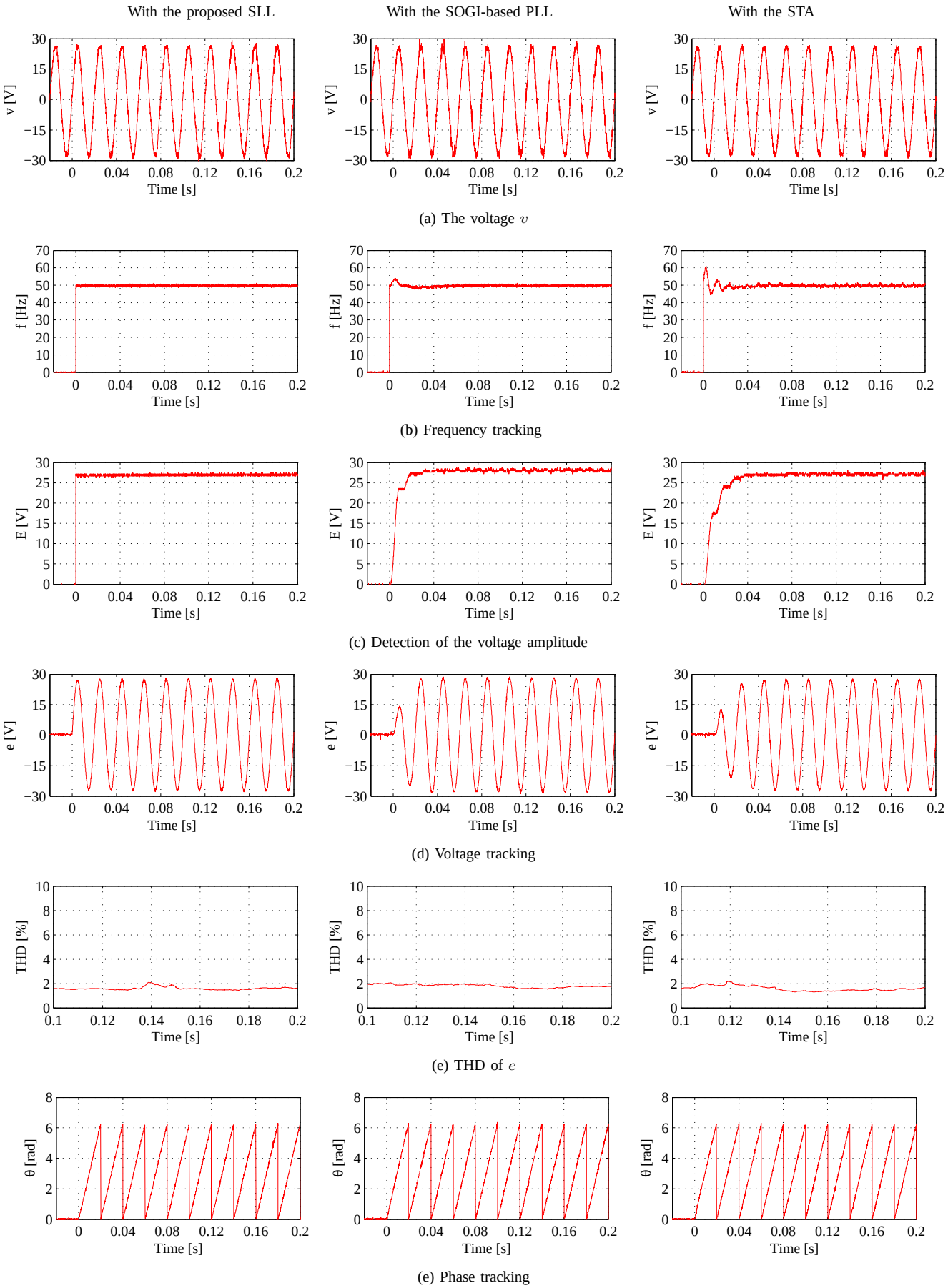

Figure 8. Experimental results: Tracking the grid voltage

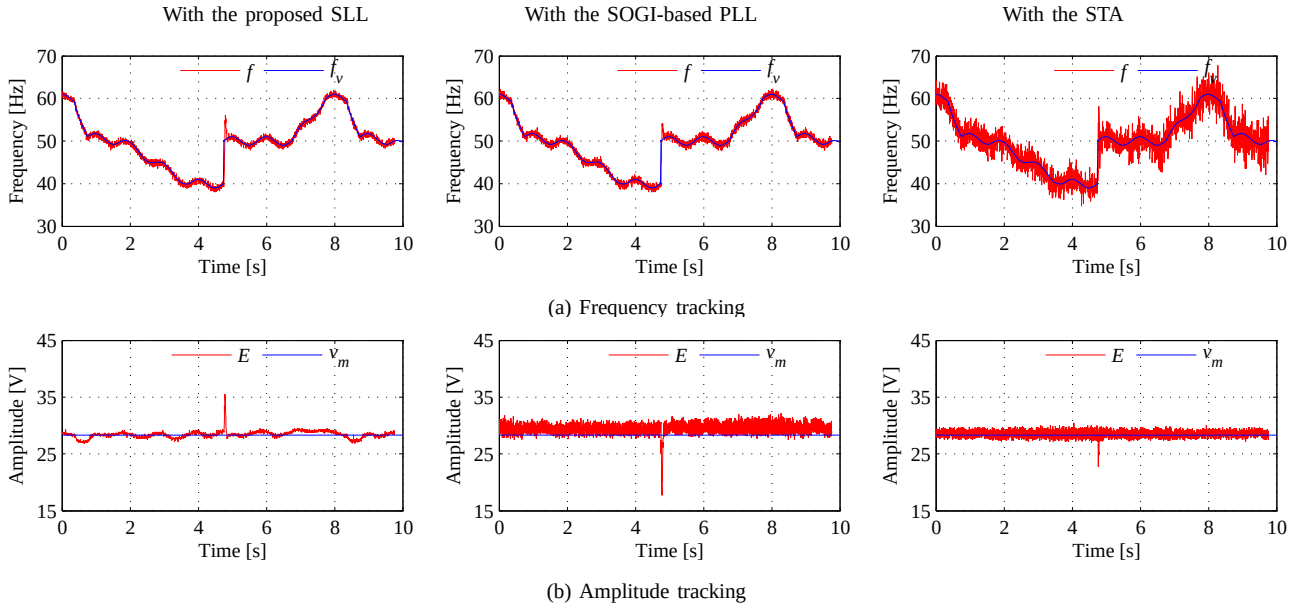

Figure 9. Experimental results: Frequency and amplitude tracking for a distorted noisy signal with a non-stationary frequency

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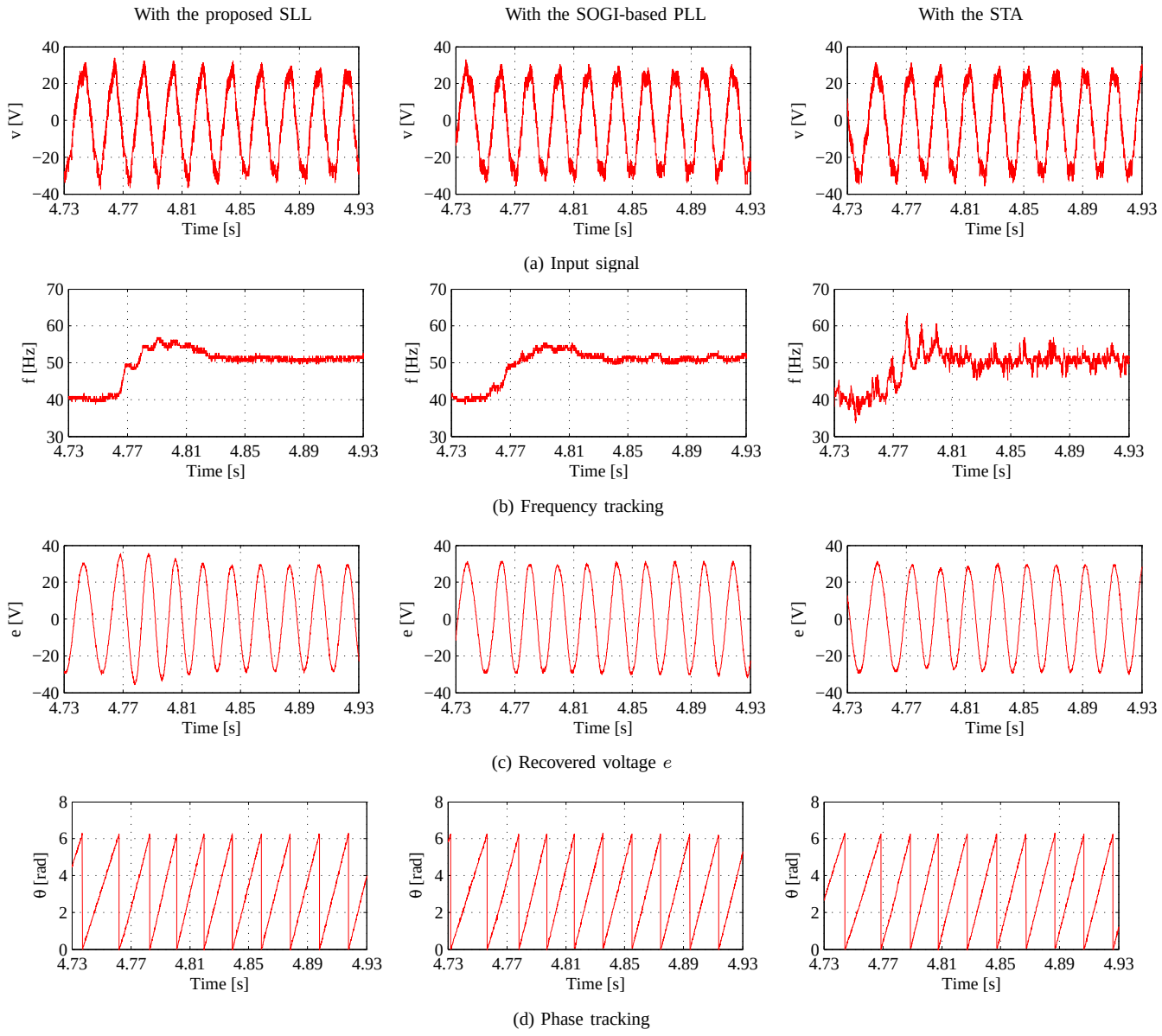

(a) Input signal

(b) Frequency tracking

(c) Recovered voltage e

(d) Phase tracking

Figure 10. Experimental results: Tracking for a distorted noisy signal with a non-stationary frequency when the frequency jumped from 40Hz to 50Hz

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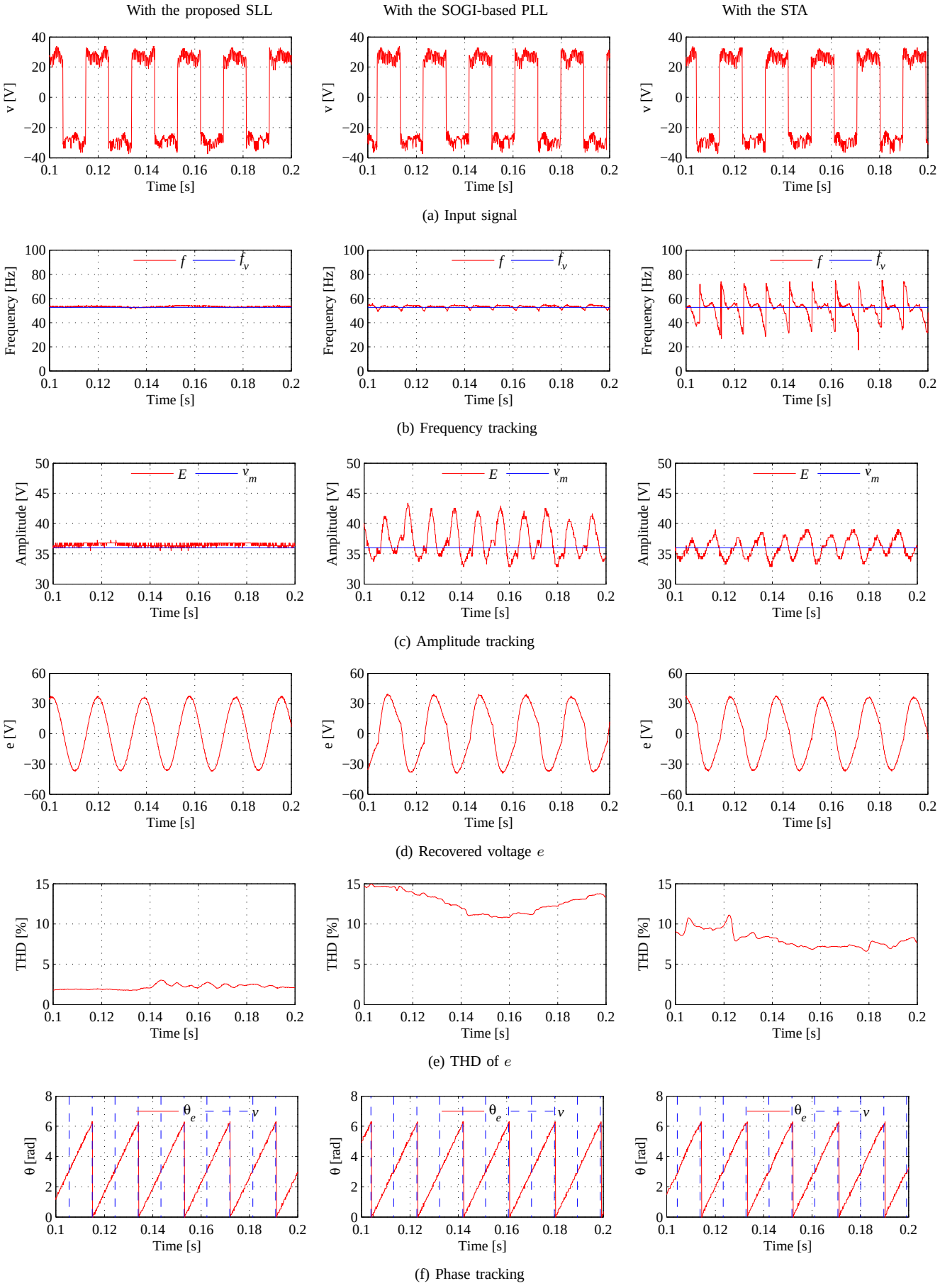

Figure 11. Experimental results: Extracting the fundamental component from a noisy distorted square wave