Inverters with Capacitive Output Impedances, Part I: Design and Parallel Operation

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***Abstract*—In this paper, it is shown that the output impedance of an inverter can be designed to be capacitive via the feedback of the filter inductor current through an integrator. Moreover, a recently-proposed robust droop controller is further developed and applied to inverters with capacitive output impedances to achieve accurate sharing of real power and reactive power and to maintain the output voltage within the desired range. Both simulation and experimental results are provided to demonstrate the feasibility and excellent performance. It is also shown that an inverter is able to achieve lower total harmonic distortion (THD) when it is designed to have a capacitive output impedance than when it is designed to have a resistive or inductive output impedance.**

Keywords: Droop control, parallel operation of inverters, proportional load sharing, inverters with capacitive output impedance, inductive output impedance, resistive output impedance

I. Introduction

Nowadays, more and more distributed generation and renewable energy sources, e.g. wind, solar and tidal power, are connected to the public grid via power inverters. They often form microgrids before being connected to the public grid [1]–[4]. Due to the availability of high current power electronic devices, it is inevitable that multiple inverters are needed to be operated in parallel for high-power and/or low-cost applications. Another reason is that parallel-operated inverters provide system redundancy and high reliability needed by critical customers. A natural problem for parallel-operated inverters is how to share the load among them. A key method is to use the droop control [5]–[13], which is widely used in conventional power generation systems [14]. The advantage is that no external communication mechanism is needed among the inverters [10], [15]. This enables good sharing for linear and/or nonlinear loads [10], [16]–[20]. In some cases, external communication means are still adopted for load sharing [21] and restoring the microgrid voltage and frequency [3], [9].

How to improve the sharing accuracy has been a main driving force in the research area of parallel operation of inverters for many years [22]–[24]. The equal sharing of linear and nonlinear loads were intensively investigated [5], [6], [16], [18], [19] and high accuracy of equal sharing can be achieved. A voltage bandwidth droop control was used to share nonlinear loads in [10] and a small signal injection method was proposed to improve the reactive power sharing accuracy in [20], which can also be extended to harmonic current sharing. An important contribution was made in [5], [18], where it was pointed out that the output impedance of the inverters plays a critical role in power sharing and a droop controller for inverters with resistive output impedances was proposed for sharing linear and nonlinear loads [6], [19]. However, all these control strategies rely on the accurate tuning of the control parameters because there is not a mechanism in the conventional droop controller so that it is robust against numerical errors, disturbances, component mismatches and parameter drifts etc [25]. The conventional droop controllers require that all the inverters have the same per-unit output resistance over a wide range of frequencies. A significant breakthrough has recently been made in [25], where a robust droop controller has been proposed to achieve accurate sharing of real power and reactive power at the same time even if there are numerical errors, disturbances, component mismatches and parameter drifts. It is also able to maintain excellent voltage regulation.

As mentioned above, it was pointed out in [5], [18] that the output impedances of inverters play a critical role in power sharing. Inverters could be designed to have resistive output impedances. The droop control has different forms for different types of output impedances [5], [12], [26]. The $Q-E$ and $P-\omega$ droop is used when the output impedance is inductive; the $Q-\omega$ and $P-E$ droop is used when the output impedance is resistive; for a complex impedance, a transformation involving the impedance phase angle needs to be introduced [23], [27]. The general understanding is that a resistive output impedance is better than an inductive output impedance because it makes the compensation of harmonics easier.

Some questions pop up immediately. For example, 1) Can the output impedance of an inverter be designed capacitive? 2) If so, how to achieve the parallel operation of inverters with capacitive output impedances? 3) What are the advantages, if any, to do so? To the best knowledge of the authors, the concept of designing an inverter to have a capacitive output impedance has not been studied in the literature. It will be shown in this paper that the output impedance of an inverter can be designed to be capacitive over a wide range of frequencies. Moreover, the robust droop controller proposed in [25] can be further developed so that it can be applied to inverters with capacitive output impedances to achieve accurate sharing of both real and reactive power. Both simulation and experimental results will be presented to demonstrate the feasibility and performance. It will also be shown that an inverter offers better THD when it is designed to have a capacitive output impedance than when it is designed to have a resistive or inductive output impedance. As a matter

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of fact, the controller can be designed to optimise the quality of the output voltage. This will be reported in Part II of this series, due to the page limit. Other advantages of designing inverters to have capacitive output impedances will be explored in the future.

The rest of the paper is organised as follows. A controller is proposed in Section II to force the output impedance of an inverter to be capacitive over a wide range of frequencies and a robust droop controller is proposed in Section III to achieve accurate power sharing for inverters with capacitive output impedances. Simulation results are presented in Section IV and experimental results are presented in Section V to demonstrate the design and analysis, followed by conclusions made in Section VI.

II. Controller Design to Achieve a Capacitive Output Impedance

Usually, the inverter output impedance is inductive because of the output inductor and/or the highly inductive line impedance. In low-voltage applications, the line impedance is predominantly resistive. Since control strategies can be used to change the output impedance, it can be easily forced to be resistive [25], inductive [5], [22], or other types; see e.g. [27]. Arguably, it is better to force the output impedance to be resistive [5], [18], [26] because its impedance does not change with the frequency and the effect of nonlinear loads (harmonic current components) on the voltage THD can be compensated more easily. In this section, a strategy is proposed to force the output impedance of an inverter to be capacitive.

Figure 1(a) shows an inverter, which consists of a single-phase H-bridge inverter powered by a DC source, and an LC filter. The control signal u is converted to a PWM signal to drive the H-bridge so that the average of u_f over a switching period is the same as u, i.e. $u \approx u_f$. Hence, the PWM block and the H-bridge can, and will, be ignored in the controller design. The inductor current i is measured for feedback so that the output impedance of the inverter is forced to be capacitive and to dominate the impedance between the inverter and the AC bus (at the fundamental frequency). This is done, as shown in Figure 1(b), via a current feedback through an integrator block $\frac{1}{sC_o}$.

The following two equations hold for the closed-loop system consisting of Figure 1(a) and Figure 1(b):

$$u = v_r - \frac{1}{sC_0} i, \quad \text{and} \quad u_f = (R + sL)i + v_o.$$

Since the average of u_f over a switching period is the same as u, there is (approximately)

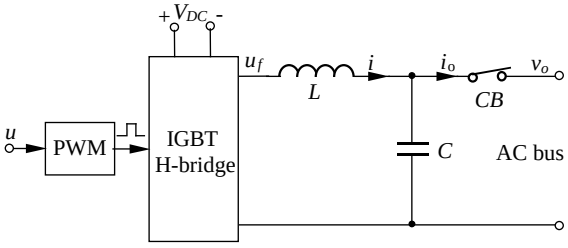
$$v_r - \frac{1}{sC_o} i = (R + sL)i + v_o,$$

which gives

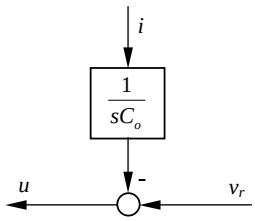
$$v_o = v_r - Z_o(s) \cdot i,$$

where the output impedance $Z_o(s)$ is

$$Z_o(s) = R + sL + \frac{1}{sC_o}. \tag{1}$$



(a) A descriptive circuit



(b) A controller to achieve a capacitive output impedance

Figure 1. A single-phase inverter with a capacitive output impedance

This is equivalent to connect a virtual capacitor C_o in series with the filter inductor L. If C_o is small enough, then the effect of the inductor $(R + sL)$ is not significant and the output impedance can be made nearly purely capacitive at the fundamental frequency, i.e., roughly

$$Z_o(s) \approx \frac{1}{sC_o}.$$

III. Droop Controller for Inverters with Capacitive Output Impedances

As mentioned before, the droop control strategy has different forms for inverters with different types of output impedances [5], [12], [26]. The $Q - E$ and $P - \omega$ droop is used when the output impedance is inductive; the $Q - \omega$ and $P - E$ droop is used when the output impedance is resistive; for a complex impedance, a transformation involving the impedance phase angle needs to be introduced [23], [27]. In this section, the droop control for inverters with capacitive output impedances will be developed.

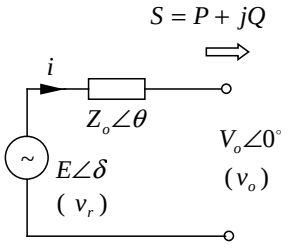


Figure 2. The model of an inverter

An inverter can be modelled as a reference voltage source with an output impedance Z_o, as shown in Figure 2. The real power and reactive power dispatched to the terminal via the

output impedance Z_o are

$$\begin{aligned} P &= (\frac{EV_o}{Z_o}\cos\delta - \frac{V_o^2}{Z_o})\cos\theta + \frac{EV_o}{Z_o}\sin\delta\sin\theta, \\ Q &= (\frac{EV_o}{Z_o}\cos\delta - \frac{V_o^2}{Z_o})\sin\theta - \frac{EV_o}{Z_o}\sin\delta\cos\theta, \end{aligned}$$

where δ is the phase difference between the supply and the terminal, often called the power angle.

For an inductive impedance, $\theta = 90°$. Then

$$P = \frac{EV_o}{Z_o}\sin\delta \quad \text{and} \quad Q = \frac{EV_o}{Z_o}\cos\delta - \frac{V_o^2}{Z_o}.$$

When δ is small,

$$P \approx \frac{EV_o}{Z_o}\delta \quad \text{and} \quad Q \approx \frac{E - V_o}{Z_o}V_o,$$

and, roughly,

$$P \sim \delta \quad \text{and} \quad Q \sim V_o.$$

Hence, the conventional droop control strategy takes the form

$$\begin{aligned} E_i &= E^* - n_i Q_i, \\ \omega_i &= \omega^* - m_i P_i, \end{aligned}$$

where, E^* is the rated RMS voltage of the inverter and ω^* is the rated frequency. This strategy is sketched in Figure 3(a).

For a resistive impedance, $\theta = 0°$. Then

$$P = \frac{EV_o}{Z_o}\cos\delta - \frac{V_o^2}{Z_o} \quad \text{and} \quad Q = -\frac{EV_o}{Z_o}\sin\delta.$$

When δ is small,

$$P \approx \frac{E - V_o}{Z_o}V_o \quad \text{and} \quad Q \approx -\frac{EV_o}{Z_o}\delta,$$

and, roughly,

$$P \sim V_o \quad \text{and} \quad Q \sim -\delta.$$

Hence, the conventional droop control strategy takes the form

$$\begin{aligned} E_i &= E^* - n_i P_i, \\ \omega_i &= \omega^* + m_i Q_i, \end{aligned}$$

This is sketched in Figure 3(b).

If the impedance is capacitive, then $\theta = -90°$ and

$$P = -\frac{EV_o}{Z_o}\sin\delta \quad \text{and} \quad Q = -\frac{EV_o}{Z_o}\cos\delta + \frac{V_o^2}{Z_o}.$$

When δ is small,

$$P \approx -\frac{EV_o}{Z_o}\delta \quad \text{and} \quad Q \approx -\frac{E - V_o}{Z_o}V_o,$$

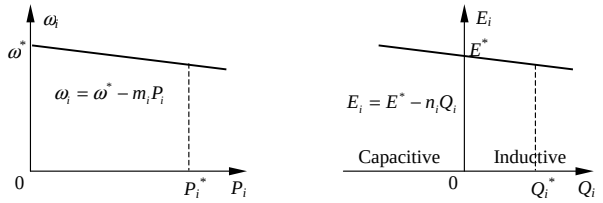
and, roughly,

$$P \sim -\delta \quad \text{and} \quad Q \sim -V_o.$$

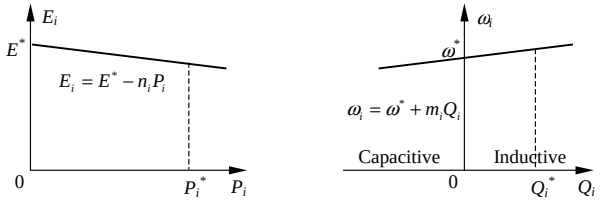
Hence, the strategy following the conventional droop control strategy for inverters with capacitive output impedances should take the form

$$\begin{aligned} E_i &= E^* + n_i Q_i, \\ \omega_i &= \omega^* + m_i P_i, \end{aligned}$$

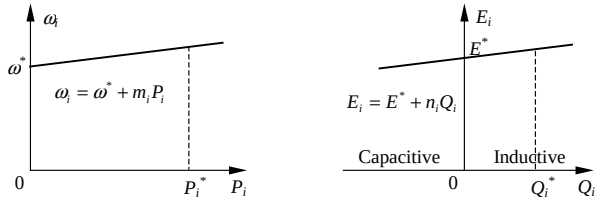
This is sketched in Figure 3(c). Note that, in order to make sure that the $Q-E$ loop and the $P-\omega$ loop are of a negative feedback, respectively, so that the droop controller is able to regulate the frequency and the voltage, the signs before $n_i Q_i$ and $m_i P_i$ are all positive, which makes them boost terms.



(a) for inverters with an inductive output impedance



(b) for inverters with a resistive output impedance



(c) for inverters with a capacitive output impedance

Figure 3. Droop control strategies

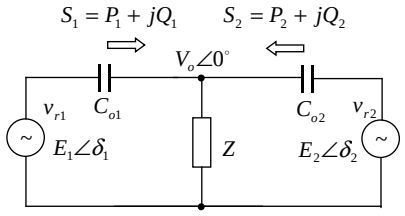


Figure 4. Two inverters with capacitive output impedances operated in parallel

The voltage reference v_{ri} for Inverter i is formed as a pure sinusoidal signal $v_{ri} = \sqrt{2}E_i\sin(\omega_i t + \delta_i)$ by taking E_i as the RMS voltage set-point and ω_i as its frequency. Figure 4 depicts the parallel operation of two inverters with capacitive output impedances. The power ratings of the inverters are $S_1^* = E^* I_1^*$ and $S_2^* = E^* I_2^*$ with the rated current I_1^* and I_2^*, respectively. They share the same load voltage v_o. Note that the load voltage drops when the load increases. This is called the load effect. In order for the inverters to share the load in proportion to their power ratings, the droop coefficients of the inverters should be in inverse proportion to their power ratings [10], [26], i.e., n_i and m_i should be chosen to satisfy

$$n_1 S_1^* = n_2 S_2^*, \tag{2}$$

$$m_1 S_1^* = m_2 S_2^*. \tag{3}$$

As reported in [25], the conventional droop control strategy is not able to accurately share both real power and reactive power at the same time because there is no mechanism to make sure that the voltage set-points are the same when numerical errors, noises and disturbances exist. Also it is impossible to make sure that the per-unit output impedances are the same because of component mismatches and parameter shifts. Hence, the voltage regulator bolted onto the conventional droop controllers for inverters with resistive (or inductive) impedances proposed in [25] should also be bolted onto the droop controller for inverters with capacitive output impedances. This results in the robust droop controller shown in Figure 5. It is able to share both real power and reactive power accurately even if the per-unit output impedances are not the same and/or there are numerical errors, disturbances and noises because, at the steady state, there is

$$n_i Q_i + K_e(E^* - V_o) = 0. \tag{4}$$

This means

$$n_i Q_i = constant,$$

as long as K_e is the same for all inverters. This guarantees the accurate sharing of reactive power in proportion to their ratings. As long as the system is stable, which leads to the same frequency, the real power can be guaranteed as well [25].

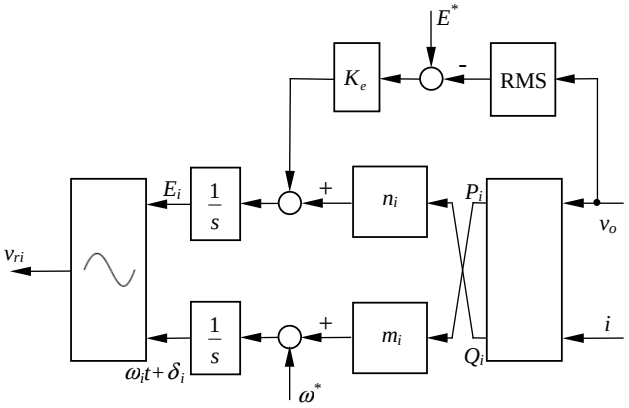


Figure 5. The proposed robust droop controller for inverters with capacitive output impedances to achieve accurate proportional load sharing

According to (4), the output voltage is

$$V_o = E^* + \frac{n_i}{K_e} Q_i = E^* + \frac{n_i Q_i}{K_e E^*} E^*,$$

which can be maintained within the desired range via choosing a big K_e. Hence, the control strategy has very good capability of voltage regulation as well, in addition to the accurate power sharing. This is the same as the inverters with resistive (and inductive) output impedances reported in [25].

The droop coefficients n_i and m_i can be determined as usual by the desired voltage drop ratio $\frac{n_i Q_i^*}{K_e E^*}$ and the frequency boost ratio $\frac{m_i P_i^*}{\omega^*}$, respectively, at the rated real power P^* and reactive power Q^*.

IV. Simulation Results

A system that consists of two single-phase inverters powered by two separate 42V DC voltage supplies was used to carry out simulations to verify the design. The capacity of Inverter 1 is 25VA and the capacity of Inverter 2 is 50VA, with the rated power factor of 0.9. It is expected that $P_2 = 2P_1$ and $Q_2 = 2Q_1$. The switching frequency is 7.5kHz and the frequency of the system is 50Hz. The rated voltage is 12V and $K_e = 20$. The filter inductor is $L = 2.35$mH with a parasitic resistance of 0.1Ω and the filter capacitance C is 22μF.

Assume that the desired voltage drop ratio $\frac{n_i Q_i^*}{K_e E^*}$ is 10% and frequency boost ratio $\frac{m_i P_i^*}{\omega^*}$ is 1%, respectively, at the rated real power $P_i^* = 0.9 S_i^*$ and reactive power $Q_i^* = 0.436 S_i^*$. As a result, $n_1 = 2.2$ and $n_2 = 1.1$; $m_1 = 0.14$ and $m_2 = 0.07$.

The capacitor is chosen as $C_o = 479\mu F$ and the corresponding impedance at the fundamental frequency is $Z_o(j\omega^*) = -j6.65\Omega$, which is capacitive and is able to dominate the impedance between the voltage reference and the terminal. In order to compare the performance with those of inverters with resistive output impedances and inductive output impedances, the current feedback controller proposed in [25] with $K_i = 4$ and $K_i = 0$ are used to obtain a resistive output impedance of about $Z_o = 4\Omega$ and an inductive output impedance of about $Z_o(j\omega^*) = j0.74\Omega$, respectively.

A. With a linear load

Simulations were carried out for a linear load with $R_L = 9\Omega$. The results for the inverters with capacitive, resistive and inductive output impedances are shown in the left, middle and right columns of Figure 6, respectively. The inverters with capacitive output impedances performed very well: the real power and reactive power were well shared; the output voltage is very close to the rated voltage; and the THD is low. The overall performance of the inverters with capacitive output impedances is slightly better than those of the inverters with resistive and inductive impedances (the THD of the inverters with resistive impedances is slightly lower than that of the inverters with capacitive impedances but they are both very low so it does not make much difference).

B. With a nonlinear load

The same simulations were carried out for a full-bridge rectifier load with an LC filter $L = 150\mu H$, $C = 1000\mu F$ and $R_L = 9\Omega$. The results for the inverters with capacitive, resistive and inductive output impedances are shown in the left, middle and right column of Figure 7, respectively. Again, the inverters with capacitive output impedances performed very well: 1) the real power and reactive power were accurately shared; 2) the voltage is closer to the rated voltage than that obtained from inverters with resistive output impedances; 3) the THD is much better than that obtained from the inverters with inductive output impedances and is slightly better than that of the inverters with resistive output impedances; 4) the 3rd harmonics in the output voltage for inverters with capacitive output impedances is made nearly zero. In summary, the inverters with capacitive output impedances offer the best

overall performance and the inverters with inductive output impedances offer the worst overall performance among the three. It is worth noting that the output impedances of the two inverters are the same, which means the per-unit output impedances are significantly different. However, the inverters shared both the real power and the reactive power accurately.

Table I
STEADY-STATE PERFORMANCE WHEN SUPPLYING THE NONLINEAR LOAD

Type of Z_o	L	R	C_o (479μF)
THD of v_o	29.38%	18.54%	17.86%
V_o	12.15	11.27	11.62
f_1	49.81	49.96	50.16
f_2	49.81	49.96	50.16
P_1	8.40	6.60	7.36
P_2	16.81	13.20	14.72
Q_1	-1.40	-1.80	-3.46
Q_2	-2.80	-3.60	-6.92

V. EXPERIMENTAL RESULTS

In order to further verify the design and analysis, experiments were carried out on a test rig, which consists of two single-phase inverters powered by two separate 42V DC voltage supplies. The parameters of the system are the same as those given in the previous section. Experiments were carried out for inverters having capacitive output impedances (with $C_o = 479\mu$F) and resistive output impedances ($K_i = 4\Omega$).

A. With a linear load

Experiments were carried out for a linear load with $R_L = 9\Omega$. The results for the inverters with capacitive and resistive output impedances are shown in the left and right columns of Figure 8, respectively. The inverters with capacitive output impedances worked very well: with accurate sharing of real power and reactive power, good regulation of voltage and low THD. With comparison to the inverters with resistive output impedances, the voltage regulation performance is slightly better because this is related to the reactive power of the load, which is small, and the frequency variation is slightly higher because this is related to the real power.

B. With a nonlinear load

Experiments were carried out for a full-bridge rectifier load with an LC filter $L = 150\mu H$, $C = 1000\mu F$ and $R_L = 9\Omega$. The results for the inverters with capacitive and resistive output impedances are shown in the left and right columns of Figure 9, respectively. Again, the inverters with capacitive output impedances worked very well with accurate sharing of real power and reactive power and good capability of voltage regulation. The inverters with capacitive output impedances demonstrated much better THD than the inverters with resistive output impedances. Moreover, when another inverter was put in parallel with an inverter, the THD of the output voltage dropped much more when the output impedances of the inverters are capacitive than when the output impedances are resistive.

VI. CONCLUSIONS

It has been shown that it is feasible to force the output impedance of an inverter to be capacitive although it normally has an inductor connected to the inverter bridge. One simple approach is to form an inductor current feedback through an integrator, of which the time constant is the desired output capacitance. This is a virtual capacitor so there is no limit on its current rating and can be applied to any power level. Moreover, the robust droop controller proposed in [25] is further developed and applied to inverters with capacitive output impedances to achieve accurate sharing of real power and reactive power. Both simulation and experimental results have shown that the THD of an inverter can be made lower when it is designed to have a capacitive output impedance than when it is designed to have a resistive/inductive output impedance. Inverters with capacitive output impedances offer the best overall performance among inverters with three different types of output impedances. It is possible to design the output capacitance to optimise the quality of the output voltage. This will be reported in Part II.

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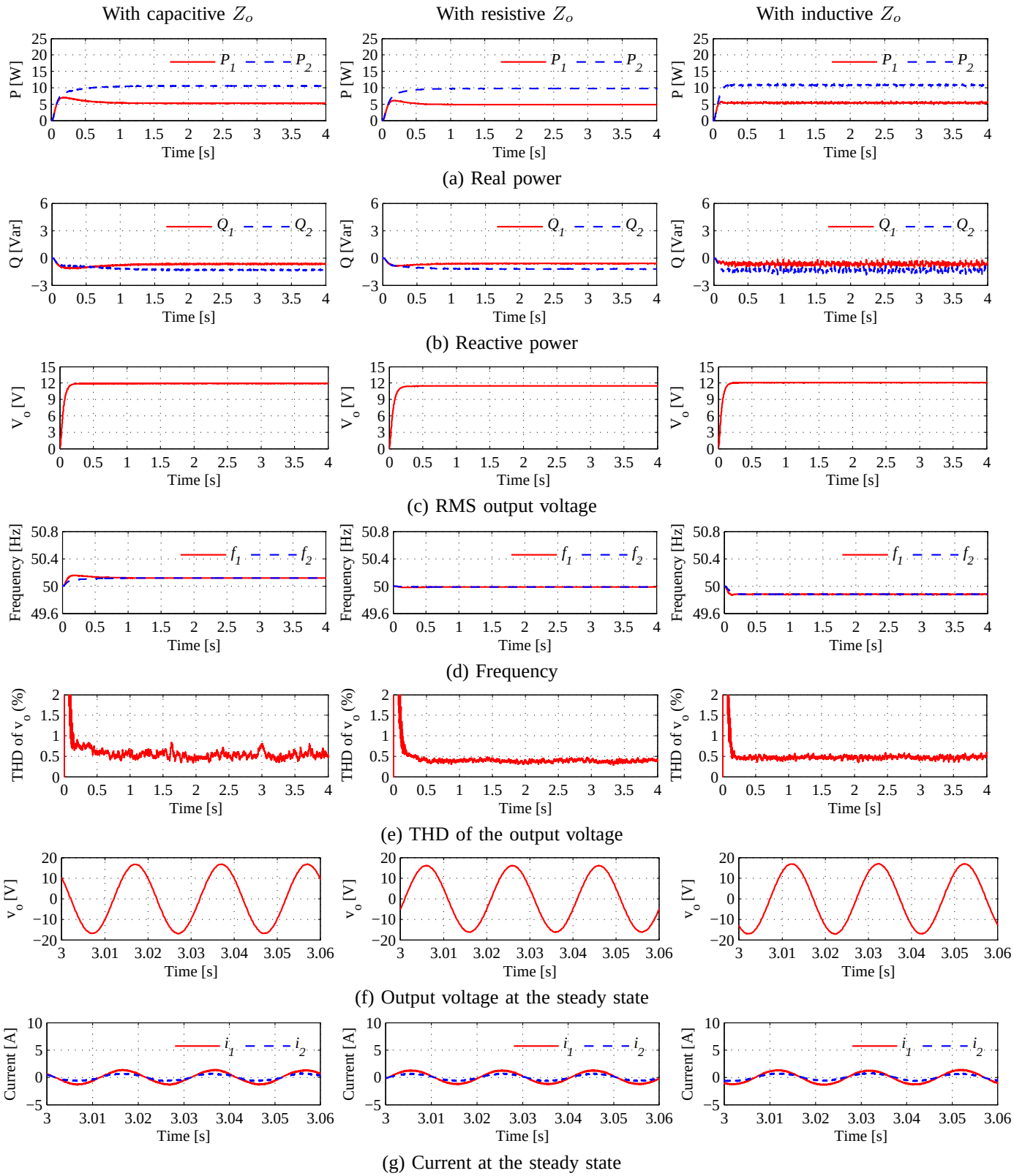

Figure 6. Simulation results for a linear load $R_L = 9\Omega$: using inverters with capacitive output impedances (left column), using inverters with resistive output impedances (middle column) and using inverters with inductive output impedances (right column).

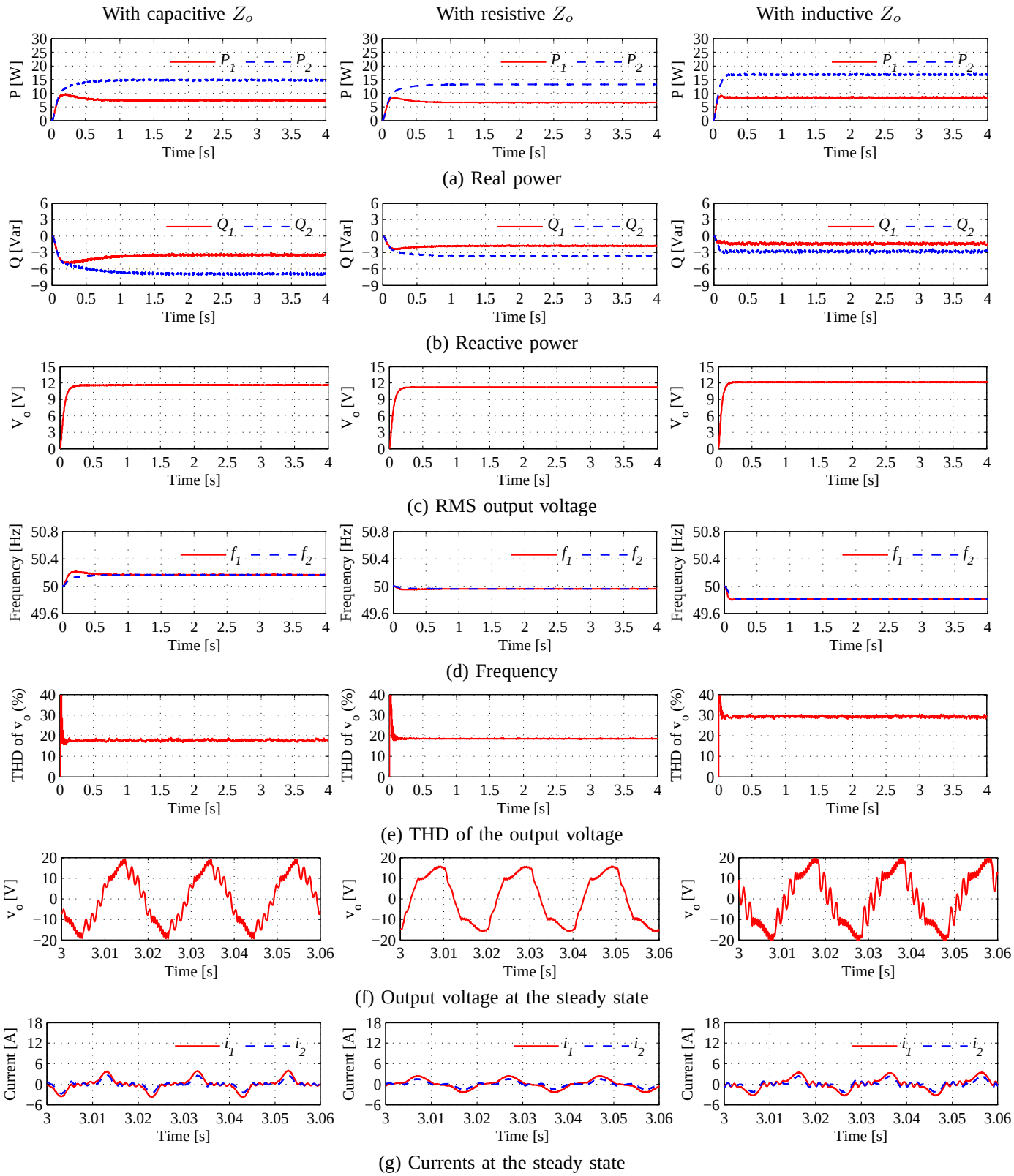

Figure 7. Simulation results for the nonlinear load: using inverters with capacitive output impedances (left column), using inverters with resistive output impedances (middle column) and using inverters with inductive output impedances (right column).

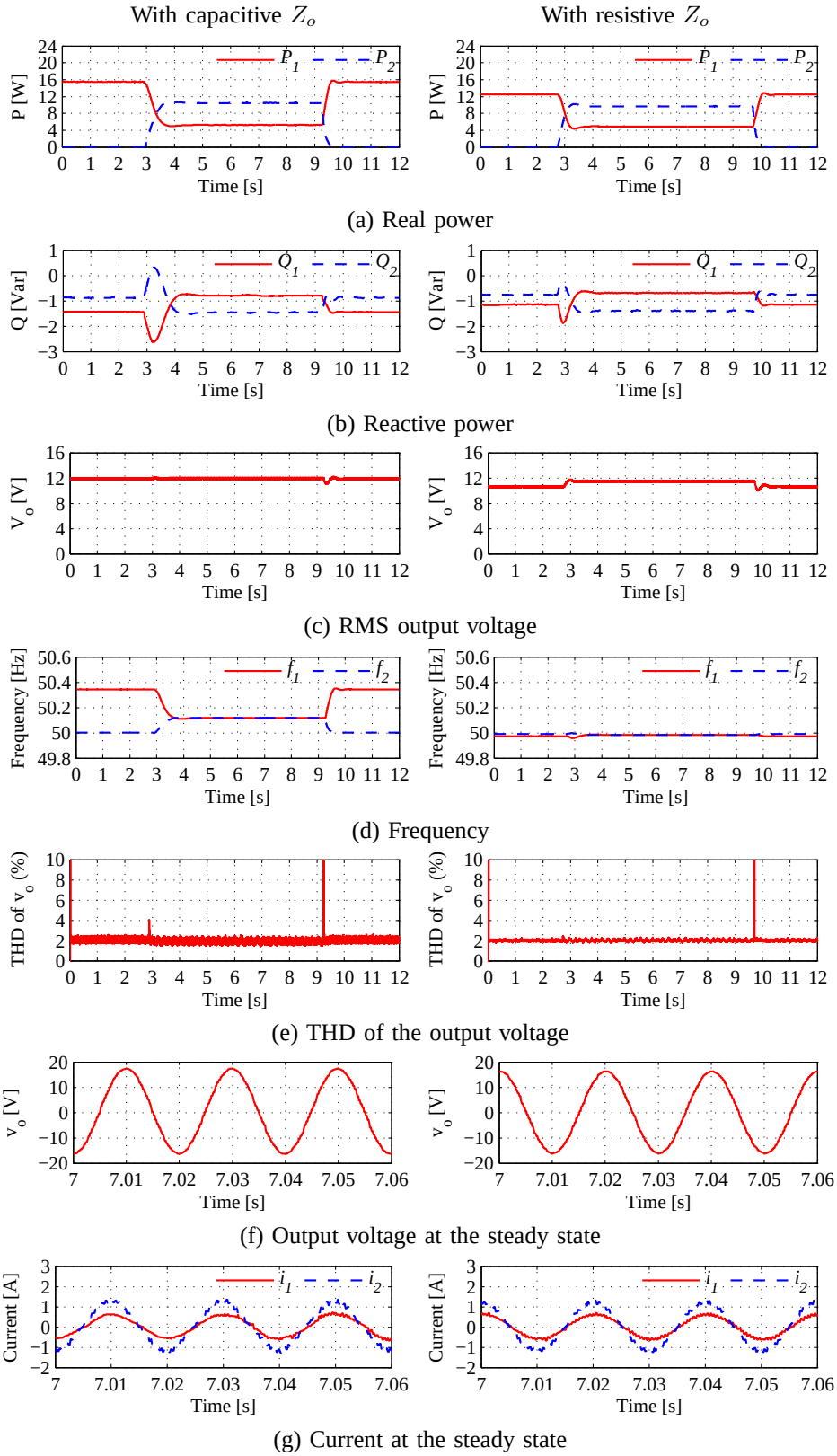

Figure 8. Experimental results for a linear load $R_L = 9\Omega$: using inverters with capacitive output impedances (left column) and using inverters with resistive output impedances (right column).

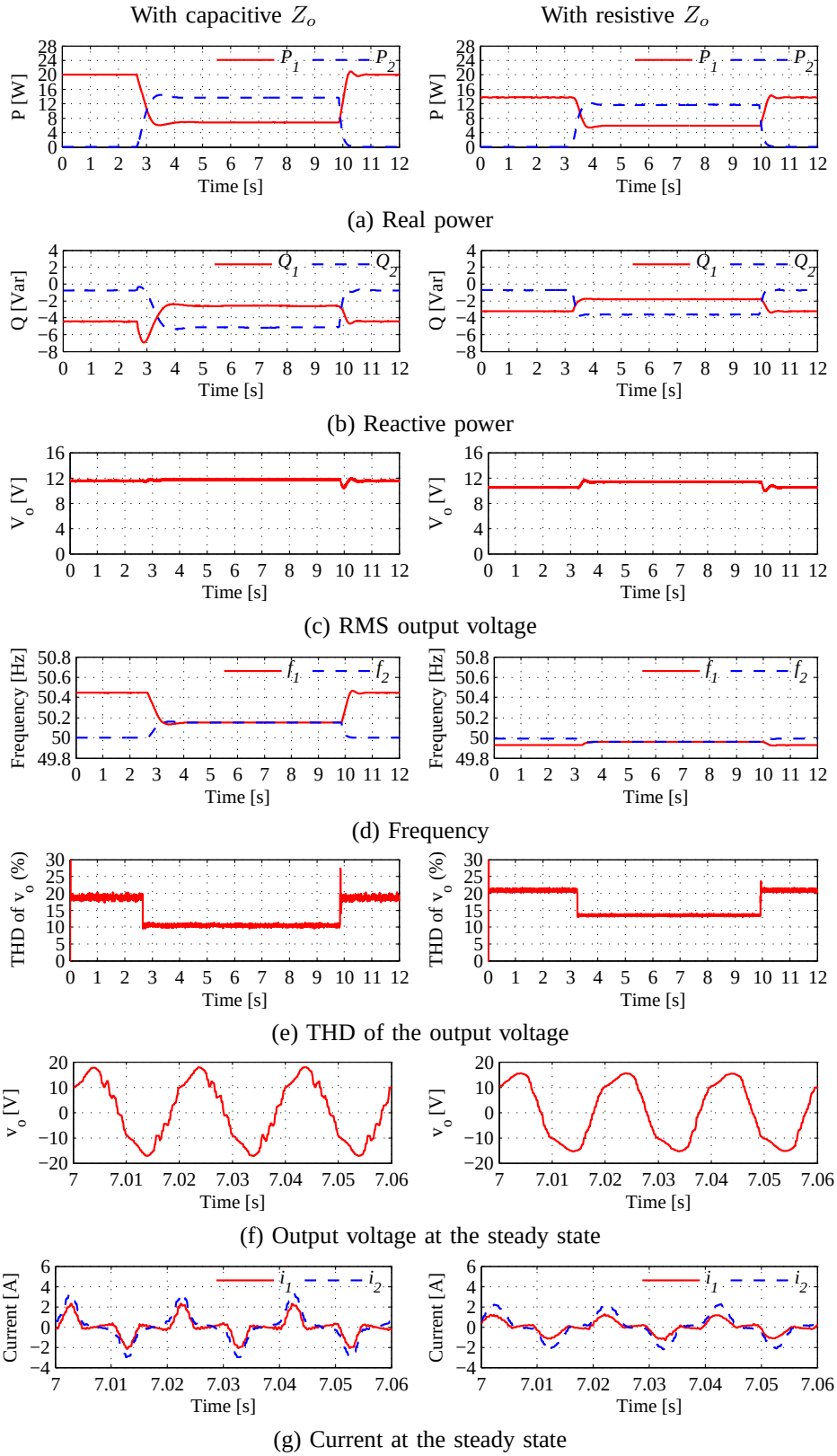

Figure 9. Experimental results for the nonlinear load: using inverters with capacitive output impedances (left column) and using inverters with resistive output impedances (right column).