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A Direct Power Conversion Topology for Grid Integrations of Hybrid AC/DC Resources

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***Abstract*—This paper proposes a multiple-input versatile matrix converter (VMC) to integrate hybrid ac/dc energy resources and storages to a power grid. The VMC is developed based on the indirect matrix converter (IMC) with its six-switch voltage source converter replaced by a nine-switch topology. The nine-switch converter can provide six input terminals for the connections of one three-phase ac source plus three dc sources to the grid. The three-phase utility grid is connected to the VMC's current source side. This configuration allows the input ac/dc sources' voltages lower than the grid voltage. The control and modulation schemes are proposed to extract the commanded current from the input ac/dc sources to the grid and guarantee high quality ac/dc inputs and ac output current waveforms with unity power factors. The proposed modulation scheme for sinusoidal outputs of the VMC is mathematically proved. The experimental results are provided to validate the effectiveness of the control and modulation schemes for the proposed VMC.**

***Keywords*- A versatile matrix converter, direct power conversion, grid integration, hybrid ac/dc sources.**

I. INTRODUCTION

As the development and deployment of distributed generation and microgrid in modern electric power industry, the integration of various energy resources and energy storage systems to a utility grid becomes a trend. Currently, the energy resources and storages can be categorized into two types based on their terminal output voltages. One is ac type, such as wind energy conversion system (WECS), diesel generator, micro turbine, flywheel energy storage system (FESS), and any other electric machine driven generation system. The other is dc type, for example, the photovoltaic (PV) panel, fuel cell (FC), battery and ultra-capacitor etc. High penetration of renewable power in a utility grid will cause voltage and frequency fluctuation due to intermittent and uncertainty characteristics of most renewable sources like wind and PV. To address this problem, different renewable sources can be integrated together to complement each other and provide relatively stable output power [1, 2]. Alternatively, renewable sources together with energy storages or dispatch-able generators can also level supply fluctuation to satisfy the grid codes.

Normally, an ac source needs a back-to-back ac/dc/ac converter for grid connection whereas a dc source needs a dc/dc boost converter as well as a dc/ac inverter for grid integration. The hybrid ac/dc sources can share their common grid-side inverter with properly designed capacity, but a separate dc/dc converter or dc/ac inverter is required for each source or storage. Therefore, it is expected to integrate multiple conversion systems with different functions into a compact converter to reduce the number of switches. The authors propose compact converter topologies for the application of PV and battery system which can save 25% semiconductors [3, 4]. However, an existing conversion system or the compact system needs a dc electrolytic capacitor to formulate two stages energy conversions for grid connection. This capacitor may cause premature failure and increase the size of the converter, it also requires sensor and control scheme for regulating its voltage to avoid damages caused by over-voltages.

To achieve one stage direct power conversion, matrix converters have attracted the attention of researchers for ac/ac conversion due to the absence of passive component in dc-link [5-11]. An indirect matrix converter (IMC) [8-11], which consists of rectifier/inverter with a fictitious dc-link is a good alternative due to its flexibility for topology extensions. The concept "fictitious dc-link" of IMC can also make it possible to achieve ac/dc "all-semiconductor" converter.

The main drawback of a matrix converter is the limited gain of 0.866 for input-to-output voltage transfer ratio and the complicated commutation issues. In applications like connection of renewable sources and energy storages to a grid, a converter only needs voltage boost function since the source voltage is usually lower than the utility grid voltage. Therefore, the input ac and dc sources can be connected to the voltage source side of an IMC to achieve voltage boost function without additional passive components or step-up transformer. This paper proposes a direct power conversion topology using a versatile matrix converter (VMC) to integrate hybrid ac/dc power sources into a utility grid. The six-switch voltage source converter of the IMC is replaced by a nine-switch topology in [12-14] to provide more terminals for the connections of multiple ac/dc sources. The modulation schemes for the VMC to produce dc inputs, sinusoidal input, and sinusoidal output currents are developed in this paper.

Carrier-based methodology is applied where the ac and dc

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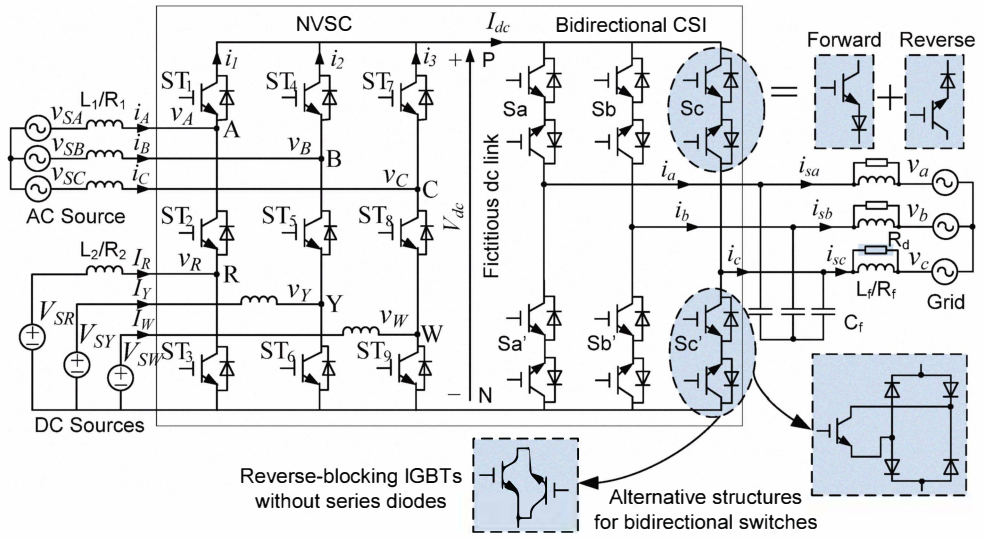


Fig. 1. The proposed VMC for the integration of one ac and three dc inputs.

modulation references share a common triangle carrier. In addition, the detailed control algorithms of the matrix converter to extract commanded power from the ac/dc sources are unveiled.

II. Topology and Modulation for the VMC

A. Topology

The VMC consists of a nine-switch voltage source converter (NVSC) and a bidirectional current source inverter (CSI), which are connected together by a fictitious dc-link as shown in Fig. 1. There are six input terminals for the connection of ac/dc sources and three ac output terminals for the VMC to be connected to a three-phase utility grid. The NVSC performs the same functions as one three-phase voltage source converter (VSC) and three dc/dc converters which share three common switches (ST_2, ST_5, ST_8). The bidirectional CSI provides current path for power flowing from input sources to grid and also from grid to the input sources if the sources like battery, ultra-capacitor, and low-speed flywheel can absorb power. The bidirectional switches in CSI are highlighted in Fig. 1, which can be treated as two sets of IGBT with series connection diode for the purpose of forward and reverse power flow operations respectively. Two alternative configurations for the bidirectional switches are also depicted in Fig. 1. One option is to use reverse blocking IGBTs, the other option is to use one IGBT plus four diodes. For safety operation, a clamp circuit consisting only of a diode and a capacitor mounted in the fictitious dc-link can absorb the magnetic energy stored in the source-side inductors when the converter has to be turned off during fault situations.

In Fig. 1, one three phase ac source and three dc sources are integrated into a grid through the VMC. The input ac/dc currents can track their own commands according to power dispatch order. It can be observed from the nine-switch topology that the middle switch ST_2 in the first leg is shared by upper ac/dc and lower dc/dc converters, and voltage v_R is always lower than voltage v_A [12-14]. The proposed VMC allows the low voltage input ac/dc sources to be connected to a relatively high grid voltage. The summation of ac and dc modulation indices must be less than or equal to 1. The terminal voltages of dc type storages like battery and ultra-capacitor are comparatively low due to their manufacture limitations. Therefore, low modulation indices are expected to produce high boost gains for dc/dc converters. Normally, the ac type source output voltage is always lower than the grid voltage, such as in a direct drive WECS. These characteristics make the proposed NVSC suitable for hybrid ac/dc and dc/dc applications. DC input currents, sinusoidal input and output currents under balanced ac supply and grid conditions can be achieved through coordinated modulation schemes for NVSC and CSI.

B. Modulation of CSI

As illustrated in Fig. 1, the CSI can impose a selected line voltage across the fictitious dc-link for further processing by the NVSC. There are six active states and three null states of the CSI as Shown in Fig. 2, where only ON switches are shown for each active state. Both the VSC and CSI have voltage boost function. Only modulation indices of VSC are regulated to cater to the required input-to-output transfer gain, the null states of the CSI will not be applied. Doing this can simplify the control system of the VMC. Taking sextant 1 ($-\pi/6 \le \theta_a \le \pi/6$) of the CSI as an example, v_{ab} and v_{ac}, corresponding to the two nearest active states of SC6 and SC1 respectively, are imposed to the fictitious dc-link. These active states SC6 and SC1 cause switch Sa to turn ON for the full switching period, hence clamping phase a to the upper dc rail. Distinction between the states SC6 and SC1 is introduced by modulating the lower switches (Sb' and Sc') so that the other two phases are alternately connected to the lower dc rail. The same interpretation can be applied to the other five sextants with only a small difference observed for the even sextants. Instead of positive rail clamping, even sextants clamp one phase to the lower dc-rail with the other two modulated to the upper dc rail in accordance to their computed duty ratios.

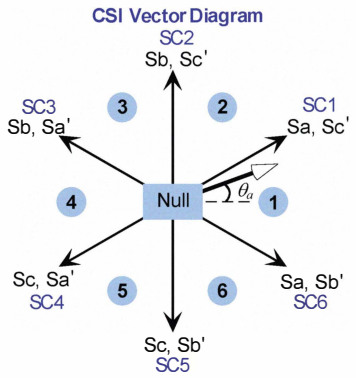


Fig. 2. Space vector representation of CSI.

Phase orientation of the CSI is synchronized with respect to the measured grid voltages, depending on the specified output power factor ϕ_o. In order to guarantee that the fictitious dc-link voltage v_{ab} and v_{ac} are no less than zero in sextant 1, the output power factor angle ϕ_o should be within the range from $-\pi/6$ to $\pi/6$. The corresponding active duty ratios (d_{o1} and d_{o2}) for the CSI in sextant 1 can be determined by first assuming the following three-phase current references (i_a^*, i_b^* and i_c^*):

$$\begin{aligned} i_a^* &= I_{om}\cos\theta_a \qquad i_b^* = I_{om}\cos\theta_b \qquad i_c^* = I_{om}\cos\theta_c \\ \theta_a &= \omega_o t \qquad\qquad \theta_b = \theta_a - 2\pi/3 \qquad \theta_c = \theta_a + 2\pi/3 \end{aligned} \tag{1}$$

where I_{om} is their common amplitude, and θ_a, θ_b and θ_c are their respective phase angles. Noting next that the sum of three-phase currents is zero, d_{o1} and d_{o2} can eventually be determined as:

$$\begin{aligned} &\cos\theta_a + \cos\theta_b + \cos\theta_c = 0, -\frac{\cos\theta_b}{\cos\theta_a} - \frac{\cos\theta_c}{\cos\theta_a} = 1 \\ &d_{o1} = -\cos\theta_b / \cos\theta_a \qquad d_{o2} = -\cos\theta_c / \cos\theta_a \end{aligned} \tag{2}$$

Equation (2), when multiplied by their associated output line voltages (v_{ab} and v_{ac}), gives the average dc-link voltage in (3) with V_{om} and ϕ_o representing the phase voltage amplitude and output power factor angle respectively.

$$V_{dc(av)} = d_{o1}v_{ab} + d_{o2}v_{ac} = \frac{3V_{om}}{2\cos\theta_a}\cdot\cos\phi_o, -\frac{\pi}{6} \le \theta_a \le \frac{\pi}{6} \tag{3}$$

The same mathematical procedure can be applied to the other five sextants with the generalized equations determined as:

$$\begin{aligned} V_{dc(av)} &= \frac{3V_{om}I_{om}}{2|i_{\max}|}\cdot\cos\phi_o, \qquad \textit{for positive rail clamping} \\ V_{dc(av)} &= \frac{3V_{om}I_{om}}{2|i_{\min}|}\cdot\cos\phi_o, \qquad \textit{for negative rail clamping} \end{aligned} \tag{4}$$

where $i_{max} = \max(i_a^*, i_b^*, i_c^*)$, and $i_{min} = \min(i_a^*, i_b^*, i_c^*)$. Equation (4) clearly states that the fictitious dc-link voltage is time-varying with its normalized variation over a fundamental period. The sixth order ripples must properly be compensated when modulating the NVSC so as to produce dc and sinusoidal input currents.

C. Modulation of NVSC

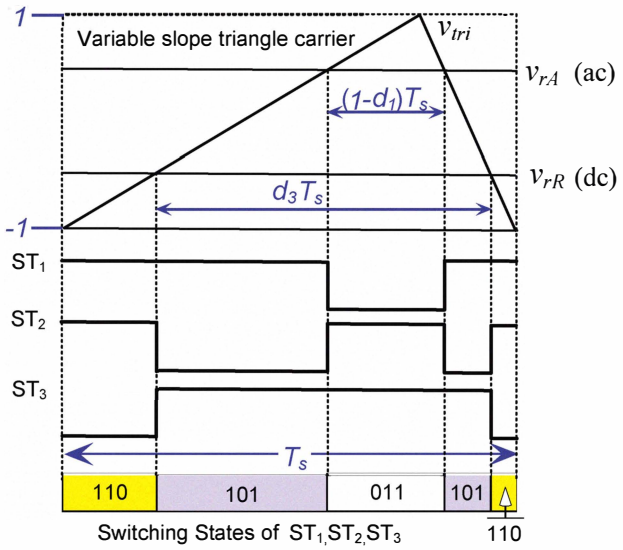


Fig. 3. PWM signal generation for leg one of the NVSC in a switching period.

Taking the first leg of the NVSC as an example, PWM signal ST_1 (ST_3) is generated through the comparison of upper ac (lower dc) reference and triangle carrier, and PWM signal ST_2 is generated by logic operation, $ST_2 = (ST_1)$ XOR (ST_3). The logic relationship is given in (5).

$$\begin{aligned} ST_1 &= \begin{cases} 1, & v_{rA} \ge v_{tri} \\ 0, & v_{rA} < v_{tri} \end{cases}, ST_3 = \begin{cases} 1, & v_{rR} \le v_{tri} \\ 0, & v_{rR} > v_{tri} \end{cases} \\ ST_2 &= ST_1 \oplus ST_3 \end{aligned} \tag{5}$$

where v_{rA} and v_{rR} are upper ac and lower dc modulation references respectively, and v_{rR} is always less than v_{rA}, v_{tri} is the common triangle carrier which has variable rising and falling slopes.

Fig. 3 shows the process of PWM gating signal generation for the first leg in one switching period. Parameters d_1 and d_3 are duty ratios for switches ST_1 and ST_3. Summarizing the constraint $v_{rA} > v_{rR}$ then leads to those three switching states per phase-leg, which also coincides with the state sequence for three signals ST_1, ST_2 and ST_3 as shown at the bottom of Fig. 3.

The NVSC performs the same function as one ac/dc rectifier and three dc/dc converters in parallel for hybrid input ac/dc sources. The upper and lower converters share the common fictitious dc-link whose average voltage has sixth order ripples. In order to guarantee good ac/dc input current waveforms without low order harmonics, the variable fictitious dc-link

voltage must be compensated. The normalized modified modulation references for ac input source are expressed in (6)

$$v_{rA} = \frac{m_i \cdot \cos(\omega_i t + \theta_A) + V_{off}}{V_{normdc(av)}/2} + V_{offup}$$
$$v_{rB} = \frac{m_i \cdot \cos(\omega_i t + \theta_B) + V_{off}}{V_{normdc(av)}/2} + V_{offup} \quad (6)$$
$$v_{rC} = \frac{m_i \cdot \cos(\omega_i t + \theta_C) + V_{off}}{V_{normdc(av)}/2} + V_{offup}$$
$$V_{off} = -0.5(\max(v_{rA}, v_{rB}, v_{rC}) + \min(v_{rA}, v_{rB}, v_{rC}))$$

where m_i, ω_i, θ_A are modulation index, angular frequency and phase angles for the input source voltage respectively, V_{off} is the triplen offset commonly added to gain an enhanced modulation indices [11], offset V_{offup} is used to lift the upper reference in order to prevent the upper and lower modulation references from intersecting each other. The same offsets V_{off} and V_{offup} are also added to phases B and C, so they can cancel each other in the line voltages to produce three-phase sinusoidal input currents.

The lower modulation reference for each leg of the NVSC is dc quantity with appropriate compensation. In order to produce dc input current without low order harmonics, the average value of converter terminal voltage v_R in Fig. 1 should contain only dc quantity, whose expression can be written as

$$v_R = (1 - d_3) \cdot V_{dc(av)} \quad (7)$$

The amplitude of the triangle carrier ranges from -1 to 1 and the duty ratio d_3 for ST_3 and corresponding voltage v_R can be calculated according to Fig. 3 as follow

$$d_3 = \frac{1 - v_{rR}}{2}$$
$$v_R = (1 - d_3) \cdot V_{dc(av)} = \frac{(1 + v_{rR})}{2} \cdot V_{dc(av)} \quad (8)$$

To make sure that voltage v_R is dc quantity without low order harmonics, the term $(1+v_{rR})/2$ should be expressed as:

$$\frac{1 + v_{rR}}{2} = \frac{m_R}{V_{normdc(av)}} \quad (9)$$

The term m_R is a dc quantity obtained from the input dc current closed-loop control as discussed in the later section. Therefore, the compensated dc modulation reference v_{rR} can be deduced in equation (10)

$$v_{rR} = \frac{m_R}{V_{normdc(av)}/2} - 1 \quad (10)$$

D. State Sequences Implementation for CSI and NVSC

The NVSC PWM generation must be synchronized with the CSI switching, so as to produce sinusoidal output currents for the overall matrix converter. The modulation arrangement and state sequences for all the three-phase upper ac and three lower dc references as shown in Fig. 4 are provided to ensure that each state of the NVSC will be divided proportionally to the two state durations of CSI. The main intention here is to force each triangular rising or falling edge to span a complete CSI switching state duration, expressed as $d_{o1}T_S$ and $d_{o2}T_S$, within the period T_S of the carrier. Therefore, the dc-link current I_{dc} is also divided proportionally to d_{o1} and d_{o2} to match with the modulation of the CSI. Taking sextant 1 of the CSI as an example, the current ratio of phase b to phase c i_b/i_c is equal to d_{o1}/d_{o2} as shown in equation (2). If the dc-link current contains $\cos\theta_a$, three-phase sinusoidal output currents for CSI can be guaranteed. Mathematical proof for sinusoidal output currents of CSI can be found in [15].

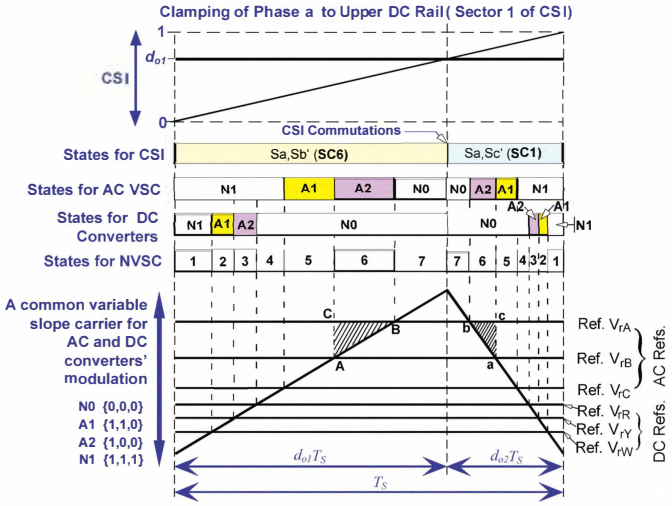


Fig. 4. Reference-carrier arrangement and state sequence for the proposed VMC

III. Control Algorithms for The VMC

A. Control Algorithm for the Upper AC VSC

The ac input source can operate at different frequency from the utility grid frequency, and its voltage is lower than the grid voltage. Unlike two stages ac/dc/ac conversion system, this direct power conversion does not have a dc-link capacitor, and hence does not need any dc-link voltage regulation. To achieve good control performances, the commanded active power should be extracted from the input ac source. Reactive power regulation remains separated for the input ac source and output grid. Unity input power factor is always set as the control objective for input ac source. Reactive power to the grid can also be adjusted by setting the output power factor angle ϕ_o appropriately. Caution must be taken to ensure that the increase in ϕ_o is not excessive since it has its own range from $-\pi/6$ to $\pi/6$, and it will lead to a decrease in dc-link voltage according to (4). Unity output power factor can be achieved by setting ϕ_o to be zero, thus the CSI three-phase current modulation references (i_a^*, i_b^* and i_c^*) are in phase with the measured grid voltages (v_a, v_b, v_c). Equations (11) and (12)

show the input voltage equations of the upper converter in ABC and *d-q* coordinates respectively:

$$L_1 \frac{d}{dt}\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} + R_1 \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} v_{SA} \\ v_{SB} \\ v_{SC} \end{bmatrix} - \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} \tag{11}$$

$$L_1 \frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -R_1 & \omega_i L_1 \\ -\omega_i L_1 & -R_1 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} - \begin{bmatrix} v_d \\ v_q \end{bmatrix} \tag{12}$$

The input current tracking of the upper VSC can be accurately achieved through the proportional and integral (PI) control in synchronous rotation frame through *dq* transformation. The control diagram for grid integration of ac source in the VMC is shown in Fig. 5. Two PI controllers are used for active and reactive currents control respectively. For unity input power factor, the reactive current reference i^*_q is set to be zero, and the commanded active current i^*_d is decided by the power dispatch order. Three phase modulation references for the VSC gating signals are obtained through dq/ABC transformation after the PI control processing. The dc-link compensation is implemented according to equation (6) and offset V_{offup} is used to lift the upper reference in the control loop to avoid intersecting with the lower dc references. The grid voltages (v_a, v_b, v_c) are sensed to produce current modulation references (i_a^*, i_b^* and i_c^*) with specified angle ϕ_o. The CSI gating signals can be generated based on the sector information and duty cycles d_{o1}, d_{o2}. Moreover, normalized fictitious dc-link variation and variable slope triangle can be produced for gating signal generation of VSC.

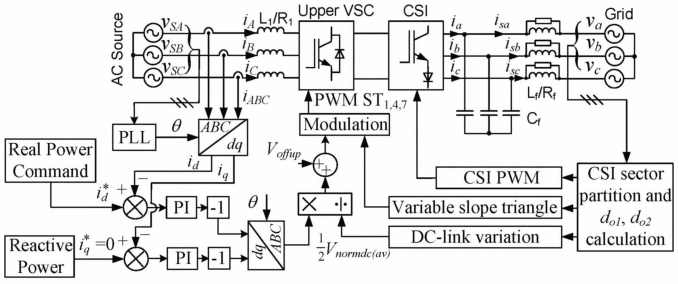


Fig. 5. Control block diagram of the VMC for integration of ac source

B. Control Algorithm for the Lower DC Converters

Compared with the control objectives for the upper ac VSC, the control for lower dc converters are much simpler due to the lack of synchronization and reactive power control issues. The power from the dc source is the only control objective. The voltage equation for the first leg of the lower VSC is:

$$V_{SR} - v_R = L_2 \cdot dI_R / dt + R_2 \cdot I_R \tag{13}$$

The control algorithms for one of the three dc/dc converters are depicted in Fig. 6. The current reference I_{Rref} is a dc quantity, so a PI controller is used to accurately track the current command. The term m_R is a dc quantity with only switching frequency variations obtained from the input dc current closed-loop control. The dc-link variation should also be compensated with additional offset -1 according to equation (10) to produce the final modulation reference v_{rR}, which can eventually eliminate the low order harmonics of the dc input current.

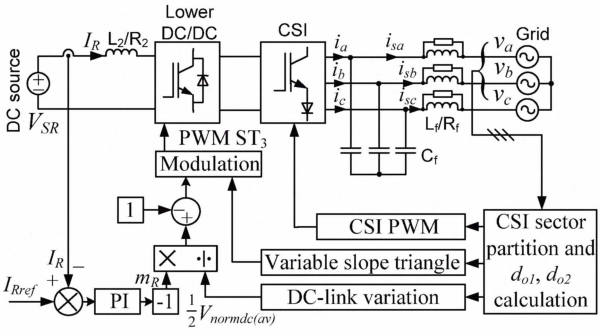


Fig. 6. Control block diagram of the VMC for integration dc source

C. Potential Applications for the proposed VMC

The VMC with hybrid ac/dc input sources can be applied in wind energy generation system and energy storage system. One example is for grid integrations of direct drive WECS using permanent magnet synchronous generator (PMSG) with hybrid battery/ultra-capacitor energy storages. Another example is for grid integrations of pure energy storage systems, inclusive of ac type low-speed flywheel and dc storages like hybrid battery/ultra-capacitor.

IV. Experimental Results

A laboratory prototype for the proposed VMC was built for experimental test. The modulation and control algorithms of the VMC are implemented together by Dspace controller and FPGA. The frequency and voltage of the three-phase ac input source are 40Hz/ 50V (phase rms). The dc input source is connected to terminal R and its voltage is 55V. Only one dc source is connected to the system due to the limitation of hardware condition. The grid frequency and voltage are 50Hz/100V (phase rms). The parameters of L_1/R_1, L_2/R_2, L_f/R_f and C_f in Fig. 1 are 6.3mH/0.3Ω, 10mH/0.3Ω, 3mH/0.2Ω and 40μF respectively. A 20Ω damping resistance R_d is connected in parallel with inductor L_f.

Fig. 7 shows various waveforms for the input ac VSC. The commanded 4A input current amplitude is tracked successfully with unity input power factor for the ac source. Fig. 8 shows the input ac/dc currents and output grid current, the dc current is controlled to be 4A as commanded.

Fig. 9 shows that the current injection into grid is sinusoidal with, the unfiltered current i_a is in phase with voltage v_a to show unity output power factor. The amplitude of output grid current is observed to be 3.4A. Phase difference between v_a and i_{sa} is contributed by the filter capacitor C_f. The capacitor current remains unchanged for a fixed grid voltage, so its influence becomes comparably smaller as i_{sa} increases.

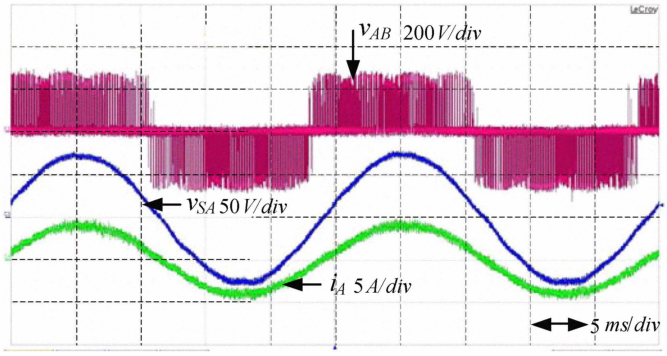


Fig. 7. Waveforms of ac input line voltage, ac phase voltage and phase current.

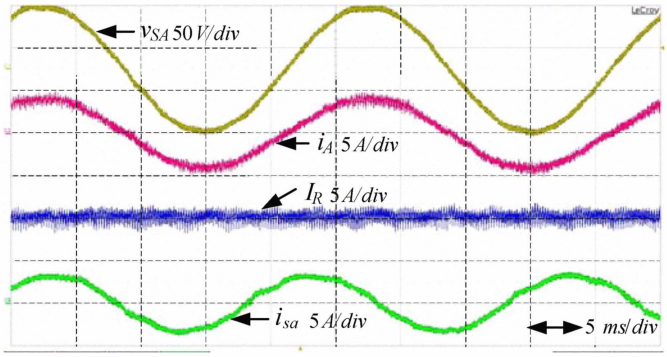


Fig. 8. Waveforms of ac source phase voltage/phase current, dc source current and grid current.

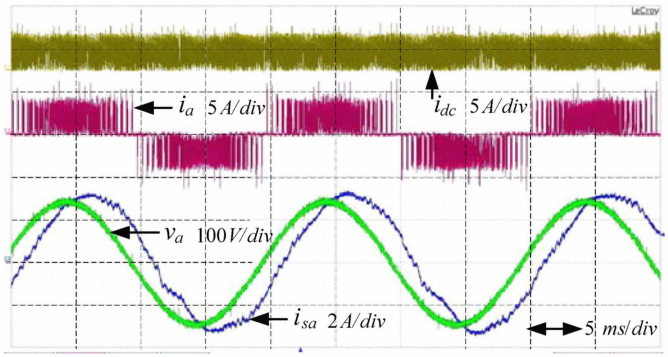
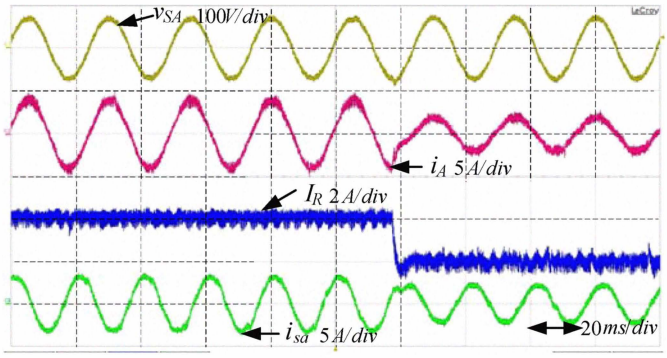
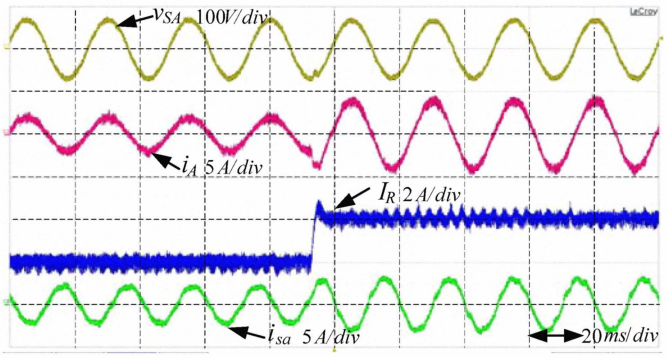


Fig. 9. Waveforms of fictitious dc-link current, unfiltered current, grid phase voltage and filtered grid current.



(a)



(b)

Fig. 10. Dynamic response of ac/dc input currents and grid current during (a) power decreasing; (b) power increasing.

Fig. 10(a) and (b) show the dynamic responses of the two ac/dc source input currents and output current to the grid when the input current amplitude commands are decreased from 4A to 2A and increased from 2A to 4A respectively. It can be seen that both the ac and dc input current can track their commands, unity input power factors are maintained for the input ac source. The output current decreases and increases accordingly.

V. CONCLUSION

A versatile matrix converter to integrate hybrid ac/dc input sources into a utility grid is proposed in this paper. The converter is based on an indirect matrix converter and a nine-switch converter where the input ac/dc sources are connected to the voltage source side and the output grid voltages are connected to the current source side. Operation in such configuration makes the converter have input-to-output voltage boost function. The modulation schemes are proposed for the converter to perform sinusoidal ac input, dc inputs and sinusoidal output waveforms. The control algorithms of the converter for grid integrations of one input ac source as well as three input dc sources are investigated. Experimental results show that the converter performs well under the proposed control and modulation algorithms.

REFERENCES

[1] M. Datta, T. Senjyu, A. Yona, T. Funabashi, and K. Chul-Hwan, "A Coordinated Control Method for Leveling PV Output Power Fluctuations of PV-Diesel Hybrid Systems Connected to Isolated Power Utility," *IEEE Trans. on Energy Conversion,* vol. 24, no. 1, pp. 153-162, Mar. 2009.

[2] K. Seul-Ki, J. Jin-Hong, C. Chang-Hee, A. Jong-Bo, and K. Sae-Hyuk, "Dynamic Modeling and Control of a Grid-Connected Hybrid Generation System With Versatile Power Transfer," *IEEE Trans. on Industrial Electronics,* vol. 55, no. 4, pp. 1677-1688, Apr. 2008.

[3] P. C. Loh, L. Zhang, S. He, and F. Gao, "Compact integrated solar energy generation systems," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, pp. 350-356.

[4] X. Liu, P. Wang, P. C. Loh, F. Blaabjerg and F. Gao, "A Compact Seven Switches Topology and Reduced DC-Link Capacitor Size for Single-Phase Stand-Alone PV System with Hybrid Energy Storages" in *IEEE Applied Power Electronics Conference and Exposition (APEC),* pp. 1920-1925, Fort Worth, Texas USA, 2011.

[5] C. Klumpner, F. Blaabjerg, I. Boldea, and P. Nielsen, "New modulation method for matrix converters," *IEEE Trans. on Industry Applications,* vol. 42, no. 3, pp. 797-806, May. 2006.

[6] H. M. Nguyen, H. H. Lee, and T. W. Chun, "Input Power Factor Compensation Algorithms Using a New Direct-SVM Method for Matrix Converter," *IEEE Trans. on Industrial Electronics,* vol. 58, no. 1, pp. 232-243, Jan. 2011.

[7] L. Helle, K. B. Larsen, A. H. Jorgensen, S. Munk-Nielsen, and F. Blaabjerg, "Evaluation of modulation schemes for three-phase to three phase matrix converters," *IEEE Trans. on Industrial Electronics*, vol. 51, no. 1, pp. 158–171, Feb. 2004.

[8] B. Wang and G. Venkataramanan, "A carrier-based PWM algorithm for indirect matrix converters," in *Proc. IEEE-PESC 2006*, pp. 2780–2787.

[9] X. Liu, P. Wang, P. C. Loh and F. Blaabjerg, "A Compact Three-Phase Single Input/Dual Outputs Matrix Converter" *IEEE Trans. on Industrial Electronics,* vol. 59, no. 1, pp. 6-16, Jan. 2012.

[10] L. Wei, T. A. Lipo, and H. Chan, "Matrix converter topologies with reduced number of switches," in *PESC Record - IEEE Annual Power Electronics Specialists Conference*, 2002, pp. 57-63.

[11] P. C. Loh, R. J. Rong, F. Blaabjerg, and P. Wang, "Digital Carrier Modulation and Sampling Issues of Matrix Converters," *IEEE Transactions on Power Electronics,* vol. 24, no. 7 pp. 1690-1700, Jul. 2009.

[12] C. Liu, B, Wu, N. R. Zargari and D. Xu, "A novel nine-switch PWM rectifier-inverter topology for three-phase UPS applications," in *Proc. IEEE-EPE'07*, pp.1-10, 2007.

[13] C. Liu, B. Wu, N. Zargari and D. Xu, "A novel three-phase three leg AC/AC converter using nine IGBTs", *IEEE Trans. on Power Electronics,* vol. 24, pp. 1151-1160, 2009.

[14] F. Gao, L. Zhang, D. Li, P. C. Loh, Y. Tang, and H. Gao, "Optimal pulsewidth modulation of nine-switch converter," *IEEE Trans. on Power Electronics,* vol. 25, no. 9, pp. 2331-2343, Sep. 2010.

[15] X. Liu, P. C. Loh, P. Wang, and F. Blaabjerg, "A Compact Versatile Matrix Converter to Integrate Various Energy Resources to Utility Network" in IEEE Energy Conversion Congress & Exposition (ECCE), USA, pp. 238-245,2011.