Modulation, Losses, and Semiconductor Requirements of Modular Multilevel Converters

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***Abstract*—This paper describes the operation of modular multilevel converter, an emerging and highly attractive topology for medium- and high-voltage applications. A new pulsewidth-modulation (PWM) scheme for an arbitrary number of voltage levels is introduced and evaluated. On the basis of this PWM scheme, the semiconductor losses are calculated, and the loss distribution is illustrated.**

***Index Terms*—Losses, modulation, multilevel systems, pulsewidth modulation (PWM), pulsewidth-modulated power converter.**

I. Introduction

MEDIUM-VOLTAGE (MV) power electronics is a technology of continuously growing importance for industrial and traction applications as well as regenerative energy sources. Substantial system advantages such as increased availability due to ride-through capability and/or a redundant converter design, drastically improved dynamic performance, extended operating range, reduced line harmonics, and adjustable power factor at the point of common coupling are the reasons, therefore, that pulsewidth-modulation (PWM) converters on the basis of insulated-gate bipolar transistors (IGBTs) and integrated gate-commutated thyristors have replaced thyristor-based converters in a wide range of applications [1]–[3]. Cycloconverters, grid-commutated converters, or load-commutated converters applying conventional thyristors (e.g., load-commutated converters) are used particularly in applications with very high power demands, which cannot be met with state-of-the-art self-commutated converters at comparable prices [1], [2]. Considering PWM converters, voltage-source-converter (VSC) topologies clearly dominate as compared to current-source converters which are offered by one manufacturer only [3]. The majority of manufacturers offer VSCs with a different number of output voltage levels. Aside from the well-known two-level VSC (2L-VSC), there are three-level neutral-point-clamped VSCs (3L-NPC-VSCs), four-level flying-capacitor VSCs (4L-FLC-VSCs), multilevel H-Bridge VSCs (ML-HB-VSC), and ML series-connected HB VSCs (ML-SCHB-VSCs, e.g., 5L-SCHB-VSCs, 7L-SCHB-VSCs, and 9L-SCHB-VSCs) available. All these topologies feature special advantages and disadvantages which enable their existence on the market in certain power and voltage ranges as well as application segments (e.g., [1], [2], and [4]–[8]). Modulation strategies for these topologies are investigated, e.g., in [9]–[13].

The modular multilevel converter (M2C) was first introduced in 2001 [14].

The topology features the following advantages:

1) distributed location of capacitive energy storages;
2) modular design;
3) simple voltage scaling by a series connection of cells;
4) filterless configuration for standard machines or grid converters [high-level number, low total harmonic distortion (THD)];
5) high resulting switching frequency;
6) simple realization of redundancy;
7) high front-end flexibility (e.g., 12p, 18p, 24p diode or active);
8) grid connection via standard transformer or transformerless;
9) possibility of common dc bus configurations for multidrive and high-power applications.

Disadvantages of the converter are the higher number of semiconductors and gate units. Furthermore, the total stored energy of the distributed capacitors is distinctly higher as compared to that of a conventional 2L-VSC or 3L-NPC-VSC [3], [15], [16].

Due to its interesting characteristics, the topology is very attractive for high-voltage dc transmission (e.g., HVDC PLUS [17]), flexible ac transmission systems, and MV converters [18]–[22]. So far, space-vector-modulation schemes [15], [23] and PWM schemes [24] have been introduced, and first experimental results have verified the function of the converter [25]–[28]. A comparison of the semiconductor power losses of the 2L-VSC and the M2C of the basis of a generalized analytical method is given in [29]. A simplified HVDC model developed for modeling the steady-state and the dynamic behaviors of the M2C is investigated in [30]. This paper describes a new PWM scheme on the basis of the principles introduced in [15] and [23]. The semiconductor current rating, losses, and the semiconductor loss distribution are determined for an MV converter family with rated voltages of 2.3, 3.3, 4.16, 6.0, and 7.2 kV.

The structure of the M2C is shown in Fig. 1 (marked with the red dashed rectangle). Considering the converter structure, it combines elements of both the ML-SCHB-VSC and the

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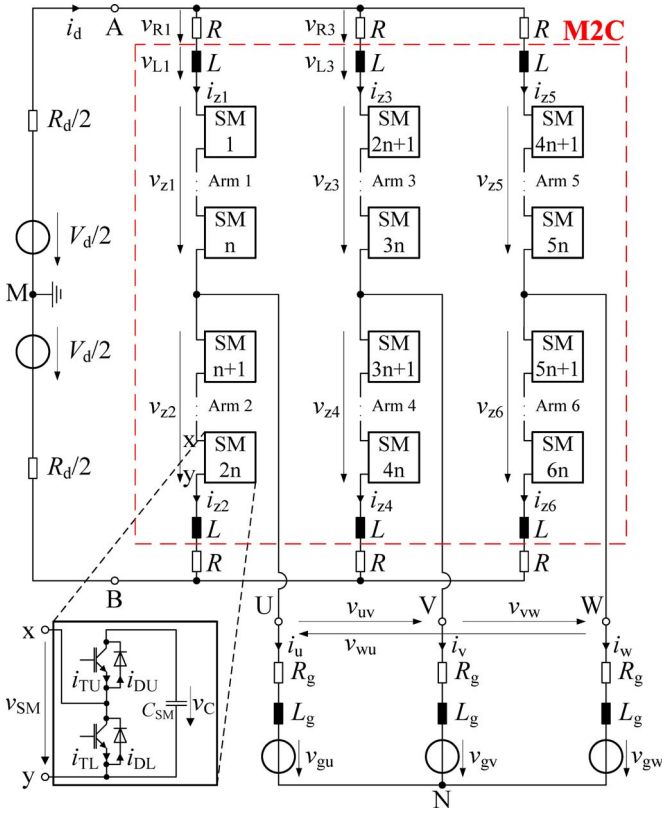

Fig. 1. Simulation model for the M2C.

FLC-VSC. The converter consists of six arms, each of which contains a series connection of n cells (resembles an ML-SCHB-VSC) and an inductor L. Each cell (also referred to as submodule) contains a half-bridge of two IGBTs and a capacitor $C_{\rm SM}$.

Capacitor $C_{\rm SM}$ is loaded with voltage $v_C(t)$ that is influenced by the phase current (resembles an FLC-VSC), which flows through the three-phase load (U, V, W). Each cell (submodule) can be toggled between two different states: the ON-state when the upper IGBT is switched on and the lower one is switched off, and the OFF-state when the lower IGBT is switched on and the upper one is switched off. With these states, cell terminal voltage $v_{\rm SM}(t)$ (from terminal x to y) can be toggled between $v_{\rm SM}(t) = v_C(t)$ (ON-state) and $v_{\rm SM}(t) = 0$ (OFF-state).

In this way, the series connection of n cells per arm can be used as a discrete-leveled voltage source. If r cells of n are in the ON-state (with $0 \le r \le n$), the sum voltage of these r capacitor voltages is generated between the points x and U (phase U).

II. Operation and Modulation of M2C

A simulation model for the M2C is shown in Fig. 1. The dc side (between points A and B) is modeled by two dc voltage sources $V_d/2$ and two resistors $R_d/2$. The three-phase ac side (at the terminals U, V, and W) is modeled by a series connection of resistor R_g, inductor L_g, and ac voltage source $v_{gu}(t)$ (phase U). This realization represents, e.g., a three-phase supply grid or an electrical machine. The IGBTs in the submodules are replaced by ideal switches. The parasitic ohmic losses in each arm are represented by a resistor R. With this model, the principle operation and modulation of the M2C will be described.

TABLE I
Phase Angle ϕ_{zk} of the Reference Arm Voltage $v_{zk,\rm ref}(t)$

	U	V	W
upper arm	$\phi_{z1} = +\frac{5}{6}\pi$	$\phi_{z3} = +\frac{1}{6}\pi$	$\phi_{z5} = -\frac{1}{2}\pi$
lower arm	$\phi_{z2} = -\frac{1}{6}\pi$	$\phi_{z4} = -\frac{5}{6}\pi$	$\phi_{z6} = +\frac{1}{2}\pi$

A. Generation of Pulse Patterns

The instantaneous line-to-line voltage on the drive terminals is dictated by the difference of the generated arm voltages of the two corresponding arms (e.g., $v_{uv}(t) \approx v_{z3}(t) - v_{z1}(t)$, Fig. 1). Voltage drops across the series resistors R and inductors L [$v_{R1}(t)$, $v_{L1}(t)$ and $v_{R3}(t)$, $v_{L3}(t)$] are neglected in the first step. To achieve a sinusoidal line-to-line voltage, reference voltages

$$v_{zk,\rm ref}(t) = \frac{V_d}{2} + m\frac{V_d}{2}\sin(\omega t + \phi_{zk}) + \frac{1}{6}m\frac{V_d}{2}\sin\left(3\left(\omega t + \phi_{zk}\right)\right), \quad \text{with } k = 1, 2, \ldots, 6 \tag{1}$$

are used with phase angles, as shown in Table I, where k represents the corresponding converter arm, m is the modulation index ($0 \le m \le 2/\sqrt{3}$), and ω is the angular frequency of the ac drive. A third harmonic component is included to increase the fundamental of the line-to-line converter voltages at the border of the linear-modulation range for a given dc voltage V_d. As shown in (1), the sum of the upper and lower reference voltages of a leg is V_d.

Reference voltage $v_{zk,\rm ref}(t)$ is shown in Fig. 2(a). The time axis is divided into time intervals of duration $T_{\rm PWM}$, the so-called PWM period. In each PWM period interval, the average of the reference arm voltage is calculated by using (1) as

$$V_{zk,\rm AV} = \frac{1}{t_b - t_a}\int_{t_a}^{t_b} v_{zk,\rm ref}(\tau)d\tau \tag{2}$$

$$= \frac{V_d}{2} + m\frac{V_d}{2}\frac{\sin\left(\omega\frac{t_b - t_a}{2}\right)}{\omega\frac{t_b - t_a}{2}} \cdot \sin\left(\omega\frac{t_a + t_b}{2} + \phi_{zk}\right) + \frac{1}{6}m\frac{V_d}{2} \cdot \frac{\sin\left(3\omega\frac{t_b - t_a}{2}\right)}{3\omega\frac{t_b - t_a}{2}}\sin\left(3\omega\frac{t_a + t_b}{2} + 3\phi_{zk}\right). \tag{3}$$

With the assumption of constant cell capacitor voltage $v_C(t) = V_d/n$, the arm voltage $v_{zk}(t)$ can be set to one of $n+1$ discrete voltage levels $(0, V_d/2, \ldots, n(V_d/2))$. In Fig. 2(b), the pulsewidth-modulated voltage $v_{zk,\rm PWM}(t)$ is set such as to have the same average value in each PWM period as the average voltage $v_{zk,\rm AV}(t)$ as calculated by (3). In each PWM period, the average voltage lies between two discrete voltage levels $V_{zk,\rm low}$ and $V_{zk,\rm high}$ [shown in Fig. 2(b)]. For example, in the PWM period between t_a and t_b, the lower discrete voltage

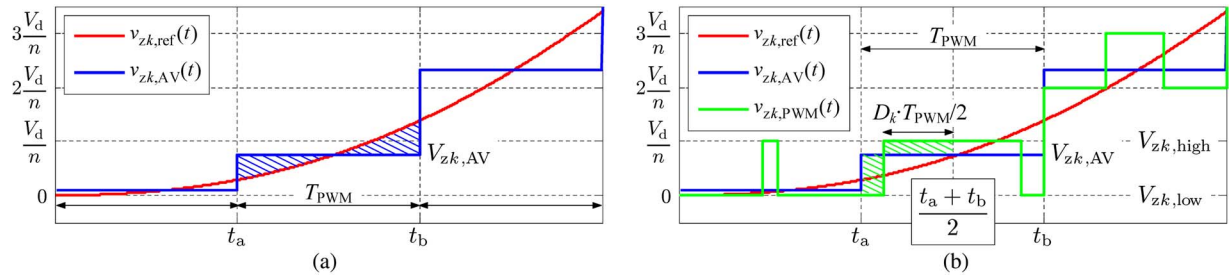

Fig. 2. Generation of pulse patterns within a PWM period interval. (a) Average voltage $v_{zk,\mathrm{AV}}$. (b) Pulsewidth-modulated voltage $v_{zk,\mathrm{PWM}}(t)$.

level is $V_{zk,\mathrm{low}} = 0$, and the higher one is $V_{zk,\mathrm{high}} = (V_d/n)$. These discrete voltage levels can be calculated with (3)

$$V_{zk,\mathrm{low}} = \left\lfloor \frac{V_{zk,\mathrm{AV}}}{\frac{V_d}{n}} \right\rfloor \cdot \frac{V_d}{n} \tag{4}$$

$$V_{zk,\mathrm{high}} = V_{zk,\mathrm{low}} + \frac{V_d}{n} \tag{5}$$

where $\lfloor x \rfloor$ stands for the floor function whose value is the largest integer that is less than or equal to x. The duty cycle of the modulated submodule in each arm D_k, as shown in Fig. 2(b), can be calculated with the approach that the hatched surface areas of the rectangles have the same value

$$(1 - D_k)\frac{T_{\mathrm{PWM}}}{2}(V_{zk,\mathrm{AV}} - V_{zk,\mathrm{low}}) = D_k \frac{T_{\mathrm{PWM}}}{2}(V_{zk,\mathrm{high}} - V_{zk,\mathrm{AV}}). \tag{6}$$

When (6) is solved for D_k, the result is

$$D_k = \frac{V_{zk,\mathrm{AV}} - V_{zk,\mathrm{low}}}{V_{zk,\mathrm{high}} - V_{zk,\mathrm{low}}}. \tag{7}$$

With the use of (4) and (5) in (7), the duty cycle D_k can be calculated with

$$D_k = \frac{V_{zk,\mathrm{AV}}}{\frac{V_d}{n}} - \left\lfloor \frac{V_{zk,\mathrm{AV}}}{\frac{V_d}{n}} \right\rfloor = \mathrm{mod}\left(V_{zk,\mathrm{AV}}\frac{n}{V_d}, 1\right) \tag{8}$$

where $\mathrm{mod}(x, 1)$ calculates the fractional part of x. In each arm and during each PWM period, there are some submodules that are permanently in the ON-state; one submodule (the so-called PWM submodule) is switched with the duty cycle calculated with (8), and the rest of the submodules are permanently in the OFF-state. As an example, in the PWM period between t_a and t_b in Fig. 2(b), there are no submodules in the ON-state, one PWM submodule, and $(n-1)$ submodules in the OFF-state. The number of submodules that are permanently on and off is calculated by

$$\mathrm{SM}_{\mathrm{on}k} = \left\lfloor \frac{V_{zk,\mathrm{AV}}}{\frac{V_d}{n}} \right\rfloor \tag{9}$$

$$\mathrm{SM}_{\mathrm{off}k} = n - (\mathrm{SM}_{\mathrm{on}k} + 1) \tag{10}$$

where n is the number of submodules per arm. The two PWM submodules of the upper and lower arms within one phase (e.g., arms 1 and 2) are switched complementarily to one another, such that, in every point of time, n submodules of the $2n$ submodules of one phase are on.

B. Selection of Submodules

With the generation of pulse patterns, only the number of submodules that are on is determined, and not specifically which submodules are on, off, and PWM switched. Initially, the series-connected submodules appear to be equivalent due to their series connection. However, conditions arise that dictate which individual submodules should be assigned which roles (on, off, or PWM switched). There are two criteria to select the ON-state submodules and the PWM submodule of each arm: 1) capacitor voltages and 2) sign of the arm currents. Selection of the submodules will be used to balance the capacitor voltages. If a submodule is on, the arm current of the arm in which the submodule lies flows through the capacitor of the submodule. For positive arm current, the capacitor voltage increases, and the capacitor will be charged. When the arm current is negative, the capacitor voltage decreases, and the capacitor will be discharged. If a submodule is off, the arm current flows through the lower IGBT, and the capacitor voltage remains constant.

With these basic facts, a general selection algorithm can be derived. For each PWM period, the capacitor voltages of each arm are measured, listed, and sorted in ascending order. The sign of the arm current and the number of submodules that are permanently on dictate which submodules will be selected. If the arm current is positive (or zero), the submodules with the lowest capacitor voltages will be switched on. Thus, the involved capacitors are charged, and the capacitor voltages increase and conform to the other capacitor voltages. The PWM submodule is defined as the following one in ascending order. If the arm current is negative, the submodules with the highest capacitor voltages will be switched on, because the negative arm current discharges the capacitors with the most charge and conforms their capacitor voltages to the lower ones. The PWM submodule is defined as the previous one in ascending order. With this selection algorithm, all capacitor voltages of an arm are balanced, and they lie within a small voltage band.

An example of the selection algorithm described earlier can be explained by Fig. 3. The capacitor voltages for an M2C with $n = 5$ are shown in Fig. 3(a). The capacitor voltages of the upper arm [arm 1, $v_{C1}(t), \ldots, v_{C5}(t)$] and the lower arm [arm 2, $v_{C6}(t), \ldots, v_{C10}(t)$] are shown in Fig. 3(b) and sorted in ascending voltage order. The number of submodules that are on are, in this example, $\mathrm{SM}_{\mathrm{on}1} = 1$ for arm 1 and $\mathrm{SM}_{\mathrm{on}2} = 2$

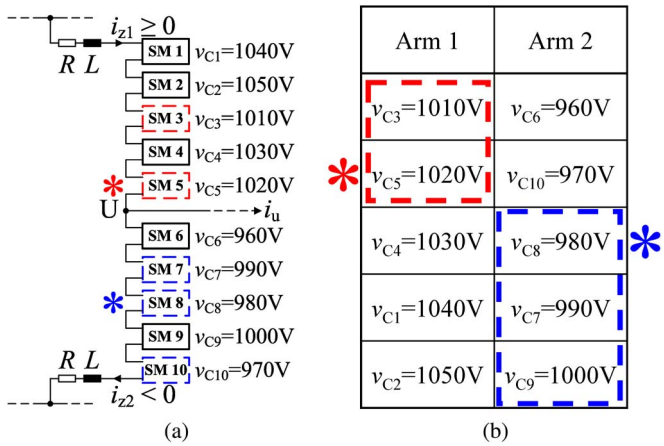

Fig. 3. Selection of on-state and PWM submodules. (a) Converter phase U. (b) Sorted capacitor voltages of arms 1 and 2 ($*$ PWM submodule).

TABLE II
CONVERTER SPECIFICATIONS

$V_{\mathrm{LL,rms,1}}$ (V)	2300	3300	4160	6000	7200
$I_{\mathrm{ph,rms,1}}$ (A)	600				
ω (s^{-1})	$2\pi 50$				
ϕ (rad)	$-\pi \ldots \pi$				
m	$2/\sqrt{3}$				
n	4	6	8	10	12
$1/T_{\mathrm{PWM}}$ (s^{-1})	1800	2700	3600	4500	5400
V_{DC} (V)	3383	4854	6118	8825	10590
R_{d} (Ω)	1				
R (mΩ)	20	30	40	50	60
L (μH)	20	30	40	50	60
C_{SM} (mF)	3				
IGBT module	Infineon/EUPEC FZ600R17KE3				
V_{CES} (V)	1700				
$I_{\mathrm{C,nom}}$ (A)	600				

for arm 2, calculated by (9). The measured arm currents are $i_{z1}(t) \geq 0$ and $i_{z2}(t) < 0$. Thus, there is only one submodule in arm 1 that is permanently on (SM 3). The PWM submodule is SM 5, marked by the asterisk symbol $(*)$. If the arm current of arm 1 were negative, the ON-state submodule would be SM 2 and the PWM submodule would be SM 1. In arm 2, the ON-state submodules are SM 9 and SM 7, and the PWM submodule is SM 8.

III. SPECIFICATIONS AND MODELING OF THE CONVERTER

A. Converter Specifications

For the converter model in Fig. 1, converter parameters shown in Table II were used. Simulations were done for a converter family of five line-to-line voltages (2300–7200 V). A fundamental rms current $I_{\mathrm{ph,rms,1}}$ of 600 A with an angular frequency of $\omega = 2\pi 50\ \mathrm{s}^{-1}$ was used, and the load phase angle ϕ was varied in the range from $-\pi, \ldots, \pi$ to analyze all four quadrants. For every line-to-line voltage, a specified number of submodules n per arm, as well as a specified PWM period time T_{PWM}, were applied. Values for the corresponding resistors, inductors, and capacitors are given in Table II as well.

In this paper, *Infineon* IGBT module FZ600R17KE3 was used for submodule switches. On the basis of the ON-state and switching characteristics given in the data sheet [31], it is possible to calculate the conduction and switching losses. This IGBT module features a maximum collector–emitter voltage V_{CES} of 1700 V and a dc-collector current $I_{C,\mathrm{nom}}$ of 600 A.

B. Calculation of Initial Values

A first step required is to determine the initial values of the energy storages, i.e., the current values in the inductors and the voltage values in the capacitors, at $t = 0$ to prepare a simulation. Phase currents were generated with current sources

$$i_u(t) = \sqrt{2} I_{\mathrm{ph,rms,1}} \cdot \sin\left(\omega t - \frac{1}{6}\pi - \phi\right) \tag{11}$$

$$i_v(t) = \sqrt{2} I_{\mathrm{ph,rms,1}} \cdot \sin\left(\omega t - \frac{5}{6}\pi - \phi\right) \tag{12}$$

where load phase angle ϕ is varied across its entire range. The load phase angle ϕ is defined in such a way that, in the interval $[-\pi/2; \pi/2]$, the energy flows from the dc side to the three-phase ac side, otherwise from the ac to the dc side. Each line-to-line voltage corresponds with a unique number of submodules n per arm. The nominal dc voltage is calculated using the line-to-line voltage with respect to the third harmonic injection and with a 4% control reserve by

$$V_{\mathrm{DC}} = \sqrt{2} V_{\mathrm{LL,rms,1}} \cdot (1.04). \tag{13}$$

Initial values (at $t = 0$) for the inductors and capacitors are calculated with the following approach. Assuming power balance, the dc part of the current $i_d(t)$ can be calculated. Thus, the initial value (at $t = 0$) is set to

$$i_d(0) = \frac{3 m I_{\mathrm{ph,rms,1}} V_{\mathrm{LL,rms,1}} \cos(\phi)}{2 V_{\mathrm{DC}}}. \tag{14}$$

With these considerations, the initial currents for inductors L are calculated with (11), (12), and (14) by

$$i_{z1}(0) = \frac{1}{3} i_d(0) + \frac{1}{2} i_u(0) \tag{15}$$

$$i_{z2}(0) = \frac{1}{3} i_d(0) - \frac{1}{2} i_u(0) \tag{16}$$

$$i_{z3}(0) = \frac{1}{3} i_d(0) + \frac{1}{2} i_v(0) \tag{17}$$

$$i_{z4}(0) = \frac{1}{3} i_d(0) - \frac{1}{2} i_v(0) \tag{18}$$

$$i_{z5}(0) = \frac{1}{3} i_d(0) - \frac{1}{2} \left(i_u(0) + i_v(0)\right) \tag{19}$$

$$i_{z6}(0) = \frac{1}{3} i_d(0) + \frac{1}{2} \left(i_u(0) + i_v(0)\right). \tag{20}$$

The initial voltages for the capacitors follow from the approach that, at any given moment, n submodules of the $2n$ submodules of a phase are on. Thus, the nominal dc voltage is divided

TABLE III
SEMICONDUCTOR SPECIFICATIONS FOR IGBT MODULE FZ600R17KE3

g	j	a	b	c
v_{CE}	i_C	0.7 V	0.010357 V	0.79806
v_F	i_F	0.5 V	0.050265 V	0.52041
E_{on}	i_C	0 J	0.00057942 J	0.9351
E_{off}	i_C	0 J	0.00066378 J	0.88671
E_{rec}	i_F	0 J	0.0088387 J	0.43627
$R_{thJC,T}$		0.04 K/W		
$R_{thCH,T}$		0.01615 K/W		
$R_{thJC,D}$		0.065 K/W		
$R_{thCH,D}$		0.02625 K/W		

equally among all submodules, and every submodule is initialized by

$$v_C(0) = \frac{V_{DC}}{n}. \tag{21}$$

In order to consider the voltage drops that occur at the resistor R_d, the voltage for the voltage sources $V_d/2$ is calculated with (14) by

$$V_d = V_{DC} + R_d i_d(0). \tag{22}$$

IV. DETERMINATION OF LOSSES AND POWER SEMICONDUCTOR CURRENT RATING

A. Calculation of Losses and Semiconductor Current Rating

Submodule switches in the simulation model in Fig. 1 are considered ideal for simulation purposes, thus decreasing simulation time. By using the simulated current waveforms, the semiconductor specifications from the manufacturer can be used to approximate semiconductor losses.

The required characteristic curves [31] for the conduction- and switching-loss calculations of the used IGBT module FZ600R17KE3 are approximated in the same way as described in [16] and [32] with

$$g(j) = a + b\left(\frac{j}{[\mathrm{A}]}\right)^c \tag{23}$$

where the coefficients are taken from Table III (the same values as used in [16]). The unit [A] (ampere) in the denominator makes the basis of the exponent c dimensionless. The resulting calculated characteristic curves generated with (23) are shown in Fig. 4. They show an excellent congruence with the corresponding given values of the datasheet [31]. The accuracy of the loss and junction temperature calculation and the thermal model being applied is evaluated in [33] and [34].

To determine the semiconductor current rating, a model for an ideal parallel connection of IGBT modules is used, as shown in Fig. 5. The parameter κ (current factor) relates how many IGBT modules are ideally parallel connected. The calculated current factor κ guarantees that the mean junction temperature of the mostly stressed IGBT or diode part reaches a value of 125 °C in one worst case operating point of four-quadrant operation.

In the example shown in Fig. 5, the current factor is chosen to be $\kappa = 2$, i.e., an ideal parallel connection of two basis IGBT

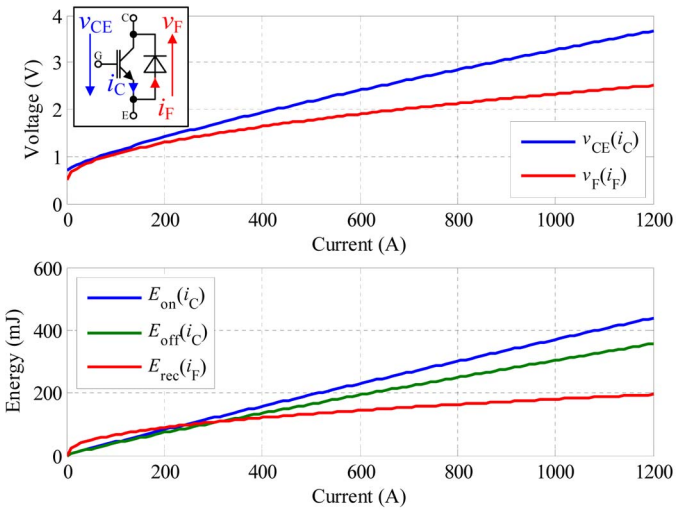

Fig. 4. (Upper diagram) on-state and (lower diagram) switching characteristics of the IGBT module FZ600R17KE3 at a junction temperature of 125 °C and a reference voltage for switching losses of $v_{CE,ref} = 900$ V.

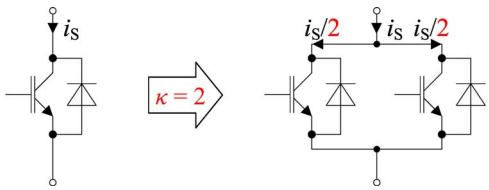

Fig. 5. Ideal parallel connection of IGBT modules for a current factor of $\kappa = 2$.

modules. Thus, only half of the current $i_S(t)$ flows to each IGBT module.

Conduction losses are calculated within one fundamental output time period $2\pi/\omega$ with the simulated currents $i_C(t)$ (IGBT part) and $i_F(t)$ (diode part) and the use of the characteristic curves of the basis IGBT module (Fig. 4) by

$$P_{conT} = \kappa \frac{\omega}{2\pi} \int_{t_s}^{t_s+\frac{2\pi}{\omega}} \frac{i_C(\tau)}{\kappa} v_{CE}\left(\frac{i_C(\tau)}{\kappa}\right) d\tau \tag{24}$$

$$P_{conD} = \kappa \frac{\omega}{2\pi} \int_{t_s}^{t_s+\frac{2\pi}{\omega}} \frac{i_F(\tau)}{\kappa} v_F\left(\frac{i_F(\tau)}{\kappa}\right) d\tau \tag{25}$$

where the current factor κ scales the losses. P_{conT} and P_{conD} are the losses in one fundamental output time period in the IGBT and diode parts of an IGBT module, respectively. The parameter t_s denotes the instant when the simulated waveforms are in steady state. Blocking state losses are neglected because they are much smaller than the conduction losses.

Switching losses are calculated within one fundamental output time period $2\pi/\omega$ by

$$P_{onT} = \kappa \frac{\omega}{2\pi} \sum_{\alpha=1}^{N_\alpha} \left\{ \frac{v_{CE,off}(t_\alpha)}{v_{CE,ref}} E_{on}\left(\frac{i_C(t_\alpha)}{\kappa}\right) \right\} \tag{26}$$

$$P_{offT} = \kappa \frac{\omega}{2\pi} \sum_{\beta=1}^{N_\beta} \left\{ \frac{v_{CE,off}(t_\beta)}{v_{CE,ref}} E_{off}\left(\frac{i_C(t_\beta)}{\kappa}\right) \right\} \tag{27}$$

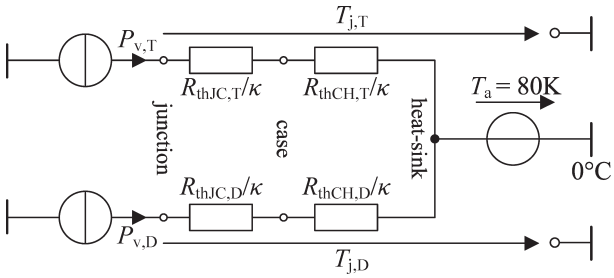

Fig. 6. Equivalent thermal circuit diagram for IGBT module FZ600R17KE3.

$$P_{\mathrm{off}D} = \kappa \frac{\omega}{2\pi} \sum_{\gamma=1}^{N_\gamma} \left\{ \frac{v_{F,\mathrm{off}}(t_\gamma)}{v_{\mathrm{CE,ref}}} E_{\mathrm{rec}} \left(\frac{i_F(t_\gamma)}{\kappa} \right) \right\} \tag{28}$$

and are likewise scaled by the current factor κ. $P_{\mathrm{on}T}$ describes the turn-on losses in one fundamental output time period in the IGBT part of an IGBT module, and $P_{\mathrm{off}T}$ and $P_{\mathrm{off}D}$ are analogously the turn-off losses in the IGBT and diode parts of an IGBT module. At every switching instant $(t_\alpha, t_\beta, t_\gamma)$, the switching-loss energies $(E_{\mathrm{on}}, E_{\mathrm{off}}, E_{\mathrm{rec}})$ are calculated using the simulated currents $(i_C(t_\alpha), i_C(t_\beta), i_F(t_\gamma))$ using the curves shown in Fig. 4. The switching-loss energies are scaled by the ratio of the occurring blocking voltage $(v_{\mathrm{CE,off}}(t_\alpha), v_{\mathrm{CE,off}}(t_\beta), v_{F,\mathrm{off}}(t_\gamma))$ to the reference blocking voltage $(v_{\mathrm{CE,ref}} = 900\ \mathrm{V})$ of the characteristic curves and are summed over the duration of a fundamental output time period, where N_α, N_β, and N_γ are the numbers of all switching actions. Diode turn-on losses are considered negligible. Total losses in the IGBT and diode are calculated by the sum of the conduction and switching losses

$$P_{v,T} = P_{\mathrm{con}T} + P_{\mathrm{on}T} + P_{\mathrm{off}T} \tag{29}$$
$$P_{v,D} = P_{\mathrm{con}D} + P_{\mathrm{off}D}. \tag{30}$$

B. Equivalent Thermal Circuit Diagram

In order to calculate the junction temperature of the semiconductors, the equivalent thermal circuit diagram shown in Fig. 6 is applied. The heat-sink temperature is assumed to be $T_a = 80\ ^\circ\mathrm{C}$. The thermal resistors are scaled with current factor κ, and the case-to-heat-sink resistor is separated for the IGBT part and diode part, as described in [35]. The values for the thermal resistances are given in Table III. The junction temperatures of the IGBT part and the diode part are then calculated by

$$T_{j,T} = P_{v,T} \cdot \left(\frac{R_{\mathrm{thJC},T}}{\kappa} + \frac{R_{\mathrm{thCH},T}}{\kappa} \right) + T_a \tag{31}$$
$$T_{j,D} = P_{v,D} \cdot \left(\frac{R_{\mathrm{thJC},D}}{\kappa} + \frac{R_{\mathrm{thCH},D}}{\kappa} \right) + T_a. \tag{32}$$

C. Loss Distribution and Semiconductor Current Rating

The ideal semiconductor current rating is determined by the current rating of the base device and the ideal current factor κ. In steady-state simulation, current factor κ is chosen such that the semiconductors achieve a mean junction temperature of 125 °C for all values of ϕ.

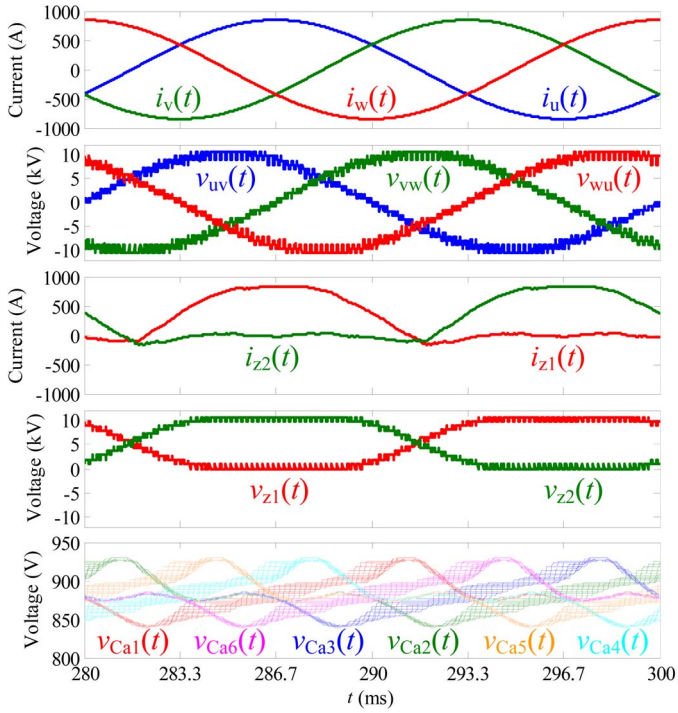

Fig. 7. Simulated waveforms for $V_{\mathrm{LL,rms},1} = 7200$ V, $I_{\mathrm{ph,rms},1} = 600$ A, and $\phi = 0$.

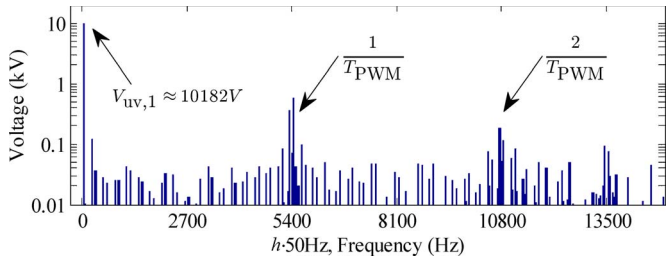

Fig. 8. Amplitude spectrum of line-to-line voltage $v_{uv}(t)$ with fundamental $V_{uv,1}$ at 50 Hz for $V_{\mathrm{LL,rms},1} = 7200$ V, $I_{\mathrm{ph,rms},1} = 600$ A, and $\phi = 0$.

One period of simulated waveforms in steady state is shown in Fig. 7. The phase currents $i_u(t)$, $i_v(t)$, $i_w(t)$ have an rms value of $I_{\mathrm{ph,rms},1} = 600$ A, and the line-to-line voltages $v_{uv}(t)$, $v_{vw}(t)$, $v_{wu}(t)$ have an rms value of $V_{\mathrm{LL,rms},1} = 7200$ V (Table II). Due to the number of submodules per arm of $n = 12$, the resulting number of voltage levels in the line-to-line voltage is $2n + 1 = 25$. The two arm currents $i_{z1}(t)$, $i_{z2}(t)$ have an average current and are shifted by a half period to one another. The arm voltages $v_{z1}(t)$, $v_{z2}(t)$ feature $n + 1 = 13$ voltage levels. The voltages are also shifted by a half period to one another. The voltages follow the reference voltage (1) with the injected third harmonic. All $n = 12$ capacitor voltages of each arm are shown in the lowest diagram and are labeled with $v_{\mathrm{Ca}k}(t)$. This diagram shows the effect of the selection algorithm: The capacitor voltages are balanced, and all voltages are within a small voltage band.

The amplitude spectrum of the line-to-line voltage $v_{uv}(t)$ is shown in Fig. 8. As expected, the spectrum shows harmonic sidebands at multiples of the inverse of the specified PWM period T_{PWM}. Thus, the parameter T_{PWM} has a strong effect on the quality of the line-to-line voltages.

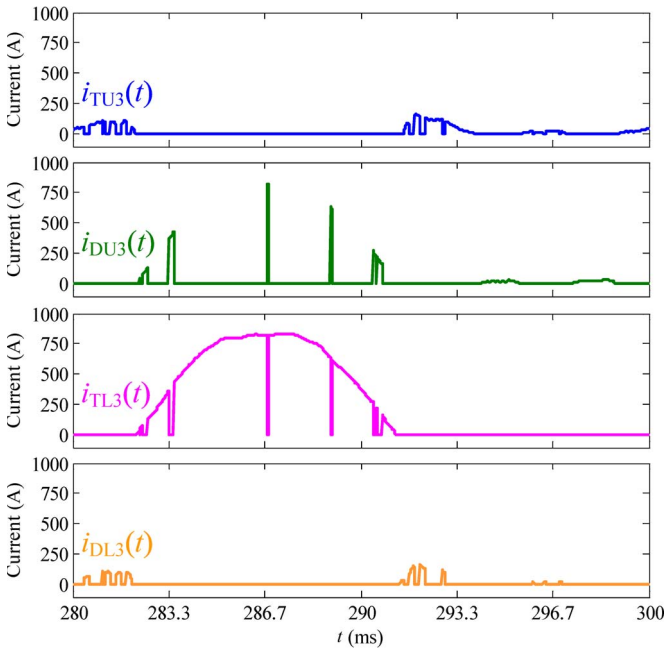

Fig. 9. Current distribution in submodule 3 for $V_{\mathrm{LL,rms},1} = 7200$ V, $I_{\mathrm{ph,rms},1} = 600$ A, and $\phi = 0$.

To evaluate the quality of the output voltage waveform in Fig. 7 (second diagram), the values of THD

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} V_{uv,h}^2}}{V_{uv,1}} \tag{33}$$

and weighted THD (WTHD)

$$WTHD = \frac{\sqrt{\sum_{h=2}^{\infty} \left(\frac{V_{uv,h}}{h}\right)^2}}{V_{uv,1}} \tag{34}$$

have been calculated to be $THD \approx 9.00\%$ and $WTHD \approx 0.265\%$, respectively. Spectrum, THD, and WTHD show an excellent quality of the output voltage waveform as compared to that of conventional MV converters (e.g., [6], [36], and [37]).

The current distribution in submodule 3 of arm 1 is shown in Fig. 9 as an example, and the current definition of submodule 3 is shown in Fig. 10. The current distributions of the other submodules are similar. The arm current $i_{z1}(t)$, which is equivalent to the total submodule current, has four parts: two currents through the upper IGBT module [IGBT part $i_{\mathrm{TU3}}(t)$ and diode part $i_{\mathrm{DU3}}(t)$] and two currents through the lower IGBT module [IGBT part $i_{\mathrm{TL3}}(t)$ and diode part $i_{\mathrm{DL3}}(t)$]. Fig. 9 shows the commutations between the upper IGBT part and the lower diode part $(i_{\mathrm{TU3}}(t) \leftrightarrow i_{\mathrm{DL3}}(t))$ as well as the commutations between the upper diode part and the lower IGBT part $(i_{\mathrm{DU3}}(t) \leftrightarrow i_{\mathrm{TL3}}(t))$. It is apparent that the current distribution of the four parts is rather unequal.

The calculated losses of the four parts of all 12 submodules of arm 1 are shown in Fig. 11. The unequal current distribution leads to an unequal loss distribution. Whereas the upper IGBT and diode parts, as well as the lower diode part, generate losses

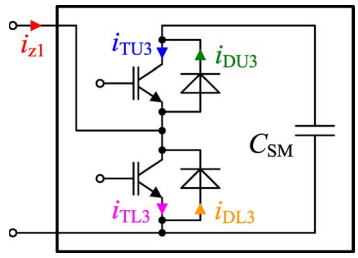

Fig. 10. Current definition of submodule 3.

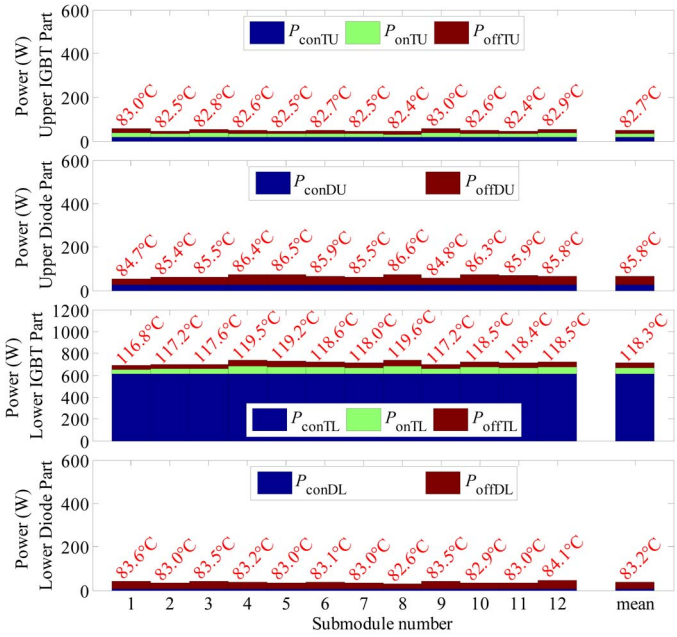

Fig. 11. Loss distribution of IGBT and diode parts in arm 1 for $V_{\mathrm{LL,rms},1} = 7200$ V, $I_{\mathrm{ph,rms},1} = 600$ A, $\phi = 0$, and $\kappa = 1.050$.

of only $\approx 50-75$ W, the lower IGBT part generates losses of 700 W. This leads to unsymmetrical junction temperatures for the four parts of $T_{j,\mathrm{TU3}} = 82.8$ °C, $T_{j,\mathrm{DU3}} = 85.5$ °C, $T_{j,\mathrm{TL3}} = 117.6$ °C, and $T_{j,\mathrm{DL3}} = 83.5$ °C.

A second important result is that, in every submodule, the corresponding loss distribution is similar. The junction temperature of all lower IGBT parts is in a range from $T_{j,\mathrm{TL1}} = 116.8$ °C (minimum value) to $T_{j,\mathrm{TL8}} = 119.6$ °C (maximum value). The variation of the minimum and maximum values from the mean value of 118.3 °C is approximately 1% quite small. Thus, it is useful to calculate the current factor κ with the corresponding mean values.

The mean loss distribution for four different values of the load phase angle ϕ is shown in Fig. 12. The first group (from left to right) shows the mean loss distribution of the upper and lower IGBT modules in a submodule for $\phi = 0$. This is the same operation point as that shown in Figs. 7, 9, and 11, where the lower IGBT part generates the highest losses.

With a load phase angle of $\phi = \pi/2$, the losses are distributed more equally. It is noteworthy that the lower IGBT module generates more than twice the losses of the upper IGBT module.

At a load phase angle of $\phi = \pi$, the most highly stressed component is the lower diode. Although the losses in the lower diode $P_{v,D} \approx 550$ W are less than that in the lower IGBT

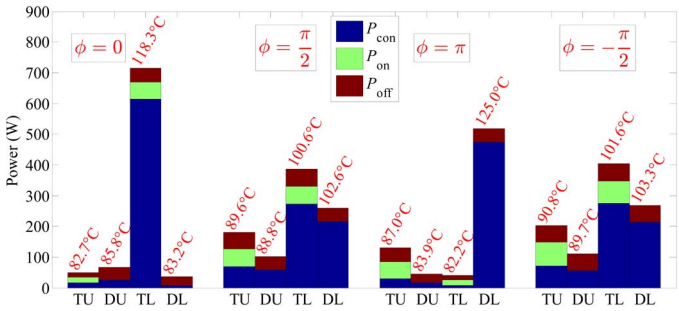

Fig. 12. Mean loss distribution of IGBT and diode parts in arm 1 for $V_{\mathrm{LL,rms,1}} = 7200$ V, $I_{\mathrm{ph,rms,1}} = 600$ A, and $\kappa = 1.050$.

TABLE IV
CURRENT FACTOR, TOTAL SEMICONDUCTOR LOSSES, AND EFFICIENCY OF M2CS

$V_{\mathrm{LL,rms,1}}$ (V)	2300	3300	4160	6000	7200
κ	1.043	1.036	1.033	1.045	1.050
$P_{\mathrm{v,tot}}$ (kW) ($\phi = 0$)	19.4	29.7	39.2	51.2	62.5
η (%) ($\phi = 0$)	99.19	99.14	99.10	99.19	99.17
$P_{\mathrm{v,tot}}$ (kW) ($\phi = \pi/2$)	19.2	28.8	39.4	53.0	66.9
η (%) ($\phi = \pi/2$)	0	0	0	0	0
$P_{\mathrm{v,tot}}$ (kW) ($\phi = \pi$)	16.6	24.8	32.6	43.2	52.9
η (%) ($\phi = \pi$)	99.31	99.28	99.25	99.31	99.30
$P_{\mathrm{v,tot}}$ (kW) ($\phi = -\pi/2$)	20.4	30.5	41.8	56.3	71.0
η (%) ($\phi = -\pi/2$)	0	0	0	0	0
$P_{\mathrm{v,tot}}$ (kW) ($\phi = \pi/6$)	20.2	29.9	40.5	52.9	65.5
η (%) ($\phi = \pi/6$)	99.03	99.00	98.93	99.03	99.00

$P_{v,T} \approx 700$ W for $\phi = 0$, the junction temperature of the lower diode reaches the maximum junction temperature of 125 °C for a selected current factor of $\kappa = 1.050$. The reason for this is the different thermal resistances, as shown in Fig. 6.

A load phase angle of $\phi = -\pi/2$ leads to very similar loss distributions as for $\phi = \pi/2$. As a result, for all load conditions, the lower IGBT module is more stressed than the upper one. For modularity reasons, the same IGBT modules have been used for the lower and the upper switches of a submodule, although the currents and losses of the lower and the upper switches are very different. The use of differently rated IGBT modules could have the potential of a reduced expense of semiconductors. However, the influence of IGBT modules with different current ratings on the converter protection and practical implementation issues (e.g., modularity and module construction) has to be considered in this case.

The final results of the semiconductor dimensioning for all considered converter voltages are summarized in Table IV. The selected current factors κ of 1.033–1.050 show that up to 5% more silicon area is required to satisfy the maximum junction temperature condition using the semiconductor FZ600R17KE3.

The parameter $P_{v,\mathrm{tot}}$ represents the total losses of the semiconductors of the M2C converter. With the converter output power

$$P_{\mathrm{out}} = \left|\sqrt{3} V_{\mathrm{LL,rms,1}} I_{\mathrm{ph,rms,1}} \cos(\phi)\right| \tag{35}$$

and the assumption that the converter input power P_{in} is the sum of the converter output power P_{out} and the total semiconductor losses $P_{v,\mathrm{tot}}$, an equation for the efficiency is attained

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{v,\mathrm{tot}}}. \tag{36}$$

In (35), the absolute value is used in order to make (36) generally applicable to all used load phase angles ϕ. The calculated converter losses and efficiencies are shown for the four load phase angles 0, $\pi/2$, π, and $-\pi/2$ in Table IV. It is obvious that the total semiconductor losses $P_{v,\mathrm{tot}}$'s depend on the load phase angle ϕ. For all investigated line-to-line voltages $V_{\mathrm{LL,rms,1}}$, a load phase angle of $-\pi/2$ causes the highest losses. The lowest losses are generated for a load phase angle of π, because the diodes in the IGBT modules conduct higher rms currents than the IGBTs and the diodes generate less conduction losses than the IGBTs at the same current [Fig. 4 (upper diagram)]. The efficiency depends on the load phase angle ϕ as well. For $\phi = \pi/2$ and $\phi = -\pi/2$, the efficiencies are zero because the converter output power P_{out} is zero.

In addition, the converter losses are calculated for a load phase angle of $\phi = \pi/6$, because this is a typical operating point for an induction-machine drive (comparable to the operating point used in [29]). The calculated converter losses for the load phase angle of $\pi/6$ result in converter efficiencies of about 99%.

V. CONCLUSION

On the basis of a described new modulation method, simulations of 2.3-, 3.3-, 4.16-, 6.0-, and 7.2-kV M2Cs have been carried out. With the attained waveforms and the loss characteristics of a specified base semiconductor, conduction and switching losses were calculated. By using a thermal circuit diagram for IGBT modules, junction temperatures of the semiconductors and, thus, the ideal semiconductor current rating were calculated.

The current distribution of the four component parts within the semiconductors of a submodule showed an unequal current, loss, and junction temperature distribution. However, the loss distribution of the arm submodules is very similar. The load phase angle has an enormous effect on the loss distribution of a submodule. The lower IGBT module generates substantially higher losses than the upper one for all investigated load phase angles. The selected semiconductors enabled a converter efficiency of approximately 99% at a typical operating point for an induction machine.

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