A Proportional + Multiresonant Controller for Three-Phase Four-Wire High-Frequency Link Inverter

Dipankar De and Venkataramanan Ramanarayanan

***Abstract*—A new solution for unbalanced and nonlinear loads in terms of power circuit topology and controller structure is proposed in this paper. A three-phase four-wire high-frequency ac-link inverter is adopted to cater to such loads. Use of high-frequency transformer results in compact and light-weight systems. The fourth wire is taken out from the midpoint of the isolation transformer in order to avoid the necessity of an extra leg. This makes the converter suitable for unbalanced loads and eliminates the requirements of bulky capacitor in half-bridge inverter. The closed-loop control is carried out in stationary reference frame using proportional + multiresonant controller (three separate resonant controller for fundamental, fifth and seventh harmonic components). The limitations on improving steady-state response of harmonic resonance controllers is investigated and mitigated using a lead–lag compensator. The proposed voltage controller is used along with an inner current loop to ensure excellent performance of the power converter. Simulation studies and experimental results with 1 kVA prototype under nonlinear and unbalanced loading conditions validate the proposed scheme.**

***Index Terms*—Digital controller, four-wire systems, high-frequency link, nonlinear loads, resonant controller.**

I. Introduction

POWER CONVERSION using a high-frequency link is being widely applied in dc–dc [1], [2], dc-to-single-phase ac [3], dc-to-three-phase ac [4], rectifier [5], [6], and ac–ac [7], [8] systems. By high-frequency link technique, heavy and bulky commercial frequency transformers are replaced by small high-frequency transformers, and size and weight of the systems can be reduced dramatically.

However, the applications of these techniques are limited to three-phase three-wire systems. But majority of loads fed by ac power supplies and uninterruptable power supply (UPS) systems are nonlinear and unbalanced in nature [9], [10]. In case of unbalanced load, if load neutral is kept floating (as in three-wire systems), it shifts from its balanced location causing severe overvoltage or undervoltage across different phases. To prevent neutral shift the only solution is to use four-wire systems. Conventionally, three-leg VSI with dc-bus midpoint as fourth wire, four-leg VSI and three-leg VSI with output delta–star transformer are used to achieve a four-wire system [11]–[16]. In this paper, a three-phase four-wire system with high-frequency transformer isolation is proposed (see Fig. 1). The isolation between input and output are inevitable for certain applications like medical facilities due to safety reasons. In such situations, this topology provides compact isolation at the cost of extra devices and associated losses.

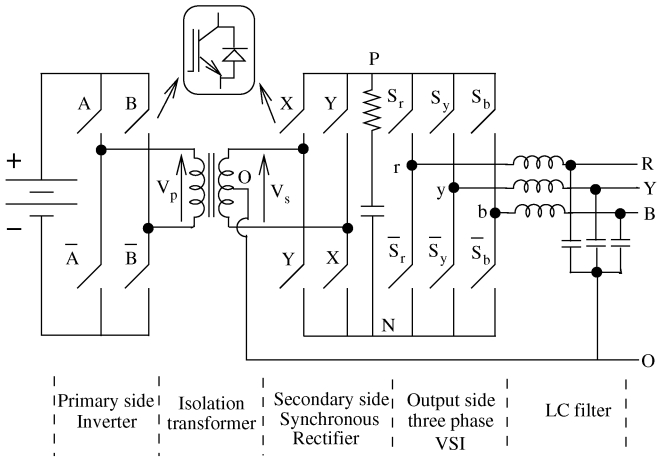

Fig. 1. Proposed three-phase four-wire high-frequency link converter.

The control structure for a three-wire system can easily be implemented either in synchronously rotating frame or in stationary reference frame. Hybrid approaches (stationary + synchronously rotating frame) were also reported in literature [17]. But inclusion of fourth wire introduces additional complexity in synchronously-rotating-frame-based control strategy. It requires positive-, negative-, and zero-sequence controllers [10], [18], [19], complicated transformations, and separation of different sequence components. Moreover, zero-sequence controller handles time-varying quantities, and thus, produces significant steady-state error. The same performance can be achieved with less implementation complexity using P + resonant controller in stationary reference frame [22], [23]. This controller structure is derived from dc controllers by suitable transformation in [24], and can easily be extended for harmonics loads [20]. However, because of poor phase margin steady-state gains of the controller at harmonic frequencies are highly limited. Specific problem related to low phase margin and the consequent high-frequency oscillation in the output voltage are highlighted. A new proposed controller adds an additional lead–lag term to overcome the earlier problem.

This paper is organized as follows. In Section II, the description of the proposed power circuit with commutation

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requirements and an example of zero-sequence current path are provided. Section III describes damping of resonance oscillation due to output *LC* filter with a inner current loop and modified structure of proposed outer voltage controller for unbalanced and nonlinear loads. The same section contains adequate simulation studies to verify the effectiveness of the controller. The measured results and conclusion of the work are presented in Section IV and V, respectively.

II. Power Circuit Description

A. Power Converter

The proposed scheme is shown in Fig. 1 and it has five cascaded stages as follows:

1) primary-side inverter or H-bridge;
2) high-frequency isolation transformer with center tap at secondary side;
3) secondary-side synchronous rectifier;
4) output-side three-phase VSI;
5) output *LC* filter.

The first stage of the power circuit is a single-phase inverter that operates in quasi-square-wave mode and generates the high-frequency ac-link voltage. The output of the isolation transformer is rectifier by secondary-side synchronous rectifier. This rectified output is converted to three-phase ac (fundamental frequency) through output-side VSI [7]. The midpoint of high-frequency transformer acts as the fourth wire, and thus, eliminates the requirement of an additional leg in the cycloconverter side. An *RC* snubber is added after synchronous rectifier to absorb the stored energy in the leakage inductance of the isolation transformer. The detailed commutation requirements of the power circuit are described in next section.

B. Commutation Requirements

The power circuit requires certain commutation procedures (shown in Fig. 2) for its safe operation. The primary-side inverter legs (A and B in Fig. 1) are operated at 50% duty ratio with a small phase shift between them. These gate pulses for A and B are generated from phase shifted carrier CA and CB respectively. Again, $\bar{\mathrm{A}}$ and $\bar{\mathrm{B}}$ are the compliments of A and B, respectively (see Fig. 1) with small dead time to prevent shoot through of the dc source. The phase shift between A and B introduces a zero voltage portion in the primary (Vp) as well as the secondary (Vs) voltage waveform. The synchronous rectifier switches (X and Y) have small overlap (shown in Fig. 2) to keep current path continuous. Again, this overlap of X and Y takes place within the zero portion of the secondary voltage (Vs) in order to avoid dead short circuit of the secondary voltage. The zero portions and overlap zones are shown larger compared to actual one for clarity. The cycloconverter link voltage (V_{PN}) is not a fixed dc but have some zero portion in it ($V_{\mathrm{PN}} = V_{\mathrm{PO}} - V_{\mathrm{NO}}$). The center point O of the high-frequency transformer acts as the fourth wire. The next stage is a standard three-phase VSI, which takes V_{PN} as its input and generates three-phase output voltages. The switches S_r, S_y, and S_b are modulated with same carrier CA to produce pole voltages (S_r and V_{rO} are shown in Fig. 2). In case of unbalanced load, the fourth wire carries zero-sequence component of unbalanced load current and helps to maintain rated voltages across all phases.

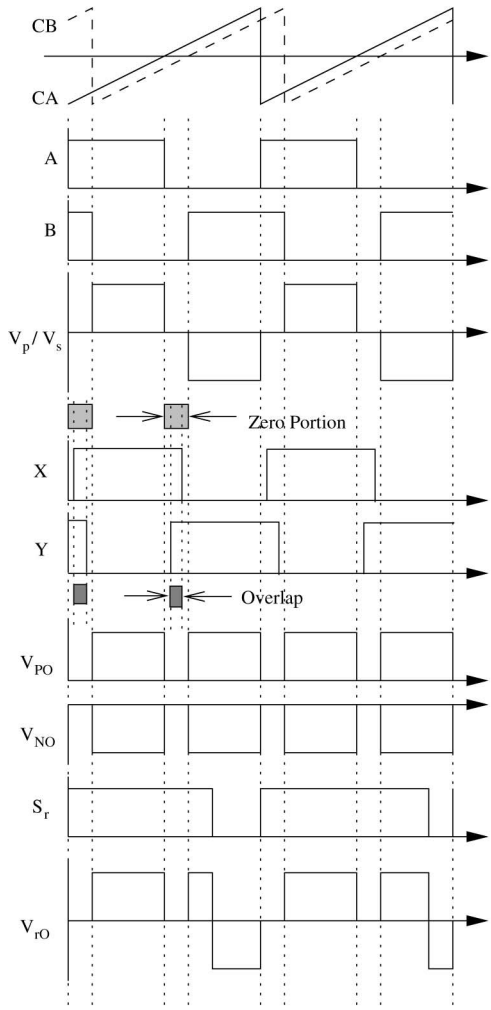

Fig. 2. Sample waveform to describe commutation requirements.

C. Illustration on Zero-Sequence Current Path

As described in previous section that fourth wire takes the zero-sequence current and allows the power circuit to cater unbalanced loads. Fig. 3 describes the paths of common-mode or zero-sequence current in secondary side of the transformer under a simple situation where only R-phase is loaded and other two phases are open circuited (so that entire R-phase current flows through the fourth wire). The primary-side inverter and Y- and B-phase legs of output-side VSI are not shown in the figure for simplicity. For a given direction of common-mode current, depending on status of switches X, Y, and S_r four different modes are possible [see Fig. 3(a)–(d)]. The important point to note here is that the transformer sees a high-frequency (switching frequency) current, whereas the actual zero-sequence current is at fundamental frequency. Hence, transformer carries common-mode current without getting into saturation.

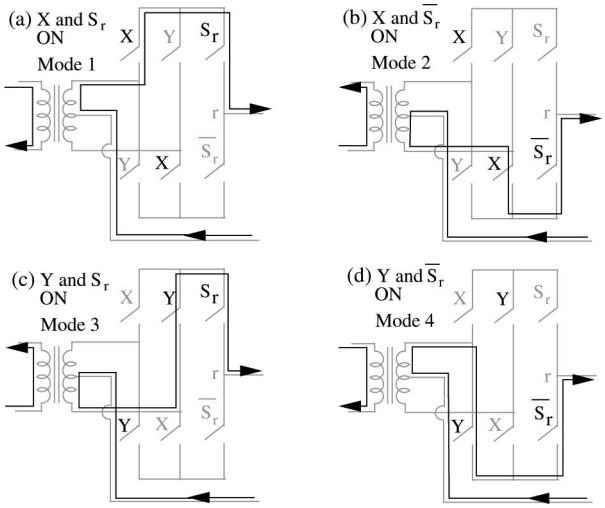

Fig. 3. Path of zero-sequence current in a simplified case (only R-phase is loaded).

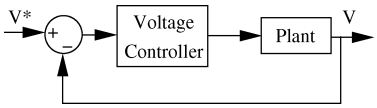

Fig. 4. Single voltage loop.

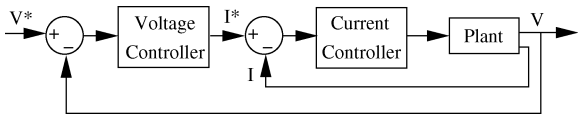

Fig. 5. Multiloop with inner current loop.

III. Control Strategy for Four-Wire System

A. General Structure

Fig. 4 shows the single voltage loop control structure. This control scheme eliminates the need of current sensors but fails to achieve high steady-state and transient responses with adequate stability margin. All three control objectives can be ensured with multiloop control (shown in Fig. 5). Only a proportional controller is enough for inner current loop though it produces a significant phase shift at operating frequency. A large gain associated with outer voltage controller is essential in order to compensate the phase shift and to ensure negligible steady-state error. In present case, a large steady-state gain is achieved by classical P + resonant controller in stationary reference frame. Again, in multiloop or cascaded loop controller, the bandwidth of the voltage controller cannot be increased beyond certain value. Hence, inner current loop plays a significant role on damping of resonance oscillation due to output *LC* filter.

B. Inner Current Loop and Damping of Resonance Oscillation

First, let us consider the configuration of inner current loop. The inner loop variable used here is inductor current for better resonance damping and power circuit protection [23]. Fig. 6

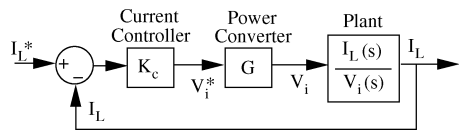

Fig. 6. Inner current loop and plant.

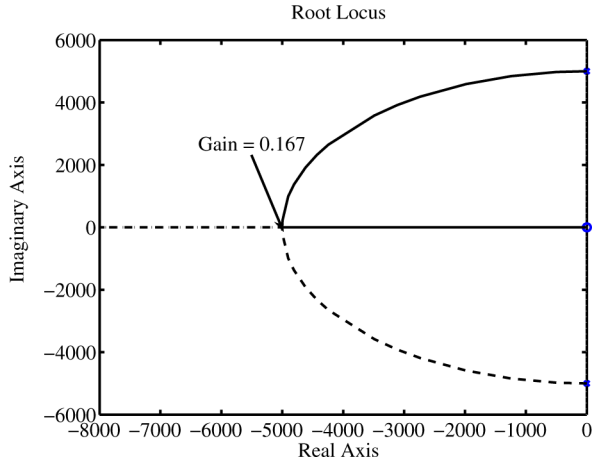

Fig. 7. Root locus plot of current loop.

shows the configuration of the current loop with a proportional controller. V_i is the inverter output voltage and $I_L(s)/V_i(s)$ is the plants transfer function when the disturbance input I_o is ignored. The plant transfer function is given by

$$\frac{I_L(s)}{V_i(s)} = \frac{sC}{1+s^2LC}. \tag{1}$$

It is marginally stable and susceptible to resonance oscillation. From (1), the closed-loop transfer function can be derived as

$$\frac{I_L(s)}{I_L^*(s)} = \frac{sC}{1+sK_cGC+s^2LC} \tag{2}$$

Equation (2) clearly indicates that if current controller gain (K_c) is increased, better damping of resonance oscillation can be achieved. Fig. 7 shows the corresponding root locus for various values of K_c. For $K_c \geq 0.167$, the oscillatory behavior of the system is completely eliminated. The closed-loop transfer function in (2) is approximated as

$$\frac{I_L(s)}{I_L^*(s)} \approx \frac{sC}{1+sK_cGC} \tag{3}$$

for design verifications of outer loop. This assumption is valid because there is considerable amount of steady-state phase and magnitude error in current loop. This is clear from the Bode plot of the closed-loop transfer function for inner current loop (shown in Fig. 8).

C. Outer Voltage Loop and Stability Analysis

From the inner current loop gain function (see Fig. 8), it may appear that a simple proportional–integral (PI) controller with high bandwidth may be used to achieve voltage control. In such a case, the dc gain of the loop will be infinity. It is found that

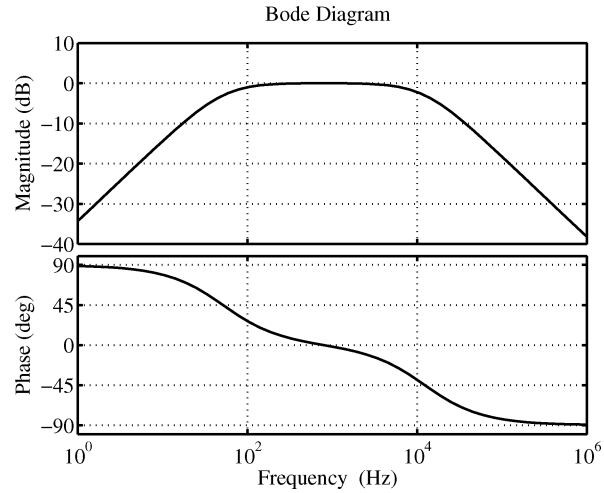

Fig. 8. Bode plot of $I_L(s)/I_L^*(s)$.

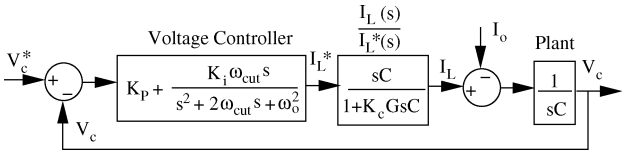

Fig. 9. P + resonant controller for fundamental component.

such a controller gives rise to starting problems since this high dc gain sometimes leads the control to get into overmodulation. Therefore, the strategy to obtain stable operating point as well as good steady-state performance requires unconventional compensator design.

The structure of the outer voltage loop with P + resonant controller is shown in Fig. 9. Because of limitations in practical implementations true resonant controller cannot be used [22]. Fig. 9 shows the approximate resonant controller with cutoff frequency $\omega_{\rm cut}$. Output of voltage controller is the reference input for inner current controller (inductor current reference I_L^*). Fig. 9 also shows the approximate current loop transfer function [as given in (3)] and load current I_o as disturbance input. Ignoring the disturbance input, the characteristics equation of outer voltage loop is given in (4), as shown at the bottom of this page. The stability criteria can be checked from Routh array given by (5), as shown at the bottom of this page. As for all possible values of $K_p > 0$ and $K_i > 0$ the first row of Routh array has no sign change, the system stability is ensured for all values of K_p and K_i. Hence, it is possible to achieve a high steady-state response for fundamental frequency ω_o. This controller structure shown

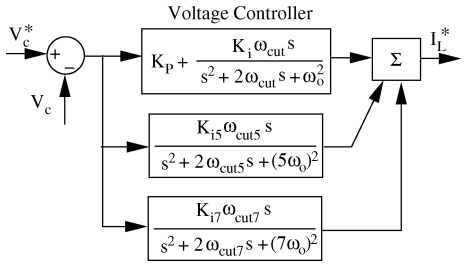

Fig. 10. P + multiresonant controller for fundamental and harmonic (fifth and seventh) components.

in Fig. 9 is a single-phase equivalent of three-phase controller. This control structure is sufficient to handle both balanced- and unbalanced-loading conditions.

D. Extension to Nonlinear Loads

When the loads on the power supply is nonlinear in nature (like rectifier load), the output voltage contains predominantly fifth- and seventh-harmonics other than fundamental. The control structure is shown in Fig. 9 is not sufficient to reject disturbing effect of load current on the output voltage. Two separate resonant controllers (as shown in Fig. 10) for fifth- and seventh-harmonic components are added with the fundamental in outer voltage loop [20]. The magnitudes of K_{i5} and K_{i7} determine the steady-state error for fifth- and seventh-harmonic components respectively. The stability analysis for this controller structure using Routh array criteria involves very complicated mathematical calculations. To maintain the simplicity of the paper, an alternate procedure (using bode plots) is used to determine the controller parameters. When K_{i5} and K_{i7} are set to zero then controller structure is suitable only for linear loads (see Fig. 11). Now, if these values are increased gradually (for example, 0, 2, 4 Ω^{-1}, etc., in Fig. 11), the steady-state error for fifth- and seventh-harmonic components decreases; however, the phase margin gradually drops. Finally, for $K_{i5} = K_{i7} = 6\ \Omega^{-1}$ (corresponds to a magnitude > 40 dB at fifth- and seventh-harmonic frequencies) the steady-state error is less than 1% for these two harmonic components. Hence, from this design criterion, K_{i5} and K_{i7} are selected. Of course, these values can be further increased to achieve better performance. However, for $K_{i5} = K_{i7} = 4\ \Omega^{-1}$ it can be seen from the bode plot that the phase margin is significantly low and its effect leads to unwanted oscillation in output voltage waveform (see Fig. 12). For $K_{i5} = K_{i7} = 6\ \Omega^{-1}$ (corresponds to desired steady-state error for harmonic components) the system is unstable (phase

$$s^3 K_c GC + s^2\left\{1 + K_p + 2\omega_{\rm cut} K_c GC\right\} + s\left\{\left(2 + 2K_p + K_i\right)\omega_{\rm cut} + \omega_o^2 K_c GC\right\} + \omega_o^2\left(1 + K_p\right) = 0 \tag{4}$$

$$\begin{array}{lcll} s^3 & : & K_c GC & \left(2 + 2K_p + K_i\right)\omega_{\rm cut} + \omega_o^2 K_c GC \\ s^2 & : & 1 + K_p + 2\omega_{\rm cut} K_c GC & \omega_o^2\left(1 + K_p\right) \\ s^1 & : & \left(2 + 2K_p + K_i\right)\omega_{\rm cut} + \dfrac{2\omega_{\rm cut}\left(K_c GC\omega_o\right)^2}{1 + K_p + 2\omega_{\rm cut} K_c GC} & 0 \\ s^0 & : & \omega_o^2\left(1 + K_p\right) & 0 \end{array} \tag{5}$$

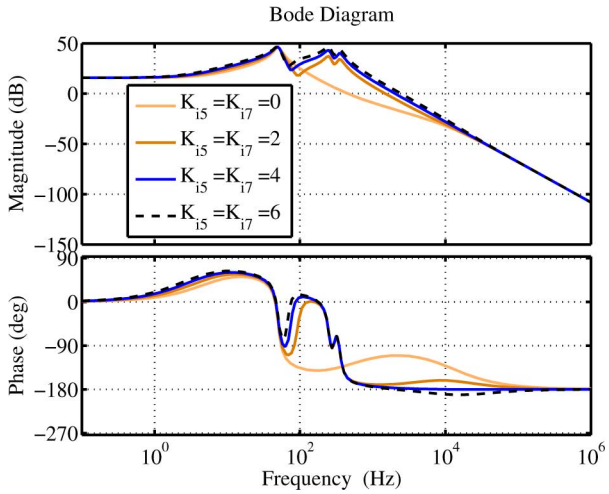

Fig. 11. Bode plot of voltage loop for different values of K_{i5} and K_{i7} (in Ohm inverse).

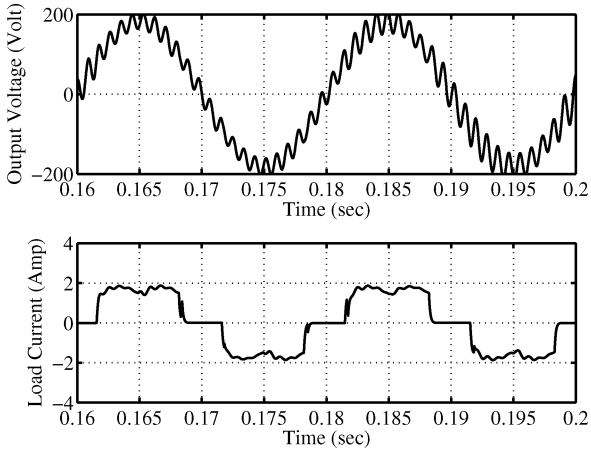

Fig. 12. Simulation result: oscillatory output voltage with $K_{i5} = K_{i7} = 4\ \Omega^{-1}$.

margin $= -1°$). In order to mitigate such problem and to reduce the steady-state error for harmonics below desired limit, the control structure need to be modified as explained in Section III-E.

E. Proposed Control Scheme

From Fig. 11, it is interesting to note that the magnitude plot of the open-loop transfer function of the voltage loop is crossing 0 dB line at -40 dB/dec for selected values of K_{i5} and K_{i7} (dotted line). This can be compensated by adding a suitable lead– lag compensator, as shown in Fig. 13. The design procedure given in [25] is followed here to select the parameters of lead–lag compensator. For a specified phase margin of $45°$, the design procedure is explained in brief as follows.

Additional phase lead required (ϕ_m) = specified phase margin − phase margin of the uncompensated system $(\phi_i) + \epsilon$, where ϵ is the margin of safety required by the fact that gain crossover frequency will increase due to compensation. By iterative method [25], ϵ is selected as $3°$. Hence, $\phi_m = 45 - (-1) + 3 = 49°$. If

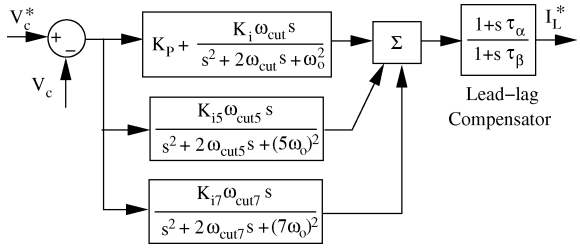

Fig. 13. Proposed control structure for outer voltage loop.

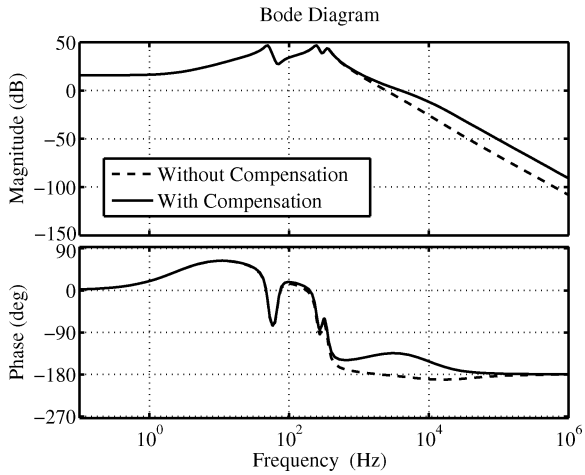

Fig. 14. Bode plot of voltage loop for selected values of K_{i5} and K_{i7} with and without lead–lag compensation.

$\tau_\beta = x\tau_\alpha$, the ratio x can be found out as [25]

$$x = \frac{1 - \sin\phi_m}{1 + \sin\phi_m} = 0.1398. \tag{6}$$

From Fig. 11 (dotted line), the frequency corresponding to the gain $-20\log(1/\sqrt{x})$ is 24818 rad/s (say ω_m). The difference between original phase margin of the uncompensated system (ϕ_i) and phase margin of the uncompensated system at this new expected crossover frequency ω_m should be less than ϵ. If it is not so, the previous procedure need to be iterated with an higher value of ϵ. Next, the value of τ_α and τ_β can be calculated as

$$\tau_\alpha = \frac{1}{\sqrt{x}\omega_m} = 108\ \mu\text{s}, \qquad \tau_\beta = x\tau_\alpha = 15\ \mu\text{s}. \tag{7}$$

The lead–lag compensator corrects the phase margin to a great extent with the selected values of K_{i5} and K_{i7} (see Fig. 14) and helps to achieve negligibly small steady-state errors for harmonic components. Again, from Fig. 14, the gain margin is also quite high for the compensated system. Adequate gain margin and phase margin ensure an oscillation free output voltage (see Fig. 15). The controller parameters are listed in Table I. In Table I, $P_{\text{out}}, V_{\text{in}}, V_o, f, 1:N, L, C, K_c, K_p, K_i, K_{i5}, K_{i7}, \omega_{\text{cut}}, \omega_{\text{cut5}}, \omega_{\text{cut7}}, \tau_\alpha,$ and τ_β denote power rating, input, output, switching frequency, turns ratio of the transformer, filter inductance, filter capacitance, current controller proportional gain, voltage controller proportional gain, voltage controller steady-state gain for fundamental, voltage controller steady-state gain for fifth-harmonic component,

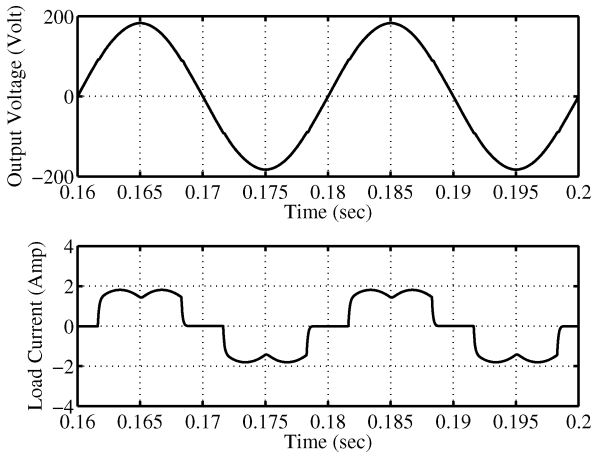

Fig. 15. Simulation result with selected values of K_{i5} and K_{i7} and lead–lag compensator.

TABLE I
POWER AND CONTROL CIRCUIT DETAILS

Symbol	Value
P_{out}	$1kVA$
V_{in}	$120V$ DC
V_o	$220V$ L-L 3ϕ 4-wire
f	$20kHz$
$1:N$	$1:4$
L	$4\ mH$
C	$10\ \mu F$
K_c	$1.28\ \Omega$
K_p	$0.0125\ \Omega^{-1}$
K_i	$1.8\ \Omega^{-1}$
K_{i5}	$6\ \Omega^{-1}$
K_{i7}	$6\ \Omega^{-1}$
ω_{cut}	$31.41\ rad/sec$
ω_{cut5}	$157.08\ rad/sec$
ω_{cut7}	$219.9\ rad/sec$
τ_α	$108\ \mu sec$
τ_β	$15\ \mu sec$

voltage controller steady-state gain for seventh-harmonic component, cutoff frequency for fundamental controller, cutoff frequency for fifth-harmonic controller, cutoff frequency for seventh harmonic controller, time constant-1, and time constant-2 of lead–lag compensator, respectively.

IV. EXPERIMENTAL INVESTIGATION

In order to verify the effectiveness of the proposed converter and control algorithm an experimental protype of 1 kVA is made and tested under both unbalanced and nonlinear loading conditions. An FPGA based digital controller is used to perform the closed-loop control. The laboratory setup with digital controller is shown in Fig. 16. Three inductor currents and three output capacitor voltages are sensed through A/D converters (ADCs) and FPGA controller performs the desired control action, as described in previous section. Finally, the optically isolated and buffered gate pulses are given to the power circuit.

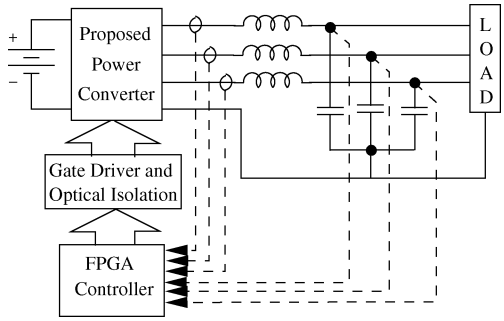

Fig. 16. Experimental setup with digital controller.

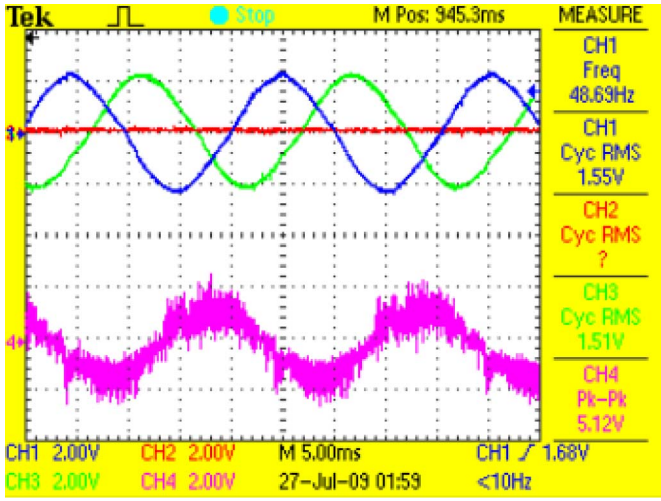

Fig. 17. Three-phase unbalanced load currents (CH1, CH2, CH3: 3 A/division) and zero-sequence current through fourth wire (CH4: 5 A/division). Time: 5 ms/division.

Fig. 17 shows the unbalanced three-phase currents with R-phase load completely open circuited. The fourth wire current is also shown in the same figure. It contains common-mode switching components other than fundamental due to unbalance. The corresponding output three-phase voltages are shown in Fig. 18. The unbalance in voltage is 3.2% according to the definition of unbalance given in (8).

$$\text{unbalance} = \frac{\text{maximum rms voltage} - \text{minimum rms voltage}}{\text{rated rms voltage}} \times 100\%. \quad (8)$$

Next, the performance of the system is investigated with nonlinear rectifier type loads. Fig. 19 shows the R-phase output voltage and load current when K_{i5} and K_{i7} are kept low (to maintain stable operation) and lead–lag compensation is not added and corresponding Fourier spectrum for voltages are shown in Fig. 20. If the steady-state gains of harmonic controllers are increased to reduce the harmonic content in output voltage further, a oscillatory behavior is observed in voltage waveform (see Fig. 21). Fig. 22 shows R-phase output voltage with load current after lead–lag compensation is added (with desired values of K_{i5} and K_{i7}) and the Fourier spectrum of the voltage is

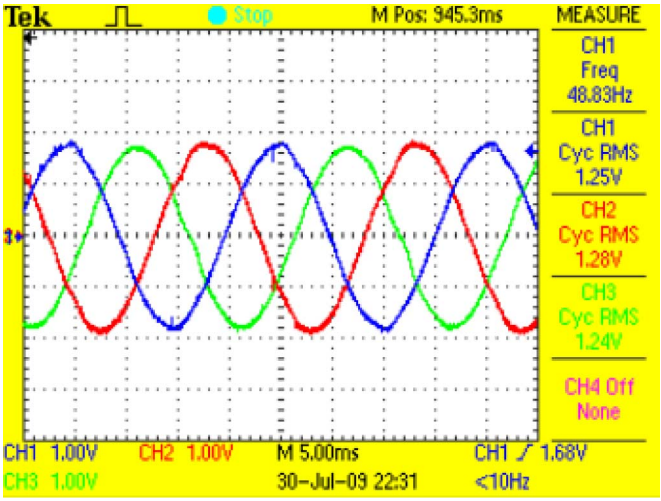

Fig. 18. Three-phase output voltage under unbalanced loading (CH1, CH2, CH3: 100 V/division). Time: 5 ms/division.

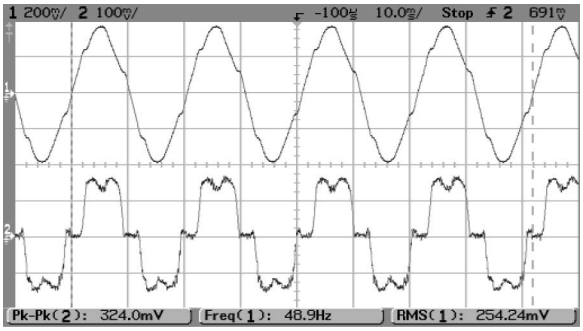

Fig. 19. R-phase output voltage (CH1: 100 V/division) and current (CH2: 2 A/division) with low values of K_{i5} and K_{i7}, time: 10 ms/division.

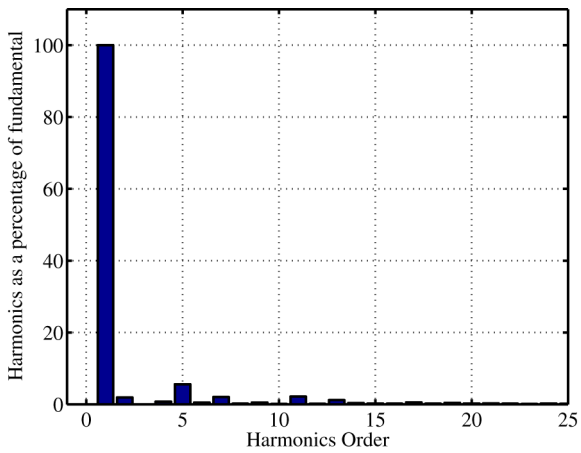

Fig. 20. Fourier spectrum of R-phase output voltage in Fig. 19: THD = 6.94%.

shown in Fig. 23. It is interesting to note that the output voltage total harmonic distortion (THD) is improved from 6.94% to 2.88%.

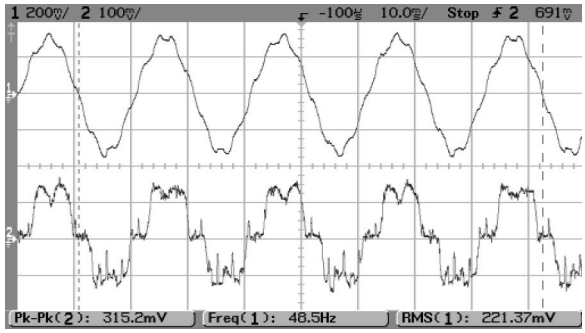

Fig. 21. R-phase output voltage (CH1: 100 V/division) and current (CH2: 2 A/division) with $K_{i5} = K_{i7} = 4\ \Omega^{-1}$ and without lead–lag compensation, time: 10 ms/division.

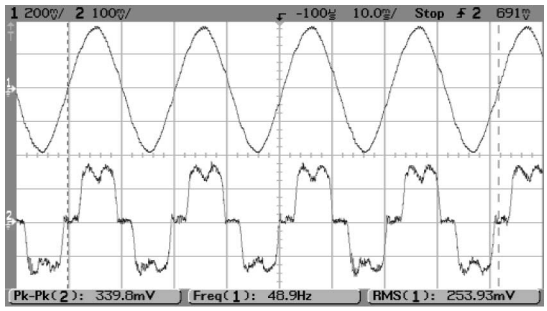

Fig. 22. R-phase output voltage (CH1: 100 V/division) and current (CH2: 2 A/division) with selected values of K_{i5} and K_{i7} and with lead–lag compensation, time: 10 ms/division.

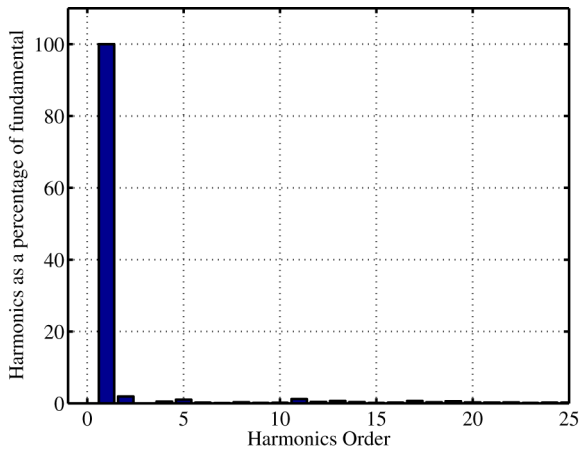

Fig. 23. Fourier spectrum of R-phase output voltage in Fig. 22: THD = 2.88%.

V. Conclusion

A new three-phase four-wire high-frequency link power converter and its novel control algorithm have been presented in this paper. If the isolation between input and output is essential in certain applications, this power converter can provide a compact isolation. The bulky capacitor in half-bridge construction is replaced by a center-tapped transformer. The fourth wire (the center point of isolation transformer) is used to supply zero-sequence component of unbalanced load current.

In order to maintain high-output-voltage quality while supplying unbalanced and nonlinear loads, a proportional +

multiresonant controller is adopted. A stability analysis is carried out to show that there is no limitations on steady-state gains from the point of view of stability if the resonant controller only for fundamental frequency is used. However, the analysis is not valid when separate resonant controllers for harmonics are added (to supply nonlinear loads). Then, the steady-state gains for harmonics components are limited by the poor phase margin of the outer voltage loop. A lead–lag compensator is used in this work to mitigate such problems. The simulation and experimental results proved the effectiveness of the proposed scheme and a THD less than 3% was achieved with harmonic loads. The proposed controller can seamlessly be applied to any standard three-phase four-wire systems.

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