Inverters with Capacitive Output Impedances, Part II: Optimisation of the Output Voltage Quality

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***Abstract*—In this paper, the degradation mechanisms of the quality of inverter output voltage are analysed and two ways are proposed to reduce the harmonic components in the output voltage. One is to provide the right amount of harmonics in the reference voltage to compensate the harmonic voltage drop on the output impedance and the other is to design the inverter to have a small output impedance at harmonic frequencies. Both indicate that the output impedance of an inverter plays a critical role in the output voltage quality. Following the concept of designing an inverter to have a capacitive output impedance proposed and implemented in Part I of this series, the output impedance of an inverter is designed in this paper to optimise the quality of the output voltage, e.g. to minimise the THD of the output voltage or to eliminate a certain harmonic component in the output voltage. Both simulation and experimental results are provided to demonstrate that inverters with capacitive output impedances can outperform inverters with resistive or inductive output impedances in terms of voltage quality.**

Keywords: Inverters with capacitive output impedances, inductive output impedance, resistive output impedance, power quality, total harmonic distortion (THD), droop control, parallel operation of inverters, proportional load sharing

I. Introduction

Nowadays, more and more distributed generation and renewable energy sources, e.g. wind, solar and tidal power, are connected to the public grid via power inverters. They often form microgrids before being connected to the public grid [1]–[5]. One of the major problems in these applications is the quality of the microgrid voltage. Since the output voltage of an inverter is pulse-width-modulated and there are often nonlinear (local) loads, there are harmonic components in the microgrid voltage. According to industrial regulations, the THD needs to be maintained low [6], [7], often below 5%.

Several feedback control schemes, e.g. deadbeat or hysteresis controllers [8], [9], have been proposed for inverters to reduce THD. However, these controller alone cannot eliminate the periodic distortion caused for example by non-linear loads. Repetitive control theory [10], which is regarded as a simple learning control method, provides an alternative to eliminate periodic errors in dynamic systems, using the internal model principle [11]. Such a closed-loop system can deal with a very large number of harmonics simultaneously, as it has a high gain at the fundamental and all harmonic frequencies of interest. It has been successfully applied to constant-voltage constant-frequency (CVCF) PWM inverters [12]–[17], grid-connected inverters [2], [6], [18] and active filters [19], [20] to obtain very low THD. Strategies are available to maintain low THD in the current exchanged with the grid [6], in the microgrid voltage [18], [21] and in both the current exchanged with the grid and the microgrid voltage at the same time [22].

When inverters are operated in parallel, the voltage quality problem could be addressed together with the power sharing problem, for example, via injecting a harmonic voltage according to the output harmonic current [23] or introducing a voltage feedback loop [24]. It is well understood [25] that the output impedance of the inverters plays an important role in power sharing and a droop controller for inverters with resistive output impedances was proposed for sharing linear and nonlinear loads [26]. In this paper, it will be shown that the output impedance of an inverter also plays a critical role in reducing the THD of the output voltage, after analysing the degradation mechanisms of the voltage quality. Following the work in Part I to design inverters to have capacitive output impedances (although an inverter usually has a filter inductor), the capacitive output impedance of an inverter will be further explored in this paper to improve the voltage quality, e.g. to eliminate a certain harmonic components in the voltage or to minimise the THD of the output voltage.

The rest of the paper is organised as follows. In Section II, the degradation mechanisms of the quality of inverter output voltages are analysed and the principles to improve the voltage quality are presented. In Section III, after reviewing how to design the output impedance of an inverter to be capacitive, the controller parameter is optimised to achieve the lowest THD or to eliminate a certain harmonic components. This paves a way to further decrease the THD with combination of other strategies. Simulation results are given in Section IV and experimental results are given in Section V, followed by conclusions made in Section VI.

II. Degradation Mechanisms of the Quality of Inverter Output Voltages

It has been widely recognised that the output voltage of an inverter as modelled in Figure 1 can be written as

$$v_o = v_r - Z_o(s) \cdot i,$$

where v_r is the voltage reference, v_o is the output voltage across the capacitor and i is the output current flowing through the inductor; see e.g. [27]. In general, there are harmonics in the current i because of nonlinear loads and/or the pulse width modulation, which cause harmonic voltage drops on the output impedance Z_o. If there are no corresponding harmonic voltage components provided by the reference v_r, then the

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harmonic voltage components appear in the output voltage, which degrades the voltage quality and causes a high THD. Another source of high THD in the output voltage is from the voltage reference v_r if it contains significant harmonic components.

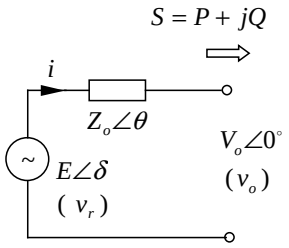


Figure 1. The model of an inverter

In order to obtain low THD for v_o, there are two options: one is to make sure that the reference voltage v_r is able to provide the right amount of harmonic voltages to compensate the harmonic voltage dropped on the output impedance and the other is to keep v_r clean and maintain a small output impedance Z_o over the range of the major harmonic current components. The first option has been widely investigated in the literature, e.g. by using the repetitive control strategy [2], [6], [16]–[19], [28]–[31] or by harmonics injection [23]. However, the second option has not been fully explored and will be studied in details in this paper. Strictly speaking, the first option should lead to a small output impedance but this fact has not been well understood.

Assume that the output current is

$$i = \sqrt{2}\Sigma_{h=1}^{\infty} I_h \sin(h\omega^* t + \phi_h),$$

where ω^* is the rated frequency. Then the amplitude of the h-th harmonic voltage dropped on the output impedance is $\sqrt{2}I_h\left|Z_o(jh\omega^*)\right|$. Moreover, assume that the voltage reference v_r is clean and sinusoidal and is described as

$$v_r = \sqrt{2}E\sin(\omega^* t + \delta).$$

Then the fundamental component of the output voltage is [1]

$$\begin{aligned} v_1 &= \sqrt{2}E\sin(\omega^* t + \delta) - \sqrt{2}I_1\left|Z_o(j\omega^*)\right|\sin(\omega^* t + \phi_1 + \theta) \\ &= \sqrt{2}V_1\sin(\omega^* t + \beta), \end{aligned}$$

where

$$V_1 = \sqrt{E^2 + I_1^2\left|Z_o(j\omega^*)\right|^2 - 2EI_1\left|Z_o(j\omega^*)\right|\cos(\phi_1 + \theta - \delta)},$$

$$\beta = \arctan\left(\frac{I_1\left|Z_o(j\omega^*)\right|\sin(\phi_1 + \theta - \delta)}{I_1\left|Z_o(j\omega^*)\right|\cos(\phi_1 + \theta - \delta) - E}\right).$$

The sum of all harmonic components in the output voltage is

$$v_H = \sqrt{2}\Sigma_{h=2}^{\infty} I_h\left|Z_o(jh\omega^*)\right|\sin(h\omega^* t + \phi_h + \angle Z_o(jh\omega^*)).$$

It is clear that v_1 and v_H do not affect each other. v_1 is determined by the clean reference voltage, the fundamental current and the output impedance at the fundamental frequency. v_H is determined by the harmonic current components and the output impedance at the harmonic frequencies. This is an important feature and enables the design of the impedance to meet different requirements.

According to the definition of THD, the THD of the output voltage is

$$\text{THD} = \frac{\sqrt{\Sigma_{h=2}^{\infty} I_h^2\left|Z_o(jh\omega^*)\right|^2}}{V_1} \times 100\%. \tag{1}$$

Hence, the THD is mainly affected by the output impedance at the harmonic frequencies. As a result, it is feasible to optimise the design of the output impedance at high frequencies to minimise the THD of the output voltage, without affecting the impedance at the fundamental frequency. In other words, the design of the output impedance can be decoupled to meet two different requirements in the frequency domain. For example, the output impedance at the fundamental frequency can be designed to meet the requirements of the droop controller for proportional load sharing, as done in Part I, and the output impedance at harmonic frequencies can be designed to reduce the THD of the voltage, as to be done in this paper. Hence, one parameter can be used to meet two requirements at the same time (one qualitatively and the other quantitatively).

III. Controller Design to Achieve an Optimal Capacitive Output Impedance

A. To achieve a capacitive output impedance

Figure 2(a) shows an inverter, which consists of a single-phase H-bridge inverter powered by a DC source, and an LC filter. The control signal u is converted to a PWM signal to drive the H-bridge so that the average of u_f over a switching period is the same as u, i.e. $u \approx u_f$. Hence, the PWM block and the H-bridge can, and will, be ignored in the controller design. The inductor current i is measured for feedback so that the output impedance of the inverter is forced to be capacitive and to dominate the impedance between the inverter and the AC bus (at the fundamental frequency). This is done, as shown in Figure 2(b), via passing the current i through an integrator block $\frac{1}{sC_o}$. This is equivalent to having a virtual capacitor C_o connected in series with the filter inductor L.

The following two equations hold for the closed-loop system consisting of Figure 2(a) and Figure 2(b):

$$u = v_r - \frac{1}{sC_o}i, \quad \text{and} \quad u_f = (R + sL)i + v_o.$$

Since the average of u_f over a switching period is the same as u, there is (approximately)

$$v_r - \frac{1}{sC_o}i = (R + sL)i + v_o,$$

which gives

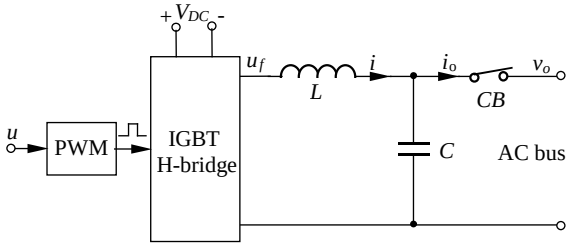
$$v_o = v_r - Z_o(s)\cdot i,$$

where the output impedance $Z_o(s)$ is

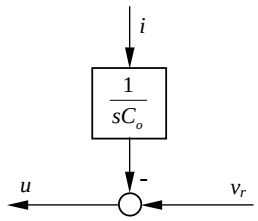
$$Z_o(s) = R + sL + \frac{1}{sC_o}. \tag{2}$$

If the capacitor C_o is chosen small enough, the effect of the inductor $(R + sL)$ is not significant and the output impedance

[1] See the trigonometric identities at http://en.wikipedia.org/wiki/List_of_trigonometric_identities.



(a) A descriptive circuit



(b) A controller to achieve a capacitive output impedance

Figure 2. A single-phase inverter with a capacitive output impedance

can be made nearly purely capacitive at the fundamental frequency, i.e., roughly

$$Z_o(s) \approx \frac{1}{sC_o}.$$

B. To optimise the quality of the output voltage

As discussed above, the THD of the output voltage mainly depends on the output impedance at the harmonic frequencies. According to (2), there is

$$|Z_o(jh\omega^*)|^2 = R^2 + (h\omega^* L - \frac{1}{h\omega^* C_o})^2.$$

In order to minimise the THD of the output voltage, the virtual capacitor C_o should be chosen to minimise

$$\Sigma_{h=2}^{\infty} I_h^2 |Z_o(jh\omega^*)|^2$$

because the fundamental component V_1 can be assumed to be almost constant. This is equivalent to

$$\min_{C_o} \Sigma_{h=2}^{\infty} i_{1h}^2 (h\omega^* L - \frac{1}{h\omega^* C_o})^2, \tag{3}$$

where $i_{1h} = \frac{I_h}{I_1}$ is the normalised h-th harmonic current I_h with respect to the fundamental current I_1. Depending on the distribution of the harmonic current components, different strategies can be obtained.

Assume that the harmonic current is negligible for the harmonics higher than the N-th order (with an odd number N). Then C_o can be found via solving (3). Define

$$f(C_o) = \Sigma_{h=2}^{N} i_{1h}^2 (h\omega^* L - \frac{1}{h\omega^* C_o})^2.$$

Then C_o needs to satisfy

$$\frac{\mathrm{d}f(C_o)}{\mathrm{d}C_o} = 2\Sigma_{h=2}^{N} i_{1h}^2 (h\omega^* L - \frac{1}{h\omega^* C_o}) \frac{1}{h\omega^* C_o^2} = 0,$$

which is equivalent to

$$\Sigma_{h=2}^{N} i_{1h}^2 (L - \frac{1}{(h\omega^*)^2 C_o}) = 0.$$

Hence,

$$\Sigma_{h=2}^{N} i_{1h}^2 L = \frac{1}{(\omega^*)^2 C_o} \Sigma_{h=2}^{N} \frac{i_{1h}^2}{h^2},$$

and the optimal capacitance can be solved as

$$C_o = \frac{1}{(\omega^*)^2 L} \frac{\Sigma_{h=2}^{N} \frac{i_{1h}^2}{h^2}}{\Sigma_{h=2}^{N} i_{1h}^2}, \tag{4}$$

which is applicable for any known harmonic distribution of current i. The corresponding $f(C_o)$ is

$$\begin{aligned} f_{min}(C_o) &= \Sigma_{h=2}^{N} i_{1h}^2 (h\omega^* L - \frac{\omega^* L}{h} \frac{\Sigma_{h=2}^{N} i_{1h}^2}{\Sigma_{h=2}^{N} \frac{i_{1h}^2}{h^2}})^2 \\ &= (\omega^* L)^2 \Sigma_{h=2}^{N} i_{1h}^2 (h - \frac{1}{h} \frac{\Sigma_{h=2}^{N} i_{1h}^2}{\Sigma_{h=2}^{N} \frac{i_{1h}^2}{h^2}})^2. \end{aligned}$$

This means that the THD of v_o is in proportion to the inductance L of the inverter LC filter. A small L does not only reduce the cost but also improves the voltage quality. However, a small L leads to a high $\frac{\mathrm{d}i}{\mathrm{d}t}$ for the switches and large current ripples. Moreover, since $\frac{1}{C_o} \sim L$, a small L leads to a small gain for the integrator, which is good for the stability of the current loop.

If the distribution of the harmonic components is not known, then it can be assumed that the even harmonics are zero (which is normally the case) and the odd harmonics are equally distributed. As a result, the optimal C_o can be chosen, according to (4), as

$$\begin{aligned} C_o &= \frac{1}{(\omega^*)^2 L} \frac{\Sigma_{h=3,5,7,...,N} \frac{1}{h^2}}{\Sigma_{h=3,5,7,...,N} 1} \\ &= \frac{1}{(\omega^*)^2 L} \frac{\Sigma_{h=3,5,7,...,N} \frac{1}{h^2}}{(N-1)/2}. \end{aligned}$$

This can be written as

$$C_o = \frac{1}{(\omega^*)^2 L} \frac{1}{(N-1)/2} (\frac{1}{3^2} + \frac{1}{5^2} + ... + \frac{1}{N^2}),$$

where $(N-1)/2$ is the number of terms in the summation. The corresponding $f(C_o)$ is

$$f_{min}(C_o) = (\omega^* L)^2 \Sigma_{h=3,5,7,...,N} (h - \frac{1}{h} \frac{(N-1)/2}{\Sigma_{h=3,5,7,...,N} \frac{1}{h^2}})^2.$$

If a single h-th harmonic component is concerned, then the optimal C_o is

$$C_o = \frac{1}{(h\omega^*)^2 L}.$$

This forces the impedance at the h-th harmonic frequency to be 0 and hence no voltage at this frequency is caused.

1) Special Case I: To minimise the 3rd and 5th harmonic components: In most cases, it is enough to consider the 3rd and 5th harmonics only. This gives the optimal capacitance

$$C_o = \frac{17}{225(\omega^*)^2 L}.$$

As a result, the output impedance is

$$\begin{aligned} Z_o(j\omega) &= R + j(\omega L - \frac{1}{\omega C_o}) \\ &= R + j\omega^* L(\frac{\omega}{\omega^*} - \frac{225}{17}\frac{\omega^*}{\omega}). \end{aligned}$$

The gain factor $\frac{\omega}{\omega^*} - \frac{225}{17}\frac{\omega^*}{\omega}$ of the imaginary part with respect to the normalised frequency $\frac{\omega}{\omega^*}$ is shown in Figure 3. It changes from negative to positive at around $\frac{\omega}{\omega^*} = 3.638$. At the fundamental frequency, i.e., when $\omega = \omega^*$, the output impedance is

$$Z_o = R - j\frac{208}{17}\omega^* L \approx -j12.23\omega^* L.$$

It is capacitive as expected because R is normally smaller than $\omega^* L$.

2) Special Case II: To minimise the 3rd harmonic component: In this case, the optimal C_o is

$$C_o = \frac{1}{(3\omega^*)^2 L}$$

and the corresponding impedance is

$$\begin{aligned} Z_o(j\omega) &= R + j(\omega L - \frac{1}{\omega C_o}) \\ &= R + j\omega^* L(\frac{\omega}{\omega^*} - \frac{9\omega^*}{\omega}). \end{aligned}$$

The gain factor $\frac{\omega}{\omega^*} - \frac{9\omega^*}{\omega}$ of the imaginary part with respect to the normalised frequency $\frac{\omega}{\omega^*}$ is also shown in Figure 3. It changes from negative to positive at $\omega = 3\omega^*$. At the fundamental frequency, i.e., when $\omega = \omega^*$, the output impedance is

$$Z_o = R - j8\omega^* L \approx -j8\omega^* L,$$

which is capacitive as well.

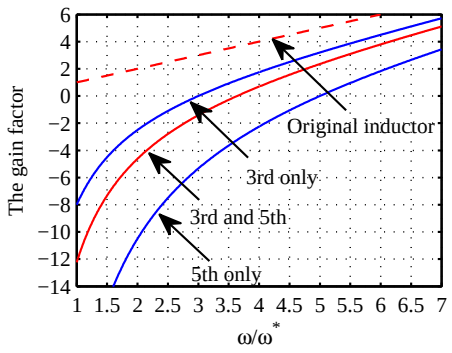


Figure 3. The gain factors to meet different criteria

3) Special Case III: To minimise the 5th harmonic component: In this case, the optimal C_o is

$$C_o = \frac{1}{(5\omega^*)^2 L}$$

and the corresponding impedance is

$$\begin{aligned} Z_o(j\omega) &= R + j(\omega L - \frac{1}{\omega C_o}) \\ &= R + j\omega^* L(\frac{\omega}{\omega^*} - \frac{25\omega^*}{\omega}). \end{aligned}$$

The gain factor $\frac{\omega}{\omega^*} - \frac{25\omega^*}{\omega}$ of the imaginary part with respect to the normalised frequency $\frac{\omega}{\omega^*}$ is also shown in Figure 3. It changes from negative to positive at $\omega = 5\omega^*$. At the fundamental frequency, i.e., when $\omega = \omega^*$, the output impedance is

$$Z_o = R - j24\omega^* L \approx -j24\omega^* L.$$

This is capacitive as well.

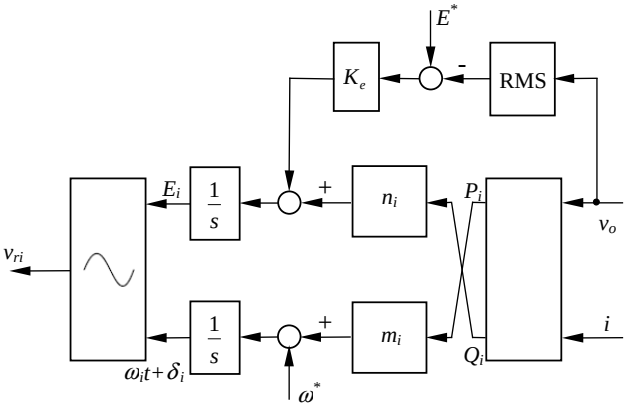


Figure 4. The robust droop controller proposed in Part I for inverters with capacitive output impedances to achieve accurate proportional load sharing

IV. Simulation Results

Simulations were carried out on a single-phase inverter powered by a 42V DC voltage supply. The inverter is equipped with the robust droop controller proposed in Part I, which is shown in Figure 4 for the convenience of readers, to regulate the output voltage. The parameters were $n_i = 2.2$, $m_i = 0.14$ and $K_e = 20$.

The switching frequency is 7.5kHz and the frequency of the system is 50Hz. The rated voltage is 12V. The filter capacitance is 22μF and the load is a full-bridge rectifier loaded with an LC filter $L = 150\mu H$, $C = 1000\mu F$ and $R_L = 9\Omega$.

Table I
STEADY-STATE PERFORMANCE OF THE INVERTER WITH $L = 2.35$MH

Type of Z_o	L	R	C_o	
			325μF (3rd+5th)	479μF (3rd)
THD of v_o	39.4%	25.9%	19.8%	25.9%
V_o	11.92	11.02	11.42	11.63

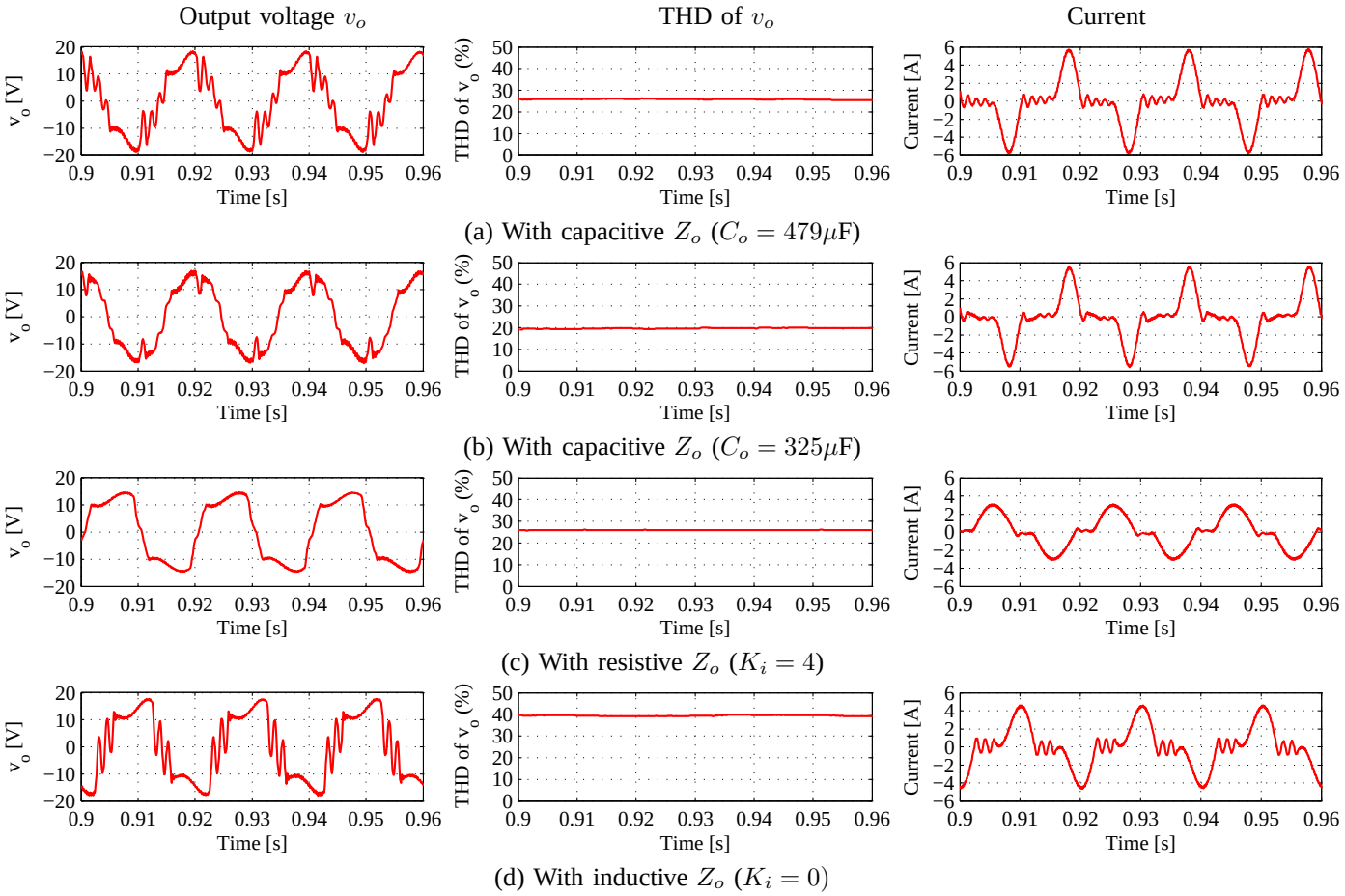


Figure 5. Simulation results for the case with $L = 2.35$mH: output voltage (left column), THD of the output voltage (middle column) and current (right column).

A. The case with $L = 2.35mH$

The parasitic resistance of the inductor is assumed to be 0.1Ω. According to the analysis in the previous section, the optimal capacitance C_o can be chosen as 479μF to minimise the effect of the 3rd harmonics in v_o and 325μF to minimise the effect of the 3rd and 5th harmonics in v_o. The steady-state performance of the system with these controllers are shown in Table I. The results of the system when the inverters were designed to have resistive output impedances (with $K_i = 4$) and inductive output impedances (with $K_i = 0$) using the robust droop controller proposed in [27] are also shown in Table I for comparison. The inverters with capacitive output impedances considerably improved the THD of the output voltage: from 39.4% obtained by inverters with inductive output impedances and 25.9% obtained by inverters with resistive output impedances to 19.8%. The lowest THD (19.8%) was obtained when the capacitor was designed as $C_o = 325\mu F$ to minimise the effect of the 3rd and 5th harmonics. The output voltage, the THD of the output voltage and the current curves for the inverters with different output impedances are shown in Figure 5. Apparently, the inverters with capacitive output impedances offer the best THD and the inverter with the inductive output impedance offer the worst THD. It is worth noting that the purpose of this paper is to demonstrate that inverters with capacitive output impedances can improve the THD of the output voltage because of the extra freedom introduced to optimise the THD but not to reduce the overall THD to meet industrial regulations. Other techniques, e.g. the ones proposed in [24], [32], can be applied to further decrease the THD.

Table II
STEADY-STATE PERFORMANCE OF THE INVERTER WITH $L = 0.25$MH

Type of Z_o	L	R	C_o	
			3100μF (3rd+5th)	4500μF (3rd)
THD of v_o	9.2%	8.2%	7.4%	7.0%
V_o	12.73	10.97	11.36	11.33

B. The case with $L = 0.25mH$

According to the above analysis, a small filter inductor helps reduce the cost and the THD of the output voltage. In order to demonstrate this, the filter inductor $L = 2.35$mH was replaced with an inductor $L = 0.25$mH and the simulations were repeated. The parasitic resistance of the inductor is assumed to be 0.045Ω. The steady-state performance of the systems are shown in Table II. As expected, the THD was reduced significantly with comparison to the case with $L = 2.35$mH. Moreover, the inverters with capacitive output impedances

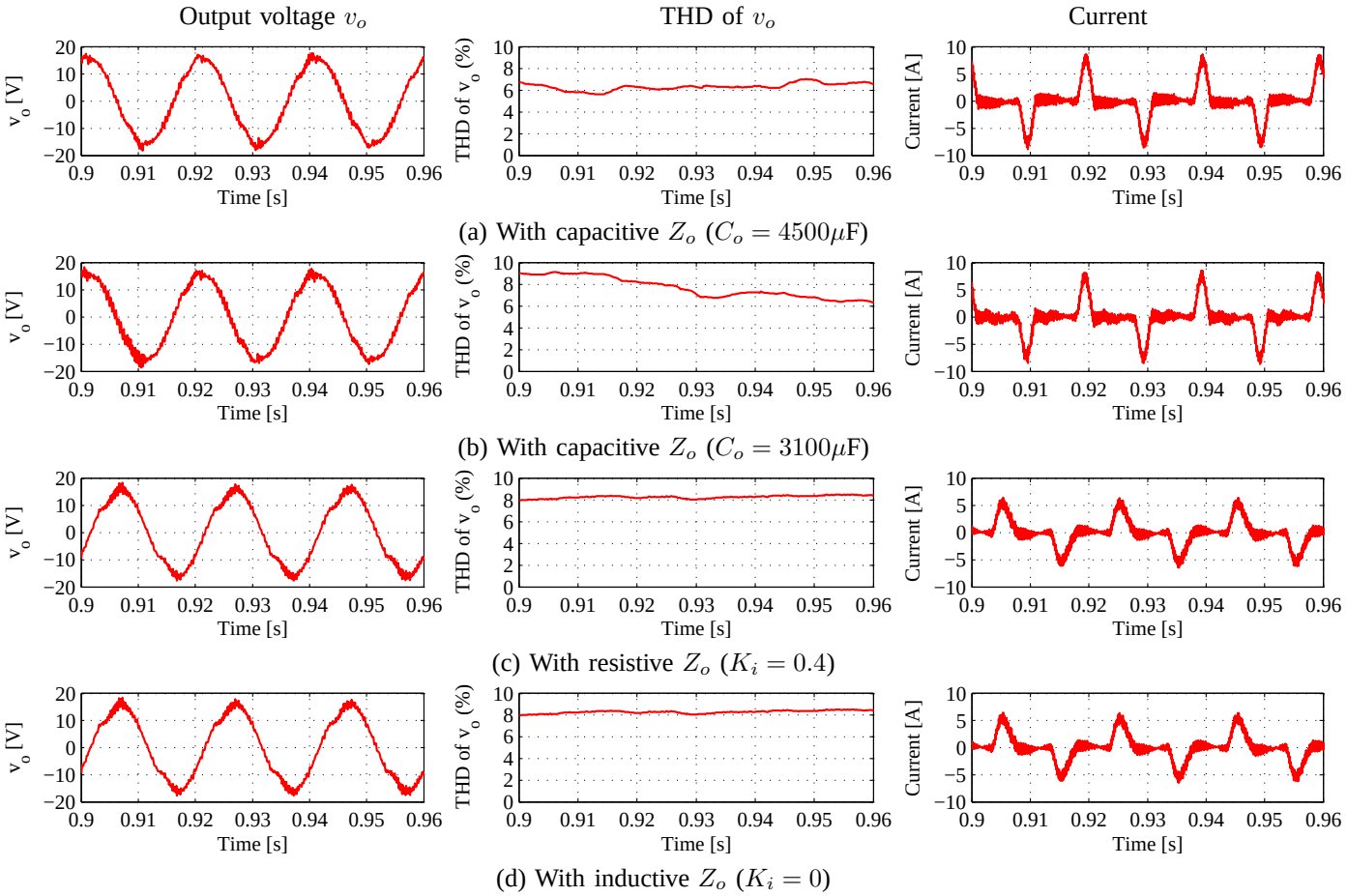


Figure 6. Simulation results for the case with $L = 0.25$mH: output voltage (left column), THD of the output voltage (middle column) and current (right column).

again improved the THD with comparison to the inverter with resistive output impedance (from 8.2% to 7.0%) and with comparison to the inverter with inductive output impedance (from 9.2% to 7.0%) as well. The best THD was obtained when the capacitor was designed to minimise the effect of the 3rd harmonics as C_o =4500μF. The output voltage, the THD of the output voltage and the current curves for the inverters with different output impedances are shown in Figure 6. Note that there are some variations in the THD of the output voltage. The values in Table II are the mean values.

V. Experimental Results

Experiments were also carried out on a test rig, of which the parameters are the same as those in the simulations, to further demonstrate the analysis. The load, which is highly nonlinear, remained the same as well. Two cases were tested: one with $L = 2.35$mH and the other with $L = 0.25$mH.

A. The case with $L = 2.35mH$

The experimental results when the inverter was designed to have different types of output impedance are shown in Figure 7. When the inverter was designed to have a capacitive output impedance to minimise the effect of the 3rd harmonics, the THD was improved by about 5% from the case with an inductive output impedance and by about 3% from the case with a resistive output impedance (with $K_i = 4$). When the inverter was designed to have a capacitive output impedance to minimise the effect of both 3rd and 5th harmonics, the THD was improved by 3% and 1%, respectively.

B. The case with $L = 0.25mH$

The experimental results when the inverter was designed to have different types of output impedance are shown in Figure 8. When the inverter was designed to have a capacitive output impedance to minimise the effect of both 3rd and 5th harmonics, the THD was improved by 2% from the case with an inductive output impedance and by nearly 4% from the case with a resistive output impedance (with $K_i = 0.4$). When the inverter was designed to have a capacitive output impedance to minimise the effect of the 3rd harmonics, the THD was improved by about 3% and 1%, respectively. It is worth noting that, when the inverter was designed to have a capacitive output impedance, the THD of the output voltage dropped below 5%.

VI. Conclusions

Two major contributions have been made in this paper. One is that the degradation mechanisms of output voltage quality

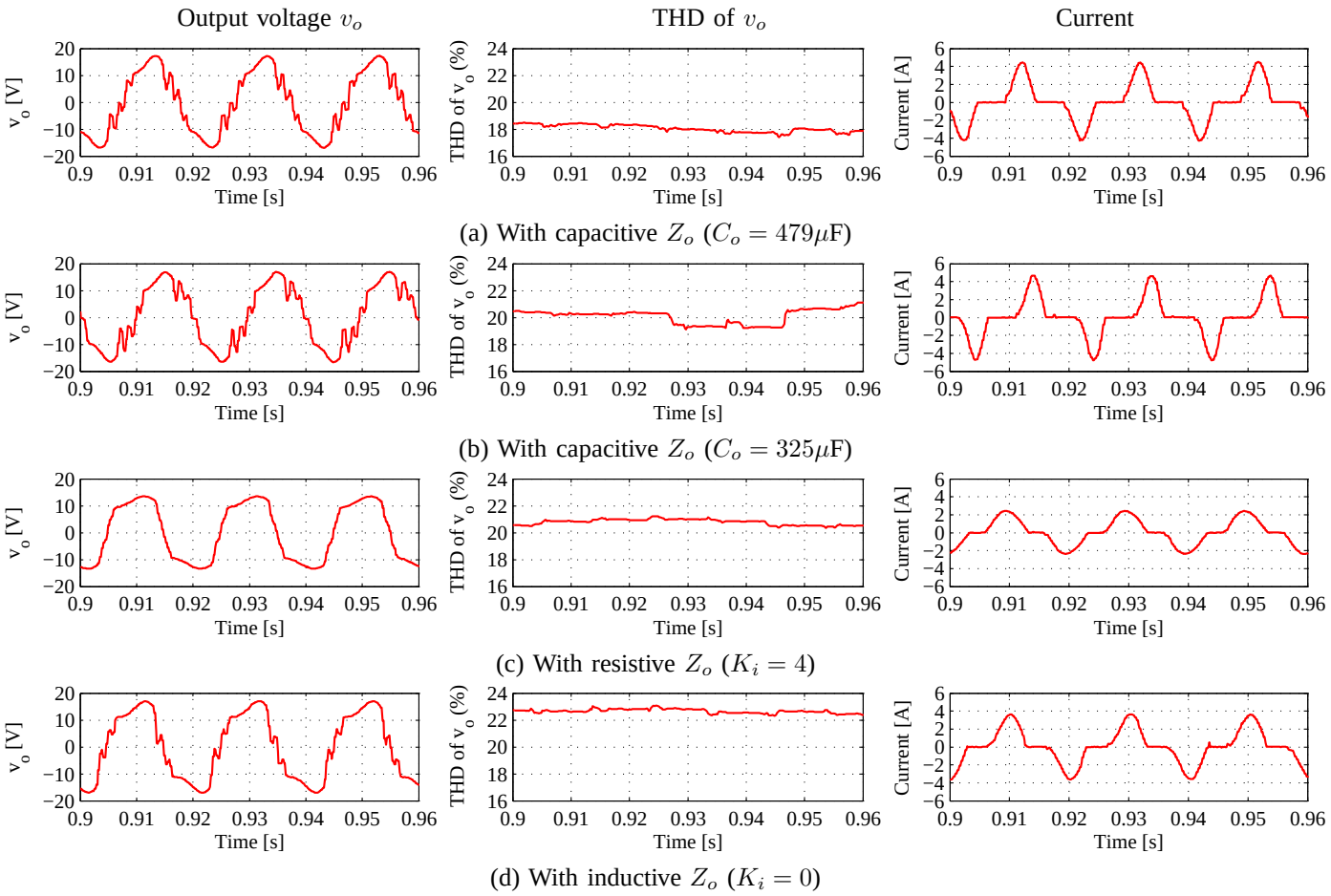


Figure 7. Experimental results when $L = 2.35$mH: output voltage (left column), THD of the output voltage (middle column) and current (right column).

of inverters have been clarified with possible ways proposed to improve the voltage quality. This can be used as the basis for developing control strategies to improve the quality of output voltage of an inverter. The other major contribution is that, following the work in Part I, the capacitive output impedance of an inverter has been designed to optimise the output voltage quality. It can be optimised to minimise the THD of the output voltage or to eliminate the effect of a certain harmonics. Both simulation and experimental results have demonstrated that inverters with capacitive output impedances are able to offer the best voltage quality among inverters with capacitive, resistive and inductive output impedances.

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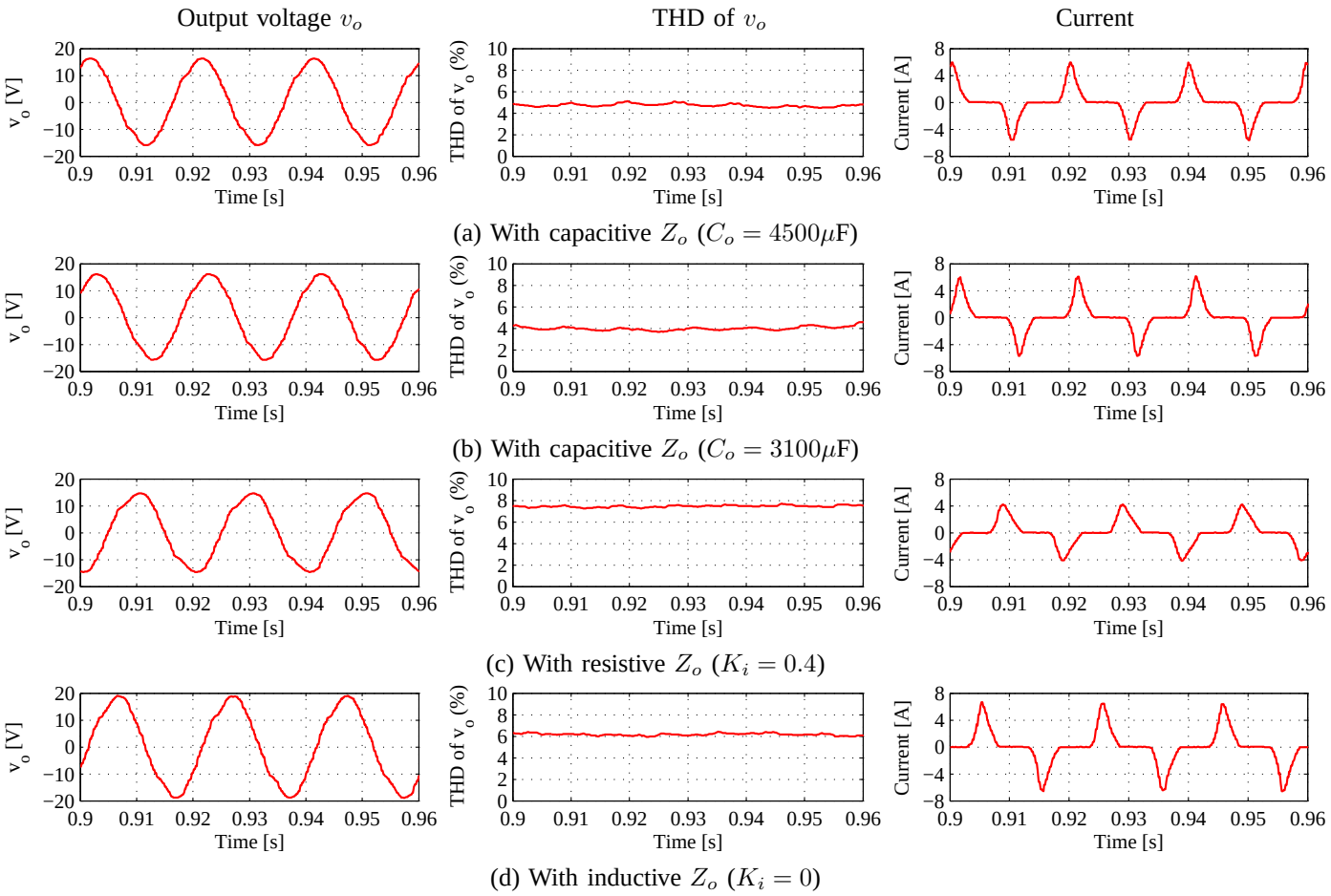

Figure 8. Experimental results when $L = 0.25$mH: output voltage (left column), THD of the output voltage (middle column) and current (right column).

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