

Resonant Switched-Capacitor Voltage Regulator with Ideal Transient Response

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Abstract— A new, small and efficient voltage regulator realized using a resonant switched capacitor converter (RSCC) technology is introduced. Voltage regulation is implemented by means of simple digital pulse density modulation (PDM). It displays an ideal transient response with a zero-order response to all disturbance types. The newly developed RSCC acts as a gyrator with a wide range of voltage conversion ratios (below as well as above unity) with constant efficiency characteristics for the entire operation range. The operation of the voltage regulator is verified on a 20W experimental prototype, demonstrating ideal transient recovery without over/undershoots in response to load and line transients. Simple design guidelines for the voltage regulation system are provided and verified by experiments.

Index Terms— Switch-mode power supplies, switched capacitor converters, voltage regulation, pulse density modulation, digital control, ideal transient recovery

I. INTRODUCTION

Following the recent proliferation of portable electronics, there has been a sharp increase in interest and demand for more compact, light, energy efficient and economical power sources [1]. As this trend continues, the requirements become more and more challenging. Tighter output voltage regulation, faster response times to load and input voltage changes and lower volume are of major concern in the design of present-day SMPS and pose a bottleneck in the advancement of the technology.

State-of-the-art voltage regulators apply switched-inductor converters combined with advanced nonlinear controllers [2]–[9] to minimize size and maximize the power processing efficiency. The main limiting factor of this general concept is the presence of a relatively large inductor that prohibits, to a large extent, miniaturization and power on-chip integration.

Present-day switched capacitor technology has become an attractive alternative for volume-sensitive applications, featuring high efficiency and economical implementation [10], [11]. However, it lacks the capability of accurate voltage regulation without the penalty of introducing losses, and its transient characteristics are limited. These limitations stem primarily from the fact that the efficiency of SCCs depends on the voltage gain [12]–[15].

A recently-developed gyrator mode resonant switched capacitor converter (GRSCC) presented in [16] has demonstrated unique potential for voltage regulation over a wide range of conversion ratios and power levels, and can be used as the main building block of a voltage regulator.

The objective of this study is to introduce a small and efficient voltage regulator that is realized by the GRSCC and a simple pulse density modulation control scheme (Fig. 1). The new voltage regulator exhibits an ideal response to load and line transients, i.e. with zero over/undershoot over the full operation range, as well as a constant efficiency profile over a wide range of voltage gain and power levels.

The main quality of the new GRSCC presented in Fig. 1 is that it disengages the efficiency of the system from the voltage gain. This is achieved by introducing an additional switching phase to balance any charge mismatch between the input and the output and, as a result, a conventional SCC topology is transformed into a voltage-dependent current source, i.e. a gyrator converter. Output voltage control is enabled by a comparator-based pulse density modulation (PDM), where the charge transfer rate to the output is controlled such that a desired voltage level is maintained. The new voltage regulator combines the virtues of both worlds: wide operation range with high efficiency (from switched-inductor converters) and reduced volume (from SCC).

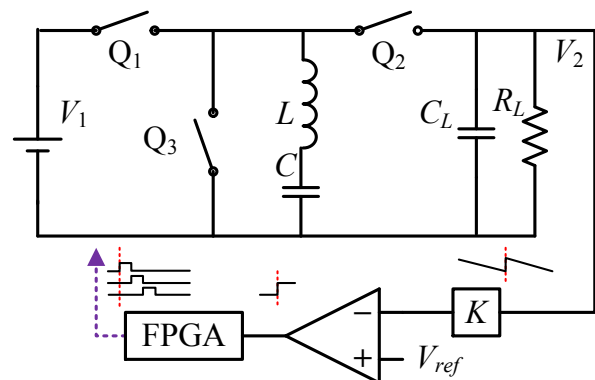


Fig. 1 The proposed voltage regulator: A new gyrator resonant switched capacitor converter and feedback loop.

II. RSCC PRINCIPLE OF OPERATION

The new Gyrator converter presented in [16] has evolved from the conventional soft-switched RSCC configuration [17]-[19]. As in the classical design, it includes two switches and a resonant tank. Additionally, a switch, Q_3 , is added to introduce an alternative resonant path of the current to balance the residual charge of the flying capacitor, i.e. restores the flying capacitor voltage to its original state by reversing its polarity. The mechanism of polarity reversal (charge balancing) lays the foundations to break the rigid connection of input/output voltage and efficiency dependency. Controlling the sequence of the switches governs the power flow direction, hence bidirectional step up/down operation.

The operation of the converter shown in Fig. 1 is described for one steady-state charge/discharge/balance cycle and is assisted by Fig. 2 that illustrates the capacitor voltage, V_C , and the resonant tank current, I_C , for the case of a non-unity step up conversion. By turning Q_1 on, a charge state (S1) is commenced, which resonantly charges the flying capacitor from the input V_1 . At zero current, Q_1 is turned off and Q_2 is turned on (state S2). At this point, the flying capacitor resonantly discharges onto the output capacitor. Since the input voltage, V_1 , and the output voltage, V_2 , are of different values, only a portion of the charge is delivered to the output and results in V_C that is different to its voltage at the starting point of S1. The amount of this voltage difference (neglecting parasitics) equals to twice the residual voltage of the flying capacitor. By turning Q_3 on (S3), the resonant tank is short-circuited. This creates the required charge-balance and reverses the flying capacitor voltage polarity such that the voltage at the end of S3 equals the voltage at the beginning of S1.

The order of the sequence governs the power flow direction, i.e. from V_1 to V_2 or from V_2 to V_1 . To deliver power from V_1 to V_2 the sequence will be (S1, S2, S3). That is, *charge* from V_1 , *discharge* on V_2 and *reverse* the flying capacitor polarity. In the case of power to be delivered from V_2 to V_1 the sequence will be changed to (S1, S3, S2). The duration of each switching state is half the resonant period and hence the switches operate at zero current switching (ZCS).

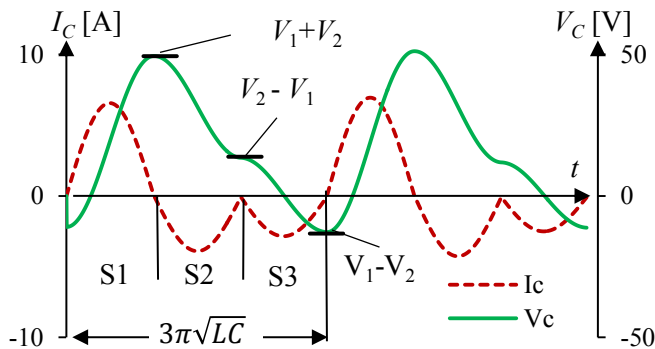


Fig. 2 Typical waveforms (obtained from simulation) of the flying capacitor voltage and current. Circuit parameters are: $V_m=20V$, $V_o=31V$, $R_s=0.15\Omega$, $L=5.2\mu H$, $C=0.25\mu F$.

Gyration ratio and power conversion efficiency

Voltage regulation is obtained by introducing a time-delay between consecutive sequences, i.e. PDM [20]-[23]. Assuming identical resonant characteristics for all states, that is, a 1/3 of the operation cycle for each state, the average input and output currents (I_1 , I_2) can be obtained and a gyrator relationship between the currents (I_1 , I_2) and voltages (V_1 , V_2) is formed as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & g^{-1} \\ g & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}, \quad \begin{cases} g = \frac{f_{max}}{f} \frac{2}{3\pi Z} \\ Z = \sqrt{\frac{L}{C}} \end{cases}, \quad (1)$$

where f is the operating frequency of the switching sequence, including the added delay. The maximum output current is obtained for zero time-delay between cycles. In this case, the converter operates at the maximum frequency, f_{max} , of three half-resonant cycles, that is:

$$f_{max} = (3\pi\sqrt{LC})^{-1}. \quad (2)$$

The relationship between the output current, I_2 , and the input voltage, V_1 can be simplified and is given by:

$$I_2 = 2V_1 f C. \quad (3)$$

For given resonant parameters L and C , the power conversion efficiency, η , can be written as a function of the series resistance, R_s , (seen in each state) and the overall voltage gain, A [16]:

$$\eta = \left(1 + \frac{\pi R_s}{2 Z} (A + A^{-1} - 1) \right)^{-1}, \quad A = \frac{V_2}{V_1}. \quad (4)$$

In the case of topology derivatives such as a voltage divider / multiplier [16], (3) and (4) would be modified using the normalized gain, \tilde{A} , instead of A , according to the base voltage gain, A_n :

$$\tilde{A} = \frac{A}{A_n}. \quad (5)$$

For a natural multiplier $A_n=2$, while for a divider $A_n=0.5$.

III. VOLTAGE REGULATION

The gyrator converter feeds the output with resonant pulsed current, in a similar operation mode to DC-DC converters in discontinuous conduction mode (DCM). To facilitate a DC output, an output capacitor, C_L , is added such that the average of the current is passed to the load (neglecting ripple). For a resistive load, R_L , the output voltage can be expressed as:

$$V_2 = I_2 R_L = 2R_L V_1 f C. \quad (6)$$

It can be observed from (6) that the input voltage to output current response is of zero order (instantaneous). This is due to the DCM-like operation of the converter which naturally

maintains per-cycle charge balance between the input and the output [21], and in the GRSCC case by the addition of the third switching phase.

If f is made controllable, the system is able to react and compensate for any changes in the input voltage, reference voltage or the load resistance such that the average output voltage is obtained without over/undershoot. The deviation of the instantaneous output voltage from the desired value is in the range of the peak-to-peak output voltage ripple, $\Delta V_{2,p-p}$, which is proportional to the operating conditions and the output capacitor, that is [16]:

$$\Delta V_{2,p-p} = 2V_1 \frac{C}{C_L} \left(1 - \frac{f}{3f_{max}} \right). \quad (7)$$

To utilize the ideal response capability of the converter derived from its DCM operation, a zero-order PDM control scheme is employed, as illustrated in Fig. 1. The output voltage is directly monitored by a comparator, referenced to a target value V_{ref} . The reference value is set to the lowest allowed voltage, taking into account the voltage ripple by:

$$V_{ref} = V_2 - \Delta V_{2,p-p} / 2. \quad (8)$$

The PDM operation of the controller is illustrated in Fig. 3. Triggered by a comparator event (when $V_o < V_{ref}$), a switching sequence of (S2, S3, S1) is initiated and followed by a time-delay until the next comparator trigger. The order of the switching sequence is arranged such that after the time-delay, which allows the output voltage to drop down to V_{ref} , a discharge state (S2) is initiated to charge the output capacitor back to $V_{ref} + \Delta V_{2,p-p} / 2$. Then, the other two states (S3, S1) are commenced to “arm” the flying capacitor, having the converter ready for a new cycle. The rate f in which the switching sequence is activated depends on the slope and the amplitude of the voltage ripple, that is, on the load current and C_L .

Following the PDM method described here, the average output voltage is constant, within the ripple margins, and is independent of R_L and V_{in} . As can be observed from (7), the ripple primarily depends on V_1 with maximum deviation of 17% from the total ripple due to changes in the load

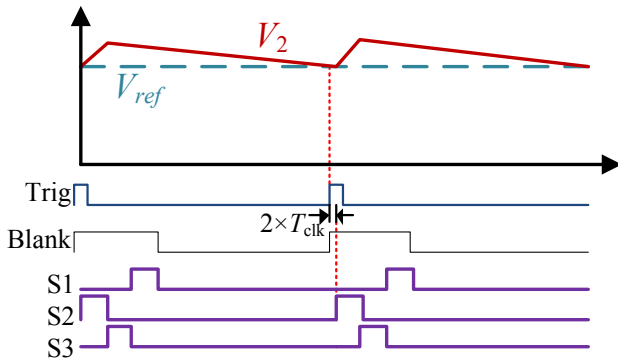


Fig. 3 Waveform relations between comparator inputs and the state signals for the proposed voltage regulator from Fig. 1. ‘Trig’ is the signal received from the external comparator, ‘Blank’ is an internal blanking signal to avoid overlapping if subsequent pulses are needed.

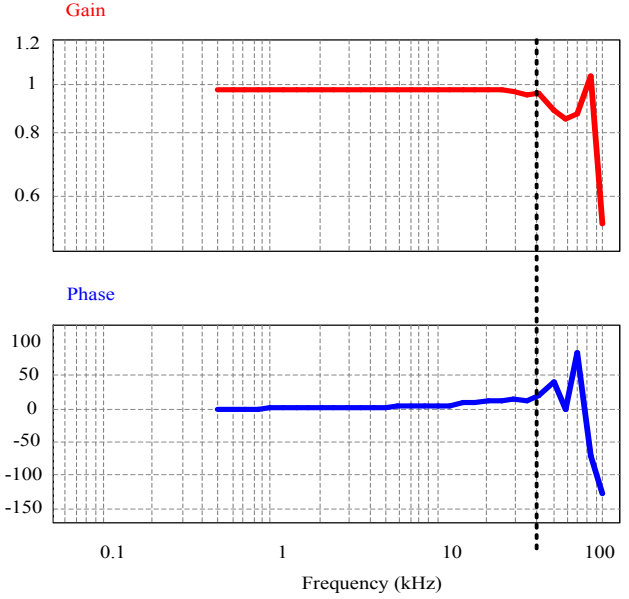


Fig. 4 Control-to-output frequency response. Top: output magnitude normalized to theoretical (ideal) output. Bottom: phase (degrees). The vertical line marks $f_s/2=35$ kHz.

(varying f). In most cases, this deviation is negligibly small, and $\Delta V_{2,p-p}$ in (8) can be approximated to an averaged ripple amplitude. Since the average output voltage is maintained at all times, i.e. no transient time, the voltage regulator can be considered to constantly operate at steady-state, and the efficiency estimated in (4) is applicable. Furthermore, no-load protection is inherent since no triggering will occur.

Upon startup, the output capacitor voltage is zero ($V_2 < V_{ref}$) and the controller reduces the time-delay to a minimum, constantly charging C_L until the desired voltage is obtained. To limit inrush currents, V_{ref} can be made to slope up slowly.

IV. VALIDATION OF THE ZERO-ORDER RESPONSE

To verify the control-to-output zero-order response feature of the GRSCC, a frequency response simulation has been constructed in PSIM (Powersim inc.). The triggering algorithm has been implemented by a C block generating a Frequency Modulated (FM) control command with carrier frequency of 90 kHz and modulating signal (magnitude) of 20 kHz. Then, the rate of the modulating signal has been swept while measuring the ratio between the output current and the magnitude of the modulating signal. Fig. 4 shows the resultant frequency response, it can be observed that the control-to-output response is virtually constant in magnitude with zero phase lag over the entire operation range, i.e. up to half of the frequency of the lower sideband of the control command. This implies that the converter is capable of accommodating load transients with zero-order response up to the rate of half the switching frequency.

V. DESIGN CONSIDERATIONS

The design procedure of a voltage regulator based on the GRSCC topology is described through an example of a 20W step down inverting voltage regulator with the target values of $V_o = 5V$, $V_{in} = 8$ to $15V$, $f_{max} < 500kHz$.

First, the values of L and C are derived by combining (2) and (3) and taking into account the worst-case of f_{max} , $V_{1,min}$ and $I_{2,max}$ as follows:

$$C = \frac{I_{o,max}}{2V_{in,min}f_{max}} \quad (9)$$

$$L = \left[(3\pi f_{max})^2 C \right]^{-1}$$

The second step is to estimate the values of the rms current that circulates in the resonant tank. This is done for the selection of the switches as well as to determine the physical sizes of L and C . Considering (4) and after some manipulations, the rms current can be expressed as:

$$I_{rms} = \sqrt{V_2 I_2 \frac{\pi}{2Z} (A + A^{-1} - 1)} \quad (10)$$

Finally, given a desired target voltage and defining the allowed voltage deviation, the output capacitor value and the reference voltage are calculated using (7) and (8) respectively.

Given the above parameters, the inductance and capacitance are calculated by (9) to be $L = 0.1\mu\text{H}$ and $C = 0.56\mu\text{F}$. These were chosen such that 20W of power can be processed from the input range specified. Given a typical loop resistances of $R_s = 20\text{m}\Omega$, the expected efficiency is in the range of 85% to 92%. Similarly to switched-inductor PDM converters, the rms currents are relatively higher than conventional converters that operate in CCM. As opposed to other PDM converters, no additional losses are present thanks to the resonant current and the resultant soft switching operation. In this particular design the rms current is estimated to be 12A at maximum effort. The main problem with higher rms currents is the stress on the flying capacitor. This can be overcome by paralleling capacitors of smaller values. The inductor however is of small value and can be realized without a ferrite core.

The inductor, although having a small inductance value, has to sustain relatively high rms currents. However, in contrary to the magnetics design in SICs, the per-cycle energy that is stored in the inductor is zero. As a result, the main factor of the inductor sizing stems from the core losses, rather than saturation limits. A convenient way to estimate the volume of the magnetic element is by the area product A_p , which can be expressed as:

$$A_p = \frac{L \Delta I_{rms}}{JK \Delta B} \quad (11)$$

where L is the desired inductance, ΔI is the maximum current variation through the inductor, ΔB is the maximum flux density variation due to ΔI , J is the current density that is allowed through the winding, and K is the fill factor.

For the particular case of the GRSCC, after some manipulations (11) can be rewritten as:

$$A_p = \frac{\max(V_1, V_2) I_{rms}}{3\pi JK \hat{B} f_{max}} \quad (12)$$

Using a ferrite core, the area product of the inductor needed for the GRSCC described in the example above is relatively large, comparable with an inductor for a buck-boost converter, designed according to the same specifications, operating in continuous conduction mode (CCM). However, since the inductance value that is required for the GRSCC is quite low ($0.1\mu\text{H}$), a ferrite-less (i.e. air core) construction is feasible. Consequently, higher peak flux density, \hat{B} , is allowed, resulting in a significantly smaller A_p . A normalized comparison between the required area products for various voltage regulator topologies and operation modes has been carried out and is summarized in TABLE I. A significant reduction of the inductor volume can be noticed for a GRSCC-based voltage regulator by one-order of magnitude, when compared to a buck-boost of the same features.

TABLE I. COMPARISON OF THE AREA PRODUCT, A_p BETWEEN VARIOUS CONVERTERS DESIGNED FOR VOLTAGE REGULATION

	Buck-boost		Buck	GRSCC	
	CCM	BCM ^a	BCM ^a	Ferrite	Air
\hat{A}_p ^b	50	12	7	37	1
\hat{B} [T]	0.2	0.2	0.2	0.05	2
L [μH]	7	0.7	1.7	0.1	0.1

a. Boundary Current Mode

b. Normalized to GRSCC with air core

VI. EXPERIMENTAL RESULTS

To verify the operation of the converter as a voltage regulator and to demonstrate the ideal transient features of the system, a 20W experimental prototype was realized using an inverting bridge configuration (Fig. 5). The target parameters and the list of components used are summarized in TABLE II. A digital PDM controller was implemented on a FPGA (Altera Cyclone IV). The ZCS operation of the gyrator RSCC is sensitive to input voltage variations, but since the input range is moderate, satisfactory results were achieved by pre-calibration.

The controller was programmed to execute a pulse sequence for the drivers whenever a trigger from a comparator was sensed for two subsequent clock-cycles or more, as illustrated in Fig. 3. An internal blanking signal was added to prevent execution overlapping during startup or when rising V_{ref} , creating sequential executions at maximum frequency, without the need for any dedicated startup routine.

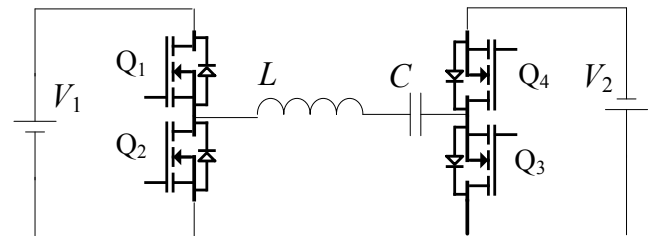


Fig. 5 The experimental inverting scheme, using four MOSFETs

Fig. 6 demonstrates the ideal transient response of the voltage regulator with zero-order response for both light-to-heavy and heavy-to-light modes for zero to nominal current (4A) load transients and for 1A to 3.5A. The deviation of the output voltage from its average value is measured to be around 100mV. A minor discrepancy is evident between the calculations of L and C for the effective operation range and is due to practical efficiency which is not taken into account in (9). This resulted in a slightly higher bound on the input voltage of 9V instead of the original 8V to deliver power of 20W to the output.

TABLE II. EXPERIMENTAL SPECIFICATIONS

Component	Value	Notes
C	1 μ F	10 \times 0.1 μ F
L	0.18 μ H	Air windings
R_s (per loop)	48m Ω	
f_{max}	250kHz	
η_{min} ; η_{max}	0.72 ; 0.83	
$V_{1,min}$; $V_{1,max}$	8V ; 15V	
I_2 , (rated) ; V_2	4A ; 5V	
C_{load} ; $\Delta V_{2,p-p}$	50 μ F ; 0.5V	5 \times 10 μ F

VII. CONCLUSIONS

A new, small and efficient voltage regulator based on resonant switched capacitor technology has been developed. Detailed analysis of the new RSCC as well as design guidelines, in the context of voltage regulation, are provided and verified by simulations and experiments.

The results have demonstrated that upon a load transient within the nominal value of the design, the operating frequency can be immediately updated (in one switching cycle) to compensate and adjust to the changes. This is similar to SICs operating in DCM and controlled by PFM. This is in contrast to CCM SICs where the inductor current has to build up/down to the new steady-state level, an action that takes several cycles to complete. In the voltage regulator presented here, any transients (line or load) occurring at a rate that is lower than half of the maximal switching frequency, $f_{max}/2$, can be compensated without any under/overshoot nor delay, i.e. a zero-order response.

A power density analysis has been carried out to estimate the expected volume of the magnetic element. It revealed that when considering a conservative design the required area product (volume) of the magnetic element is within the range of its comparable candidates (e.g. a buck-boost converter). However, due to the significantly lower inductance value that is required for the operation of the GRSCC, a ferrite-less design is feasible, which increases the power density of the voltage regulator at least one-order of magnitude.

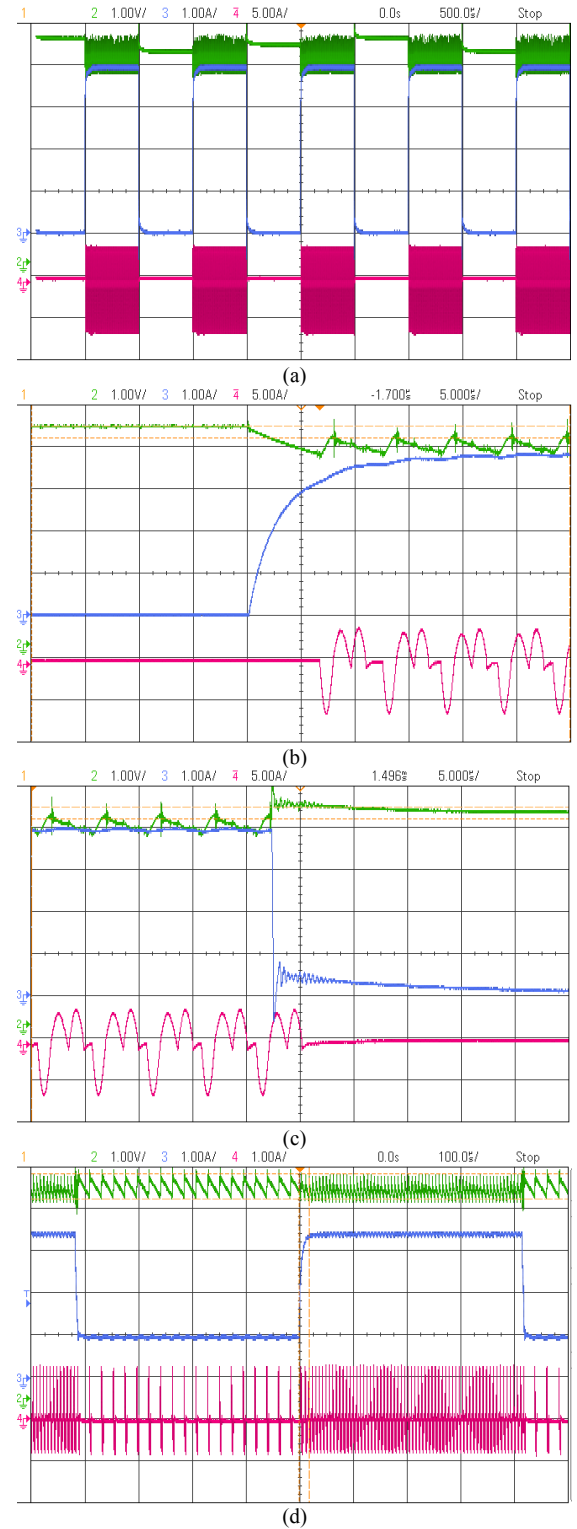


Fig. 6 Screenshots obtained from the experimental setup. $V_1=12V$, $V_2=5V$, $I_2=\{0A, 4A\}$. Signals are: top- V_2 , mid- I_2 , bottom- I_C . (a) zoomed out view on voltage stabilization with full range of load step, $I_2=\{0A, 4A\}$ switched repeatedly at 1kHz, (b) light-to-heavy load step, $I_2=\{0A, 4A\}$, (c) heavy-to-light load step, $I_2=\{4A, 0A\}$ (d) mid-range load step variation, $I_2=\{1A, 3.5A\}$ switched at 1kHz.

Size estimation of the output capacitor has found that although the output filter has to be sized for a higher peak current, the fact that the voltage regulation can be obtained with zero-order response, i.e. continuous steady-state operation, significantly reduces the required capacitance value and size.

Combining the benefits of the relatively simple converter design, the virtually no-effort approach for voltage regulation presented, and high power density of the passive components, the GRSCC-based voltage regulator can be considered as an attractive candidate for voltage regulation applications that require high response rate. Furthermore, the possibility of a ferrite-less magnetic design increases the power density of the converter, and allows for the power supply to be fully integrated (omitting the output filter) on a chip.

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