The Augmented Modular Multilevel Converter

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ABSTRACT

The Controlled Transition Bridge (CTB) is a class of converter topology that combines series connected semiconductor "director valves" with chains of switched capacitor modules, "chainlink circuits", in such a way that the director valves carry the main current for a significant portion of the period and the chainlink circuits provide a controlled traverse of voltage between different director valves conducting. This combination is applicable to HVDC where efficiency is paramount, since it allows thyristors or diodes to be used for the director valves to reduce the conduction losses, with the chainlink circuits providing commutation and direct control of the rate of change of transition voltage. Since the chainlink portion of the AMMC only has to manage the transition between the upper and lower director valves, the size of the capacitors in the individual sub-modules can be reduced, reducing the converter footprint. Also the trapezoidal waveform that results can be tailored to give reduced harmonic levels, so reducing filtering required for the AC waveform to meet regulations on distortion at the point of common coupling for the converter (PCC).

An analysis is presented of an example of this type of converter where a modular multilevel converter (MMC) is combined with a conventional thyristor bridge, the Augmented MMC (AMMC). Various aspects of the operation of the bridge are discussed, including the management of the charge in the chainlink capacitors and the converter losses.

Introduction

High Voltage DC transmission has been dominated by thyristor based Line Commutated Converters (LCC) for many years. The LCC has the capability of transmitting thousands of megawatts of power and is very efficient. While the approach has many advantages there are a number of technical limitations that means it cannot fulfil the future ambitions of, for example, providing a DC connection to offshore wind farms or being connected as part of a large scale DC grid. For this the Voltage Source Converter (VSC) provides the main alternative and in the 1990's there was a major technical effort into developing VSC systems based on six pulse bridges using the principles developed for variable speed drives. The Modular Multilevel Converter (MMC) proposed by Marquardt, [1], presented an alternative method that has the main advantages that the output waveform needed little or no filtering to achieve the specified level of harmonic distortion and that it requires very little switching from the IGBTs, giving an overall efficiency of the converter that is much higher than for the six pulse VSC bridge, although still worse than for the LCC type converter. Investigations into alternative topologies combining series connected semiconductor "director valves" with chains of switched capacitor modules, "chainlink circuits", are now offering the promise that the next generation of HVDC converters will be more efficient and have a reduced footprint. Examples of such converters are given in [2] and [3]. One class of these new converters is the Controlled Transition Bridge (CTB) where the director valves carry the main current for a significant portion of the period and the chainlink circuits provide a controlled traverse of voltage during the transitional period between the different director valves conducting,

resulting in a trapezoid waveform being generated, Fig. 1. A form of this kind of converter is the Augmented Modular Multilevel Converter (AMMC) that may be described as a combination of six pulse VSC bridge and a MMC, Fig. 2 It is proposed that in normal operation the chainlink circuits will, in addition to managing the voltage transition, provide soft-switching of the director switches to the point that the IGBTs shown in the figure can be replaced by thyristors and the chainlink circuits perform a full commutation at the end of the director switch conduction period.

The Trapezoid Waveform

The operation of the AMMC centres on generating trapezoid waveforms at the AC terminal of the converter. Fig. 1 illustrates the basic form of a trapezoid waveform however another form of transition waveforms will be used that gives greater flexibility and improved Total Harmonic Distortion (THD). [4] describes the derivation of a form of trapezoid waveform that allows the THD to be reduced to the region of 1%, a level small enough to be used in conjunction with minimal filtering within HVDC while also giving the ability to regulate the fundamental of the waveform. Fig. 3 presents a range of such curves that maintain low THD for a range of fundamental magnitude. The information required for defining these curves is held within a look up table with a control input of the required ratio of fundamental magnitude to the DC rail voltage.

Converter Operation

General

Having two converter bridges overlaid means that there are a number of ways in which the converter can be operated. The main purpose in combining the converters is to allow a low loss “director switch”, such as one based on thyristors, to be used in such a manner that each switch only operates once per power cycle and that the overall effect is to provide an independent controllable AC voltage source. So the director valves will conduct current during the flat topped region of the trapezoidal waveform and the chainlink circuits provide a controlled voltage traverse between these conduction states.

Beyond the basic AC functionality of the converter it is important that other functions are managed over the power cycle. For the MMC it is well recognised that current can circulate through the converter in an undesirable manner in normal operation, [5], so for the AMMC it is important that the chainlink circuits are used to regulate current flow within the bridge. For most of these conditions it is normally important to ensure that the current in the chainlink circuit is driven to zero; however it is also important that the charge in the sub-module capacitors is reset to a defined value following the transition. The operation of the converter will inevitably be primarily that of a “quasi-square”, six pulse converter being modified by the operation of the chainlink circuits. Thus, with no compensation the DC current will have a high level of ripple, so it is also important that the chainlink circuits are used to pass current between the DC rails to cancel this.

Transition Operation

The top and bottom chainlink circuits each have a series inductor to allow them to operate as a current source when the director switches are closed. With a third inductance associated with the AC system, for the transition period it is necessary to regulate the flow of current in each inductance. For continuous operation such as for the MMC, a reasonable control can be configured that will regulate these currents effectively; however for the proposed discontinuous operation of the AMMC such a control is not sufficient.

The six pulse bridge operating as an inverter using the principle of quasi square wave in which the converter is switched at a 50:50 ratio, typically used for variable speed drives at high speed, will have a DC ripple equivalent to that of a bridge rectifier. For this arrangement the current is directed to the positive or negative rail. For the trapezoid

waveform the equivalent is that the current direction is changed mid-way through the transition. This form of operation has the clear requirement that the current flow must be defined by, for example, using one of the chainlink circuits as a voltage source, with the opposing chainlink circuit being used in current mode with the reference set to zero, these modes being swapped midway through the transition operation.

Chainlink operation when a director switch is closed – associated chainlink

When a director switch is closed the associated chainlink circuit and its associated inductance have their terminals shorted. At the instant the director switch is closed current becomes trapped in this inductor. This current needs to be set to zero so that the director switch takes all the current, so ideally the chainlink should be utilised to regulate this. The chainlink circuits are composed of half bridge circuits making the converter operation more efficient, then the voltage cannot be reversed giving only control of one polarity of trapped current. To resolve this an additional four quadrant sub-module is added to provide this functionality of regulating the current in the director switch when it is closed. At this time the chainlink circuit will be placed in bypass.

The possible use of thyristors for the director switch will require that the voltage from the chainlink must be capable of varying so as to draw the current out of the thyristor circuit to allow the thyristors to commutate off. This could also be managed by this additional four quadrant sub-module.

Chainlink operation when a director switch is closed – opposing chainlink

When a director switch is closed, the opposing chainlink circuit must provide two functions: -

- It can draw a compensating current to restore the energy in the chainlink circuit following the variation imposed by a transition.
- It can draw current between the rails to cancel the ripple in the DC.

The two functions must not conflict so the current injection to balance the capacitor charge must have a significantly lower frequency variation than that for the ripple cancelation. While much of the bridge control can be performed on a per phase basis, the ripple cancelation must be done on the basis of the overall converter state. The use of the star/delta transformer means that the AC phase currents must sum to zero. With the three phases being directed to one or other DC rail, the ripple can be cancelled by passing the difference for the DC rail carrying a single phase current and the effective DC current to the opposing rail.

Bridge states

Table I shows the operation states for the converter bridge over a power cycle. Primarily the director valve states are shown with the associated control states for the chainlink circuits. Also as a reference for compensating the DC ripple, the flow of current in the DC rails is shown, taking note of the sign convention for current and power flow as defined in Fig. 4. In this the chainlink circuit is controlled either under voltage control (V), under current control during the transition with a zero current reference (I_1), voltage control to the DC rail with an auxiliary four quadrant sub-module regulating the current to zero (I_2), or under current control where the voltage is across the ±DC rails and the current reference is a combination of DC link ripple current combination and sub-module capacitor voltage compensation (I_3).

Control Functionality

The use of “dual slope” trapezoid waveforms have the majority of their solutions with the intercept with the DC rail outside the $\pi/6$ limit. Where this occurs there are overlap periods where one transition is finishing and another is starting. The significance of this is that the current to compensate for the DC ripple cannot be shared between two phases during this period.

Devices	Director Valves						Chainlink Circuits						DC Currents	
Phase range	SW1	SW4	SW3	SW6	SW5	SW2	CL1	CL4	CL3	CL6	CL5	CL2	+Ve	-Ve
0 - π/6	-	-	-	On	On	-	V	I_1	I_3	I_2	I_2	I_3	I_A+I_C	-I_B
π/6 - π/3	On	-	-	On	-	-	I_2	I_3	I_3	I_2	V	I_1	I_A+I_C	-I_B
π/3 - π/2	On	-	-	On	-	-	I_2	I_3	I_3	I_2	I_1	V	I_A	-I_B-I_C
π/2 – 2π/3	On	-	-	-	-	On	I_2	I_3	I_1	V	I_3	I_2	I_A	-I_B-I_C
2π/3 – 5π/6	On	-	-	-	-	On	I_2	I_3	V	I_1	I_3	I_2	I_A+I_B	-I_C
5π/6 - π	-	-	On	-	-	On	V	I_1	I_2	I_3	I_3	I_2	I_A+I_B	-I_C
π - 7π/6	-	-	On	-	-	On	I_1	V	I_2	I_3	I_3	I_2	I_B	-I_A-I_C
7π/6 – 4π/3	-	On	On	-	-	-	I_3	I_2	I_2	I_3	I_1	V	I_B	-I_A-I_C
4π/3 – 3π/2	-	On	On	-	-	-	I_3	I_2	I_2	I_3	V	I_1	I_B+I_C	-I_A
3π/2 – 5π/3	-	On	-	-	On	-	I_3	I_2	V	I_1	I_2	I_3	I_B+I_C	-I_A
5π/3 – 11π/6	-	On	-	-	On	-	I_3	I_2	I_1	V	I_2	I_3	I_C	-I_A-I_B
11π/6 – 2π	-	-	-	On	On	-	I_1	V	I_3	I_2	I_2	I_3	I_C	-I_A-I_B

Table I: Bridge states over a power cycle

The control uses three identical controls for the phases, each taking in a phase angle for that respective phase and generating a "state" value to determine which of the director switches are conducting. The angle value is also used to determine the voltage reference value for the transition waveform. The state value for each of the three phases are passed to a central control to determine the overall state of the converter and so derives the various reference current demands for the I_3 control function to cancel the DC ripple.

The Sub-Module Capacitor Value

To obtain a first estimate of the capacitor value required for the submodules within the chainlink element, the capacitors are assumed to be pre-charged with an overall capacitor energy at the start of a transition given as:

$$E_C = \frac{1}{2} \cdot C_m \cdot \sum_{i=1}^{N_m} V_{Ci}{}^2 = \frac{1}{2} \cdot C_m \cdot N_m \cdot V_{Cav}{}^2 \tag{1}$$

Where N_m is the number of modules, C_m is the capacitor value and V_{Ci} is the voltage for the i^{th} capacitor in the chainlink circuit and V_{Cav} is the average voltage for all the capacitors in the chainlink circuit. Taking the peak capacitor energy, the change in capacitor voltage will be given as:

$$E_C + \Delta E = \frac{1}{2} \cdot N_m \cdot C_m \cdot \left(V_{Cav} + \Delta V_C\right)^2 \tag{2}$$

Simplifying this expression and solving for the quadratic gives:

$$\frac{\Delta V_C}{V_{Cav}} = -1 \pm \sqrt{1 + \frac{\Delta E}{E_C}} \tag{3}$$

If the sub-module is based on, for example, a 3.3kV IGBT, the operating voltage should ideally be in the range of 1.7kV to 1.8kV. From this the peak ripple might be selected to be in the region of ±150V. From equation (3) the base chainlink energy at the start of the cycle must be 800kJ and a capacitor value in the region of 1.5mF is required, which is a significantly smaller value than for a conventional MMC of the same rating.

Modelling

Power Circuit

Fig. 5 shows the form for the MATLAB/Simulink model of the AMMC for a 700MW/200MVAr rated system operating with a DC link voltage of ±300kV. The power circuit uses ideal DC voltage sources and distributed parameter models to represent the 460km HVDC cable transmission system. A star/delta transformer connects the converter to the AC system, this being represented by an ideal voltage source of nominally 300kVp and a series reactor equivalent to 2000MW short circuit rating. A low Q harmonic filter has been used to reduce the converter harmonic content. The converter bridge is represented as three individual phase blocks as shown in Fig. 6. The top and bottom voltage sources in Fig. 6 connected in series with the chainlink circuits represent the four quadrant sub-module to be used for zeroing the current in the series inductor when the director switch is closed. The director switches are presently represented by the switches shown, so no attempt has been made to represent the need to commutate off the thyristors.

The representation of the chainlink circuit is shown in Fig. 7. To obtain time efficient modelling the sub-modules are represented in Simulink with the enabled sub-modules having their calculated voltages summed to give a value that is passed to the voltage source within the electrical circuit to give the overall chainlink circuit voltage. The antiparallel diode represents the lumped diodes in the sub-modules and the IGBTs allow the circuit to be blocked while its anti-parallel diode represents the lumped top diode in the sub-modules that allows the sub-modules to be charged when the converter is in the blocked state. During this condition the current passes through all the sub-modules, so the "or" gate on the left of the model causes the measured current to be passed to all the integrators representing the individual sub-modules.

Control

The operation of the model is open loop so the control is composed of three main blocks: -

- A block that takes in the values of time, power, quadrature power, DC voltage and AC voltage and computes the time varying values of phase, AC voltage and converter voltage. Reference values of AC and DC current are also computed.
- A block that provides the main control function as described in the section "Bridge states" above. This includes the various controls for the different operating modes of each phase, the capacitor selection function and the capacitor charge balancing functions. The transition used is as presented in [4] and is defined using lookup tables based on a ratio of the peak fundamental voltage to the DC voltage. Due to the droop in the DC rail voltage this ratio is continuously updated through the first block.
- A block that collects the main analysis functions for the model, including the analysis of conduction and switching losses for the converter.

Loss Analysis

The analysis of losses within the chainlink circuit is carried out by processing the instantaneous current flowing within the sub-modules and the switching state of each sub-module. For the conduction loss it is standard practice to approximate the on-state drop of the semiconductor devices by a slope resistance and a zero current voltage offset. Similarly the switching loss can be estimated by applying an approximate straight line to the energy curve. Typically for the IGBT the E_{on} and E_{off} curves have an intercept value that is sufficiently small that it may be discounted. For the diode there is no "turn-on" loss but the energy loss as the device recovers, E_{rec}, can be significant. For the director switch a GTO has been selected rather than a thyristor. Like the IGBT this also has a turn-off and turn on energy loss that has been approximated by a slope straight line having a slope and intercept value. Table II shows the detailed loss table for a number of devices considered for use in

the model. For the modelling described below the Mitsubishi IGBT was used for the chainlink circuits and the IXYS GTO was used for the director switch.

Device Function	Device	Characteristic	Intercept	Slope
Sub-module IGBT	Mitsubishi CM1500HC-66R	Conduction loss	1.6V	1.11V/kA
		Turn on energy	2mJ	0
		Turn off energy	0.7J	1.4J/kA
Sub-module anti-parallel diode	Mitsubishi CM1500HC-66R	Conduction loss	1.0V	0.8V/kA
		Turn off energy	0.9J	0.9J/kA
Director Switch GTO	IXYS G3000TF450	Conduction loss	1.6V	0.9V/kA
		Turn off energy	0	2.8J/kA
Director Switch anti-parallel diode	Westcode E2400TC45C	Conduction loss	1.4V	0.9V/kA
		Turn off energy	0	2J/kA

Table II: Semiconductor Loss Data Used in the Modelling

For the conduction loss the current flow will vary through the sub-module according to whether it is gated on or off and according to the polarity of the current flow through the chainlink circuit. Since the switching state for the sub-modules is given as a vector of Boolean values defining the state for each sub-module, the resulting multiplication between the loss values for the diode and IGBT will be a vector of loss values, defining loss in each sub-module. The overall semiconductor conduction loss for the chainlink circuit is thus the sum of all these terms. The conduction loss for the Director Switch is merely determined by whether the current flowing is forward, i.e. through the thyristor or reverse, through the anti-parallel diode

The switching loss analysis is addressed in a similar manner to that for the conduction loss, except that a switching action must be detected. The loss value is derived from the current the switching state is compared to a delayed version of itself in conjunction with the polarity of the current flow, giving six main values for the four conditions of the two IGBTs turning on and off and the diode recovery. The IGBT losses are then summed to give the total losses for the upper and lower IGBT.

The switching loss analysis for the Director Switch considers the turn on and off for the thyristor as being defined by the gating signal whereas the turn on and off of the diode is determined by the polarity of the current.

All the output data from the four blocks loss analysis blocks contain transient spikes representing the instantaneous switching loss terms. To give an average value they are passed through a unity damped second order filter with a 1Hz knee point.

Model Operation

General

Operating the model at 700MW, 200MVAr the current flow in phase A of the bridge is shown in Fig. 8. This shows clearly the manner in which the phase current is passed through the top and bottom chainlink circuits, with a “cut out” where the current is transferred to the top and bottom director switches. The transfer is relatively slow due to the voltage control representing the two four quadrant chainlink circuits being used to regulate this current having a voltage being restricted to a maximum of 4kV. While the director switches are in operation current still passes through the opposing chainlink to restore the sub-module capacitor charge and to cancel ripple in the DC ripple. This current can be seen to subtract from the Director Switch current.

AC and DC voltages

The transformer secondary voltage is shown in Fig. 9, clearly showing the dual slope trapezoid waveform but including a number of notches due to current being transferred from one path to another within the bridge. The transformer provides a degree of filtering for these high frequency notches, which detract from the harmonic distortion (THD) for the transformer primary voltage. Fig. 10 shows that these notches are now small but are clearly visible so the resulting harmonic distortion as presented in Fig. 11, while small, is significantly higher than the 0.5% THD level typically required for VSC.

The transient spikes appear in the DC circuit, which is the reason the LCR filter had been added between the bridge and the cable as shown in Fig. 5. Fig. 12 shows the DC voltage ripple at the terminals of the DC cable showing this is acceptably small at 3kVp-p. The current in the DC part of the bridge circuit is shown in this diagram and, discounting the transient spikes, can be seen to have a ripple of nominally 100Ap-p.

Chainlink Circuit Operation

Section "The Sub-Module Capacitor Value" discusses the derivation of the capacitor value required for the chainlink sub-modules for the converter. Fig. 13 shows both the number of sub-modules enabled and the average sub-module capacitance over a power cycle for phase A. The number of sub-modules used for each chainlink circuit within the model is 360 and this figure shows that the minimum required number of sub-modules is nominally 350.

The peak to peak capacitor voltage is nominally 300V in agreement with the requirement given above.

Converter Losses

To obtain the loss figures the model needed to be run for 2s to ensure the filters providing the average loss figure settle to a steady value. Because the model is open loop and, for the present, does not include a compensation for the AC voltage droop, the power transmitted needs to be optimised by trimming the AC voltage to 310kVpp giving 645MW. Table III presents the losses per device for the model, with these scaled to represent the per phase losses as a percentage of the full converter power being transferred. From this the results show that the nominal losses for all the semiconductors are less than 0.6%.

	Top conduction (W)	Top switching (W)	Bottom conduction (W)	Bottom switching (W)
Bottom IGBT	303.7	360.6	304.5	354.1
Top IGBT	46.36	177.3	46.41	171.8
Bottom Diode	16.07	194.5	15.99	187.8
Top Diode	40.54	210.8	42.6	206.5
DS Thyristor	745	0	745.8	0
DS Diode	1.458	8.722	1.448	8.669
Total for phase	1,288,020W			
Total for converter	0.599% of 645MW			

Table III: Loss figures for P = +700MW (Inverting), Q = +200MVAr, VAC = 310kVp

Conclusons

The development of a model to demonstrate the operation of the Augmented Modular Multilevel Converter has been described. The operation of the converter is complex and a strategy for ensuring both a low AC total harmonic distortion while maintaining a low DC ripple must be chosen. The main potential advantage of the converter is that it should be able to utilise a director switch made up of thyristors or equivalent, so provided the control

strategy ensures a significant conduction period for these over the power cycle, the losses should be significantly less than for the MMC. The calculation of losses for the detailed operation of the converter suggests that the results will be in the region of 0.6% compared to the notional 0.7% loss typical for an equivalent MMC.

In addition to the above the energy ripple associated with the chainlink circuit operation is reduced with the result that the sub-module capacitors can be significantly reduced to 1.5mF, around one quarter of that used in the MMC, so reducing the footprint of the converter.

The results show the main problem with the converter is that the process of switching between different channels within the bridge is leading to transient spikes appearing in the terminal waveforms. [4] suggests that using a trapezoidal waveform with a two slopes per quarter cycle during the transition will yield a waveform with a THD of less than 0.5% whereas the present THD is 1.5%. Similarly, with the transient spikes removed the DC ripple is of the order of 100Ap-p, suggesting that there should be no requirement for a capacitor on the DC link. Thus further work must address this weakness.

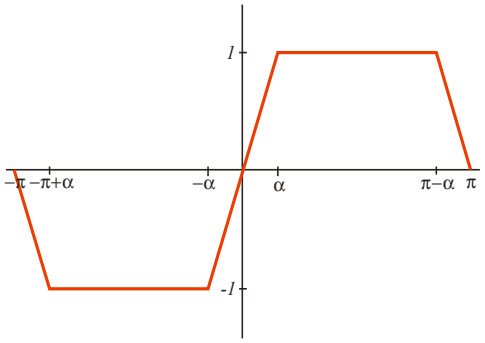

Fig. 1: Basic trapezoid waveform

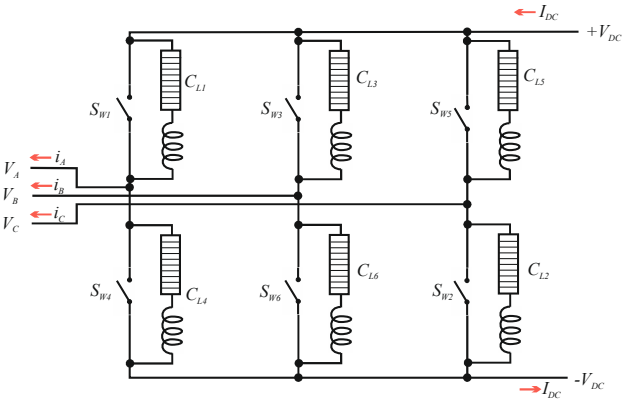

Fig. 2: Augmented MMC Topology (one phase)

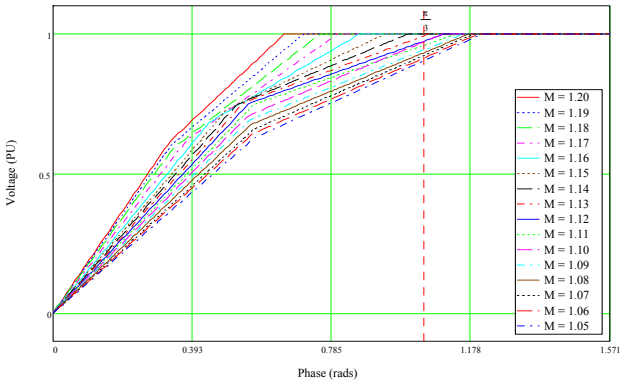

Fig. 3: Range of waveform solutions using minimisation

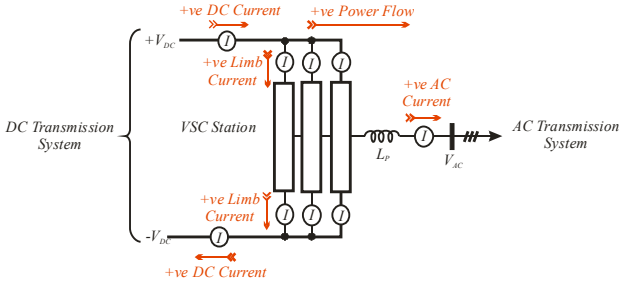

Fig. 4: Polarity of the current transducers and the power flow

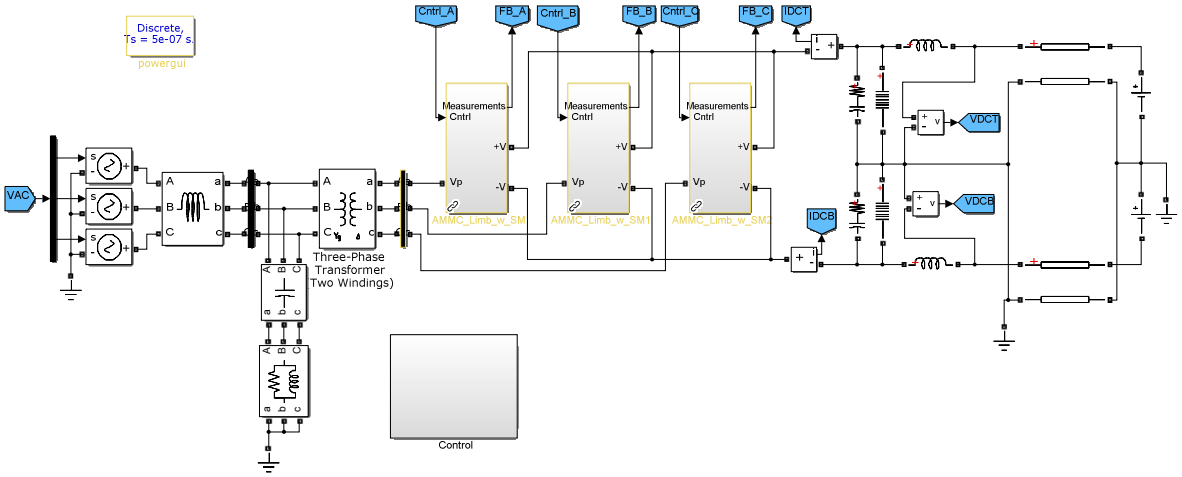

Fig. 5: MATLAB model for the AMMC

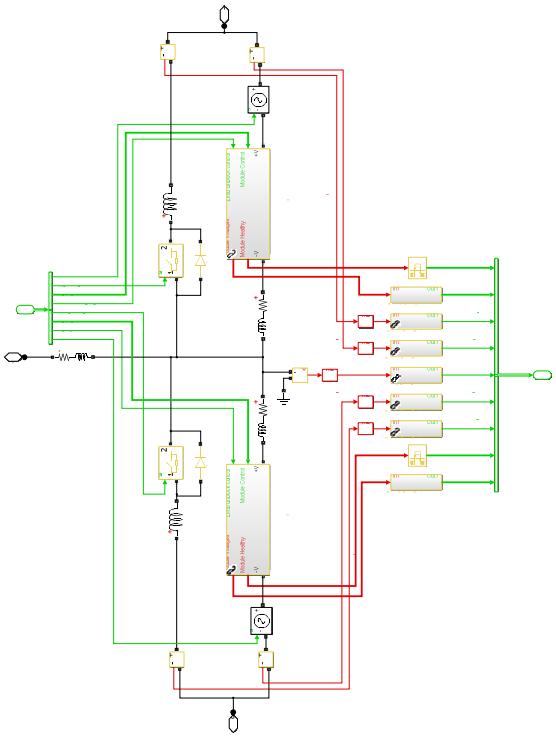

Fig. 6: Phase representation for the AMMC

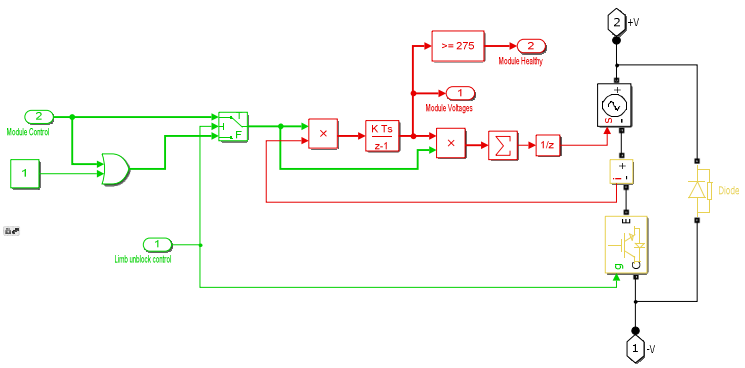

Fig. 7: Chainlink Circuit Model

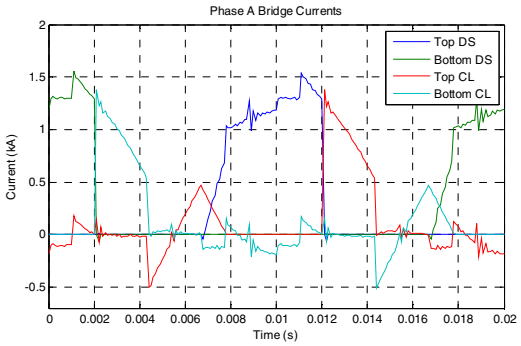

Fig. 8: Phase A bridge currents

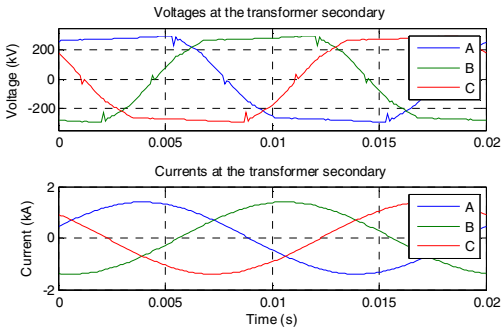

Fig. 9: Converter transformer secondary voltages and currents

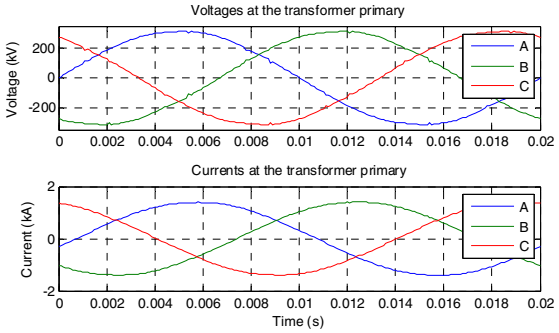

Fig. 10: Converter transformer primary voltages and currents

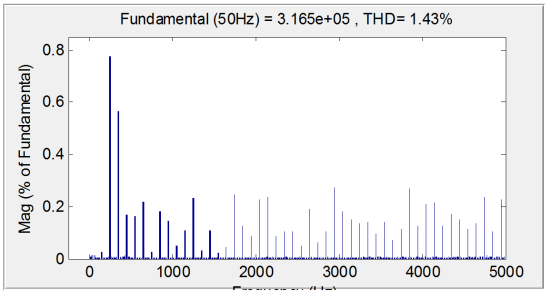

Fig. 11: Harmonic Spectrum for the transformer primary voltage

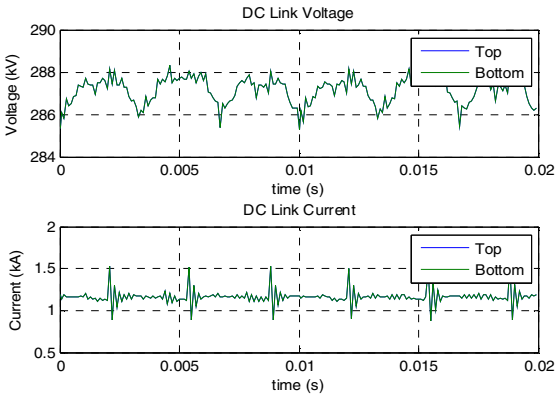

Fig. 12: DC link voltage and current ripple

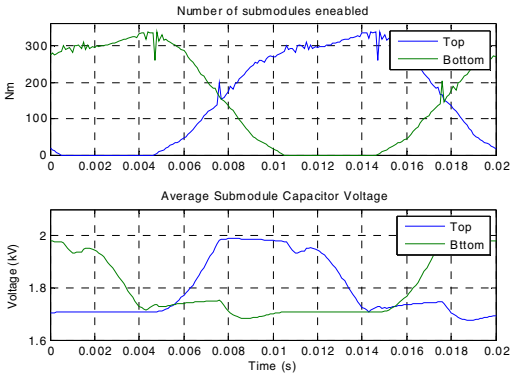

Fig. 13: Number of enabled submodules and average submodule capacitor voltages

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