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A dsPIC-based Excitation Control System for Synchronous Generator

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***Abstract* – The hardware architecture and characteristics of the excitation control system based on dsPIC are described in this paper. The generation method of firing pulse for controlled rectifier utilizing input capture and output compare modules of dsPIC is introduced. The software structure, CAN bus interface and Ethernet communication designs of automatic voltage regulator are presented. The high performance of this system has been proved by factory and filed testing.**

Index Terms* – *Excitation control system, AVR, dsPIC, controlled rectifier.

I. INTRODUCTION

Excitation control system plays an important role in keeping the synchronous generator and electrical power system operating stably and safety. The basic function of an excitation system is to provide direct current to the synchronous generator field winding. In addition, the excitation system performs control and protective functions essential to the satisfactory performance of the power system by controlling the field voltage and thereby the field current. The control functions include the control of voltage and reactive power flow, and the enhancement of system stability. The protective functions ensure that the capability limits of the synchronous generator, excitation system, and other equipment are not exceeded [1].

The functional block diagram of a typical static excitation system for a synchronous generator is shown in Fig.1. In this system, the controlled power rectifier supply the excitation current directly to the field of the generator. The supply of power to the rectifier is fed from the generator terminal through the excitation transformer (ET). The potential transformer (PT) and current transformer (CT) and excitation current transducer (ECT) provide feedback signal to regulator. The AVR (Automatic Voltage Regulator) performs PID operation and generates the firing pulse signal to rectifier.

The AVR is the core of the excitation control system. It is mainly consists of industrial control computer or single chip microcontroller at present. The industrial control computer system is more complex in structure and therefore has lower reliability according to the reliability theories [2]. The single chip microcontroller system is too simple to satisfy the requirement of DCS (Distribute Control System) network interface, friendly HMI (Human-Machine Interface) and other new function demand in the modern power plant. The design of new excitation control system that possesses simple structure with high reliability and enough expanded ability in function is necessary.

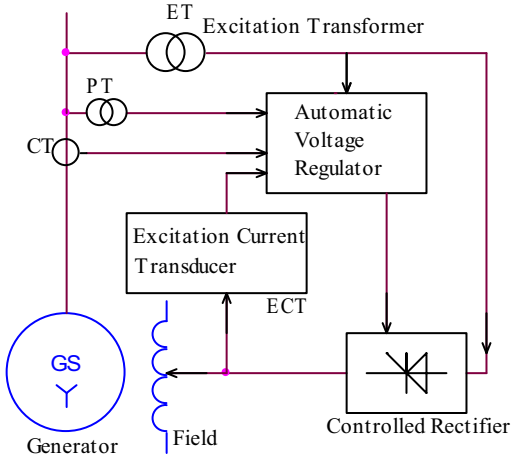

Fig.1. Functional block diagram of an excitation system

The dsPIC Digital Signal Controller (DSC) manufactured by Microchip employs a powerful 16-bit architecture that seamlessly integrates the control features of a microprocessor (MCU) with the computational capabilities of a digital signal processor (DSP). The resulting functionality is ideal for the design of next-generation AVR in excitation control system.

II. MAIN HARDWARE DESIGN

A. *The dsPIC Device and AVR Overview*

The dsPIC DSC core is a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including support for DSP. The core has a 24-bit instruction word, with a variable length opcode field.

The dsPIC DSC devices integrate an array of on-chip functions, such as: five 16-bit timers/counters, eight 16-bit capture input, eight 16-bit compare output, two addressable UART modules with FIFO buffers, two 3-wire SPI modules, I^2C interface, two CAN bus modules compliant with CAN 2.0B standard and up to 16 input channels 12-bit analog-to-digital converter. They also include 8 Kbytes of on-chip data RAM, 144 Kbytes on-chip Flash program space and 4 Kbytes non-volatile data EEPROM.

The dsPIC DSC have wide operating voltage range (2.5V to 5.5V) and high sink/source I/O current (25mA/25mA) [3].

In the design of excitation control system, the AVR usually consists of two identical hardware redundancy channels to meet the desired reliability and availability [4]. Each channel of AVR mainly includes signal processing unit, communication managing unit, synchronous signal processing unit, and pulse generate unit etc. The hardware function block diagram of regulator is shown in Fig.2.

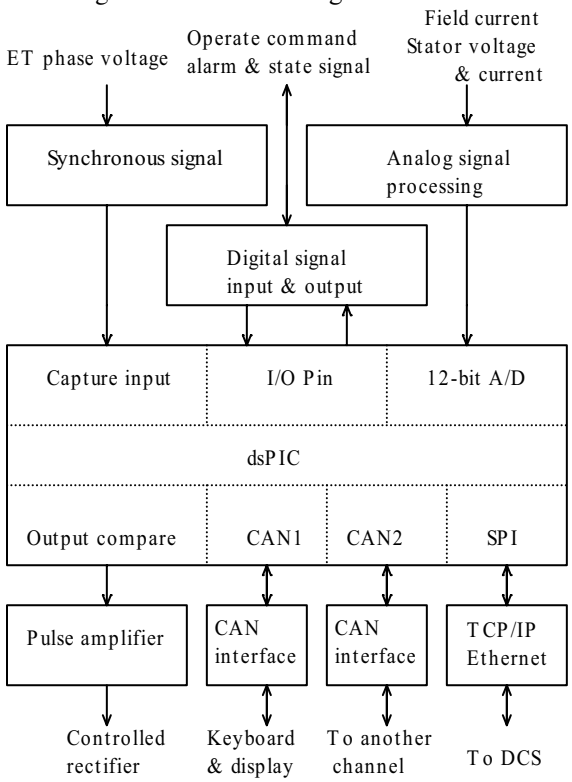

Fig.2 hardware function block diagram of regulator

B. *Signal Processing*

The digital input signals are the operate commands such as raise and lower command and auxiliary contacts of main breakers etc. Each input signal is galvanic isolated by means of a photoelectric coupler and connected to I/O pin of dsPIC.

The output signals from the I/O of dsPIC are alarms and position signals such as active channel etc. Each signal drives a photoelectric coupler and a relay to obtain galvanic isolated output.

The analog signals include 3 phase stator voltage and current from PTs and CTs, and field current from transducer. They are scaled to the 12-bit A/D input tolerant by transformer, transducer and related circuits. The active power, reactive power and frequency of generator may be calculated from stator voltage and current by software arithmetic.

C. *Communication Design*

In this excitation control system project, CAN bus was used to communicated with other function modules, the first CAN port is connected to the keyboard and display module for modify and display all necessary parameters to constitute the friendly HMI; the second CAN port is connected to another AVR channel to perform automatic follow up [5].

The CAN interface circuit is shown in Fig.3. It can achieve galvanic isolation, lever transfer and perform high speed communications.

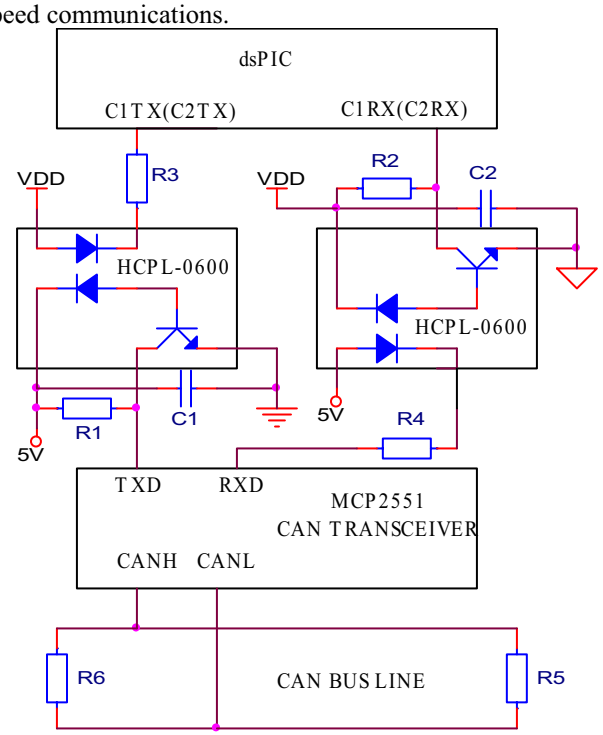

Fig.3 CAN interface circuit

TCP/IP Ethernet was used to communicate with DCS in modern power plant. It is realized by stand-alone Ethernet controller ENC28J60 with SPI interface in this system. The schematic diagram is shown in Fig.4. SPI2 was used to interface with ENC28J60.

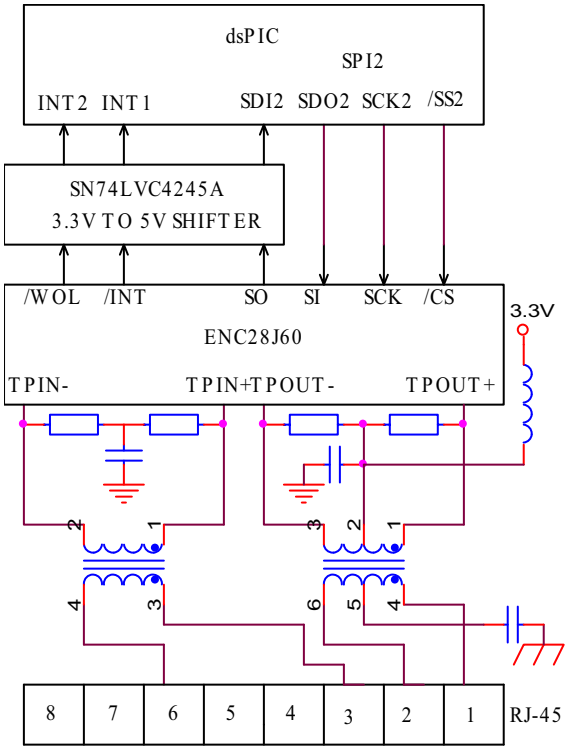

Fig.4 Ethernet interface schematic diagram

D. Firing Pulse Generating

The main power output of excitation system was produced by 3-phase full-controlled thyristor rectifier. The output current was controlled by changing the trigger angle of firing pulse. In this project, the input capture module and output compare module of dsPIC are used to generate firing pulse. The scheme is shown in Fig.5.

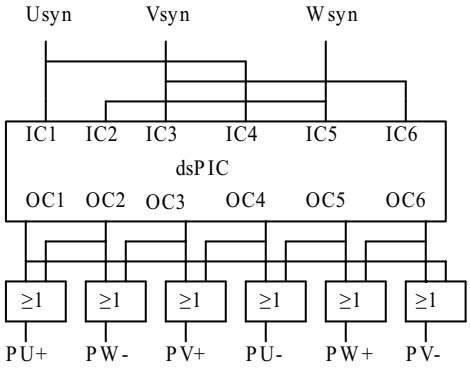

Fig.5 Firing pulse generating scheme

The sinusoidal synchronous signals which came from excitation transformer first transform to low voltage rectangular wave and then feed to the pin of input capture IC1 to IC6. The captured timer value plus the firing angle value sent to the output compare module and generate single firing pulse by the choice of single pulse generating mode of dsPIC. The final firing pulses were formed by the additional OR gates.

III. Software Design

The software of the excitation control system consists of two kinds of program, periodical program and interrupt service routine. The periodical program includes all necessary regulate routines. The interrupt service routine control the communication task and firing pulse generate program etc.

A. Periodical Programs

The periodical programs are organized in 3 different period task groups (5ms, 20ms, and 100ms) according to the task property.

The analog signal processing module, PID calculating and firing pulse angle generate module accomplished in the 5ms groups.

The set-point generator module and limiters routines were running in the 20ms groups. The others programs such as digital signal processing were performed in 100ms task groups.

The regulator software function block diagram is shown in Fig.6.

The set-point value of the AVR can be adjusted by means of raise and lower commands. The excursion time from minimum limit to maximum limit can be adjusted independently from the set-point range.

The function of the Q-static is intended to add additional signals proportionally to the reactive power to the set-point value. The reason is the compensation of the voltage drop caused by the reactive power across the unit transformer and/or the transmission line.

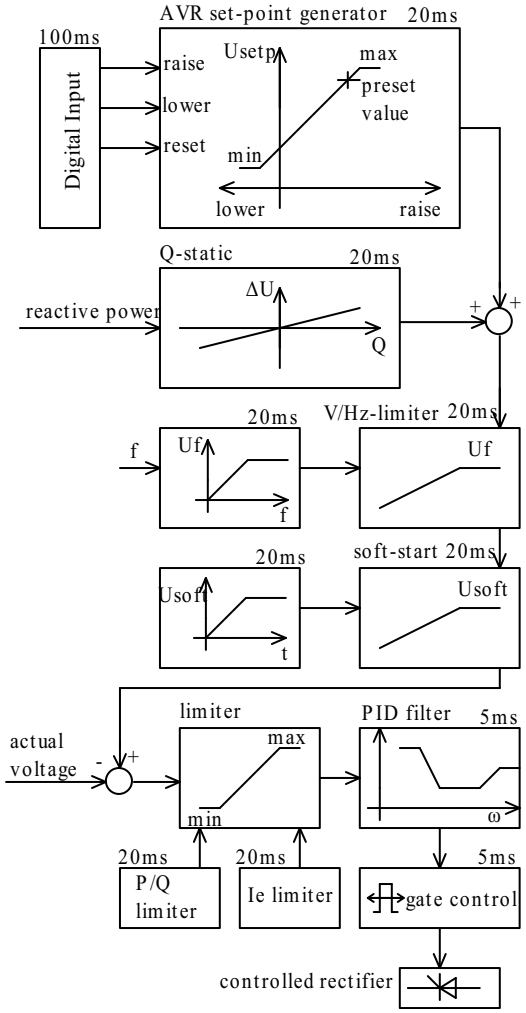

Fig.6 Regulation function block diagram

The soft start function prevents overshooting of the terminal voltage when building up the excitation (field flashing).

The V/Hz limiter is provided in order to avoid overfluxing of the transformers. If the set-point of the AVR is too high for an adjustable frequency, the set-point will be reduced according to a pre-adjusted V/Hz characteristic. The limiter becomes active after a preset time delay.

In order to achieve operation safety, excitation systems include limiter functions. Their objective is to keep the machine operating within permissible limits in order to avoid its unnecessary disconnection as a result of a trip caused by a protection relay.

The P/Q limiter is basically an under excitation limiter intended to prevent the machine being operated beyond practical stability limits. The limiting curve can be set for 5

active power levels (P=0%, P=25%, P=50%, P=75%, P=100%) by defining the 5 reactive power values.

The maximum field current limiter has basically two different set-points: One for ceiling limitation (field forcing) and a second for thermal limitation (maximum continuous).

The input voltage of the PID controller represents the voltage error which is the difference between an actual value and a set-point. The output of the PID controller is input signal for the gate control unit. The feedback parameters of the PID controller can be adjusted in order to achieve an optimum control performance of the synchronous machine.

The gate control unit produces the corresponding time value of firing angle for output compare module to control the output of rectifier.

B. Firing Pulse Generation

The three phase controlled thyristor rectifier is controlled by firing pulse. In this design, the input capture (IC1 to IC6) and output compare module (OC1 to OC6) of dsPIC were used. The software principle of pulse generating is shown in Fig. 7.

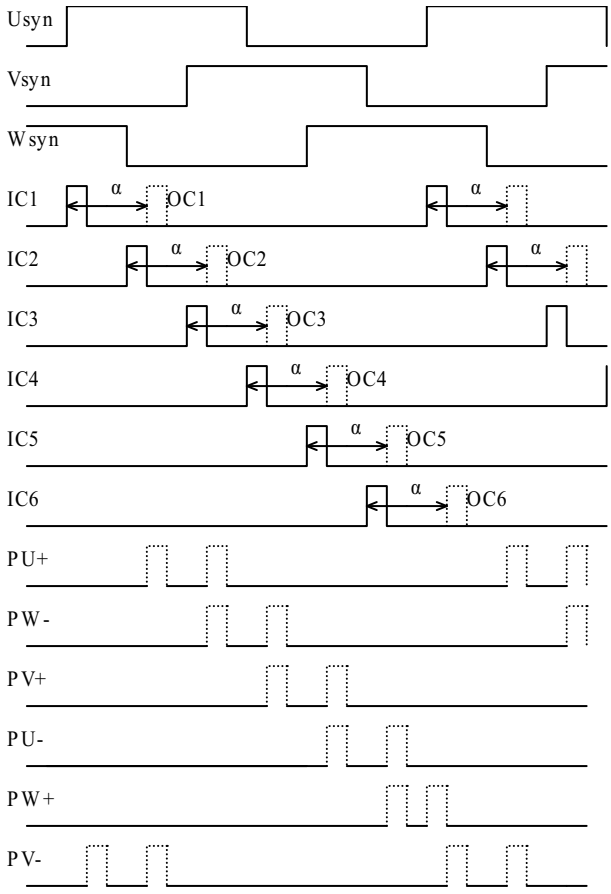

Fig.7 The principle of firing pulse generating

The routines for PU+ pulse are as follows.

```
void __attribute__((__interrupt__)) _IC1Interrupt(void)
{
  int IC1VALUE;
  IC1VALUE=IC1BUF;
  OC1R=IC1VALUE+ALPHA;
  OC1RS=IC1VALUE+ALPHA+PULSEWIDTH;
}
void CONFIG_PULSE_UPLUS(void)
{
   IC1CON=0x0083; /*TMR2, Rising edge*/
            /* 0x0082, Falling edge */
   OC1CON=0x0004; /*TMR2, single pulse */
}
```

In configuration file IC1 and OC1 select Time2 as time base, IC1 operating in capture every rising edge of synchronous signals (Usyn, Vsyn and Wsyn) and OC1 selects the mode of generates single pulse. For the pulse of PU-, PV-, PW-, capture IC4, IC6, IC2 set to operating in capture every falling edge of synchronous signals.

In the IC1 interrupt routine, the capture value plus the firing angle ALPHA sent to OC1R to generate the rinsing edge of the firing pulse, and send above sum plus the pulse width to OC1RS to generate the falling edge of the firing pulse.

The other firing pulses were generated in the same way.

C. SPI Ethernet Interface

The SPI2 serial port of dsPIC consists of following Special Function Registers (SFR):

SPI2BUF: Address in SFR space that is used to buffer data to be transmitted and data that is received.

SPI2CON: A control register that configures the module for various modes of operation.

SPI2STAT: A status register that indicates various status conditions.

The operation of the ENC28J60 depends entirely on commands given by dsPIC over the SPI interface. These commands take the form of instructions, of one or more bytes, which are used to access the control memory and Ethernet buffer spaces. At the least, instructions consist of a 3-bit opcode, followed by a 5-bit argument that specifies either a register address or a data constant. Write and bit field instructions are also followed by one or more bytes of data.

A total of seven instructions are implemented on the ENC28J60 [6]. They are Read Control Register (000), Read Buffer Memory (001), Write Control Register (010), Write Buffer Memory (011), Bit Field Set (100), Bit Field Clear (101) and Soft Reset (111). The read control register command sequence is shown in Fig.8.

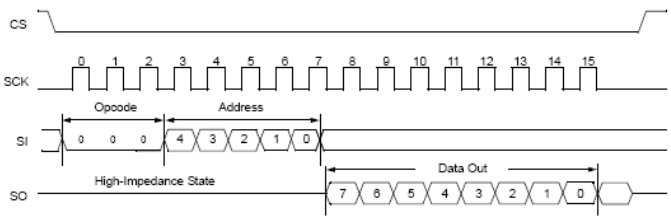

Fig.8 The read control register command sequence

IV. CONCLUSION

This dsPIC-based excitation control system has been applied in power plant. Two primary testing oscillograms are shown as follows.

The field flashing test of generator is shown in Fig.9. This oscillogram shows the terminal voltage has no overshoot in the build-up procedure.

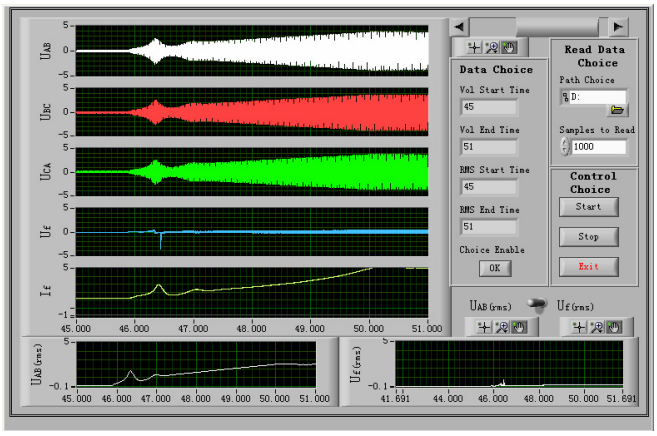

Fig.9 The field flashing procedure of generator

The 10% step change respond testing procedure is shown in Fig.10. With this test, we can demonstrate that the generator voltage is fast response to input step changing and can reach a new steady state rapidly.

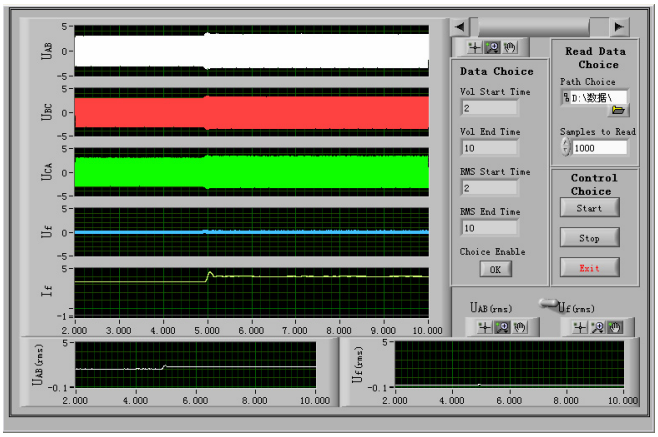

Fig.10 The 10% step change respond test

The factory and field test results verified this excitation control system met the specifications of relative standards.

In conclusion, the dsPIC-based excitation control system provided with a simplified hardware structure, efficiently software architecture, powerful functions, and high reliability is suitable for the modern power plant.

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