DSP and FPGA based platform for rapid prototyping of power electronic converters and its application to a sampled-data three-phase dual-band hysteresis current controller

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***Abstract*- A platform for prototyping industry relevant power electronic converters and systems is presented. The use of a digital signal processor (DSP) and programmable logic (Field Programmable Gate Array – FPGA – and Complex Logic Device – CPLD) shortens implementation time and reduces Electromagnetic Interference (EMI) susceptibility. The design concept is demonstrated with an implementation of a modified three-phase dual hysteresis band current controller.**

I. INTRODUCTION

The design of a universal rapid prototyping platform for industry relevant power electronic converters and systems is presented. Flexibility and wide range applicability are key elements.

A. Design Motivation and Requirements

The proposed platform is intended for use in a laboratory environment in ongoing research and teaching exercises. In particular, the following (power) electronic systems are targeted:

- Multiple axes drives, up to 4 axes
- Switched Reluctance Motor (SRM) drives
- Active power filters (single- or three-phase)
- Active Front Ends (AFE)
- Resonant converters
- Choppers (buck / boost) and braking choppers
- High-bandwidth electric power meters.

Currents and voltages in these applications will unlikely exceed 25 A and 440 V respectively. The change between applications must be possible with minimal hardware changes. Ideally, this would only comprise wiring changes, the rest of the configuration being software based.

It is also observed that there would often be the same distinct classes of tasks to be performed:

1. measurements (of e.g. current, voltage, and speed) at high speed and at precise instants to use the acquired data in fast control loops requiring low latency;
2. signal processing based upon the acquired data. This includes all generalized digital filters such as Kalman adaptive filters and the Fast Fourier Transform (FFT);
3. user interface to control the power electronic system under test. It must be possible to switch it on and off safely under all circumstances and to provide set-points (e.g. speed);
4. monitoring to evaluate internal signals of the system under test. This may require considerable bandwidth, especially during debugging.

Eventually, multiple tasks of each class must be executed in parallel, even on a different time scale. Implementing this on the platform should not require extensive programming experience.

Being able to use the same platform for all experiments lowers the cost, which is clearly an advantage for educational applications. Therefore, the application is cost-sensitive and the solution must not be too expensive.

B. Trends in Power Electronic Design

Some current trends in power electronic design are listed below. Together with the above requirements, they define the final concept of the experimental platform.

- a modular approach, reusing parts of designs and even complete Power Electronic Building blocks (PEBBs) [1];
- the reduction of the analog input section, thereby avoiding problems associated with EMI and drift. At the earliest possible stage the analog sensor signals are converted into the digital domain. At the output section, drive signal generation is already commonly performed using digital circuitry. Finally, converters will evolve into almost fully digital systems;
- integration of different parts of a converter system. For example, the same controller can control a drive inverter and its active front end. Integration lowers the cost and eases software development.

C. Proposed Hardware Solution

By now it is possible to formulate a design concept of the experimental platform. Obviously, such a platform has to

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be largely digital. Programmable analog system building blocks exist [2], but none are (yet) available with sufficient bandwidth for this application. On the other hand, numerous programmable digital building blocks exist (microcontrollers, microprocessors, DSPs, FPGAs, CPLDs and PLDs) with sufficient computational power.

The platform therefore comprises a limited analog section based on a high performance analog to digital converter (ADC). This section also includes the galvanic isolation required for safety and electromagnetic compatibility (EMC).

The rest of the system is fully digital. A powerful general-purpose DSP is selected for the signal processing, user interface and monitoring. A large FPGA takes care of data acquisition and fast control loops. It also provides buffering of the data subsequently used by the DSP.

Fig. 1 shows the entire concept. Multiple connection boards surround the FPGA core. Galvanically isolated sensors and inverter leg modules are the building blocks of the power electronic system under test.

D. Software

Software plays a major role in the design concept. The 'C' programming language is used for the DSP. A basic input/output system (BIOS) relieves the programmer from housekeeping and task scheduling jobs. To configure the hardware, the 'VHDL' hardware description language (HDL) is used, supported by nearly all PLD vendors.

It should be noted that the implementation of a design includes reprogramming of both DSP and FPGA. Assigning a set of input/output (I/O) tasks to the FPGA and reusing that set throughout all designs by only changing the DSP software is possible (and commonly done), but does not necessarily exploit the full possibilities of the system.

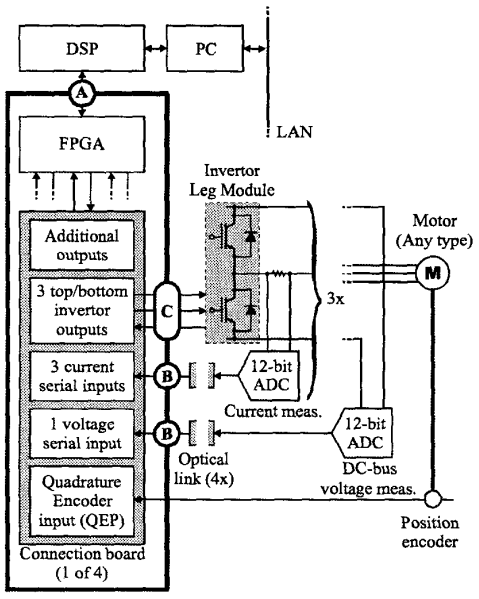

Fig. 1. Generalized concept. Encircled capitals indicate an optional CPLD in the data path (see section V).

The platform supports a 'hardware/software co-design'.

II. Experimental Setups

There are two laboratory setups outlined below. The first one is based on a powerful DSP only; the second one adds an FPGA.

A. Setup without FPGA

The experiment uses a 150 MHz Texas Instruments (TI) TMS320C6711 DSP based Starter Kit (DSK). It is selected to provide ample headroom while designing other types of converters. Especially in motor control, several authors have reported lack of computing power in experimental setups [3-5]. In addition, the DSK has a standardized daughtercard connection used by third-party hardware developers [6]. Fig. 2 shows the block diagram of the system.

Two 500 kSamples/s 12-bit A/D converters (TI ADS7818) are used. The serial data format allows galvanic isolation using only 3 optocouplers with a high common mode rejection (CMR) performance. The results of the converters are consecutively read by the high-speed serial port (McBSP0) of the 'C6711.

Precision current shunt resistances have an excellent phase behavior at high frequencies and are chosen over current transformers or Hall effect based sensors.

Good 'EMI immunity is achieved by placing the ADC on the 'hot side' and by keeping the analog circuitry footprint very small.

Three IGBT inverter legs control an induction machine at no-load as a highly inductive load ($P = 0{,}8$ kW, $U = 245$ V, $I_N = 3.6$ A, $L = 20$ mH). The inverter has an unusually high *dv/dt* (10-100 kV/µs) at its output to evaluate the EMI immunity of the system. The DSK has a small daughtercard with latch output, directly controlling the inverter. The required dead time (1.0 µs) is generated by external hardware.

The dc bus voltage is 200 V. Beyond this value, current samples are sometimes corrupted due to EMI. Current sample corruption was also reported in [7], where it limited

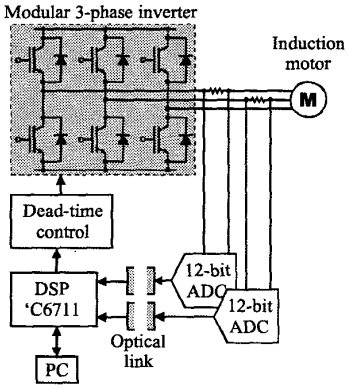

Fig. 2. Block diagram of the setup with FPGA.

the dc bus voltage to 60 V. Section III.C presents a solution to overcome this problem.

B. Second Setup (with FPGA)

The second experiment uses a 60 MHz TI TMS320C31 DSP based DS1102 control board from dSPACE Systems [8]. This DSP is less powerful than the previous one but, with the FPGA attached, its performance is not too critical anymore and user-friendly control software is available.

The high-speed serial port of the DSP is connected directly to an Altera Flex10K FPGA (EPF10K10LC84-4) based interface board (Fig. 3).

This board further includes a 20 MHz oscillator, a display and some additional I/O. It is connected to the same converter and current sensors as in the previous experiment. FPGA programming is performed using the JTAG interface.

As selective blanking of corrupted current samples is possible, the dc bus voltage is now limited to 340 V by the inverter. The blanking technique is explained in the next section.

III. FPGA Implementation Details

A. EMI Countermeasures

The IGBT half bridges and current sensors are galvanically isolated from the control part of the system, but some coupling capacitance between the input and output is unavoidable. Table I reveals that the power supply capacitances dominate. The sensors use a commercially available dc-dc converter for their power supply whereas the IGBT half bridges use a custom built supply.

TABLE I
Typical Coupling Capacitances (pF)

	Control bus	Power supply
1 IGBT half bridge	3.9	4.0
1 Sensor	1.8	26.0

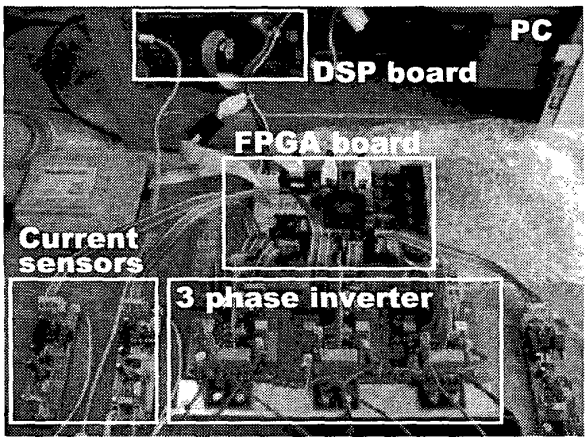

Fig. 3. Experimental setup with FPGA

Large capacitive current spikes (proportional to the output *dv/dt* of the inverter) travel along the data cables when the inverter switches, possibly causing data loss. Using ground connections and common mode chokes these effects are reduced. It should be restated that the inverter has a very high *dv/dt* at its output in order to verify the EMI immunity of a complex modular system with many connections.

B. Clocking and Synchronization

The FPGA board is entirely synchronized to its own 20 MHz clock, ensuring that no race conditions can exist. The FPGA is configured as a master in the communications link with the DSP, i.e. it provides transmit and receive clocks.

C. Blanking

Although many EMI countermeasures are taken, the switching of an IGBT still upsets the current transducers. Table II lists the consecutive samples taken from the two current transducers during a switching transition. The sample frequency is 312.5 kHz. Channel A has a transition, whereas channel B remains 'quiet'.

The table indicates that three samples become unusable after a switching transition. 'x' marks an undefined bit. After t = 0.0 µs, 2 samples are still corrupted. Therefore, 3 samples are blanked.

Possible causes include *dv/dt* failure of the optocouplers (at t = 0.0 µs) and overload recovery phenomena in the ADC. Performance will be better after a redesign of this module (e.g. a stray current path was inadvertently created from input to output underneath the ADC), but the use of an FPGA enables rejecting just these 3 samples every time an inverter leg switches. The effect of blanking on the control algorithm is briefly discussed in section IV.D.

D. Protection

Although a hardware protection (comparator) is still present on the IGBT half bridges, it is also possible to protect the system against excessive currents by watching the digital current sensor signals alone. The response time is short enough to protect the IGBTs even from direct short circuits (short circuit withstand time of the IGBTs is 10 µs), although blanking may extend this response time.

TABLE II
Current Samples During an Inverter Output Transition at t = 0.0 µs

Time	Channel A	Channel B
-3.2 µs	011110111011	011111111000
0.0 µs	0111101xxx11	0111111xx100
3.2 µs	100000011001	100000111001
6.4 µs	011111001110	100000001010
9.6 µs	011110111001	011111111111

Therefore, in the final system, a desaturation protection remains the only 'analog' protective system in effect.

IV. Evaluation Of The Concept – Three Phase Dual Hysteresis Band Current Controller

FPGA based current controllers have already been proposed and implemented in multiple areas of power electronics [7, 9, 10]. To evaluate the design concept and its ability to quickly implement a different type of controller, a three-phase dual hysteresis band current controller based on [11-15] is simulated and modified to run directly on both experimental setups (with and without FPGA). Other types of current controllers [16] can be implemented as well. This algorithm is chosen as, to the authors' knowledge, it has not been implemented digitally before and does not only contain simple comparisons but also some decision logic.

A. Theoretical Overview

Dual-band hysteresis current controllers, also known as space-vector based hysteresis current controllers, use the advantages of both hysteresis current control [17] and space vector modulation (SVM). By applying the proper vectors according to the voltage region, the inverter switching frequency can be significantly reduced. This type of controller requires knowledge of the load back-EMF. The outer hysteresis band acts as a voltage region detector and selects a set of three nearest space vectors, whenever the previous set of voltage vectors is unable to keep the current vector within the inner hysteresis band any further. The inner hysteresis band also determines which vector out of this set must be applied to follow the current shape. The selection of the new vector set is implemented with a look-up table.

To be able to use the controller in an all-digital system, however, a formula was derived to calculate the maximum switching frequency as a function of the inner and outer hysteresis bandwidths $\pm\varepsilon_1$ and $\pm\varepsilon_2$, and as a function of the sampling frequency f_{sa}. Because the inner hysteresis band determines the appropriate switching vector, it determines the maximum switching frequency f_{sw} as well:

$$f_{sw} \le \frac{u_{DC}}{12\varepsilon_1 L}, \tag{1}$$

where u_{DC} represents the dc-bus voltage and L the load inductance.

The minimum difference between inner and outer band is determined by the sampling frequency f_{sa}, as the controller must be able to measure and react on a crossing of the inner band before the outer band is reached:

$$f_{sa} \ge \frac{8u_{DC}}{2\cdot 3(\varepsilon_2 - \varepsilon_1)L}. \tag{2}$$

The factor 2 in the numerator of (2) appears because of the latency between sampling instant and the instant at which the appropriate vector is applied. This latency is needed for the digital algorithm to perform and lasts on average 1 sample period. As the back-EMF and the load voltage vary, a minimum value for both hysteresis bands must be determined.

B. Simulations and Measurements Without FPGA

For the implementation, the control algorithm is entirely written in 'C'. The compiler optimization level is -o2 (function level). The DSP/BIOS DSP operating system of TI is used. The maximum achievable sample rate is now 50 kHz.

In the simulations, the motor is modeled in steady-state condition, i.e. as an RL-impedance. $f_{sw,max}$ is set to 25 kHz (the DSP transmits control signals at 50 kHz). Figures. 4 and 5 show the simulation and measurement results respectively at a 50 kHz sampling rate.

Each time, the top graph shows the motor currents. The second graph indicates the voltage region the current regulator is currently operating in. The third graph displays the actual SVM output states. Few transitions to vector 0 (000) and 7 (111) indicate operation close to the maximum output voltage.

Although a fast 150 MHz DSP is used, execution speed is low (50 kHz). Table III compares the performances of some selected DSPs. A 60 MHz 'C31 was able to execute a

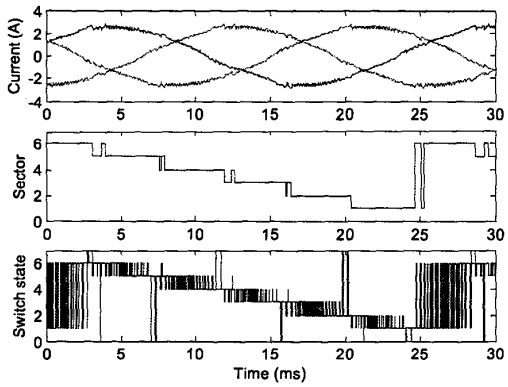

Fig. 4. Simulation result

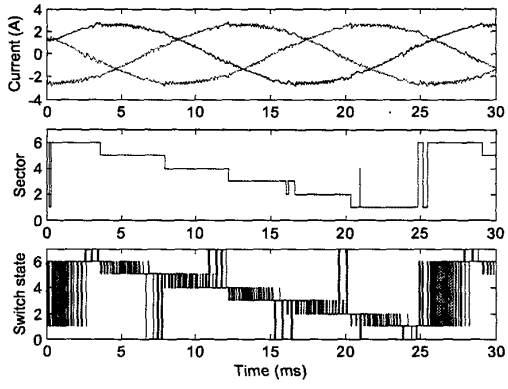

Fig. 5. Measurements (without FPGA).

TABLE III
PERFORMANCE COMPARISON OF SOME SELECTED DSPS

Mftr.	Type & speed (MHz)	MIPS	MFLOPS
Texas Instruments	TMS320C31-60	30	60
	TMS320F240-20	20	-
	TMS320C6711-150	1,200	900
Analog Devices	ADSP21161-100	600	600

comparable algorithm at 20 kHz. Clearly, the 'C6711 is not used efficiently at all.

Modern DSPs depend heavily on their pipeline architecture and cache. Interrupts disturb these mechanisms and slow down execution speed. Most state-of-the-art DSPs contain a DMA controller to move data in and out without interrupting the CPU, but for most control applications such as power electronic converters, this is useless since the data have to be processed immediately with a low latency.

In the second setup, an FPGA is used for data buffering and the low-latency current control loop in order to overcome this limitation.

C. Simulations and Measurements with FPGA

The second implementation allows the maximum sample rate to increase, only limited by the FPGA clock: 312.5 kHz. 86 % of the FPGA resources are used, including all protection features and communications.

Since the dc bus voltage in the first experiment was limited to 200 V, a simulation is used to predict the performance of the current controller with f_{sa} = 50 kHz at 340 V. Fig. 6 shows these currents in more detail. Due to the increased dc bus voltage, the hysteresis bands must be chosen large compared to Fig. 4 in order not to exceed the maximum IGBT switching frequency (25 kHz).

Fig. 7 indicates the simulation result of the dual hysteresis band current controller running at 312.5 kHz, followed by Fig. 8, presenting the actual measurements on the FPGA implementation.

There is clearly a significant decrease of the ripple on the generated current waveforms when the sample frequency is increased to 312.5 kHz.

D. Effect of Blanking

Blanking of three current samples after an output transition does not cause significant problems because the transition itself is meant to alter the current so that it will be returning inside the hysteresis band during the next few µs. Multiple blanking events are always separated by at least one valid measurement on both channels.

V. CONCLUSIONS

The experimental results clearly show that:

- a fully digital implementation of traditionally analog circuitry is feasible using high speed ADCs.
- there is an excellent correspondence between simulations in the design phase and measurements.
- for increased flexibility and speed, the use of an FPGA as an interface between DSP and power

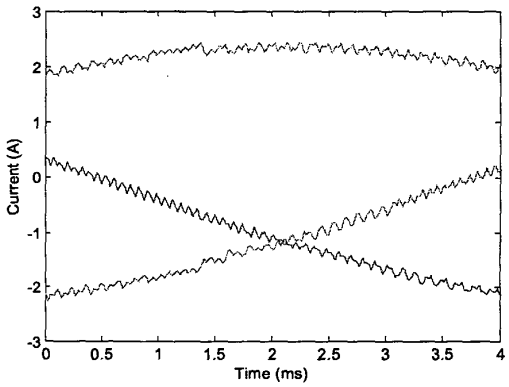

Fig. 7. Simulation result (f_{sa} = 312.5 kHz, U_{DC} = 340V)

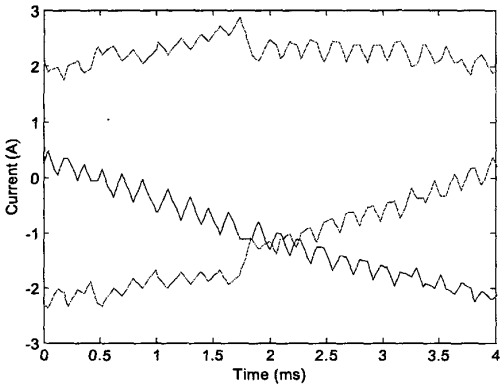

Fig. 6. Simulation result (f_{sa} = 50 kHz, U_{DC} = 340V).

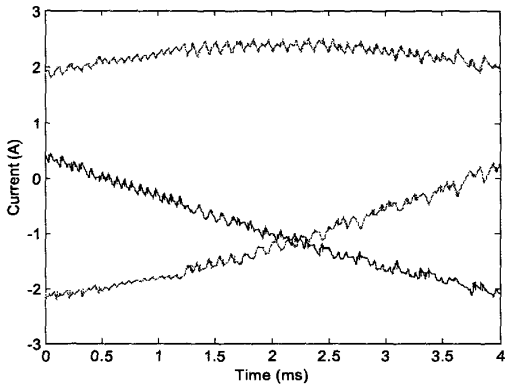

Fig. 8. Measurement (f_{sa} = 312.5 kHz, U_{DC} = 340V)

electronics is necessary: it is considered to be an indispensable component of the prototyping platform.

- EMI can be a serious problem but proper blanking of corrupted samples provides a workable solution.

These conclusions led to the design and development of the final DSP prototyping platform using FPGAs

In this final system, EEPROM based CPLDs are introduced as well. They are configured once to protect the setup against programming mistakes in the FPGA. Referring to the data paths encircled by a capital on Fig. 1, they:

A. facilitate the configuration of the SRAM based FPGA by the DSP.

B. provide system level protection by directly checking the measured value in the current transducers.

C. protect the half bridges from erroneous input signals and prevent the FPGA from re-applying signals after an error has occurred.

The Altera EPF10K10 FPGA will be replaced by an EP1K100, which accommodates 4,992 logic elements instead of 576. A multi-FPGA solution based on four EPF6016 devices was rejected because of the reduced complexity, lower cost and easier programming of a single, larger device.

Futher research work includes detailed analysis of the effects of blanking on the current controller performance.

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