

Modular Multilevel Converter Modelling, Control and Analysis under Grid Frequency Deviations

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Abstract

A tool for component sizing for MMCs has been developed and tested through simulations in PLECS. The steady-state behaviour under grid frequency deviations - interesting for offshore wind farm connections - has been analysed, providing insights in MMC characteristics and further testing the proposed tool.

Introduction

In recent years, increasing attention has been drawn to the application of voltage source converter HVDC (VSC-HVDC) for connection of large offshore wind power plants to the on-land grid. Furthermore, interconnections between distant and asynchronous networks look attractive in order to improve the economic efficiency and stability of power systems, thus offering more room for accommodating large shares of fluctuating renewable energy. The conjugation of both aspects may possibly lead to the construction of vast multi-terminal HVDC grids with several offshore wind farms.

Recent advances in VSC-HVDC technology have shifted the focus from the classical two-level configuration to the new modular multi-level converter (MMC) concept [1, 2], which offers a number of technical advantages, such as very low inherent harmonic voltage content and low switching losses. Such benefits appear to have recently outweighed volume and cost drawbacks.

The first written footprint over the modular multilevel converter circuitry was introduced in 1975 [3] based on series connection of full-bridge cells, while in 2002, a topology with an alternative module structure was introduced by R. Marquardt [4], in which half-bridge modules were utilized. The reduced number of switches, along with advances in power electronic technology, then facilitated the use of this topology in HVDC systems.

Wind turbine manufacturers thus face the need for understanding the operation of this new converter topology and, going beyond that, to investigate their behaviour and capabilities against variation of offshore voltage and frequency, which may naturally arise as a consequence of the offshore grid configuration or, alternatively, be utilised as actual control signals [5]. For this reason, a first analysis of the operation of a MMC is presented in this article, focusing, for the time being, on steady-state harmonic spectra.

Proposed topologies

More in detail, four main HVDC converter topologies have been so far proposed from the industrial manufacturers that utilize modular multilevel conversion concept, and still intensive research takes place in further improving their performance. These include following:

- **Modular Multilevel Converter with half-bridge modules (half-bridge MMC), fig. 1(a):** half bridge cells consist of single IGBT modules with integrated free-wheeling diodes, DC capacitor, bypass thyristor and a bypass electro-mechanical relay switch for cell protection [6].
- **Cascaded Two Level Converter with half-bridge modules (half-bridge CTL), fig. 1(b):** maintains similar operation principle to MMC, but has an original half bridge cell design, in which single IGBTs are replaced by valves made by eight series-connected press-packed IGBT stacks. Due to press-pack IGBT short-circuit failure mode, no bypass thyristors or mechanical switches are required. In case of a single IGBT failure, all remaining IGBTs continue to operate at slightly increased voltage level between maintenance periods [2].
- **Modular Multilevel Converter with full-bridge modules (full-bridge MMC), fig. 1(c):** full-bridge modules are used in the cascaded topology, which operation principle remains similar to the previous cases. Single IGBT modules are used in each cell that are additionally equipped with DC capacitor, by-pass thyristor, protection switch and bleeder resistors.
- **Hybrid multilevel converter with full-bridge modules (Hybrid MMC), fig. 1(d):** by inter-connecting each full-bridge module terminal with director IGBT switch, a voltage wave can be shaped in the desired manner while at the same time allowing zero-voltage switching for the two-level operation [7].

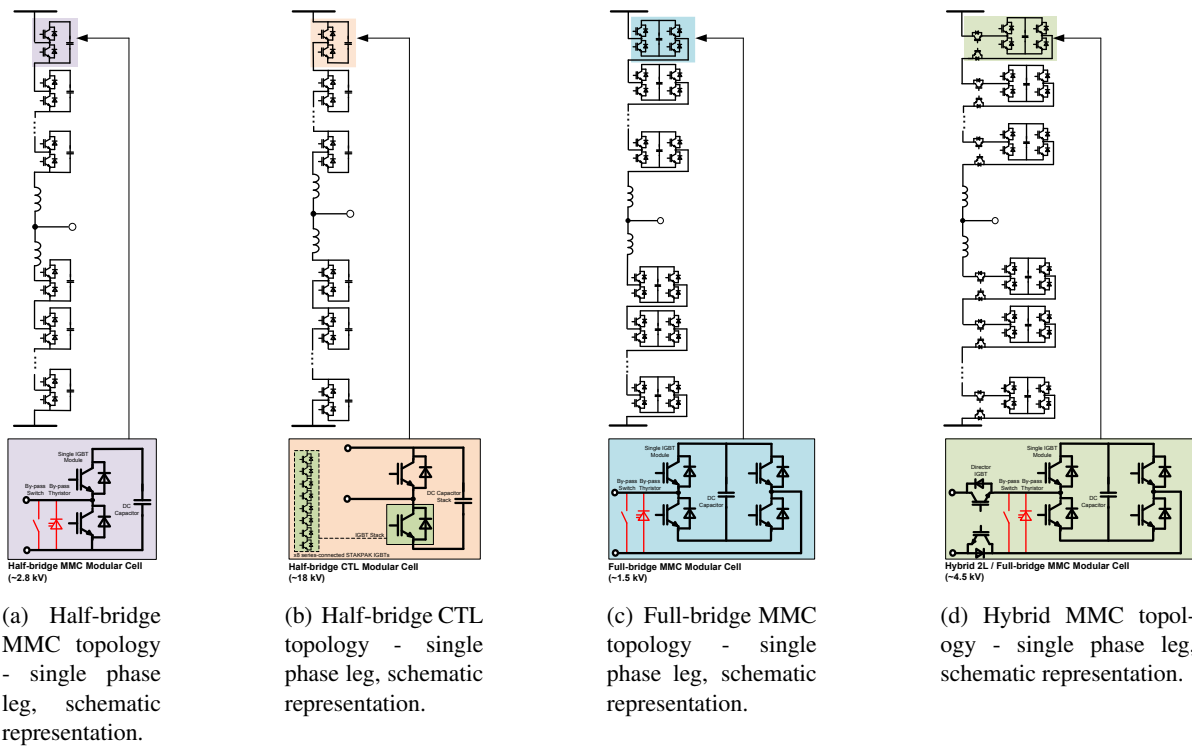


Figure 1: Summary of proposed VSC-HVDC technologies.

Control Strategies

Besides the classical outer control loops also presented by older VSC-HVDC applications in which the two level converter type is adopted, the control of multilevel converters in principle relies on the combination of current, balancing and cell voltage controllers [8, 9, 10]. As control actions, the following requirements are addressed:

- Equal sharing of phase current between phases.

- Control of the total energy in the converter - power balance between DC and AC power.
- Energy balance between arms - limitation of oscillating circulating current.

The first target is achieved by setting equal arm voltage targets, while the other two objectives can be achieved by exploiting the fact that adding the same quantity to the target arm voltage of opposite arms does not affect the AC quantities but only the total energy balance and the arm energy discrepancy. The general control block diagram of the modular multilevel converter controller can be illustrated such as is represented in fig. 2.

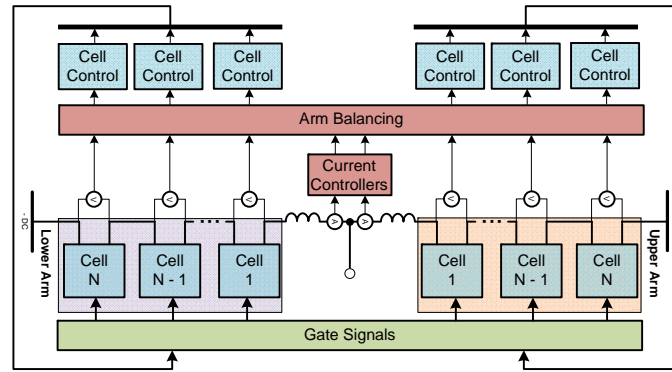


Figure 2: MMC general control block diagram.

Besides the cell structure mentioned above, the current VSC-HVDC main vendors (Siemens, ABB and Alstom Grid) also provide different approaches for control implementation based on fig. 2. The two main differences are referenced to the cells voltage controllers and the way in which the arm balancing is performed [11, 12, 8, 2, 13, 14].

Cell Controllers

For the cell voltage balancing controllers, the first approach requires the selection of a number of cells to be switched on and off [11, 12]. The firing control system is based on an accurate sorting algorithm which measures the DC voltages in each cell and selects the appropriate number of cells which are bypassed. In this case, the balancing methods based on cell selection can be faster and with lower level of complexity when compared with a distributed voltage controller in each of the cells [8].

For the distributed cell control scheme, a PWM based modulation is presented. In each of the cells, an error signal between the cell voltage measurement and set point value is generated and its result is combined with the modulation signals coming from the balancing and current controllers. This signal is then compared with a triangular carrier and the PWM pattern is applied directly to the switching devices. Moreover, the PWM pulse number can be a non-integer value, this technique being applied to improve the cell voltage balancing even further [2, 13].

Balancing Strategies

Two main strategies are applied by the main HVDC vendors to keep the voltages between upper and lower arms balanced. The first method is performed by a closed loop compensation of arm currents and/or capacitor voltage measurements. By doing this, the firing pulses sent to the upper and lower arms are slightly different for compensating the voltage differences. The approach is centralized and each cell is only provided with a monitoring station that transmits data back to the arm control and accomplishes what such control unit orders.

The alternative approach requires extra hardware in the circuit between the arm reactors and the converter AC output. This component is a tunable LC-filter which limits 2nd harmonic voltage ripple and allows lower losses and voltage ratings of power modules. Apart from the 2nd harmonic, 3rd harmonic is

damped enough to allow both lower voltage ratings and wye-connected transformer at the converter-side [14].

System Benchmarking and Sizing

Design Engineering Studies

In order to optimally size the HVDC system at a first step approximation, the following studies have been carried out in this work:

- **Load flow analysis:** allows to rate components for maximum current ampacity under normal operation. Based on applied system diagram, load flow analysis is divided into external load flow (fig. 3(a)) and internal load flow (fig. 3(b)), which includes only the analysis of the 2nd harmonic circulating current flowing within converter arms.
- **Harmonic analysis:** allows optimal sizing of filters within the HVDC system. Harmonic analysis is utilized via applied Discrete Fourier Transform of arm voltage staircase waveforms obtained through specific PWM modulation technique.
- **DC short-circuit analysis:** allows rating arm reactors for the reliable protection of half-bridge cells in case of the DC short-circuit state.

System Description and Modelling

A schematic representation of the analysed HVDC system is presented on fig. 3(a) and 3(b). The following main parts can be derived within its internal design:

- **AC System:** reflects the external influence of the AC-side on the HVDC system performance. AC system is modelled with Thevenin equivalent AC voltage source V_{AC} and a short-circuit impedance Z_{AC} , which can be measured at the point of common coupling (PCC).
- **DC System:** reflects the external influence of the DC-side on the HVDC system. DC system is modelled with Thevenin equivalent DC voltage V_{DC} and load resistance R_{DC} .
- **High Frequency Filter:** used for reactive power compensation at the PCC. Implemented design is a 2nd order high-pass filter modelled with $C_{f(AC)}$, $L_{f(AC)}$ and $R_{f(AC)}$ parameters.
- **Power Transformer:** required due to different voltage levels between AC and DC systems. It is modelled with inductance L_{tr} and resistance R_{tr} accordingly for leakage flux distribution and copper losses.
- **Arm Reactors:** used for limiting load and short-circuit arm currents to the desired value, which are restricted by nominal ratings of the half-bridge cells. Each arm reactor is modelled with inductance L_{arm} and resistance R_{arm} , which reflects its copper losses.
- **Half-Bridge Cells:** for load flow and harmonic analyses, cells are modelled with ideal switches and a DC voltage source, which reflects the electrical behaviour of the single cell capacitor. For DC short-circuit analysis, cells are modelled with specified IGBT switches, which characteristics include their short circuit withstand range.
- **DC Filter:** used to provide harmonic path for the parasitic currents. In this manner, AC harmonic currents on the DC side will not flow through DC lines and induce electromagnetic fields, which might generate losses and interference in neighbouring communication systems. DC filter is modelled with a pair of capacitors $C_{f(DC)}$ interconnected between DC buses and ground. Capacitor losses are reflected by equivalent series resistance $R_{f(DC)}$.

Assumptions

In order to simplify the first step modelling of the MMC converter, the following assumptions were made:

1. All six arms are loaded equally on the DC-side, as they operate in identical manner. Such assumption allows dividing common DC load resistance R_{DC} into six corresponding arm DC load resistances $R_{DC(arm)}$, according to relation:

$$R_{DC(arm)} = \frac{3}{2} R_{DC} \quad (1)$$

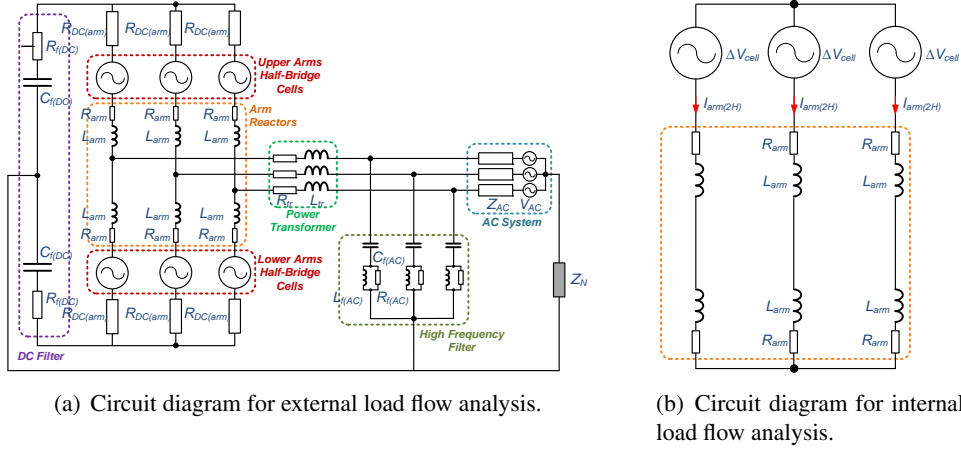


Figure 3

- Generated cell voltage ripple ΔV_{cell} consists entirely of the 2nd harmonic component. Consequently, internal load flow analysis can be derived and made separately only for the 2nd harmonic circulating current enclosed through MMC phase legs (fig. 3(b)).
- Sizing for cell capacitors is made based on zero-, fundamental- and second-harmonic average arm current values according to:

$$C_{cell} = \frac{I_{arm(1H)} + I_{arm(2H)} + I_{arm(DC)}}{\Delta V_{cell}} \quad (2)$$

All higher-order harmonic currents are considered negligible to influence cell capacitance sizing.

- Specific methodology for sizing DC filter is out of scope of this work. Hence, assumed required DC capacitance corresponds to 2 ms time constant.

Methodology

A generic algorithm structure for populating the HVDC system with optimal parameter values for the first step approximation is shown on fig. 4. The whole procedure can be divided into three main parts:

Preliminary system configuration, which includes:

- Power transformer rating** - power transformer is rated for the nominal AC power S_{AC} of the HVDC system and a voltage ratio V_{ratio} of

$$V_{ratio} = \frac{m V_{ref}}{V_{AC}} = \frac{m \sqrt{3} \frac{V_{DC}}{2\sqrt{2}}}{V_{AC}} \quad (3)$$

where V_{ref} is the reference arm voltage RMS value and m stands for the modulation index.

- Cell sizing** - number of cells per arm N_{cells} can be calculated from the assumed nominal cell voltage V_{cell} according to

$$N_{cells} = \text{ceil} \left(\frac{V_{DC}}{V_{cell}} \right) \quad (4)$$

- Arm reactors sizing I** - the first criterion for sizing arm reactors is through limiting AC arm currents I_{arm} to the desired values, which need to be limited due to the strict cell IGBT and cell capacitor continuous current ratings.

Based on MMC operation principle, the dominant impact of the 1st harmonic arm current $I_{arm(1H)}$ and 2nd harmonic arm current $I_{arm(2H)}$ is taken into account. Reactors tuning is performed by solving AC circuit diagrams shown on figure 3(a). The final arm current values which change with respect to the reactor inductance L_{arm} are obtained as a sum of their most relevant components

$$I_{arm}(L_{arm}) \cong I_{arm(1H)}(L_{arm}) + I_{arm(2H)}(L_{arm}) \quad (5)$$

derived from an external and internal load flow analyses.

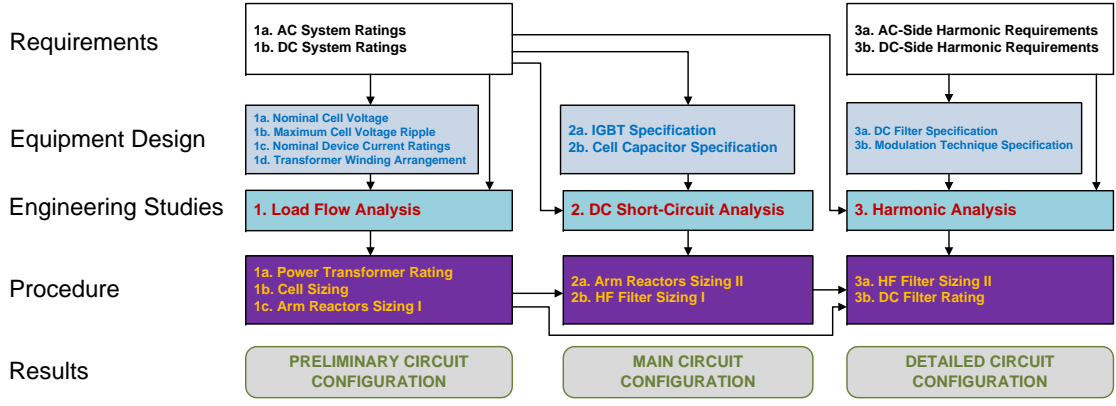


Figure 4: Generic algorithm structure for the 1st approximation optimal sizing of the HVDC System.

Main system configuration, which includes:

- *Arm reactors sizing II* - the second criterion for sizing the arm reactors is through limiting the rate of change of possible DC short-circuit current between arms. In order to protect the cell capacitors from extensive fault current and minimize their short-circuit contribution; the applied IGBT switches in all cells should be able to safely disconnect the capacitors during fault occurrence. In this work, time required for safe IGBT turn-off operation under fault conditions includes: turn-off delay time $t_{d(off)}$, fall time t_f and short-circuit withstand time t_{SC} . The minimum inductance of arm reactors is defined as

$$L_{arm} = \frac{dt}{di}u \cong \frac{t_{d(off)} + t_f + t_{SC}}{I_{SC}} \quad (6)$$

where I_{SC} is IGBT rated short-circuit current.

The final value for the arm inductance is the higher one - chosen among the described sizing criteria.

- *HF filter sizing I* - Final value of arm reactor inductance allows, when necessary, preliminary sizing of the $C_{f(AC)}$ and $L_{f(AC)}$. In order to assure reactive power compensation at PCC, $C_{f(AC)}$ is calculated from

$$C_{f(AC)} = 6 \left(\frac{I_{arm}}{V_{AC}} \right)^2 L_{arm} \quad (7)$$

$L_{f(AC)}$ is applied to provide harmonic current resonant path, so that minimum current distortions are injected into the grid

$$L_{f(AC)} = \frac{1}{\sqrt{2\pi f_{res} C_{f(AC)}}} \cong \frac{1}{\sqrt{2\pi f_{sw} C_{f(AC)}}} \quad (8)$$

$L_{f(AC)}$ is sized based on optimal estimation of the resonant frequency f_{res} , which should be close to effective switching frequency f_{sw} of the MMC converter.

Detailed system configuration is obtained, which includes:

- *HF filter sizing II* - By applying specified PWM modulation technique to cell IGBT switches, a harmonic analysis is provided in order to identify resonant frequencies at specific operating points and further size filters for optimal HVDC system according to the external requirements. Resistance $R_{f(AC)}$ is sized based on calculated quality factor q from

$$R_{f(AC)} = 2\pi \cdot f_{res} \cdot L_{f(AC)} \cdot q \quad (9)$$

Optimal q value is set for specific harmonics damping based on derived impedance characteristic plot in the frequency domain. Requirements regarding AC-side harmonics damping are assumed to be provided by the grid operator.

- *DC filter rating* - the assumed DC filter must be rated for harmonic voltages and currents, which will flow causing its extensive heating. For this reason, harmonic magnitude and phase spectra of current and voltages are obtained, which allow deriving maximum voltage peak for insulation coordination along with the resulting RMS current for thermal management.

Control Strategy

As mentioned above, the control of a MMC can be implemented in different ways and the control objectives are variegated [4, 13]. In this work, a mixed approach has been used and the control blocks have been developed in C-code. The main control features are as follows:

- The grid current control perfectly resembles a classical VSC-converter's control in dq reference frame [2].
- The balancing action is performed by control of circulating current [4], suppressing its 2nd harmonic component and controlling its DC part. The validation of the components sizing tool, however, required this controller to be switched off. Its features will be presented in future work.
- The cell voltage control is realised in a distributed manner, correcting the modulation index on every cell based on the filtered cell voltage error [2].

Simulation Cases

Table I provides system parameter values derived according to the methodology presented above.

Element	Parameter Description	Symbol	Unit	Value
<i>Modulation</i>	Carrier-based PWM, phase shifted			
	Cell PWM switching frequency	f_{cell}	$[Hz]$	1250
<i>HVDC System</i>	Nominal Power	S_{AC}	$[MVA]$	22.5-j25.5
<i>AC System</i>	Nominal voltage (RMS)	V_{AC}	$[kV]$	21.210
	Frequency	f_{AC}	$[Hz]$	50±5%
	Phase impedance	Z_{AC}	$[m\Omega]$	12.1+j121.3
	Neutral point impedance	Z_N	$[m\Omega]$	∞
<i>DC System</i>	DC system pole-to-pole voltage	V_{DC}	$[kv]$	120
	Nominal power	P_{DC}	$[MW]$	36
<i>Cell rating</i>	Nominal cell voltage	V_{cell}	$[kV]$	30
	Number of cells per arm	N_{cell}		4
	Maximum cell voltage ripple	ΔV_{cell}	%	±5%
	Cell capacitance	C_{cell}	$[mF]$	0.315
	Cell IGBT turn-OFF delay time ¹	$t_{d(OFF)}$	$[\mu s]$	1.75
	Cell IGBT fall time ¹	t_f	$[\mu s]$	0.71
	Cell IGBT short circuit time ¹	t_{sc}	$[\mu s]$	10
	Cell IGBT short circuit current ¹	I_{sc}	$[A]$	12x200
<i>Power Transformer</i>	Voltage ratio	V_{ratio}	$[kV : kV]$	1:1
	Phase inductance	L_{tr}	$[mH]$	0.014
	Phase resistance	R_{tr}	$[m\Omega]$	1.830
<i>HF Filter</i>	Phase capacitance	$C_{f(AC)}$	$[\mu F]$	4.6230
	Phase inductance	$L_{f(AC)}$	$[mH]$	87.671
	Phase resistance	$R_{f(AC)}$	$[\Omega]$	1377.13
<i>Arm Reactor</i>	Arm inductance	L_{arm}	$[mH]$	50.00
	Arm resistance	R_{arm}	$[m\Omega]$	48.00
<i>DC Filter</i>	Leg capacitance	$C_{f(DC)}$	$[\mu F]$	41.11
	Leg resistance	$R_{f(DC)}$	$[m\Omega]$	5.00

¹ According to IGBT 5SMY 12N4500 datasheet.

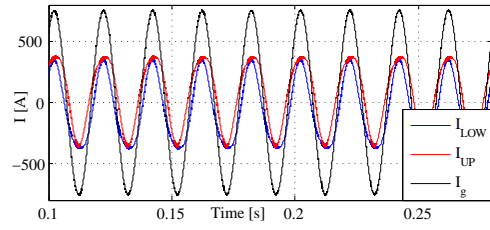
Table I

Steady State Operation

A computer model has been developed in PLECS in order to validate the tool for sizing the components. Three simulation cases have been made with regard to the grid frequency, which is nominal (50Hz), 5% below nominal (47.5 Hz) and 5% above nominal (52.5 Hz). Chosen under- and over-frequency values are close to maximum frequency operating ranges for Irish ESB grid code [15].

Nominal frequency $f_{AC} = 50$ Hz (no frequency deviations)

Fig. 5 shows the steady-state arm and grid currents on phase a. Harmonic analysis of the arm currents has been made in order to assess the accuracy of the proposed sizing tool. The table from fig. 5 provides arm current sequence values for dominant 0^{th} -harmonic, fundamental and 2^{th} -harmonic.



Phase a arm and grid currents $f_{AC} = 50$ Hz.

Harmonic	Theoretical Analysis			Computer Analysis		
	+seq	-seq	0seq	+seq	-seq	0seq
0^{th} [A]	0.06	0.06	61.13	0.154	0.154	63.41
1^{st} [A]	254	3.98	0.378	255	0.065	0.059
2^{nd} [A]	11.4	65.8	12.3	0.058	54.72	0.185

Comparison of 0^{th} , 1^{st} and 2^{nd} harmonic currents at $f_{AC} = 50$ Hz.

Figure 5: Simulation results for $f_{AC} = 50$ Hz.

On the left column of fig. 9, harmonic spectra are observed for each sequence arm current - taken both from computer analysis and theoretical analysis. It can be observed that harmonic peak regions for both analyses are overlapping each other, which proves good accuracy of the sizing tool. Higher magnitudes of the harmonics derived from the theoretical tool allow sizing components, thus providing reasonable safety margin.

Fig. 6(a) shows deviations in cell voltage ripple level for different set of cell capacitances, both for values obtained from (2) for theoretical analysis and measured across cell for computer analysis.

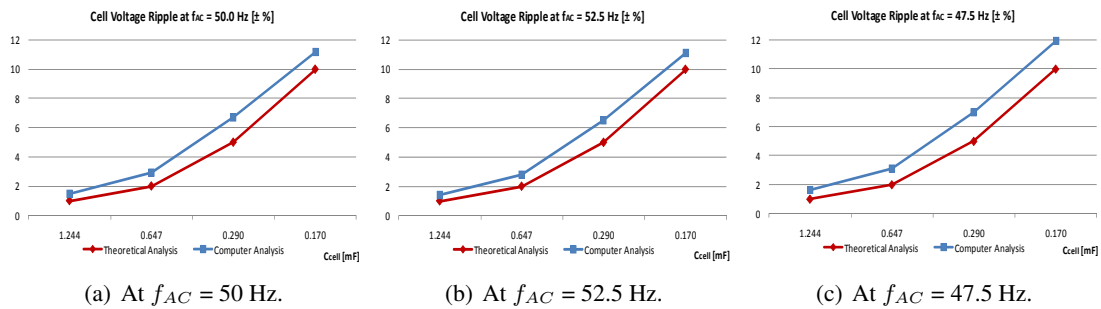


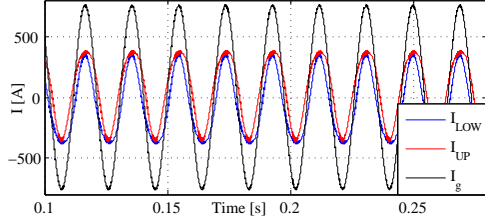
Figure 6: Cell voltage ripple variations as a function of C_{cell} .

Maximum differences in 1.7% of the ripple occurred for the $C_{cell} = 0.290$ mF, which can be explained by means of additional impact of higher harmonics, which provide circulating current causing voltage unbalance.

High frequency deviations $f_{AC} = 52.5$ Hz

For over-frequency case, the same figures are analysed and reported in fig. 7. Reasonable accuracy level is obtained over all dominant values (zero-seq. DC current, positive-seq. fundamental current and negative-seq. circulating current).

Imposed harmonic spectra from the theoretical and computer analyses on the central column of fig. 9 show good accuracy of the theoretical model for the over-frequency state. Similarly as for nominal



Phase a arm and grid currents $f_{AC} = 52.5$ Hz.

Harmonic	Theoretical Analysis			Computer Analysis		
	+seq	-seq	0seq	+seq	-seq	0seq
0^{th} [A]	0.01	0.01	61.13	9.71	9.71	63.37
1^{st} [A]	250	5.48	0.413	255	9.38	0.225
2^{nd} [A]	5.25	67.7	0.819	12.29	53.16	0.135

Comparison of 0^{th} , 1^{st} and 2^{nd} harmonic currents at $f_{AC} = 52.5$ Hz.

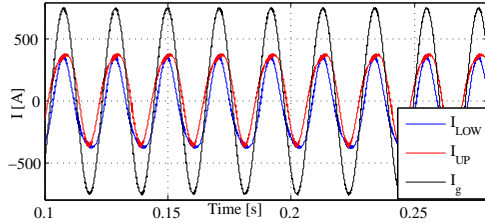
Figure 7: Simulation results for $f_{AC} = 52.5$ Hz.

frequency case, higher harmonic magnitudes for theoretical model provide reasonable safety margin for component sizing.

Fig. 6(b) shows the cell voltage ripple deviation with regard to cell capacitance. It can be observed that no particular impact is made from over-frequency operation for the accuracy of the theoretical model. The largest difference for $C_{cell} = 0.290$ mF is 1.5%.

Low frequency deviations $f_{AC} = 47.5$ Hz

Again, the same figures are presented in fig. 8 for low frequency at level of 47.5 Hz. Table from the fig. 8 lists dominant harmonic values, which are similar to the values for the previous cases. In the same manner, harmonic spectra for under-frequency operation on the right column of fig. 9 are accurately overlapping each other, with higher harmonic magnitude values computed by theoretical sizing tool.



Phase a arm and grid currents $f_{AC} = 47.5$ Hz.

Harmonic	Theoretical Analysis			Computer Analysis		
	+seq	-seq	0seq	+seq	-seq	0seq
0^{th} [A]	0.01	0.01	61.13	11.2	11.2	63.28
1^{st} [A]	250	5.48	0.413	252	12.5	0.054
2^{nd} [A]	5.25	67.7	0.819	10.78	53.02	0.214

Comparison of 0^{th} , 1^{st} and 2^{nd} harmonic currents at $f_{AC} = 47.5$ Hz.

Figure 8: Simulation results for $f_{AC} = 47.5$ Hz.

It can be concluded from fig. 6(c) that cell voltage ripple accuracy of the theoretical model is not affected by under-frequency operation. Highest ripple difference of 2% is obtained for $C_{cell} = 0.290$ mF.

Conclusion

A tool for quickly sizing electric components for modular multilevel converters has been developed and its validity has been tested through simulations using the power electronics simulation tool PLECS.

Good accuracy of the derived method has been observed and the theoretical analysis slightly overestimates the actual harmonic content of circulating arm currents, allowing for a safe design of the components.

The influence of the cell capacitance on its voltage ripple has been tested and a satisfying match was found between theoretical analysis and simulated results.

Moreover, grid frequency deviations were introduced in order to investigate the steady-state behaviour of the converter under such disturbance and the developed tool proved to offer satisfying results in this regard as well. Future work will present the control strategy in more detail and provide results on transient behaviour of the converter under the same disturbing events.

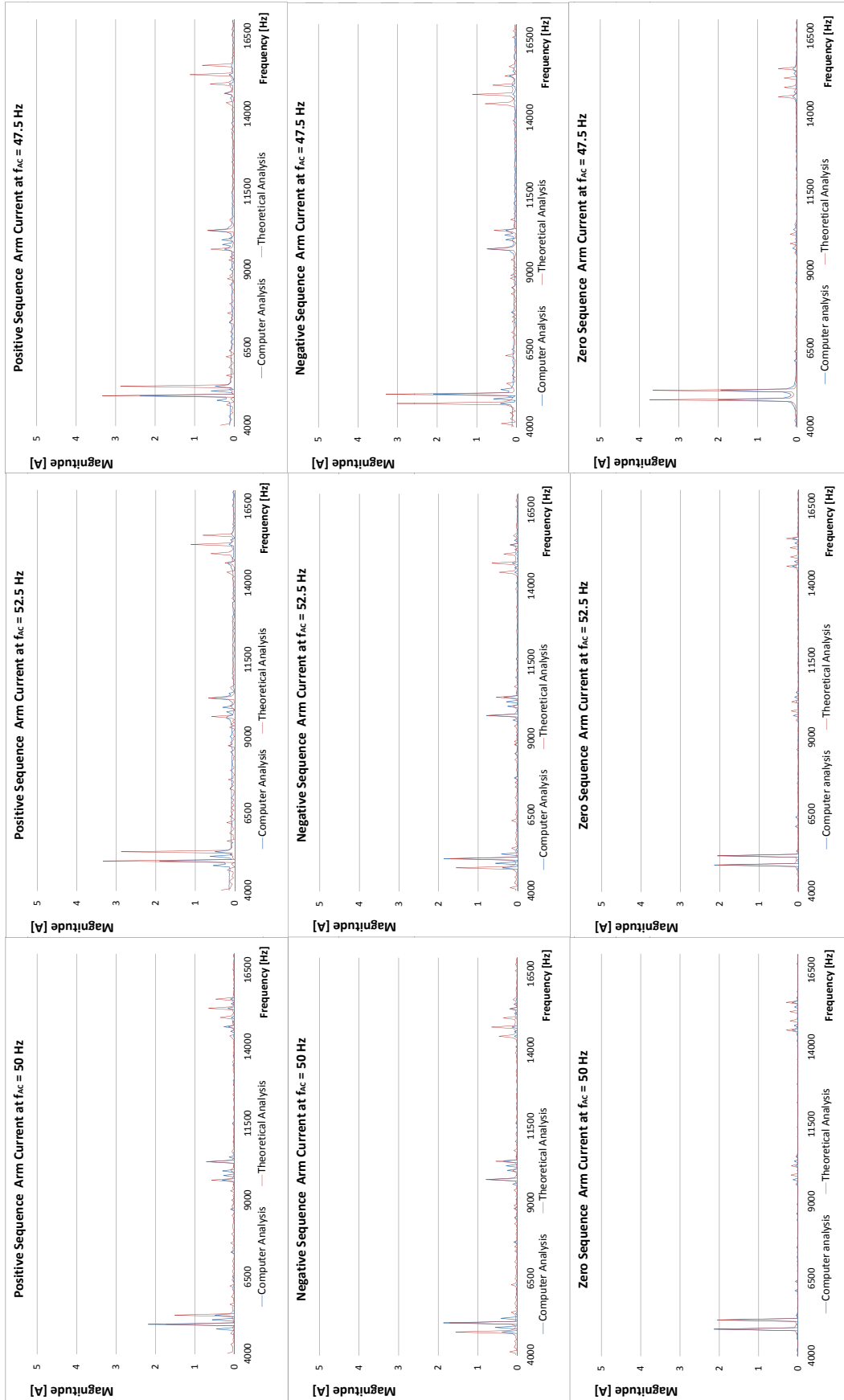


Figure 9: Comparison of sequence current harmonic spectra for different values of f_{AC} .

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