

# Elahe Jalalpour

## Curriculum Vitae

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### Research Interests

- Computer Networks
- Software Defined Networking
- Internet of Things
- Computer and System Architectures
- FPGA

### Education

2012–2016 **B.Sc. Computer Engineering**, Amirkabir University of Technology, Tehran.  
GPA – 17.31 out of 20

2008–2012 **High School, Diploma of Math & physics**, Manzoumeh Kherad Institute, Tehran.  
GPA – 19.80 out of 20

### Patents

Title *Intelligent Control System of Steering Wheel*

Issued 03 / 2011

IR Patent 69363

### Working Experiences

Summer 2015 **Iranian Telecommunication Research Center (ITRC)**, Tehran, Iran.

ITRC is the leading company in Iran in the field of Network. Since I was interested in SDN, I worked on a firewall application then I ran it on Ryu controller. The source code can be found [here](#).

### Teaching Experiences

Winter 2014 **Teacher Assistant**, COMPUTER ARCHITECTURE, Amirkabir University of technology, Under supervision of Prof.Zarandi.

Fall 2015 **Teacher Assistant**, INTRODUCTION TO PROGRAMMING, Amirkabir University of technology, Under Supervision of Prof.Bakhshi.

Fall 2015 **Teacher Assistant**, COMPUTER NETWORKS II, Amirkabir University of technology, Under Supervision of Prof.Sabaei.

Fall 2015 **Teacher Assistant**, OPERATING SYSTEMS, Amirkabir University of technology,  
Under Supervision of Prof.Zarandi.

## Awards

- 2013–2015 Ranked in top 4 Computer Hardware Engineering Students
- 2014 Eligible to choose **second major** due to outstanding performance
- 2012 Ranked in top 0.6% of Nation-wide University Entrance Exam among all Iranian Students of Math. & Physics
- 2012 Ranked in top 0.1% of Nation-wide University Entrance Exam among all Iranian Students of Foreign Languages (English)
- 2011 **1st** Place in Iran Open Robocup Competition Demo League as a Member of *Kherad* team
- 2010 & 2011 Semi-finalist at National Mathematics Olympiad
- 2009 Earned **Merit Medal** in International World Youth Mathematics Competition (IWYMIC) Durban, South Africa

## Computer skills

- **Programing & Hardware Design Languages.**  
Java, C/C++, Python 3, Verilog, VHDL, 8086 Assembly
- **Typesetting.**  
L<sup>A</sup>T<sub>E</sub>X, Microsoft Word, LibreOffice, Pages, Vim
- **Hardware Simulators.**  
Xilinx ISE Design Suite, P-Spice, H-Spice, Proteus
- **Web Development.**  
HTML
- **Other.**  
Netbeans, Eclipse, Wireshark
- **Operating Systems.**  
Windows, OS X, Ubuntu, Fedora

## Publications

- 2015 **E.Jalalpour**, *Consistent Update in SDN*, Tehran.  
technical report for Research Method and Technical Report Writings course (In Persian)
- 2014 **E.Jalalpour**, *Real Time Cache Performance Analyzing for Multi-core Parallel Programs*, Tehran.  
project report for Computer Architecture course (In Persian)
- 2015 **E.Jalalpour**, *Introduction to SDWall Platform*, Iranian Telecommunication Research Center (ITRC), Tehran.  
guide to use and install SDWall platform (In Persian)

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## Research Experiences

- 2015 **Consistent update in SDN**, Tehran.  
This research was done for Research Method and Technical Report Writings course (Technical Report and Poster)
- 2015 **SDN platforms and tools**, *Iranian Telecommunication Research Center (ITRC)*, Tehran.  
Research on different platforms, controllers and apps on SDN

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## Languages

- Persian **Native proficiency**  
(Farsi)
- English **Professional working proficiency**
- French **Elementary proficiency**

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## Projects

- 2012 **Phone Book**, C.  
Implementation of Phone Book with file
- 2014 **HTTP Proxy**, JAVA.  
Implementation of a HTTP and HTTPS proxy server
- 2013 **JUMONG (Java Ultimate Maze Obstacle Neutralizer Game)**, JAVA.  
Implementation of a graphical game with multiplayer support
- 2013 **River Rider**, JAVA.  
Implementation of a graphical game with multi-threading support
- 2013 **Bubbles**, JAVA.  
Implementation of a Java based bubbles screen saver
- 2014 **FAT Parser**, C.  
Implementing FAT-16 and FAT-32 parser with delete, list and retrieve support
- 2014 **Disassembling DOS Executable File**.
- 2015 **FPGA Co-Design**, C & VHDL.  
Implementing hardware modules in VHDL and using them for having a cryptographic algorithm in a software environment
- 2015 **Transistor Level Ripple Adder**, HSPICE.  
Designing and implementing transistor level ripple adder in three families: Static CMOS, Dynamic CMOS and DCVSL
- 2013 **Simon Game**, *Proteus*.  
Design and implementation of Simon game's logic circuit

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## References

**Professor Bahador Bakhshi**, *Assistant Professor*.  
Computer Engineering and IT Department, Amirkabir University of Technology  
Email: bbakhshi@aut.ac.ir

**Professor Hamid Reza Zarandi**, *Assistant Professor*.

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**Professor Masoud Sabaei**, *Assistant Professor*.

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