Course Plan

FPGA-based Digital System Design

Part I: SystemVerilog HDL, Xilinx vivado

1. **SystemVerilog HDL Basics**
    - Modules
    - Combinational logic
    - Case statements
    - If statements
    - Truth tables with don't cares
    - Sequential logic
    - Blocking and non-blocking assignments
    - Synchronous and asynchronous design
    - Behavioral and structural modeling
    - Data types
    - Parameterized modules
    - Testbenches
2. **Digital Design Basics**
    - Digital Combinational/Sequential Building Blocks
        - Arithmetic circuits (Addition, subtraction, comparators, ALU, shifters and rotators, multiplication, division)
        - Counters
        - Shift registers
        - Memories
    - Finite State Machines
        - Design strategy (Meally and Moore models)
        - Sequencers
        - Traffic light controller
        - Factoring state machines
        - Case study: SDRAM controller
    - Timing of sequential logic
        - System timing (setup time and hold time)

        - Clock skew
        - Metastability
        - Synchronizers
        - Derivation of resolution time

3. Parallelism (Pipelines)

4. FPGA structure (building blocks)

- Overview on Xilinx different families

5. Selection of best FPGA for a specific project

- Selection criteria

6. FPGA design flow (in Xilinx Vivado)

7. Testbenches in different levels

- Behavioral
- Post-synthesis
- Post-place and route

8. Overview on ZYBO Z7 development board

9. Writing an XDC file

- Pin assignment
- Timing constraints

10. Adding IP from IP catalog

- Clocking wizard
- Memories

11. Timing Analysis in Vivado

- Timing parameters
- Critical path
- Maximum frequency

12. Timing Issues in FPGA Synchronous Circuits

13. Clock Domain Crossing and Meta-stability

- Dual-clock FIFOs
- Using FIFO generator

14. HDL Project 1: Simple HDMI processor

15. HDL Project 2: Audio meter/recorder/player

16. HDL Project 3: Digit recognizer

Course Plan

FPGA and Processor-based Digital System Design

Part II: C/C++, Xilinx SDK

1. **Generating Block Designs**
2. **Xilinx SDK**
3. **Writing software (C/C++) for the processor**
4. **Efficient C and C++ code for embedded systems**
5. **Integrating hardware and software flows**
    a. Synthesise and place&route the whole system on ZYBO Z7 board
6. **Projects**