## **DAC YF**

## Read Performance Optimization of High-Density NAND Flash Memory

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Work 1: Interference between Reads and Writes is serious due to the significant Solid state drives (SSDs) has been widely latency gap in high-density flash memory. deployed due to the development of high--- Access Characteristic auided Partition Scheme density and low-cost NAND flash memories. However, the read performance is degraded RQ WQ because of its low reliability. Reliability degraded! Read-Only Write-Only Requests Requests I/O Requests Work 2: The read latency of high-Host Interface Logic density flash is increasing due to the Chip1 Chip2 Chip3 Chip4 latency variation among multiple bits. SSD Controller Chip5 Chip6 Chip7 Chip8 -- Read Latency Variation Aware Scheme Address Mapping Read Area Write Area Partition Scheme Hot Data FTL I/O Scheduling Wear Leveling Key Takeaways: **ECC Garbage Collection** Hot Data Hot Data Increased Latency Decreased Reliability Hot Data Cold Data Hot Data Hot Data Flash memory is developed with large capacity, low cost but low reliability. Hot Data Chip1 Chip2 Chip3 Chip4 Cold Data Cold Data We focus: 1-Page → Cold Data Hot Data Interference between R&W 2-Page -Chip5 Chip6 Chip7 Chip8 Exploit the read latency variation 3-Page → amona multiple pages in a wordline The Architecture of SSD Identification and Placement(QLC SSD)