QIE11 Specifications

Production version

Tom Zimmerman, Fermilab
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The QIE10 and QIE11 are the latest additions to the family of QIE devices. They are targeted for the CMS and ATLAS upgrades. Both devices are designed for negative-only inputs. QIE10 has a hardwired gain of approximately 3 fC/LSB and maintains constant input impedance over the whole dynamic range, making it suitable for reading out PMTs that are connected to the QIE with a significant length of cable (transmission line). QIE11 has programmable gain (accomplished with programmable input shunts) and lower (non-constant) input impedance. This document covers the specifications and operation of the QIE11.

QIE11 integrates negative input charge pulses in 25 nS buckets over a large dynamic range and digitizes the result with approximately constant resolution over the entire dynamic range. It accomplishes this by simultaneously integrating the input charge on four different ranges which are scaled by factors of 8. Based on the signal magnitude, just one of these ranges is selected for digitization. The appropriate integrator output is fed to a custom on-chip pseudo-logarithmic FADC. The FADC bin size doubles several times over its full range, so that the bin size at the top of the FADC is 8 times the bin size at the bottom of the FADC. Since the 4 integrator ranges are also scaled by a factor of 8, the end result is that the QIE resolution (the FADC bin size divided by the signal magnitude) is held between 0.7% and 1.4% over the entire dynamic range of the QIE (except at the low end, of course).

This scheme essentially provides a floating point digitization of the input charge every 25 ns. The resultant digital output consists of 6 bits of mantissa (FADC outputs) and 2 bits of exponent (range code). The QIE operation is pipelined with 4 phases to allow deadtimeless operation, so a 2-bit "CapID" code is also provided to indicate which phase is associated with each result. Ideally, each phase or CapID has identical response, but in practice there can be small differences in the pedestal at the low end, so a pedestal adjustment for each phase is provided. The digital output result for a given integrated input pulse has a 4 clock period latency. Since the QIE11 is pipelined with 4 phases, it is integrating the input charge for the CapID0 phase while outputting the digitized result of the previous CapID0 integration.

A TDC is also included on the chip. A programmable-threshold discriminator detects the time at which the input pulse occurs. This latches the state of a TDC Delay Locked Loop (DLL), which divides the 25 ns clock period into fifty 500 ps intervals. A 6-bit TDC code is output along with the mantissa and exponent. The discriminator digital output (LVDS) is also available.

There are 8 digital data outputs (LVDS) to convey the mantissa, exponent, TDC, and capID (total of 16 bits). New data is output on each edge of the clock, yielding an effective 80 MHz data output rate.

Many of the chip parameters are programmable via a serial shift register, which is used to load

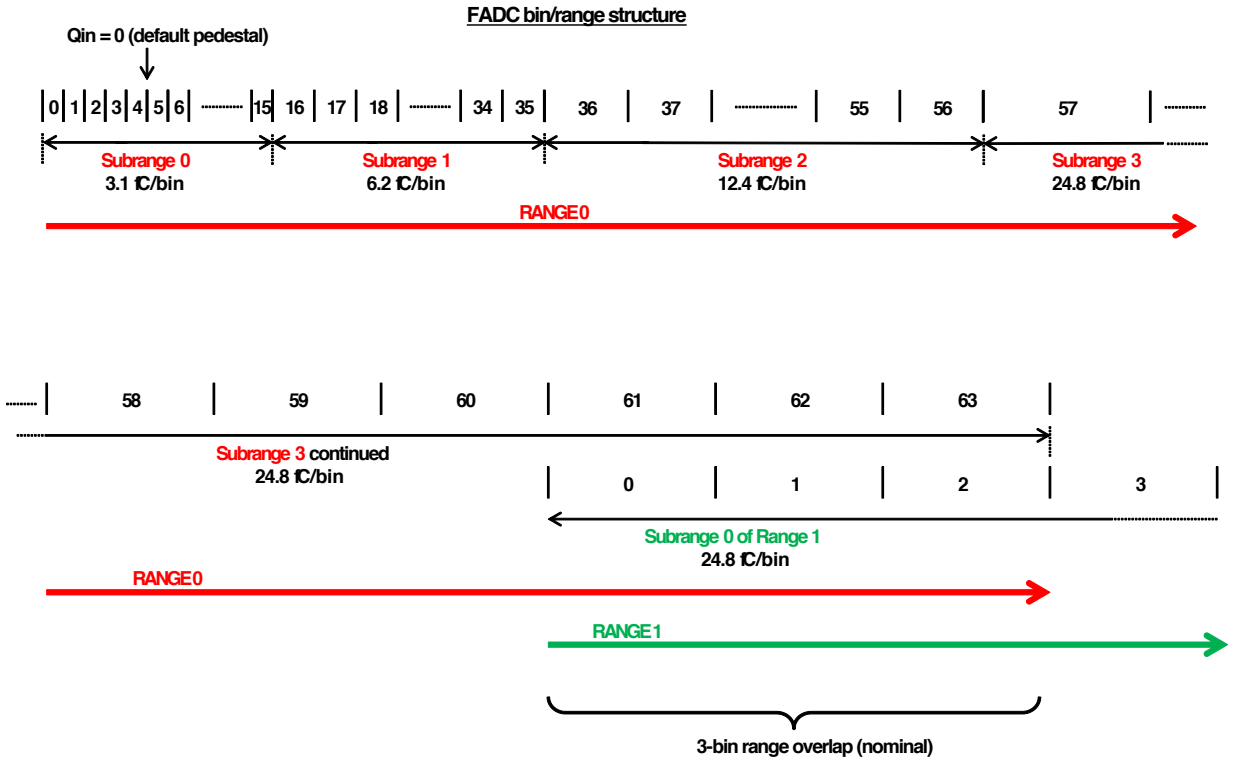
an SEU-hard shadow register. The shadow register contents can be transferred back to the serial shift register for subsequent readout and verification.

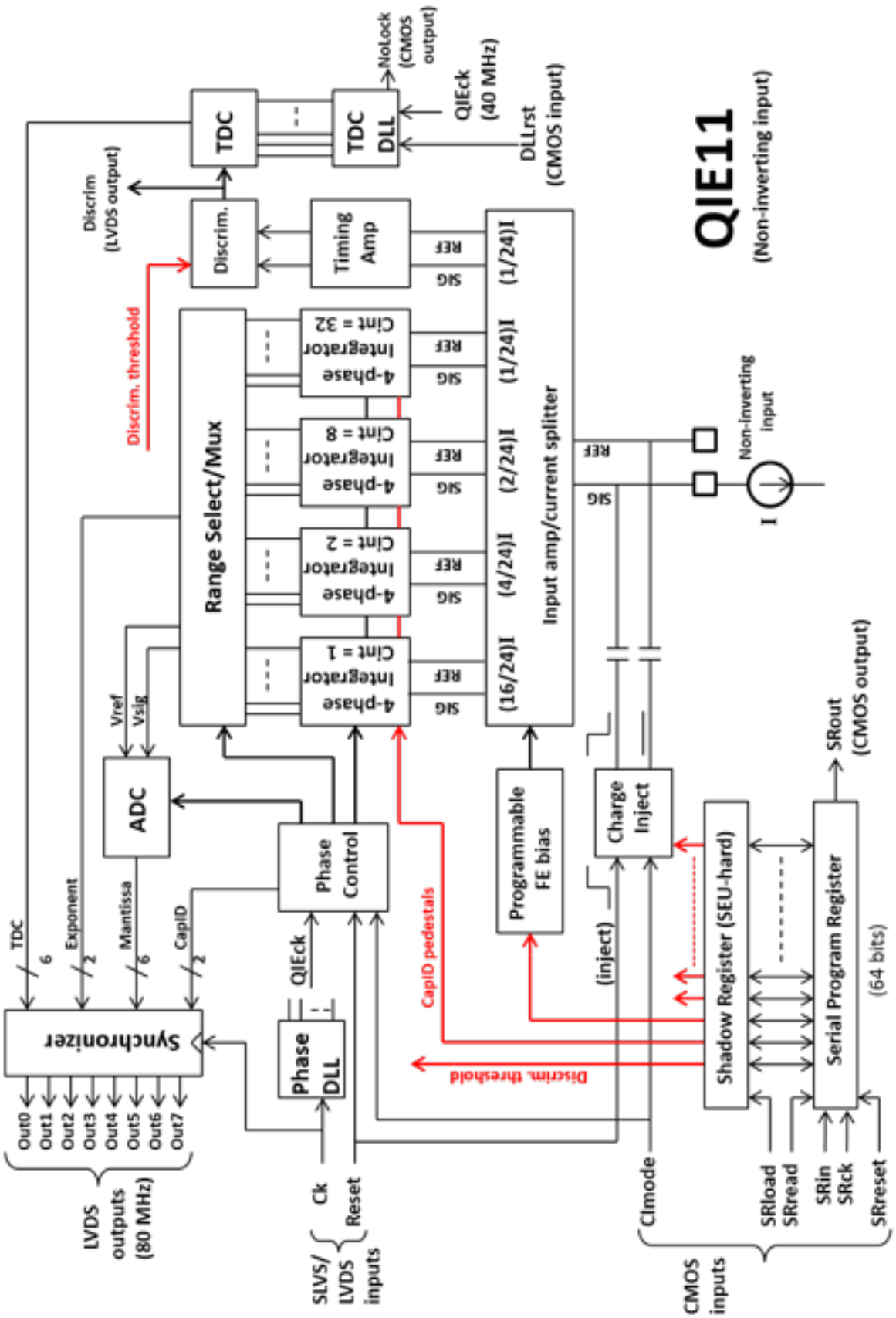
The 25 ns bin structure is driven by the LVDS input clock, which should run at 40 MHz. The actual internal integration window time is somewhat delayed from the input clock, due to fixed internal delays. However, an input pulse that arrives at the very beginning of the internal integration window should always result in TDC bin 0. If desired, the phasing of the integration window relative to the input clock can be additionally delayed. This is done by activating a Phase DLL, providing 0.5 ns delay steps across the whole 25 ns period. The desired delay tap is chosen with a program register setting.

The nominal sensitivity of QIE11 is 3.1 fC per count at the low end (with no programmable input shunt selected). The gain of any particular chip can vary from this nominal value due to process variations, so each chip must be calibrated. The nominal maximum charge that can be digitized is approximately 350 pC, yielding a nearly 17-bit dynamic range. The following table shows the nominal mapping of input charge to output code, assuming the default pedestal and a nominal range overlap of 3 bins. In reality, each range will require a gain and offset calibration constant.

Nominal input charge to output code mapping for default settings:

Range (Exp.)	Input Charge	ADC Code (Mant.)	Sensitivity (Q/bin)
0	-16 fC – 34 fC	0 – 15	3.1 fC/bin
0	34 fC – 158 fC	16 – 35	6.2 fC/bin
0	158 fC – 419 fC	36 – 56	12.4 fC/bin
0	419 fC – 592 fC	57 – 63	24.8 fC/bin
1	517 fC – 915 fC	0 – 15	24.8 fC/bin
1	915 fC – 1910 fC	16 – 35	49.6 fC/bin
1	1910 fC – 3990 fC	36 – 56	99.2 fC/bin
1	3990 fC – 5380 fC	57 – 63	198.4 fC/bin
2	4780 fC – 7960 fC	0 – 15	198.4 fC/bin
2	7960 fC – 15.9 pC	16 – 35	396.8 fC/bin
2	15.9 pC – 32.6 pC	36 – 56	793.6 fC/bin
2	32.6 pC – 43.7 pC	57 – 63	1587 fC/bin
3	38.9 pC – 64.3 pC	0 – 15	1587 fC/bin
3	64.3 pC – 128 pC	16 – 35	3174 fC/bin
3	128 pC – 261 pC	36 – 56	6349 fC/bin
3	261 pC – 350 pC	57 – 63	12.70 pC/bin


FADC bin/range structure
Qin = 0 (default pedestal)
0 1 2 3 4 5 6 ..... 15 16 17 18 ..... 34 35 36 37 ..... 55 56 57 .....
Subrange 0
3.1 fC/bin
Subrange 1
6.2 fC/bin
Subrange 2
12.4 fC/bin
Subrange 3
24.8 fC/bin
RANGE 0
..... 58 59 60 61 62 63
Subrange 3 continued
24.8 fC/bin
0 1 2 3
Subrange 0 of Range 1
24.8 fC/bin
RANGE 0
RANGE 1
3-bin range overlap (nominal)


QIE11
(Non-inverting input)
TDC
TDC DLL
NoLock (CMOS output)
QIEck (40 MHz)
DLLrst (CMOS input)
Discrim (LVDS output)
Discrim.
Timing Amp
Discrim. threshold
Range Select/Mux
4-phase Integrator Cint = 32
4-phase Integrator Cint = 8
4-phase Integrator Cint = 2
4-phase Integrator Cint = 1
REF
SIG
(1/24)I
(1/24)I
(2/24)I
(4/24)I
(16/24)I
Input amp/current splitter
Non-inverting input
I
Vref
Vsig
ADC
Phase Control
Programmable FE bias
Charge Inject
(inject)
CapID pedestals
Discrim. threshold
Shadow Register (SEU-hard)
Serial Program Register
(64 bits)
SRout (CMOS output)
TDC
Exponent
Mantissa
CapID
6
2
6
2
Synchronizer
QIEck
Phase DLL
Out0
Out1
Out2
Out3
Out4
Out5
Out6
Out7
LVDS outputs (80 MHz)
Ck
Reset
SLVS/ LVDS inputs
Clmode
SRload
SRread
SRin
SRck
SRreset
CMOS inputs

QIE11 pin summary

Analog inputs
InSig
InRef

Power/gnd
vdd (3.3V)
vddFE (3.3V)
dvdd (3.3V)
avdd (5.0V)
agnd
dgnd

Analog bias
Idcset
Rsetp
ClampRef
Clamp
IdumpSig
Rref

LVDS digital inputs
Reset

SLVS/LVDS digital inputs
Ck

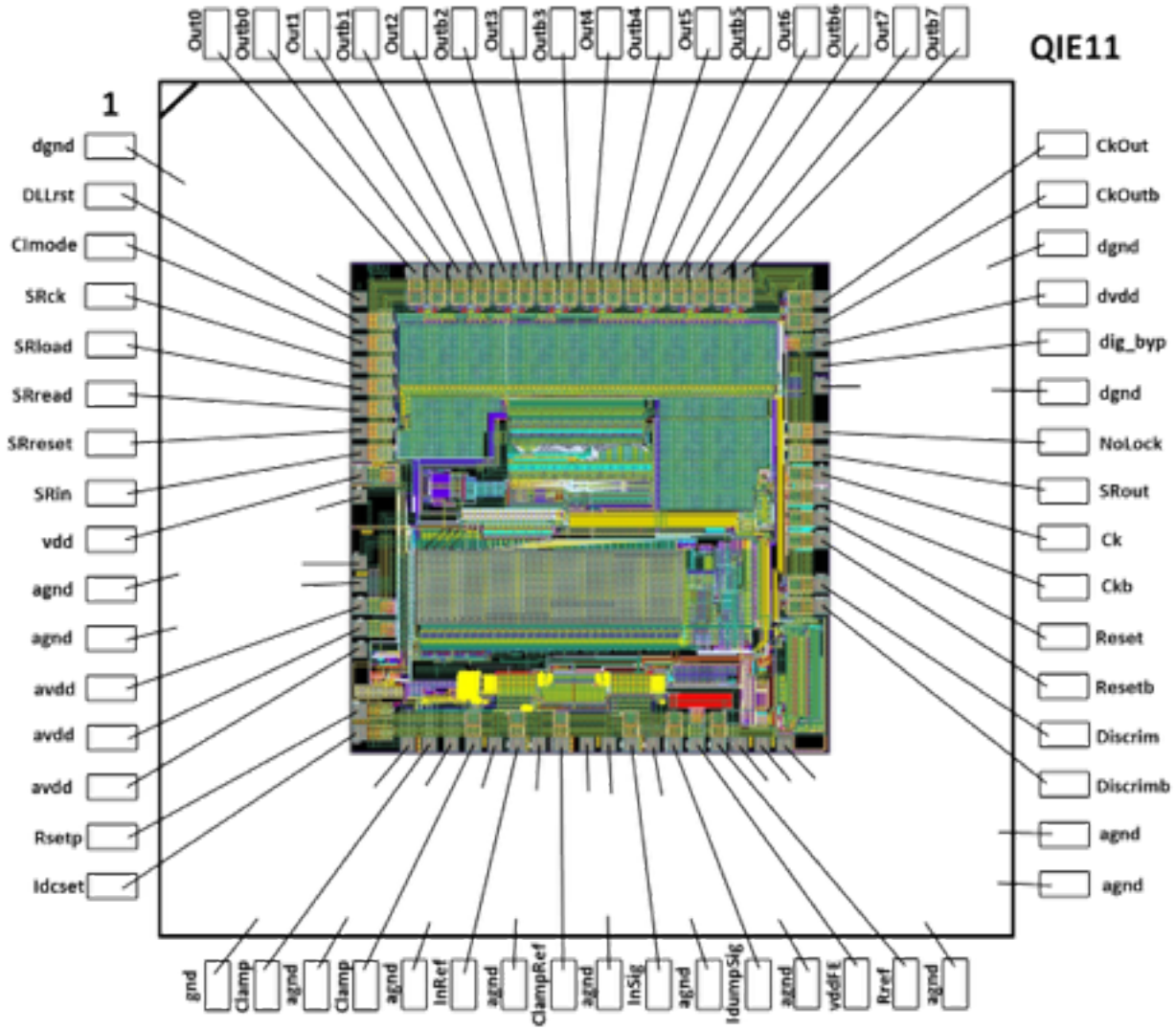
CMOS digital inputs
DLLrst
CImode
SRin
SRck
SRreset
SRload
SRread

CMOS digital outputs
SRout
NoLock

LVDS digital outputs
Out0-7
Discrim

CkOut

QIE11 bonding diagram



Pin assignments and descriptions

See the "Recommended PCB layout" figure below for the QIE11 connection philosophy.

1. **dgnd:** Digital ground. Connect only to the digital ground plane of the PCB.

2. **DLLrst:** Delay Locked Loop reset. 3.3V CMOS level, high = reset. Forces a reset on both of the internal DLLs, after which they should find lock when the input clock (**Ck**) starts running. However, the DLLrst should typically not be needed. When the QIE11 is powered up, the DLLs will automatically be reset, and when a clock input is applied they should find lock (typically within a few microseconds). If a DLL does happen to lose lock, it should automatically correct itself and find lock again as long as the clock is running. Default = low if pin is not connected.

3. **CImode:** Charge Inject mode. 3.3V CMOS level, high = Charge Inject mode. In this mode, the functionality of the Reset input is changed, so that a positive-going transition of the Reset input causes a negative input charge to be injected through an on-chip capacitor (in this mode, toggling Reset does **not** reset the chip and the capID). The magnitude of the charge is controlled by 3 bits in the program register. The subsequent negative-going transition of the Reset input will then inject the *opposite* polarity (positive) pulse at the input, and the QIE will then be effectively disabled for some period of time while it recovers. The recovery time will depend on the magnitude of the injected pulse. Default = low if pin is not connected.

4. **SRck:** Serial program shift register clock (CMOS). See "serial shift register programming" timing diagram below for functionality of the serial program register section. Default = low if pin is not connected.

5. **SRload:** Shadow register load (CMOS). Transfers the serial shift register contents to the shadow register. The shadow register is what actually controls the programmable chip settings and is SEU hard. Default = low if pin is not connected.

6. **SRread:** Shadow register read (CMOS). Transfers the shadow register contents to the serial shift register so that it can then be read out to verify the settings (CMOS). Does not alter the shadow register contents. Default = low if pin is not connected.

7. **SRreset:** Shift register reset (CMOS). Resets the serial shift register to its default condition (see shift register bit assignments below). However, it does not load the shadow register – this must be done explicitly with the **SRload** pin. Power-up is a special case: the serial shift register is automatically reset to default conditions and subsequently transferred into the shadow register with no external action required. Default = low if pin is not connected.

8. **SRin:** Shift register input (CMOS). Data input to the serial program register, shifted

through with **SRck**. Default = low if pin is not connected.

9. **vdd:** 3.3V analog supply for the ADC.

10. **agnd:** Analog ground. Connect only to the analog ground plane of the PCB.

11. **agnd**

12. **avdd:** 5.0V analog supply for the bandgap reference, autoranger, and ADC.

13. **avdd:** 5.0V analog supply for the integrators.

14. **avdd:** 5.0V analog supply path used to dump excess input signal current.

15. **Rsetp:** DC bias setting for the input feedback amplifier. The input impedance at the low end of the dynamic range is determined by the value of this bias current. The actual amplifier bias current is 30 times larger than the value set at the pin. The nominal Rsetp bias current is 200 uA out of the pin, and the nominal pin voltage is 435 mV. Therefore, use a 2.2K resistor from the Rsetp pin to ground. A lower bias current can be used if somewhat higher input impedance is acceptable.

16. **Idcset:** DC bias current setting for the input splitter. The actual splitter bias current is 4 times smaller than the value set at the pin. The nominal pin bias is current is 72 uA into the pin. This bias level is appropriate for the nominal clocked integration period of 25 ns. The nominal pin voltage is 1.04V, therefore use a 31K resistor to 3.3V. This bias current can also be completely set by the program register, in which case no external resistor is required. The splitter bandwidth is determined by the value of Idcset, therefore the program register can be used to tweak the bandwidth to some extent. However, the bandwidth should not need to be set with high accuracy, so tweaking is probably not necessary. The default program register setting is for an internal Idcset bias of zero, and in this case Idcset is completely determined by the external resistor value.

17. **agnd**

18. **Clamp:** Internally generated bias voltage used by the input amplifier. There are two pin instances of the Clamp signal, pin 18 and pin 20. With the QIE11, these two pins must be treated separately (unlike the QIE10). Pin 18 should be connected through a series damping resistor of 24 ohms to a 5 pF capacitor to ground. This connection path should be as short as possible (lowest inductance).

19. **agnd**

20. **Clamp:** Connect to a 1uF capacitor to ground with the shortest possible connection path (lowest inductance).

21. **agnd**

22. **InRef:** Reference input. This reference input ideally will have a cable or interconnect attached to it which looks identical to the signal input (although the reference input should actually have no signal applied to it).

23. **agnd**

24. **ClampRef:** The QIE11 will be operational if this pin is left floating, however, for minimum equivalent input noise, it should be bypassed to ground with 0.1 uF.

25. **agnd**

26. **InSig:** Signal input. This input accepts negative input charge only (current out of the pin). The signal input trace should be connected directly to this input, and should be completely encased with ground planes and traces right up to the pin.

27. **agnd**

28. **IdumpSig:** Path for shunted signal current to be dumped (when Gsel<0:4> is non-zero). This pin must be bypassed to ground with a 1 uF or larger capacitor. It is important to maintain the minimum possible inductance in this connection path.

29. **agnd**

30. **vddFE:** 3.3V analog supply for the front end.

31. **Rref:** Reference resistor for the timing discriminator. The value of this resistor sets the timing discriminator threshold DAC bit size. The pad voltage is internally held to approx. 400 mV. Use a 10K resistor from the pad to ground to set a 40 uA reference current, which gives a DAC sensitivity of 0.156uA/bit (which translates to 24 X 0.156 uA, or approx. 3.7 uA, at the QIE11 input). This "current" threshold sensitivity depends only on the value of **Rref** resistance, but transposing it to a "charge" threshold of course depends on the pulse shape. If a triangular input pulse shape has an input rise time of 3 ns and a fall time of 10 ns, then an LSB of the threshold DAC corresponds to an input charge of about 24 fC. Instead of an external resistor, an internal **Rref** resistor can be selected with the program register, in which case an external resistor is not required. However, if absolute accuracy is required, an external 1% resistor should be used.

32. **agnd**

33. **agnd**

34. **agnd**

35. **Discrimb:** Timing discriminator output complement (LVDS).

36. **Discrim:** Timing discriminator output (LVDS). A rising digital transition is observed here when the QIE11 input current exceeds the threshold set by the timing discriminator threshold DAC. The output falls when the input current goes back below the threshold. There is internal hysteresis in the discriminator in order to avoid multiple output pulses due to noise.

37. **Resetb:** QIE reset input complement (LVDS).

38. **Reset:** QIE reset input (LVDS). The QIE11 Reset input has two functions. If **CImode** is low (QIE11 "normal" mode), a **Reset** pulse serves to set the QIE11 to a known condition where CapID = 3. If **CImode** is high (QIE11 "charge inject" mode), the positive-going transition of **Reset** injects charge into the input. The value of this charge is determined by a 3-bit code in the program register. The negative-going transition of **Reset** injects an opposite-sign pulse into the input, which will de-bias the QIE11. Some recovery time will then be required, depending on the charge injection magnitude.

39. **Ckb:** QIE clock input complement. (SLVS or LVDS).

40. **Ck:** QIE clock input (SLVS or LVDS). This clock input controls the integration gate and other internally clocked analog functions. The nominal frequency is 40 MHz (25 ns integration gate).

41. **SRout:** Serial shift register output (CMOS). When daisy-chaining chips, connect this output directly to the **SRin** of the next chip.

42. **NoLock:** CMOS output that goes high whenever either of the Delay Locked Loops on the chip are not locked (the Phase DLL or the TDC DLL).

43. **dgnd**

44. **dig_byp:** Return for the external **dvdd** bypass capacitor. Connect a 0.1 uF capacitor directly between this pin and **dvdd** (pin 45). Do <u>not</u> connect this bypass cap to a ground plane or anywhere else.

45. **dvdd:** Digital power supply (3.3V). The same regulator can be used to supply all 3.3V supply pins (both digital and analog), but a separate traces should be used that meet only at the regulator output.

46. **dgnd**

47. **CkOutb:** LVDS output copy of the input clock (complement).

48. **CkOut:** LVDS output copy of the input clock. The typical delay between the LVDS clock input (pins 39 and 40) and the LVDS CkOut (pins 47 and 48) is 4.2 ns. The 8 LVDS data outputs are all delayed approximately 1.5 ns from the CkOut transition, so that CkOut may be used to reliably latch them before they change state (effective 1.5 ns

hold time.

49. **Out7b:** Data output7 complement (LVDS). See Output Data Format diagram below.

50. **Out7:** Data output7 (LVDS). See timing diagrams below.

51. **Out6b:** Data output6 complement (LVDS).

52. **Out6:** Data output6 (LVDS).

53. **Out5b:** Data output5 complement (LVDS).

54. **Out5:** Data output5 (LVDS).

55. **Out4b:** Data output4 complement (LVDS).

56. **Out4:** Data output4 (LVDS).

57. **Out3b:** Data output3 complement (LVDS).

58. **Out3:** Data output3 (LVDS).

59. **Out2b:** Data output2 complement (LVDS).

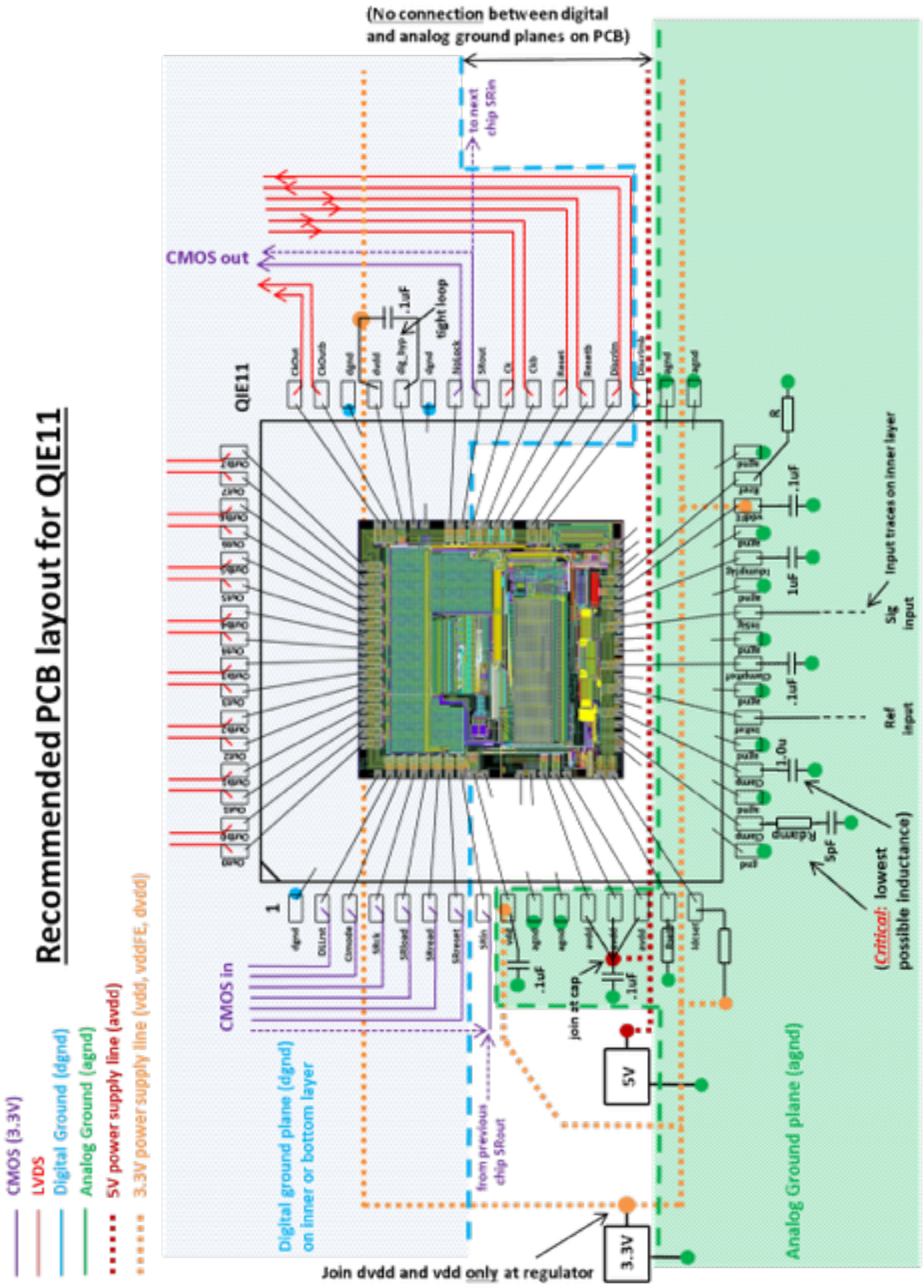
60. **Out2:** Data output2 (LVDS).

61. **Out1b:** Data output1 complement (LVDS).

62. **Out1:** Data output1 (LVDS).

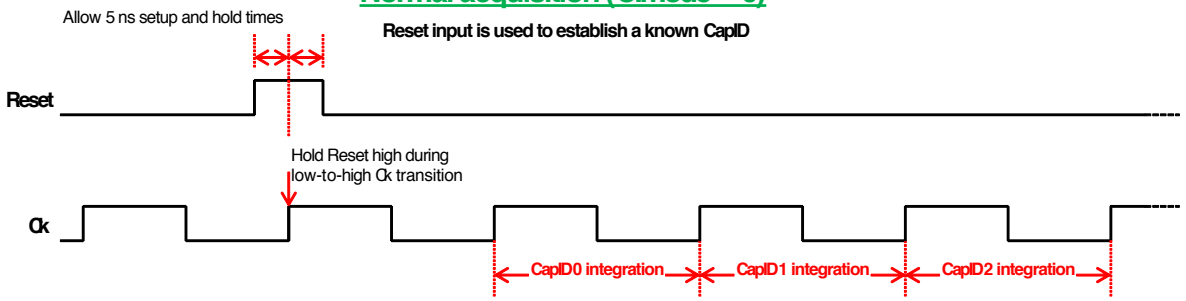
63. **Out0b:** Data output0 complement (LVDS).

64. **Out0:** Data output0 (LVDS).


Recommended PCB layout for QIE11
CMOS (3.3V)
LVDS
Digital Ground (dgnd)
Analog Ground (agnd)
5V power supply line (avdd)
3.3V power supply line (vdd, vddFE, dvdd)
(No connection between digital and analog ground planes on PCB)
to next chip SRin
CMOS out
QIE11
.1uF
tight loop
CMOS in
from previous chip SRout
Digital ground plane (dgnd) on inner or bottom layer
join at cap
5V
3.3V
Join dvdd and vdd only at regulator
Analog Ground plane (agnd)
Input traces on inner layer
Sig input
Ref input
1uF
1.0u
5pF
(Critical: lowest possible inductance)

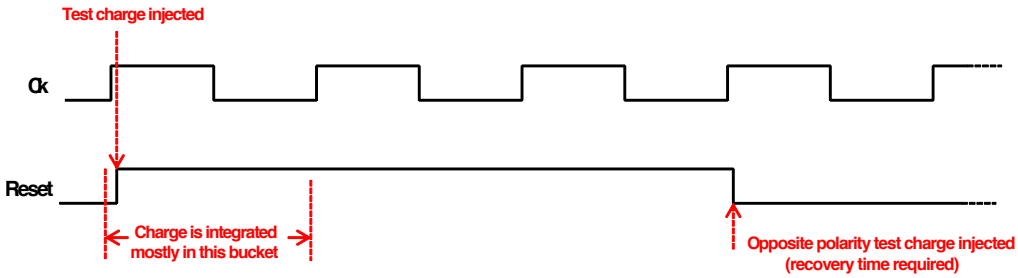
QIE11 modes of operation

Normal acquisition (CImode = 0)



At power-up, the CapID is automatically set to 3
with an internal power-up reset circuit.

Charge Inject mode (CImode = 1)

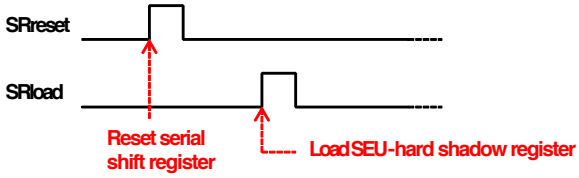


QIE11 serial shift register programming

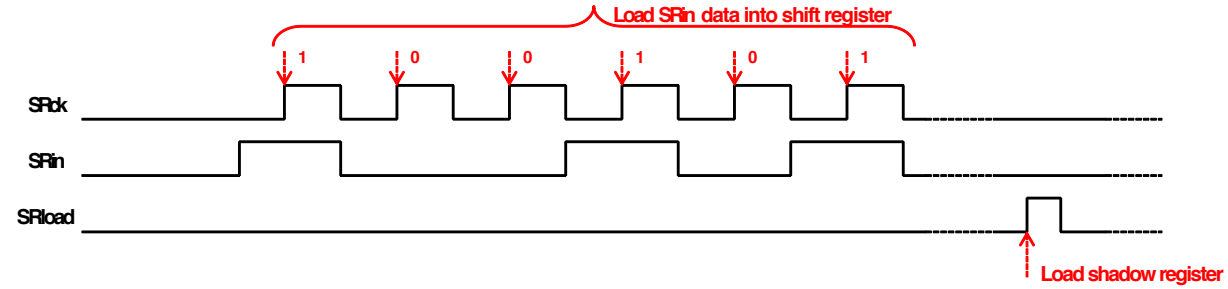
Serial Shift Register programming

Default program register values are automatically loaded with an on-chip power-up reset circuit.
If default values are desired then no action is necessary after power-up.

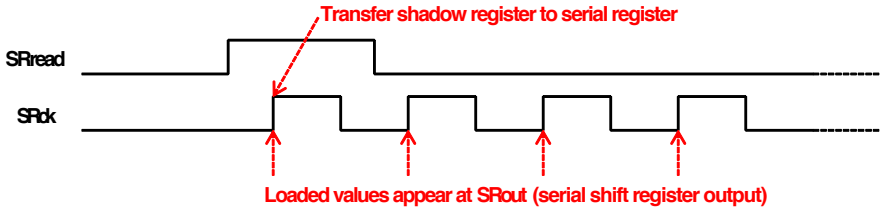
Restore default settings:



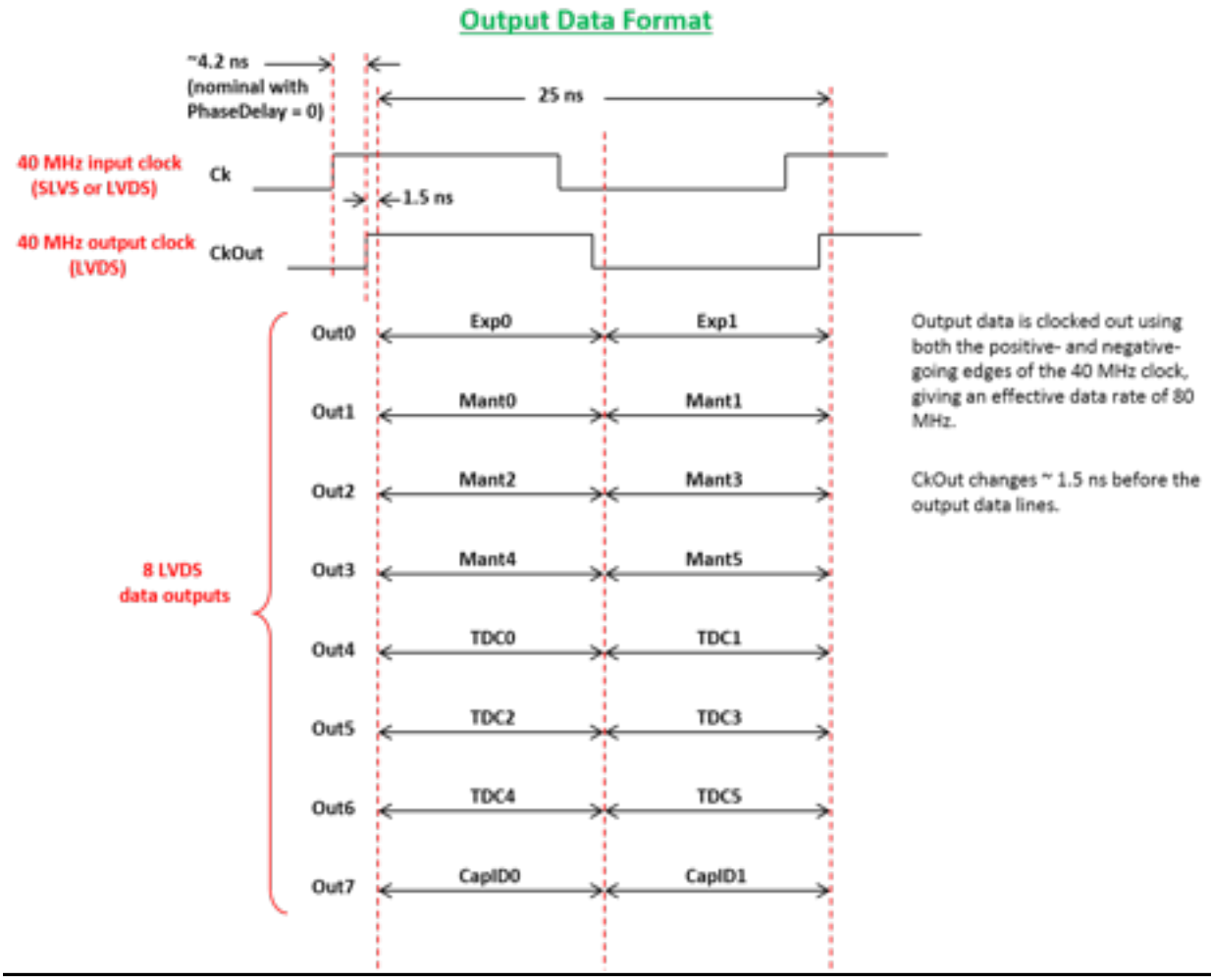
Shift in arbitrary settings:



Read back the loaded shadow register values:



Output Data Format



Output data is clocked out using both the positive- and negative-going edges of the 40 MHz clock, giving an effective data rate of 80 MHz.

CkOut changes ~ 1.5 ns before the output data lines.

TDC functionality

A 6-bit TDC code is generated each clock cycle and is read out along with the mantissa and exponent. The TDC Delay Locked Loop divides the 25 ns clock period into 50 periods of 500 ps each, giving 50 valid time codes. In addition, there are 6 special codes.

The TDC can be programmed to respond to multiple pulses (more than one pulse above threshold in a given bucket) in one of two different ways. In "First Mode", the TDC digitizes the time of the first pulse and ignores subsequent pulses in that bucket. This is the default mode for the TDC, and the intended mode of operation. In this mode, the first pulse in a bucket generates an inhibit signal which prohibits the TDC from seeing any further pulses until bin 1 of the following bucket. Therefore, if a pulse happens to occur in bin 0 of the next bucket, this pulse will actually read out as having occurred in bin 1 of that bucket.

If the TDC is set to "Last Mode", then it will digitize the arrival time of the last pulse that occurs in a given bucket. However, the TDC is not optimized for this mode and there are caveats. If a first pulse occurs in the first half of a bucket, and another pulse then occurs in bin 49, then an error will result. Also, if a first pulse occurs anywhere in a bucket and another pulse occurs in bin 0 of the next bucket, an error will result. In both of these situations, a code 58 (Invalid Code) will be put out by the TDC.

When the TDC DLL is locked, the valid TDC time codes are 0 – 49, and are produced only when the discriminator output starts low and goes high within a given bucket.

Special codes: Special code 62 is generated when the discriminator starts high. Special code 63 is generated when the TDC discriminator starts low and remains low (nothing happened). Special code 58 indicates "Invalid Code". This can be caused by an SEU in the TDC encoder logic. It can also happen in certain situations when the TDC is operated in "Last Mode", as discussed above. Code 59 is generated if the either of the Delay Locked Loops on the QIE11 (the Phase DLL or the TDC DLL) are not locked. Code 60 is generated when the Phase DLL is unlocked (but the TDC DLL is locked), and code 61 for the TDC DLL unlocked (but the Phase DLL is locked). If either of the DLLs on the chip are unlocked, this takes precedence over any TDC data that might be present, and the appropriate DLL no-lock condition is reported.

QIE11 serial program shift register bit assignments

The 64 bits are given in the order that they are to be presented at **SRin** for downloading.

0: LVDS/SLVS: Input type select for input **Ck** receiver (**Ck** receiver *only* – the **Reset** input is LVDS only). High is LVDS mode and Low is SLVS mode. Default = high (LVDS). An LVDS input Ck signal may actually work satisfactorily in SLVS mode, but for certain process corners it may not.

1-2: P0, P1: LVDS output level trim bits. A 100 ohm termination is assumed. The default output level is 350 mV.

2-bit code	**Vout**
00	150 mV
01	250 mV
10	350 mV
11	450 mV

3: DiscOn: Enables the discriminator LVDS output. If DiscOn is low, then the discriminator LVDS output is disabled and does not consume any current. If DiscOn is high, then it operates normally. Default = low (off).

4: TGain: Controls the timing amplifier gain. If TGain is low, the timing amplifier gain is at its nominal value, which is optimized for smaller signals. Under this condition, the timing amplifier will saturate with input signals in the upper half of its intended range (when Iref is 40 uA). Therefore, if the Timing Threshold DAC is set in the upper half of its range, TGain should be set high to avoid timing amplifier saturation. Default is low.

5-12: TimingThresholdDAC<0:7>: 8-bit threshold DAC for the timing circuit. The magnitude of the LSB is determined by the Rref resistor. Rref is nominally 10K, which gives a nominal Iref of 40 uA. This gives an LSB magnitude of 0.156 uA at the timing circuit, or 3.74 uA referred to the QIE11 input. For a triangular input pulse with rise time of 3 ns and fall time of 10 ns, the nominal LSB is then equivalent to a charge of ~24 fC. The DAC has a 1-LSB offset, so that for a DAC setting of all zeroes, the charge threshold sits at 24 fC. The maximum threshold (all ones) is then 6120 fC. The default setting is all ones (largest threshold value).

13-15: TimingIref<0:2>: 3-bit code selecting an internal **Rref** resistance value to replace the external **Rref** resistor (see description for pin 34). The resultant internal Iref (current through **Rref**) values are given below, but these can vary substantially (up to 20%) due to internal resistor process variations. The nominal setting for Iref is 40uA. Note that for a setting of 000, no internal Iref is generated. The default setting is 000, in which case Iref must be set with an external **Rref** resistor. The highest accuracy is realized by using an external 1% resistor.

3-bit code	Iref	LSB	LSB at input
000	0	0	0
001	10 uA	0.039 uA	0.94 uA
010	20 uA	0.078 uA	1.87 uA
011	30 uA	0.117 uA	2.81 uA
100	40 uA	0.156 uA	3.74 uA
101	50 uA	0.195 uA	4.68 uA
110	60 uA	0.234 uA	5.62 uA
111	70 uA	0.273 uA	6.55 uA

16-21: PedestalDAC<0:5>: 6-bit code controlling the pedestal DAC, which adjusts the pedestal on the lowest range. The MSB sets the pedestal polarity (1 = positive, 0 = negative), and the remaining 5 bits set the pedestal magnitude, with an LSB of 2fC. Therefore the nominal pedestal can be varied from -62 fC to +62 fC. The default setting is +12 fC (100110).

22-25: CapID0pedestal<0:3>: 4-bit pedestal tweak for CapID0 (lowest range only). The CapID pedestal bits are only required if it is necessary to equalize random or systematic pedestal variation between the four phases (CapIDs). The MSB is the polarity bit (1 = positive, 0 = negative), and the remaining 3 bits set the pedestal magnitude, with an LSB of approximately 0.6 output mantissa ADC counts (~1.9 fC). Default setting = 0.

26-29: CapID1pedestal<0:3>: 4-bit pedestal tweak for CapID1.

30-33: CapID2pedestal<0:3>: 4-bit pedestal tweak for CapID2.

34-37: CapID3pedestal<0:3>: 4-bit pedestal tweak for CapID3.

38: FixRange: one bit to select the ranging mode. 0 = autorange mode, 1 = fixed range mode (where the **RangeSet** bits determine which range). Default setting = 0 (autorange).

39-40: RangeSet<0:1>: 2-bit code to set the range in fixed-range mode.

41-43: ChargeInjectDAC<0:2>: 3-bit code to set the magnitude of charge injection. Nominal values are given below. The overall accuracy is around 10%, but the scaling should be more accurate. The values are arranged so that there are several points on each of the first three QIE11 ranges. The default setting is 100 fC (000).

3-bit code	**Charge**
000	90 fC
001	180 fC
010	360 fC
011	720 fC
100	1.44 pC
101	2.88 pC
110	5.76 pC
111	8.64 pC

44-48: Gsel<0:4>: 5-bit code that sets the transfer gain. If all 5 bits are zero, then the nominal gain is 3.1 fC/LSB (as in QIE10). Each of the Gsel bits controls a parallel input splitter shunt that diverts and dumps some fraction of the input current, modifying the transfer gain. **Gsel<0>** engages a half-size shunt splitter (as compared to the input splitter), **Gsel<1>** an equal size shunt splitter, **Gsel<2>** a double size, **Gsel<3>** a triple size, and **Gsel<4>** a quadruple size shunt splitter.

Gsel code	**fC/LSB**
00000	3.1
00001	4.65
00010	6.2
00100	9.3
01000	12.4
10000	15.5
10010	18.6
10100	21.7
11000	24.8

11010	27.9
11100	31
11110	34.1
11111	35.65

49-53: Idcset<0:4>: 5-bit code to internally set the input splitter bias level (Idcset), nominally 4.5 uA/LSB with a range of 0 – 139.5 uA. This internal bias level adds to any current that is set with an external resistor at the **Idcset** pin. The total Idcset bias can therefore be formed from an external resistor only, from the internally programmed bias only, or from a combination of both. The default setting is 0 (relying only on an external R).

54: CkOutEn: LVDS CkOut enable. If low, it is disabled. Default = high (on).

55: TDCmode: Programs the TDC response to multiple pulses in one bucket. If low, the TDC operates in the intended "First Mode", digitizing the first pulse arrival in a bucket. If high, the TDC is in "Last Mode" and digitizes the last pulse arriving in a bucket, with certain caveats that are explained elsewhere. Default is low (First Mode).

56: Hsel: Hysteresis select for the timing discriminator. If set high, the amount of hysteresis is doubled as compared to when set low. When set low, the hysteresis is less than the peak-to-peak noise, which can produce multiple-pulsing due to the noise. However, for fast pulses (a few ns rise/fall), multiple pulsing is quite rare and this setting may be just fine. Multiple pulsing due to noise will occur much more often for slow pulses (tens of ns rise/fall). In this case, double hysteresis (Hsel high) may be desirable. Larger hysteresis widens the minimum pulse width coming out of the comparator somewhat. The default setting for this bit is low.

57-63: PhaseDelay<0:6>: 7-bit code that sets the phasing delay between the input clock and the internal integration window. This is controlled by the Phase DLL in 0.5 ns increments. With a setting of 0000000, the Phase DLL is disabled, and the internal integration window occurs approximately 4.2 ns after the input clock transition, due to fixed internal delays. Settings 0000001 to 0110001 (1 - 49) activate the DLL and add 0.5 ns integration window delay per bit. The MSB effectively adds one bucket (25 ns) of delay, which is accomplished by simply resetting the capID to 2 instead of 3 when the QIE is reset. Therefore, a setting of 1000000 disables the DLL and resets capID to 2, for an effective delay of 25 ns, and settings 1000001 to 1110001 activate the DLL and effectively add a delay of 25.5 ns to 49.5 ns. The default setting is 0000000.

QIE11 Input Impedance

Unlike the QIE10, the QIE11 input impedance does not remain constant over the entire dynamic range. QIE11 is designed to deliver the lowest possible input impedance. For small input signals, the input impedance is approximately 15 ohms, and for the largest signals, the impedance is of order 1 ohm. Adding a splitter shunt to modify the gain tends to reduce the input impedance somewhat.

With a very low resistive input impedance (like 1 ohm for large signals), the parasitic inductance of the input connection between the detector and the QIE11 becomes very significant. Any appreciable inductance in series with a finite detector capacitance will form a high-Q tank circuit that is prone to ringing. Very careful layout will be required to minimize the characteristic impedance of the detector-to-QIE11 connection. Insertion of a series resistor (a few ohms) at the QIE11 input will be helpful if the resultant increase in total input impedance can be tolerated.

SEU mitigation strategy

The Dice FF cell is used in certain critical areas of the chip to minimize sensitivity to SEUs:

The shadow registers, to which the serial programming shift register contents are transferred, are composed of Dice FF cells so that disruption of programmed settings due to SEUs is minimized.

The ring counter, which rotates the capIDs, is composed of Dice FF cells. This should prevent the ring counter from assuming an “illegal” state. However, the ring counter clock circuitry could see an SEU transient, which would advance the ring counter. If this happens, the capID would be different than expected but the chip should continue to operate. An alternative ring counter circuit based on triple redundancy has been designed and tested, and is functional. However, it has not been evaluated in a radiation environment. This configuration could implement redundant clock buffer circuitry, which would reduce the probability that the ring counter could unintentionally advance due to an SEU.

The ADC and TDC designs use standard FFs, which are vulnerable to SEUs. Therefore, SEUs could occasionally corrupt ADC/TDC output data. However, a corrupt output data value should not affect subsequent proper operation of the chip.