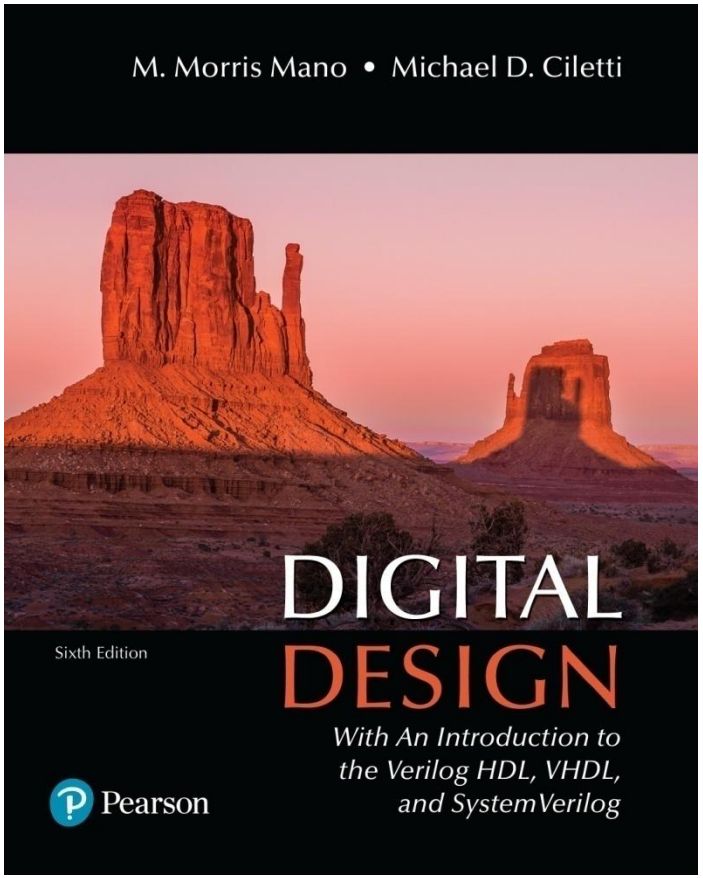
Digital Design

With an Introduction to the Verilog HDL, VHDL, and SystemVerilog

6th Edition



Chapter 05

Synchronous Sequential Logic

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Figure 5.1
Block diagram of sequential circuit.

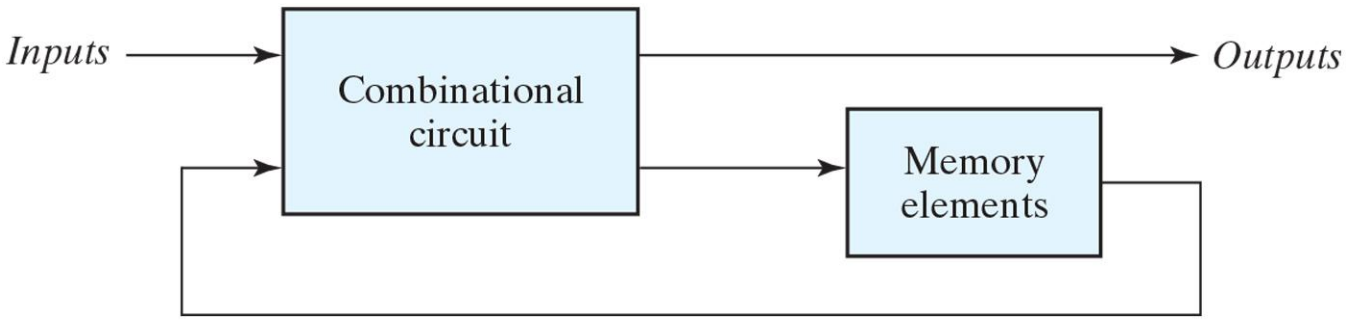

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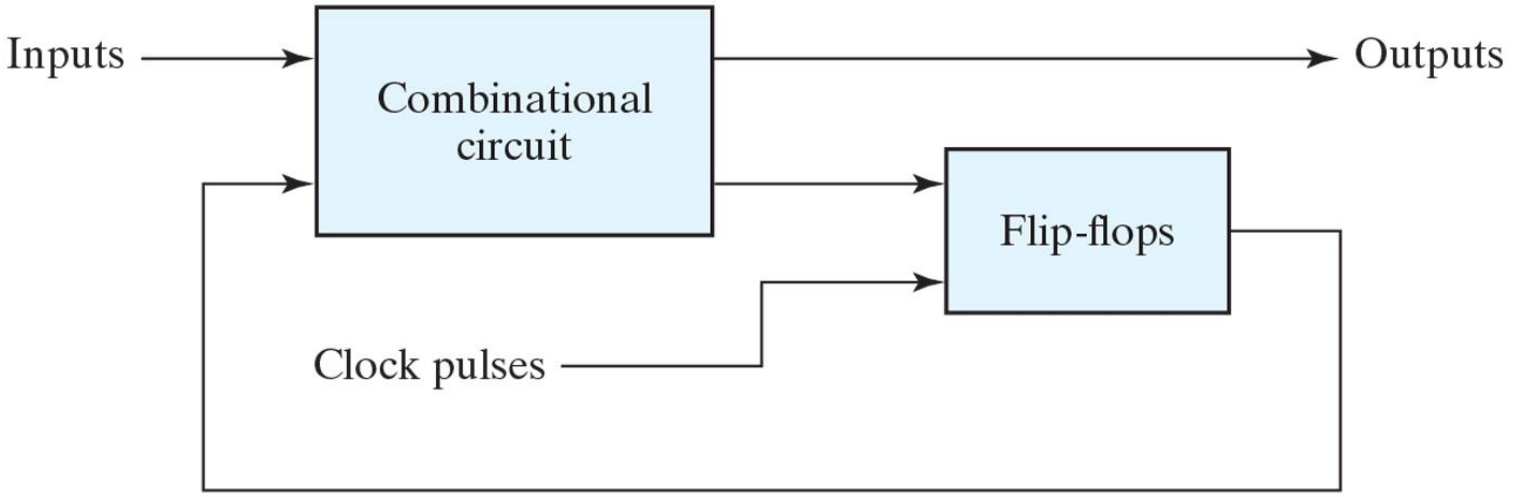
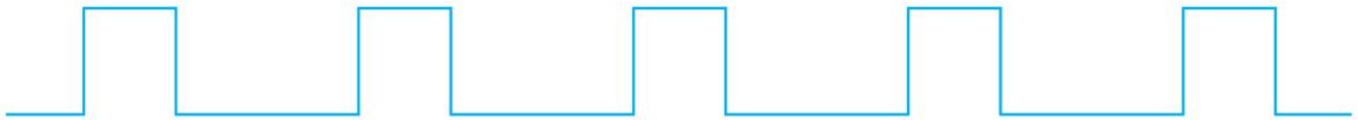
Figure 5.2
Synchronous clocked sequential circuit.



(a) Block diagram



(b) Timing diagram of clock pulses

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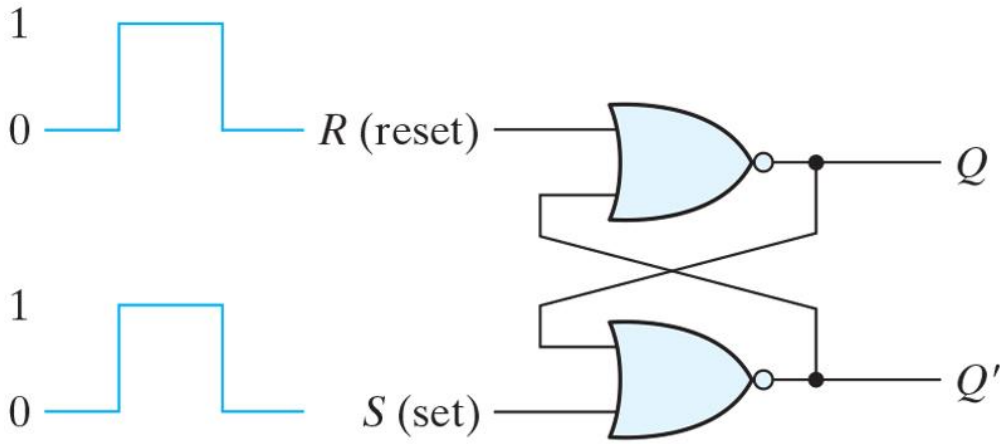
Figure 5.3
SR latch with NOR gates.



(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

(b) Function table

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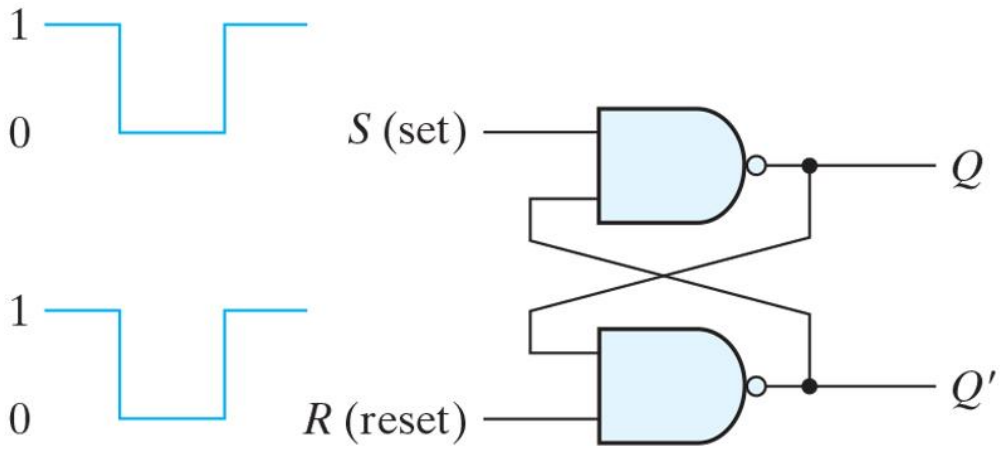
Figure 5.4
SR latch with NAND gates.



(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

(b) Function table

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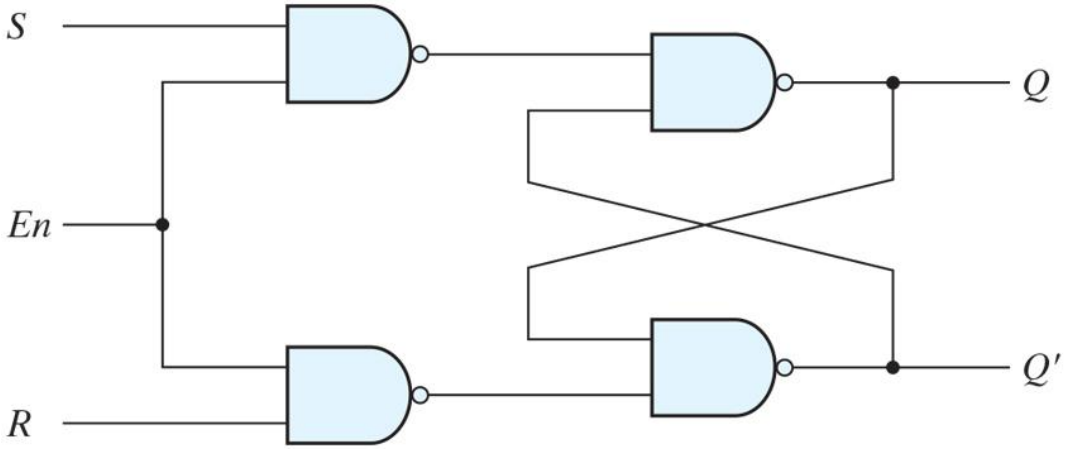
Figure 5.5
SR latch with control input.



(a) Logic diagram

En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

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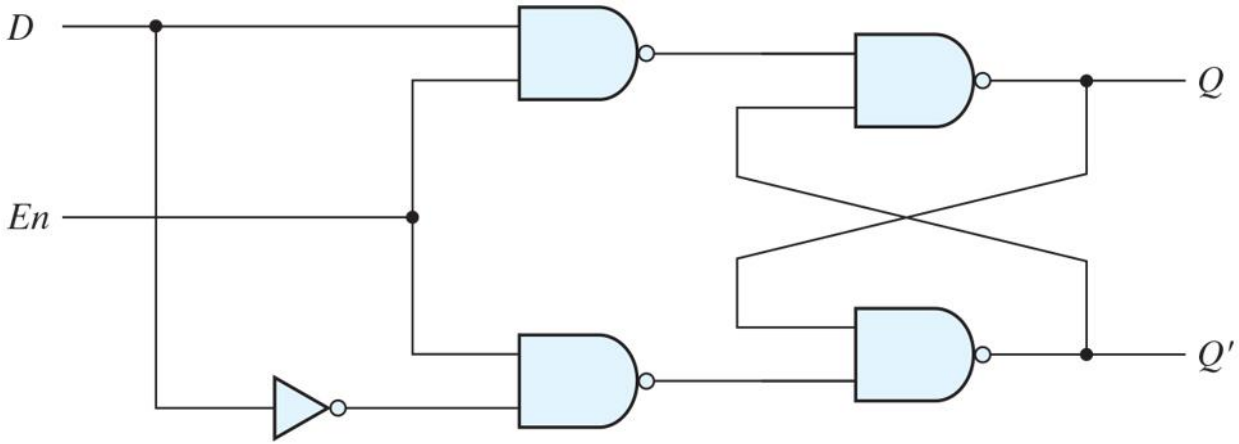
Figure 5.6
D latch.



(a) Logic diagram

En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

(b) Function table

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Figure 5.7
Graphic symbols for latches.

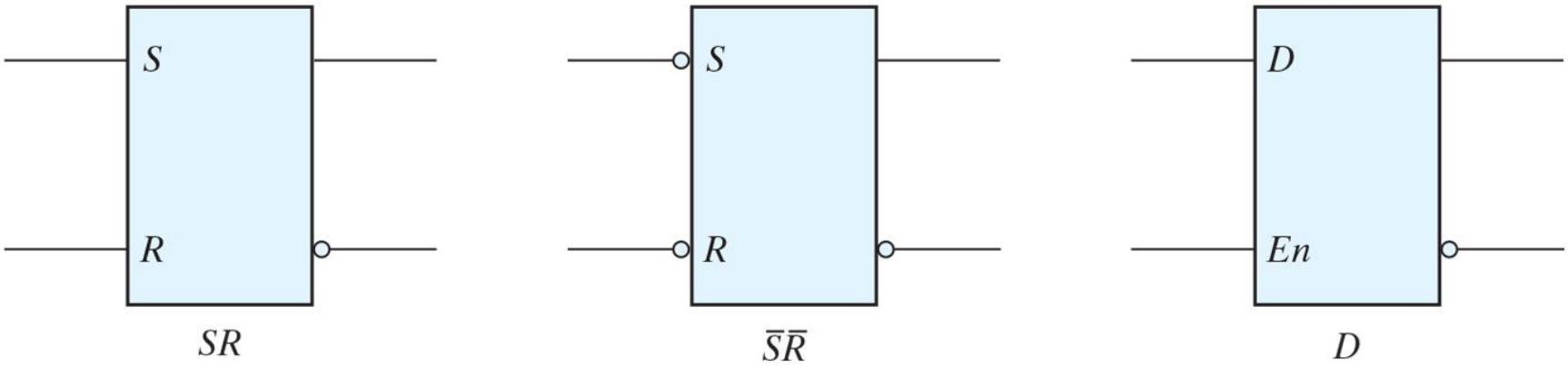

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Figure 5.8
Clock response in latch and flip-flop.

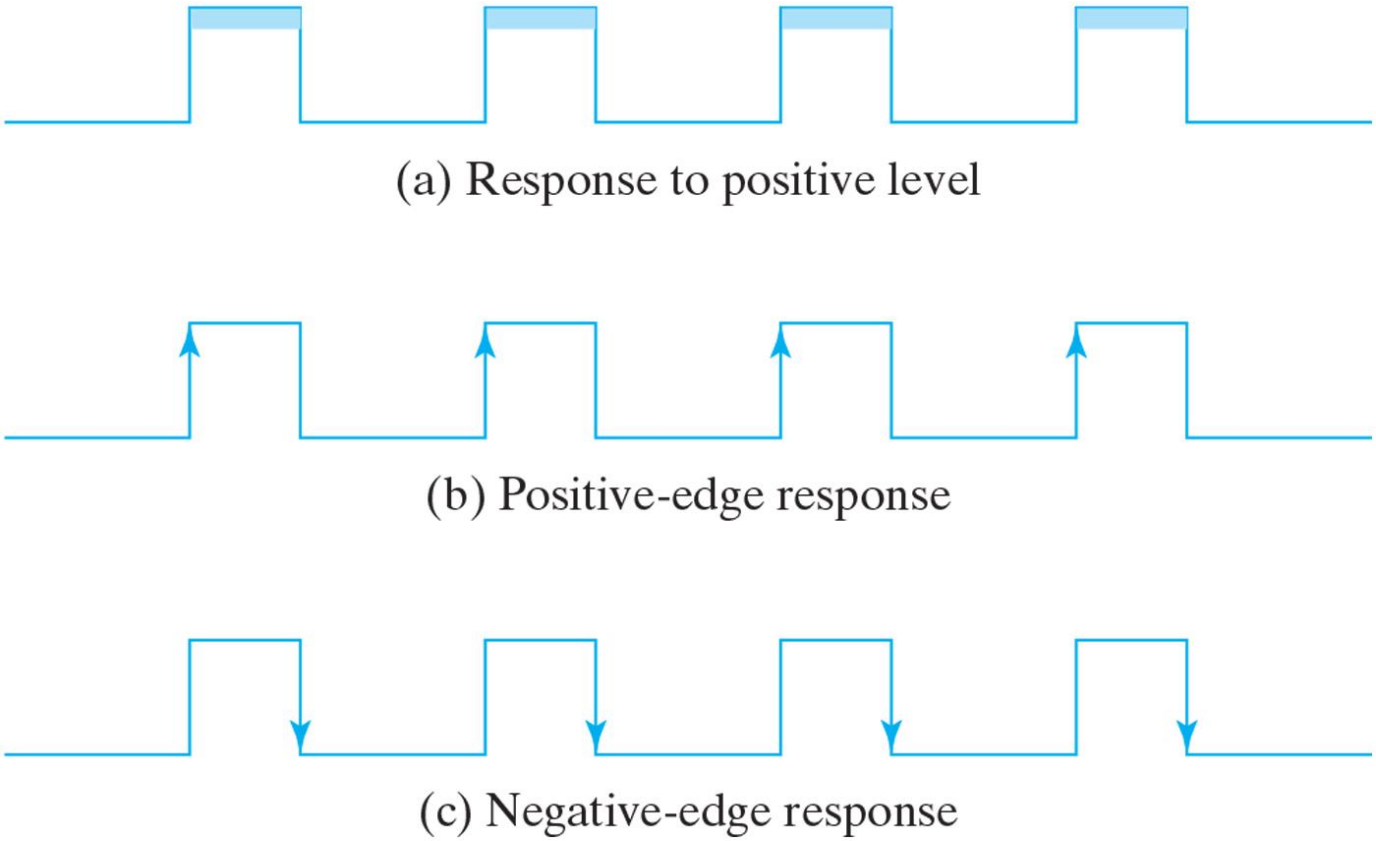

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Figure 5.9
Master–slave *D* flip-flop.

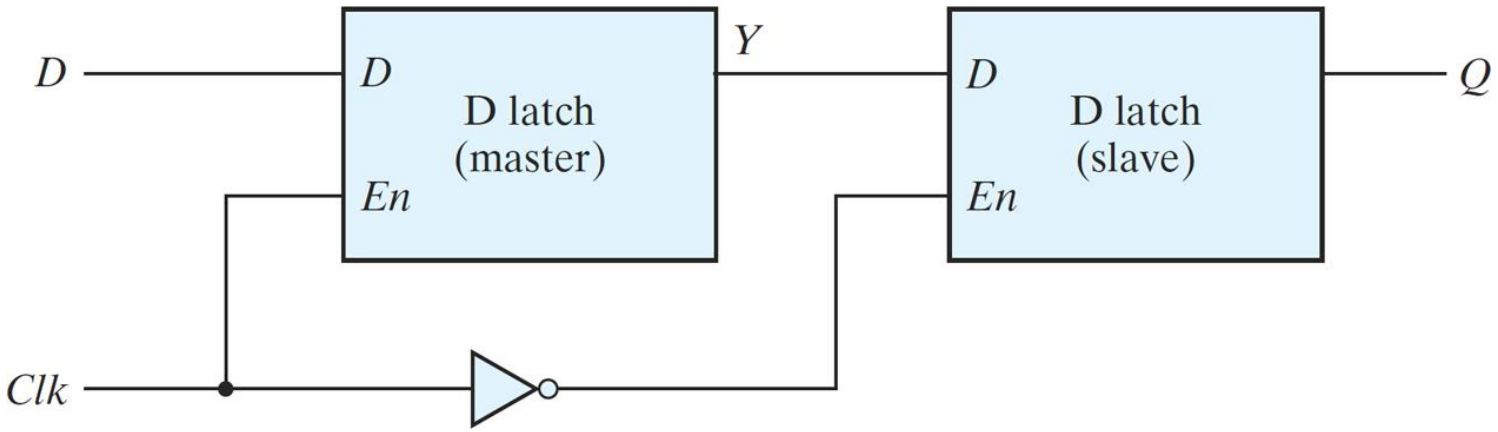

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Figure 5.10
D-type positive-edge-triggered flip-flop.

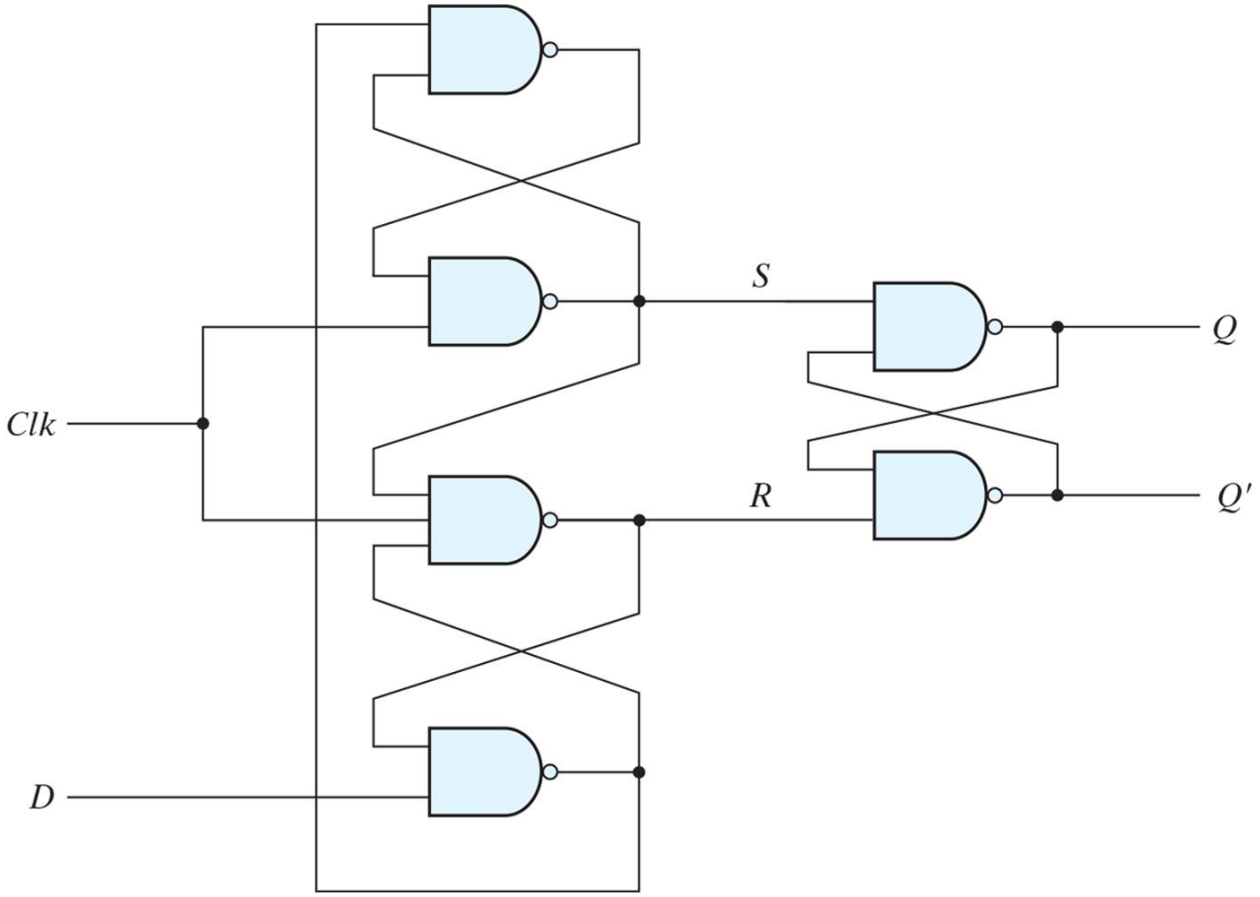

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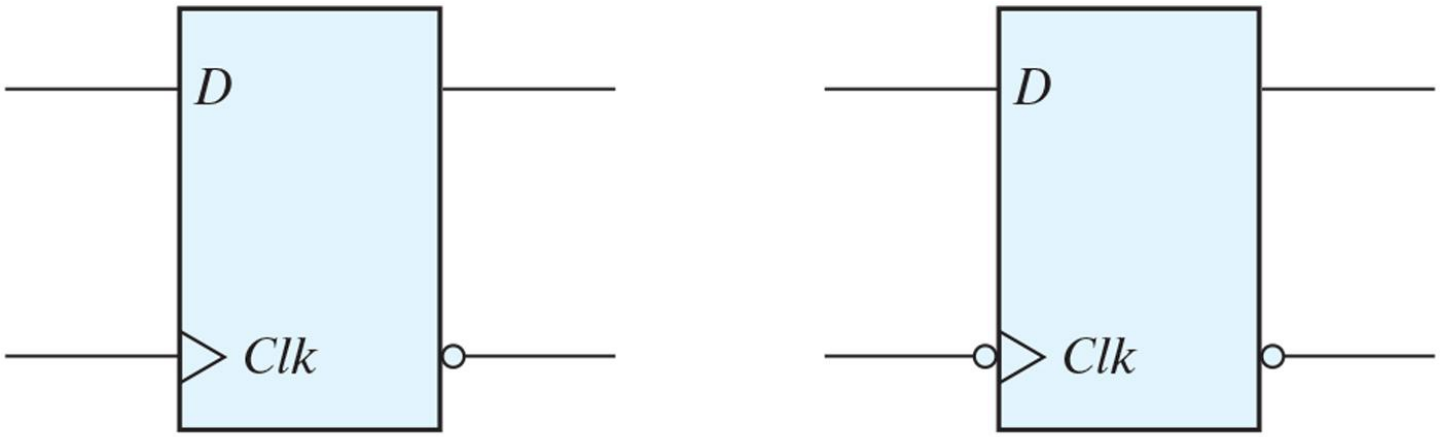
Figure 5.11
Graphic symbol for edge-triggered *D* flip-flop.



(a) Positive-edge (b) Negative-edge

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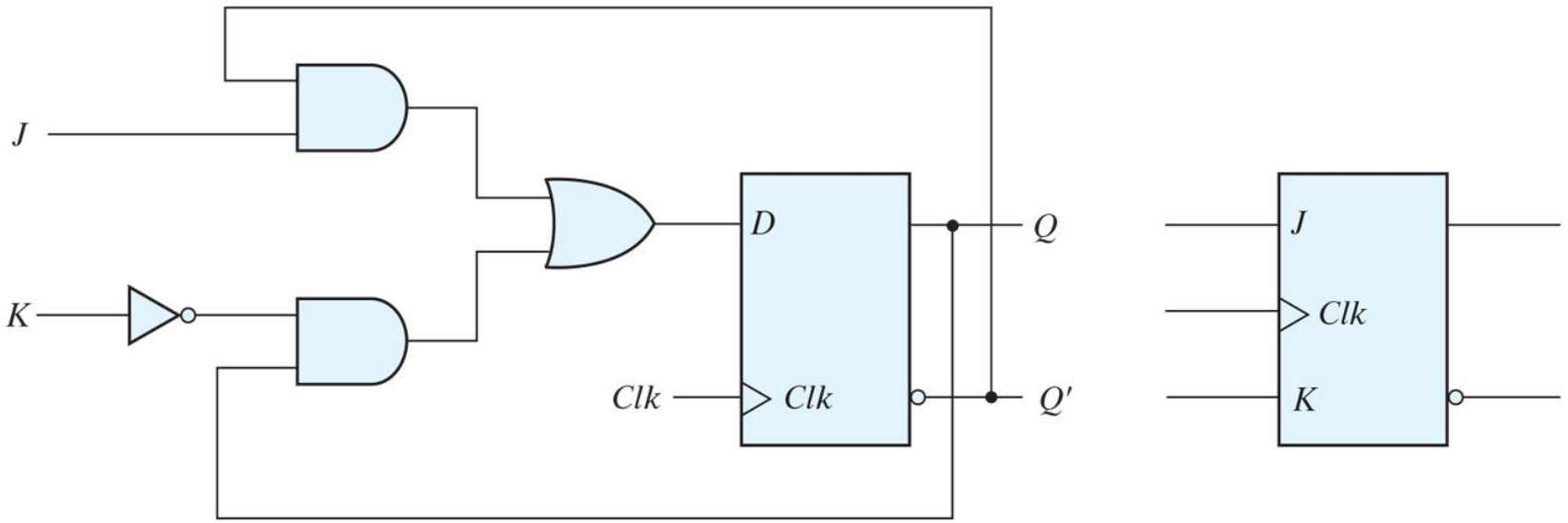
Figure 5.12
JK flip-flop.



(a) Circuit diagram

(b) Graphic symbol

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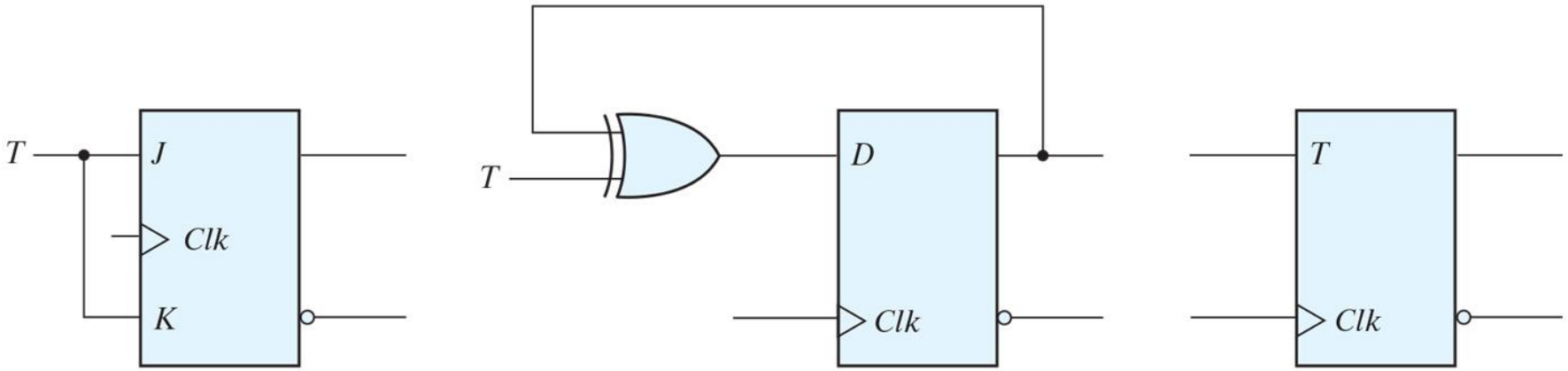
Figure 5.13
T flip-flop.



(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

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Table 5.1
Flip-Flop Characteristic Tables.

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

D Flip-Flop

D	Q(t + 1)	
0	0	Reset
1	1	Set

T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

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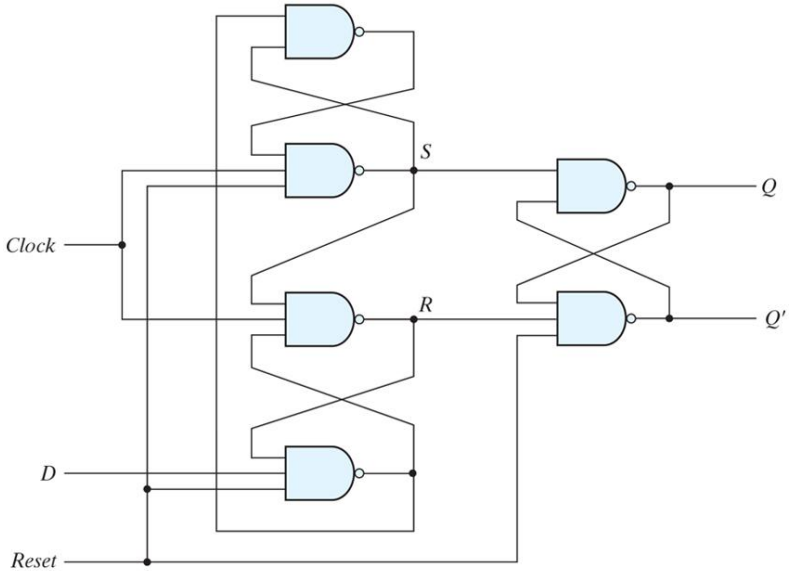
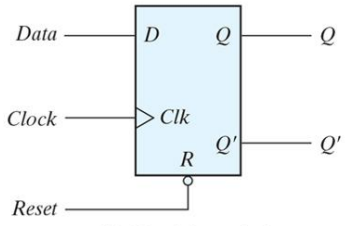
Figure 5.14
D flip-flop with asynchronous reset.



(a) Circuit diagram



(b) Graphic symbol

R	Clk	D	Q	Q′
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(c) Function table

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Figure 5.15
Example of sequential circuit.

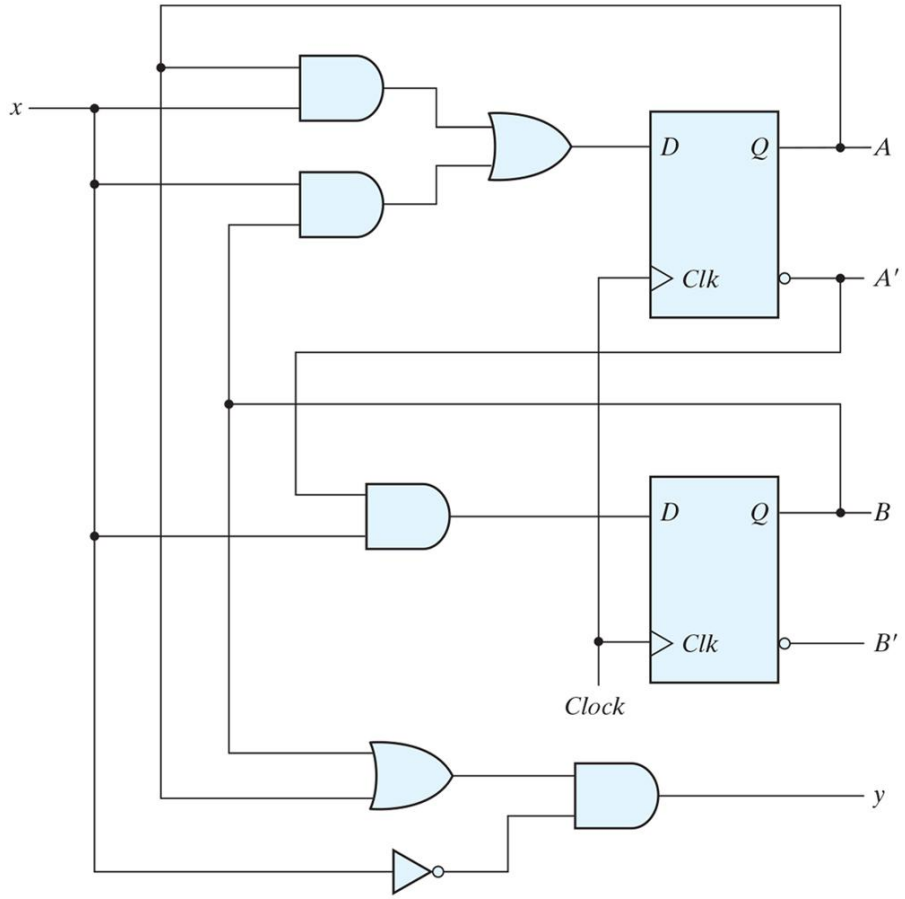

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Table 5.2
State Table for the Circuit of Fig. 5.15.

Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

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Table 5.3
Second Form of the State Table.

Present State		Next State				Output	
		$x = 0$		$x = 1$		$x = 0$	$x = 1$
A	B	A	B	A	B	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

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Figure 5.16
State diagram of the circuit of Fig. 5.15.

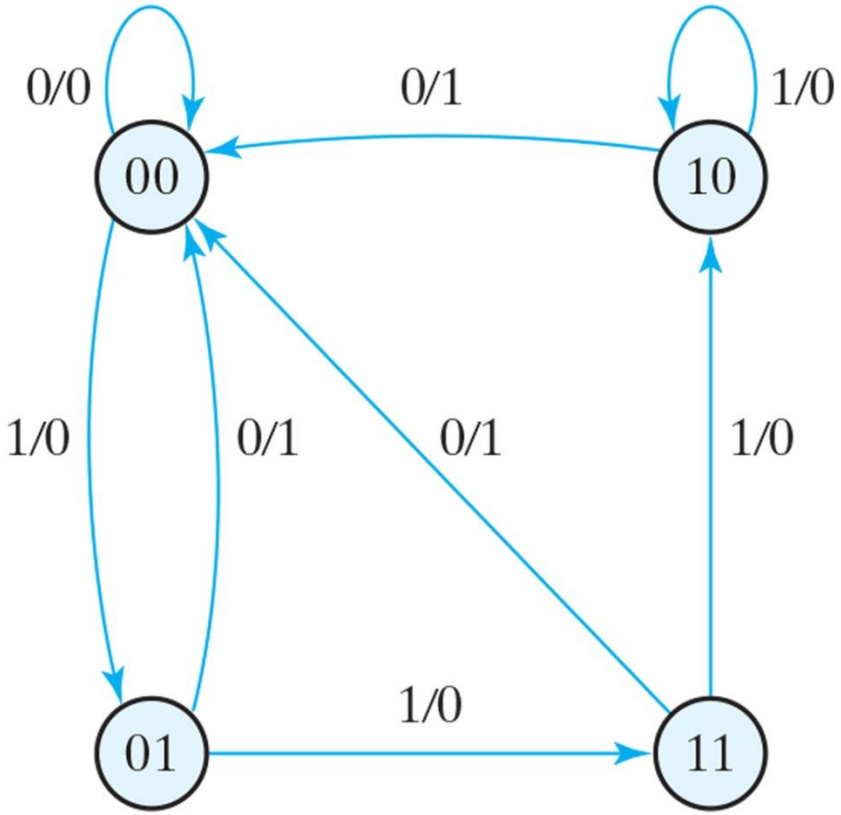

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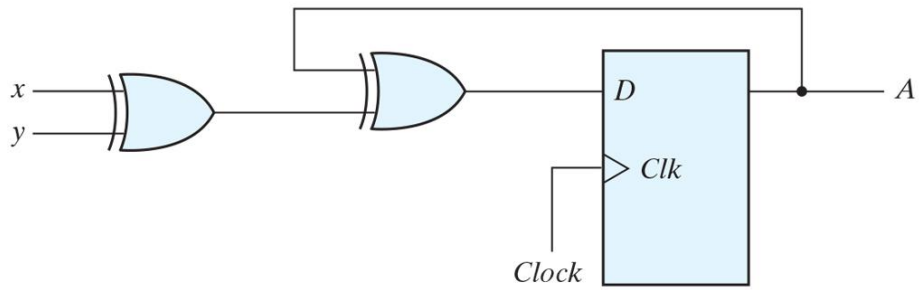
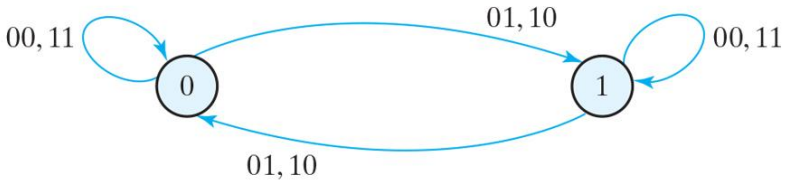
Figure 5.17
Sequential circuit with *D* flip-flop.



(a) Circuit diagram

Present state	Inputs		Next state
A	*x*	*y*	*A*
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b) State table



(c) State diagram

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Figure 5.18
Sequential circuit with *JK* flip-flop.

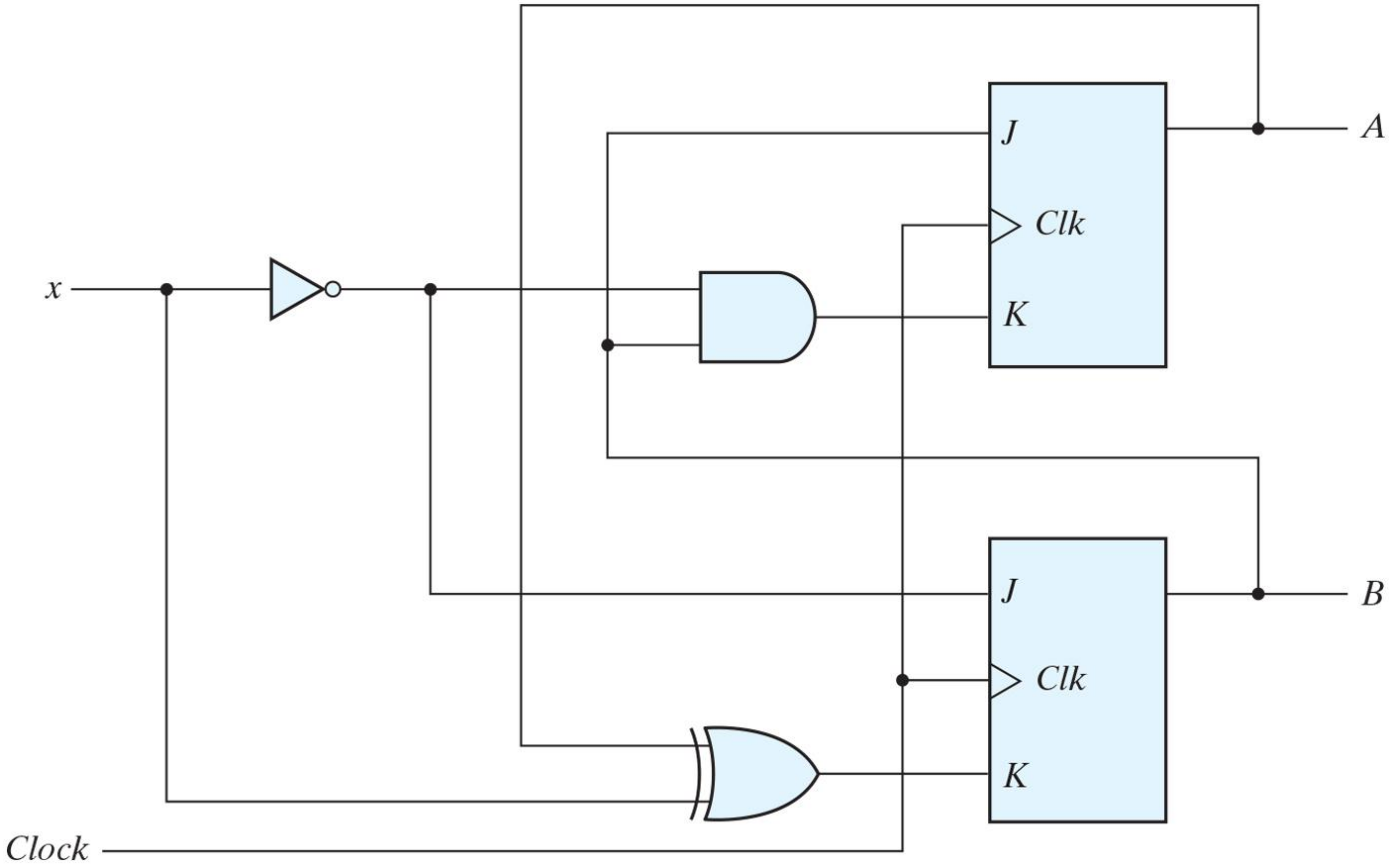

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Table 5.4
State Table for Sequential Circuit with JK Flip-Flops.

Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

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Figure 5.19
State diagram of the circuit of Fig. 5.18.

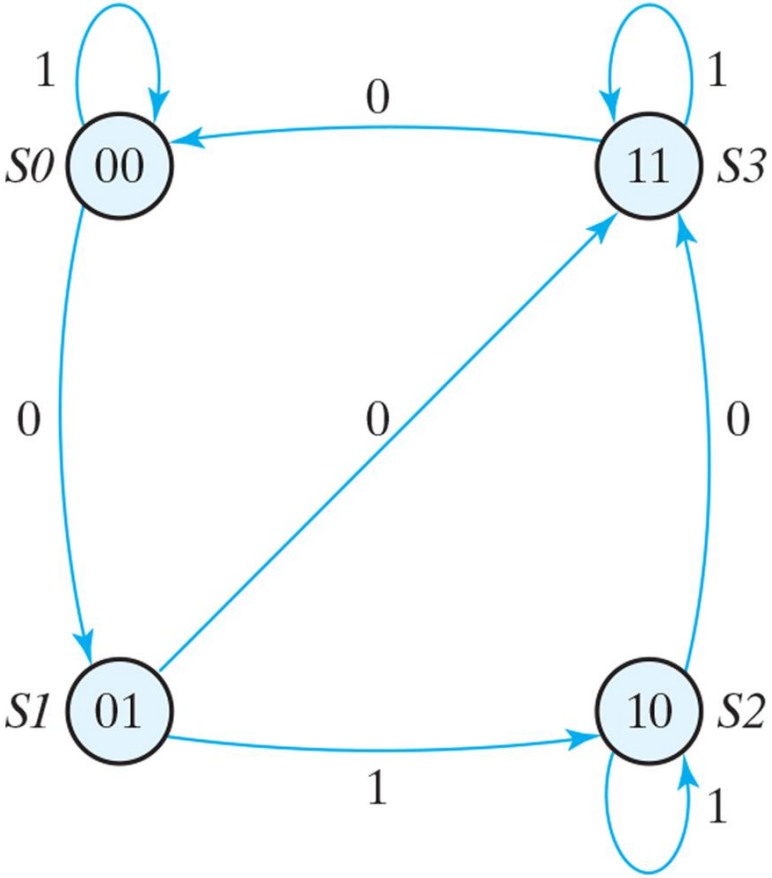

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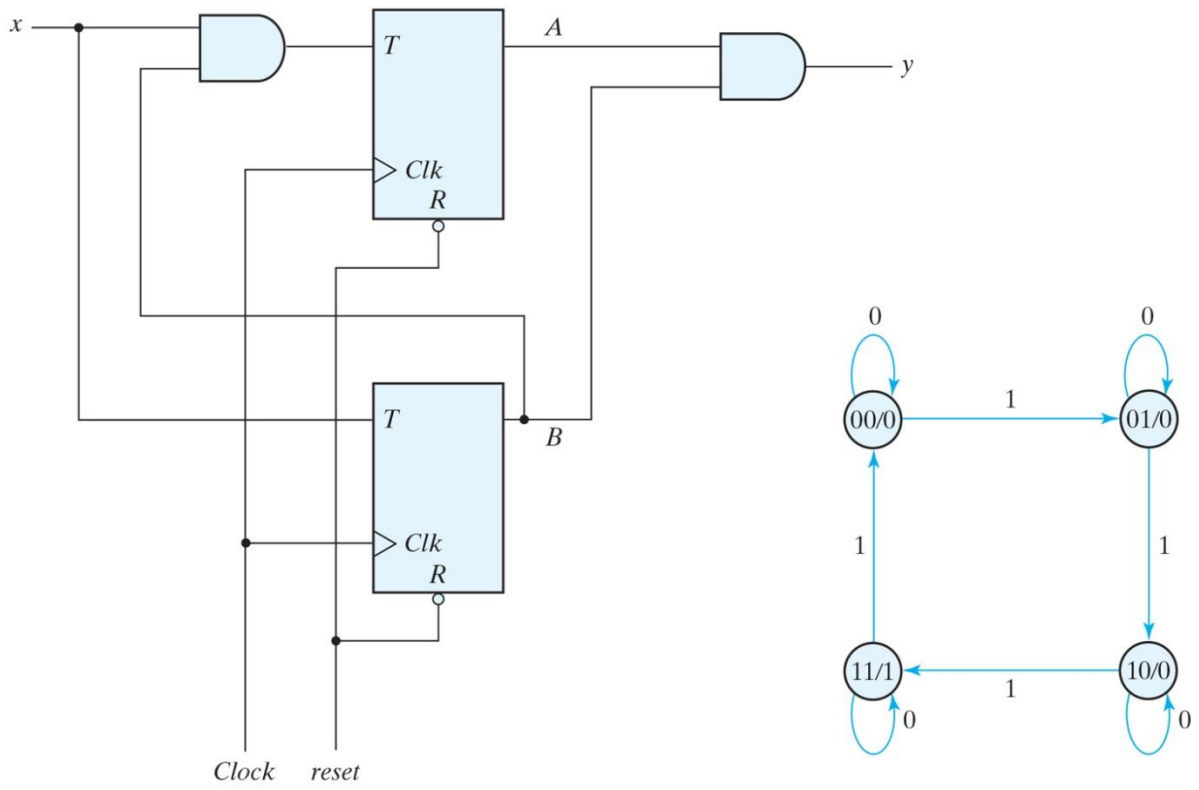
Figure 5.20
Sequential circuit with T flip-flops (Binary Counter).



(a) Circuit diagram

(b) State diagram

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Table 5.5
State Table for Sequential Circuit with T Flip-Flops.

Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

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Figure 5.21
Block diagrams of Mealy and Moore state machines.

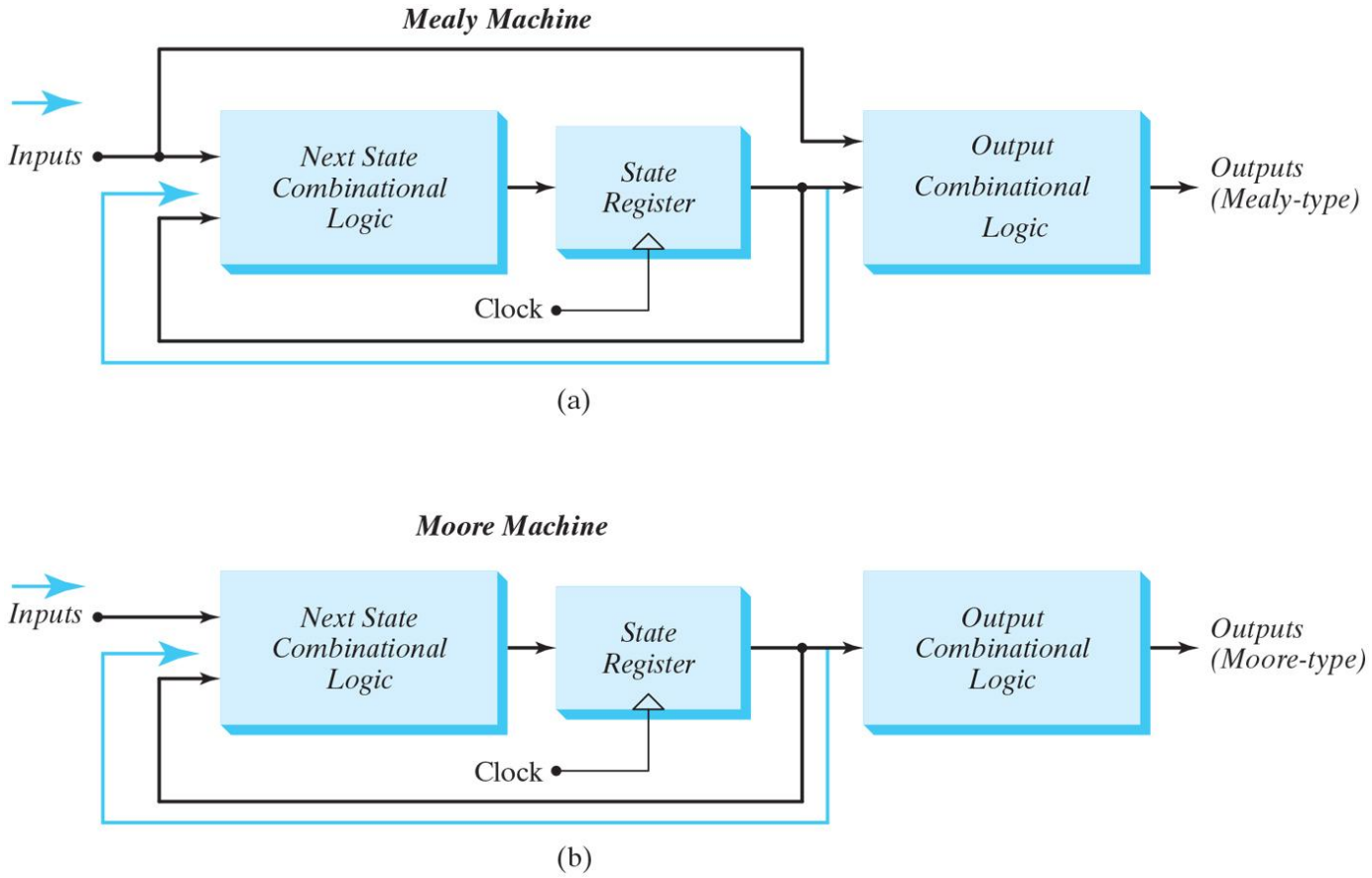

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Figure 5.22
Simulation output of *Mealy_Zero_Detector*.

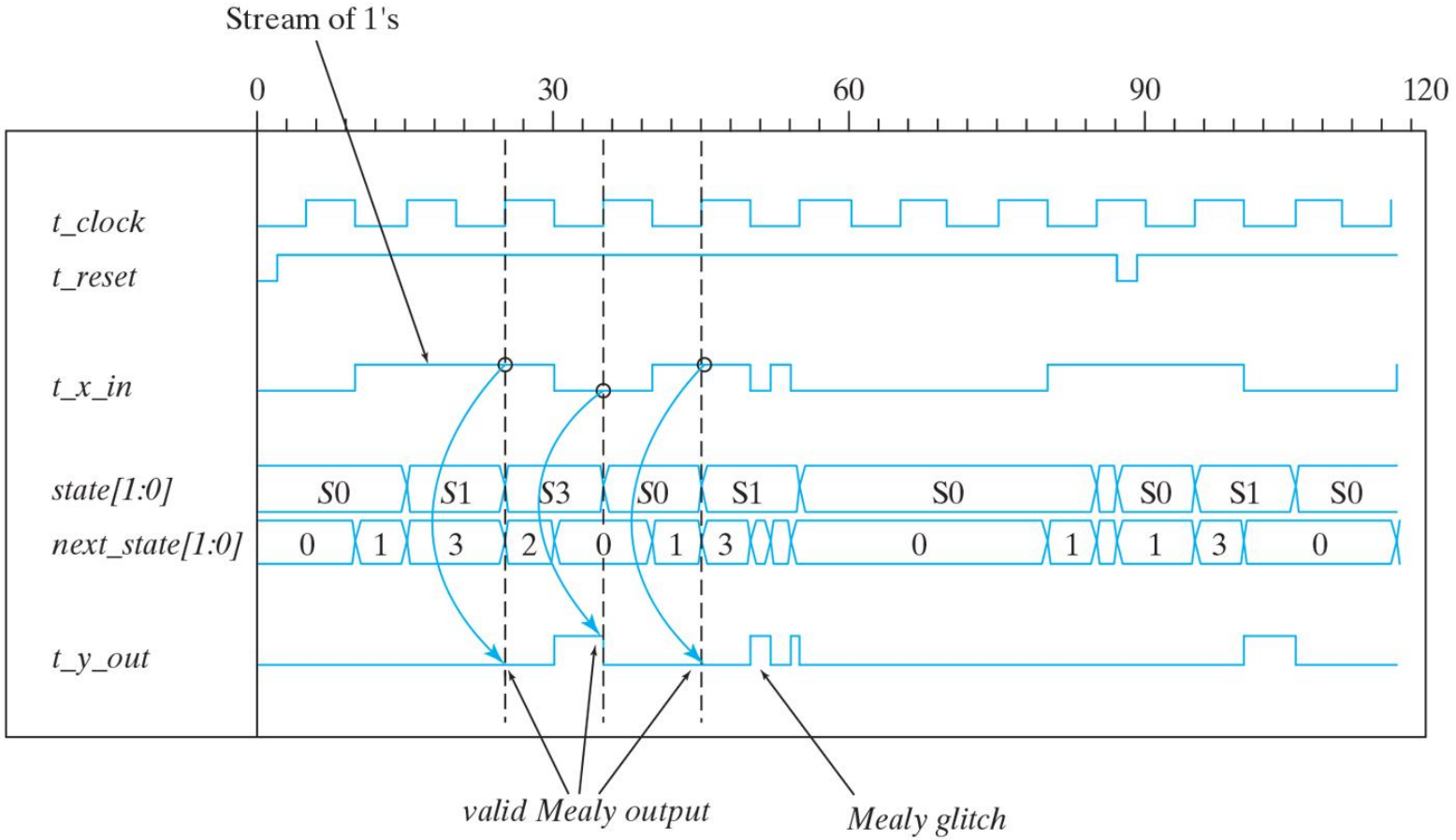

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Figure 5.23
Simulation output of HDL Example 5.6.

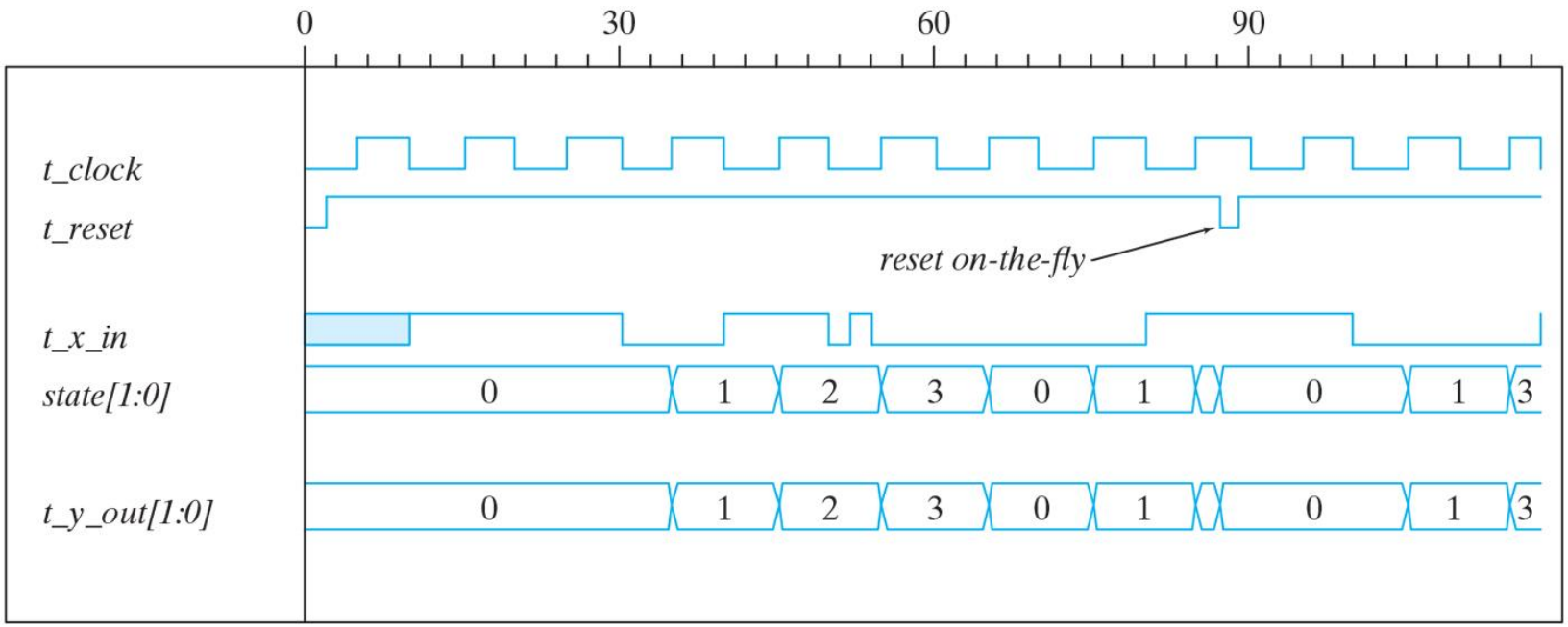

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Figure 5.24
Simulation output of HDL Example 5.7.

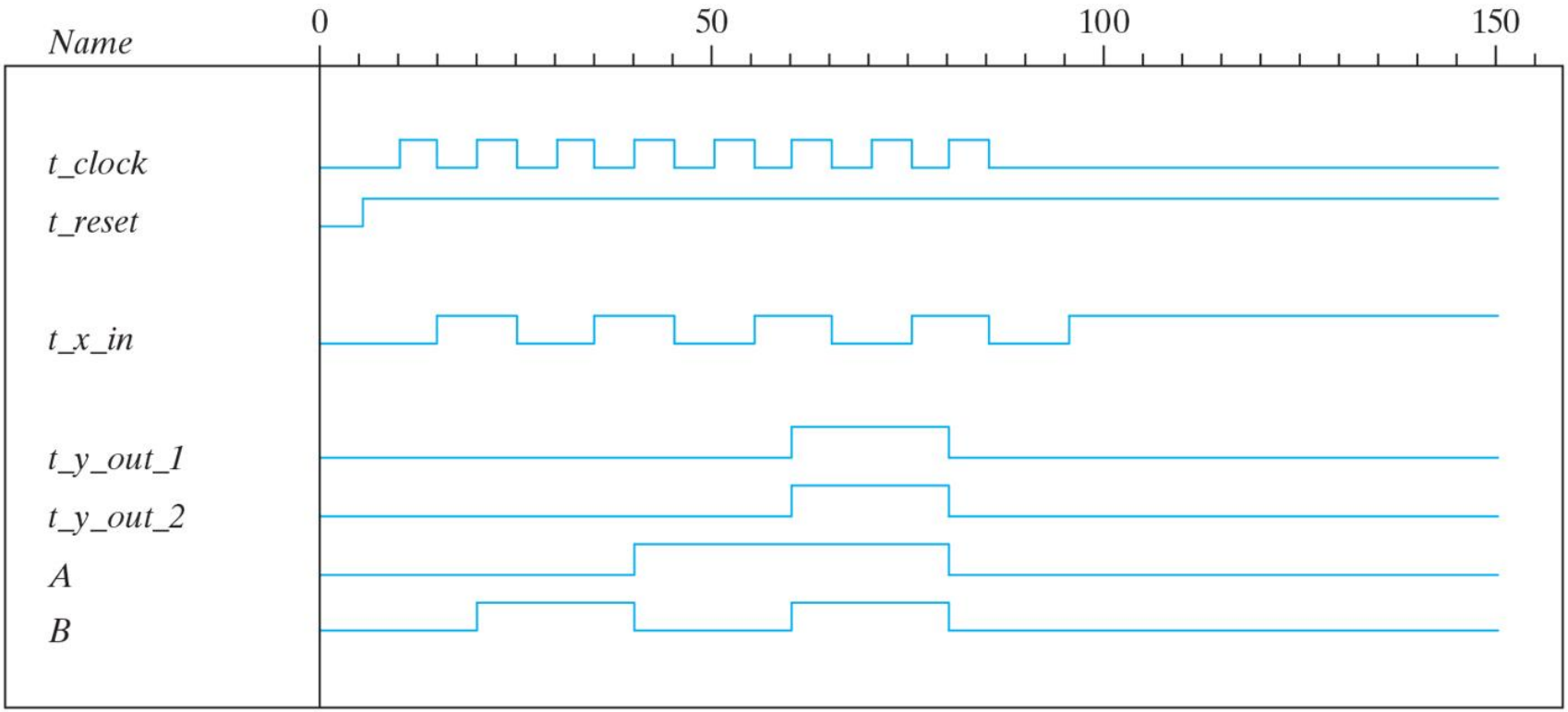

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Figure 5.25
State diagram.

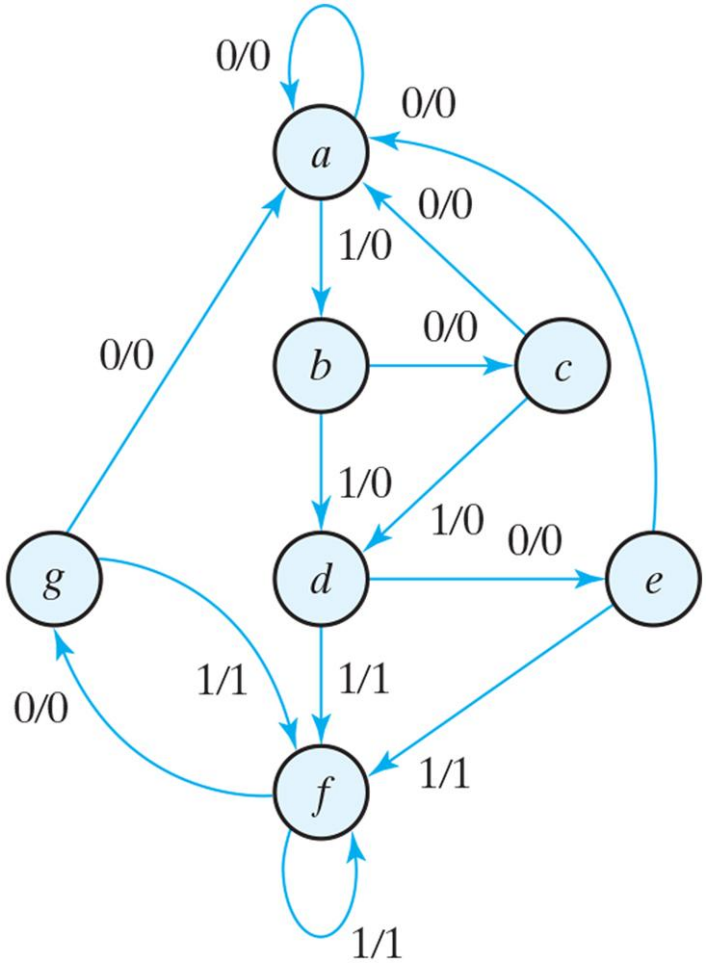

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Table 5.6
State Table.

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

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Table 5.7
Reducing the State Table.

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

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Figure 5.26
Reduced State diagram.

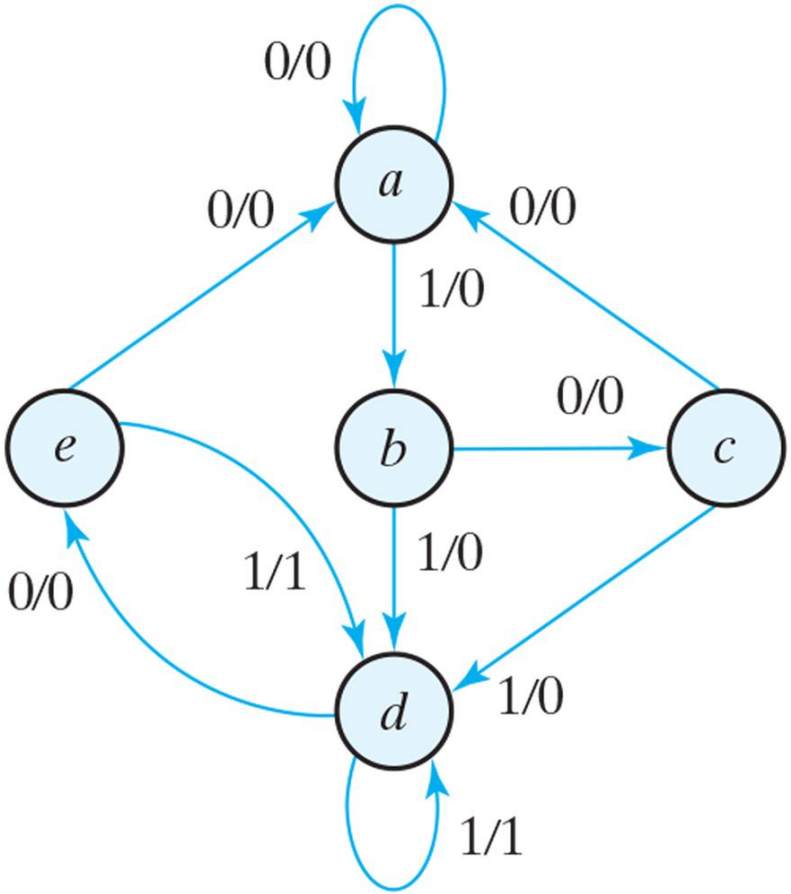

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Table 5.8
Reduced the State Table.

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

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Table 5.9
Three Possible Binary State Assignments.

State	Assignment 1, Binary	Assignment 2, Gray Code	Assignment 3, One-Hot
a	000	000	00001
b	001	001	00010
c	010	011	00100
d	011	010	01000
e	100	110	10000

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Table 5.10
Reduced State Table with Binary Assignment 1.

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
000	000	001	0	0
001	010	011	0	0
010	000	011	0	0
011	100	011	0	1
100	000	011	0	1

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Figure 5.27
State diagram for sequence detector.

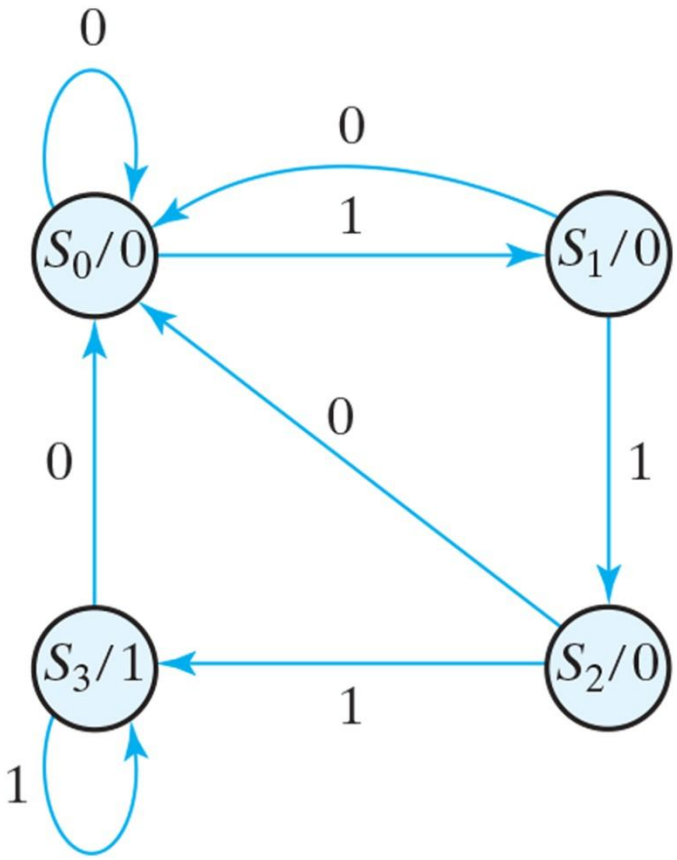

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Table 5.11
State Table for Sequence Detector.

Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

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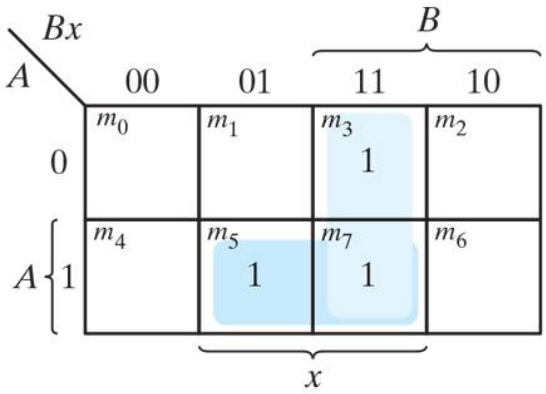
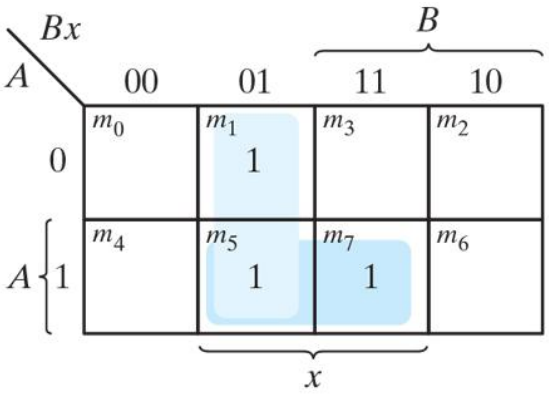
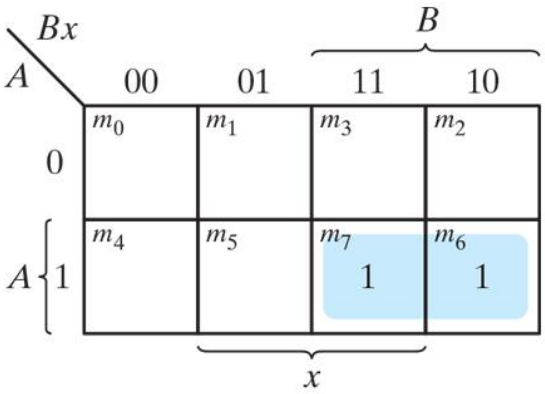
Figure 5.28
K-Maps for sequence detector.



$D_A = Ax + Bx$



$D_B = Ax + B'x$



$y = AB$

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Figure 5.29
Logic diagram of a Moore-type sequence detector.

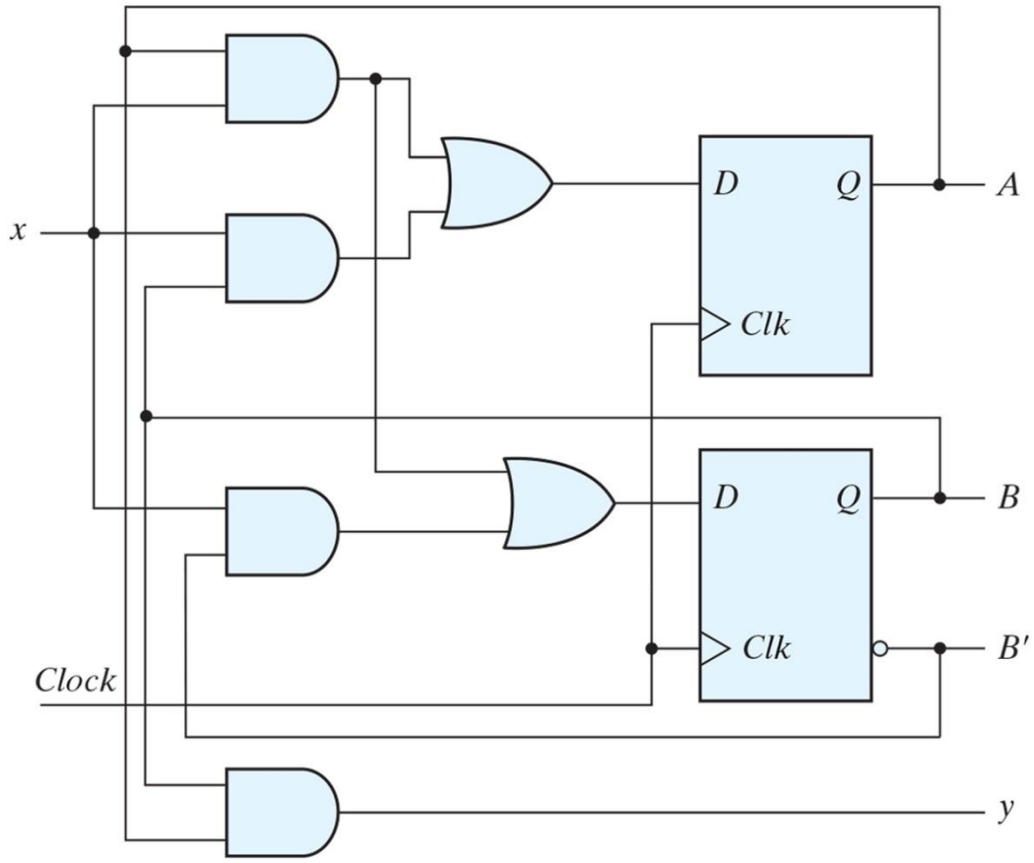

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Table 5.12
Flip-Flop Excitation Tables.

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(a) *JK* Flip-Flop

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

(b) *T* Flip-Flop

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Table 5.13
State Table and JK Flip-Flop Inputs.

Present State		Input	Next State		Flip-Flop Inputs			
A	*B*	*x*	*A*	*B*	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

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Figure 5.30
Maps for *J* and *K* input equations.

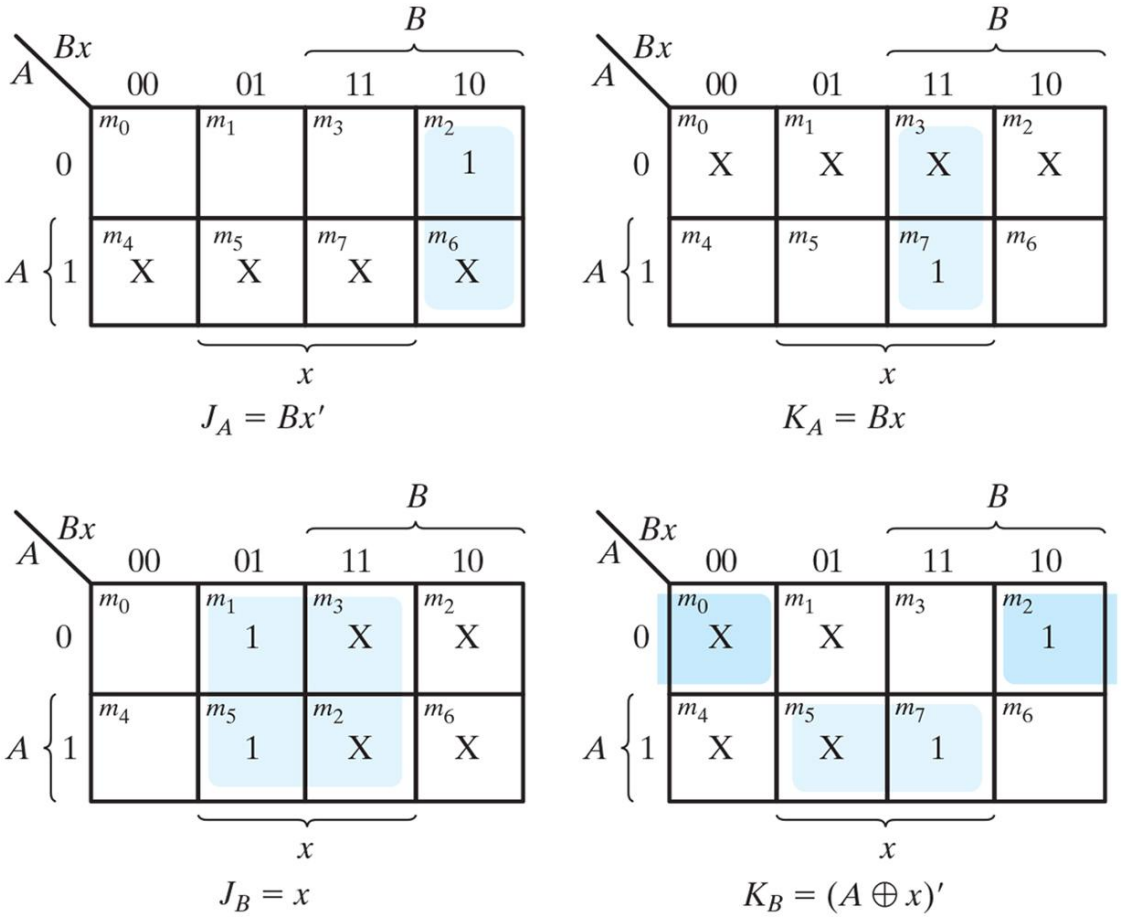

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Figure 5.31
Logic diagram for sequential circuit with *JK* flip-flops.

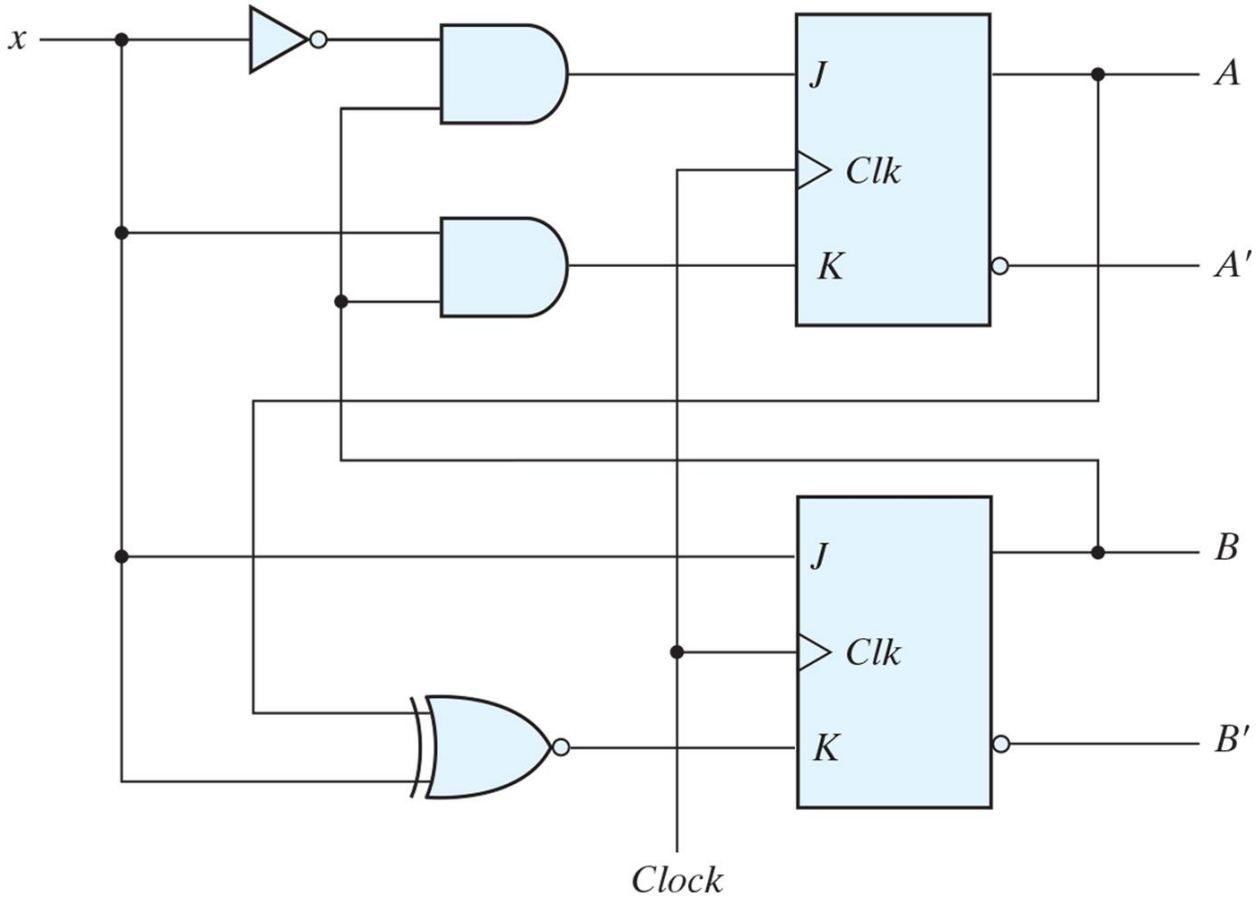

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Figure 5.32
State diagram of three-bit binary counter.

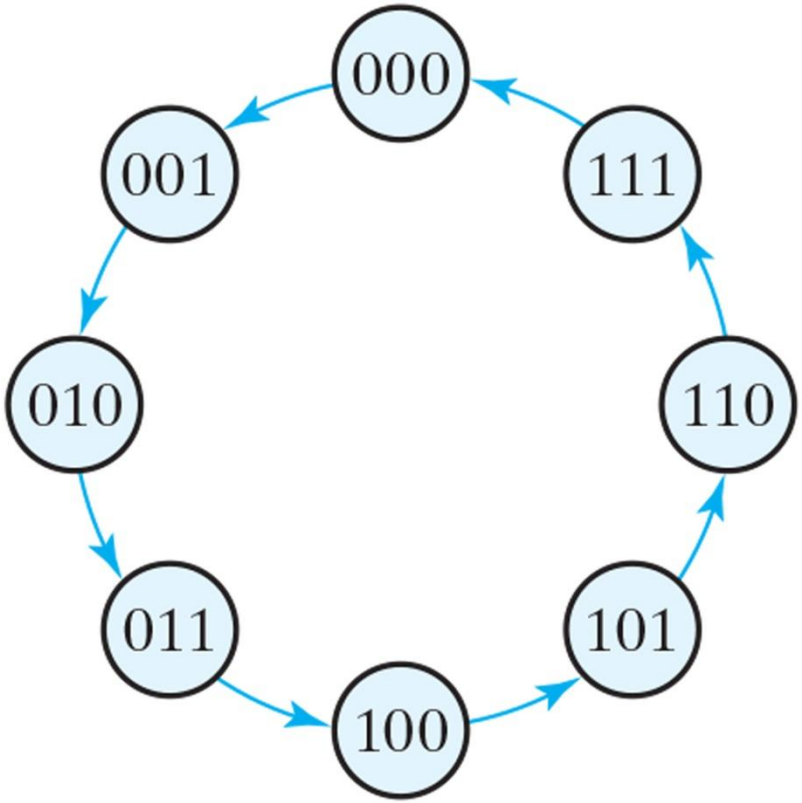

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Table 5.14
State Table for Three-Bit Counter.

Present State			Next State			Flip-Flop Inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

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Figure 5.33
Maps for three-bit binary counter.

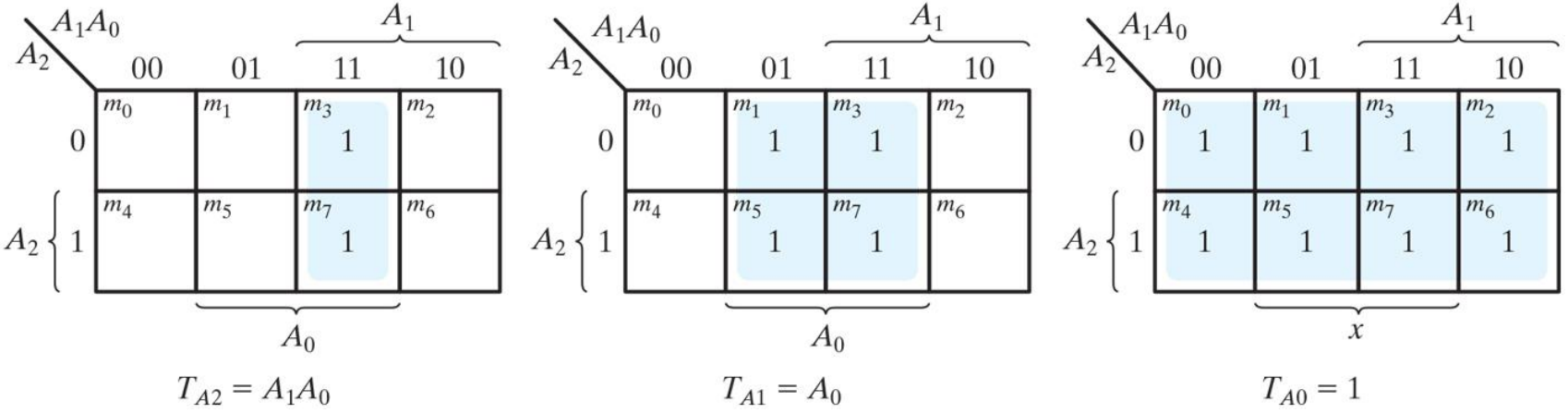

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Figure 5.34
Logic diagram of three-bit binary counter.

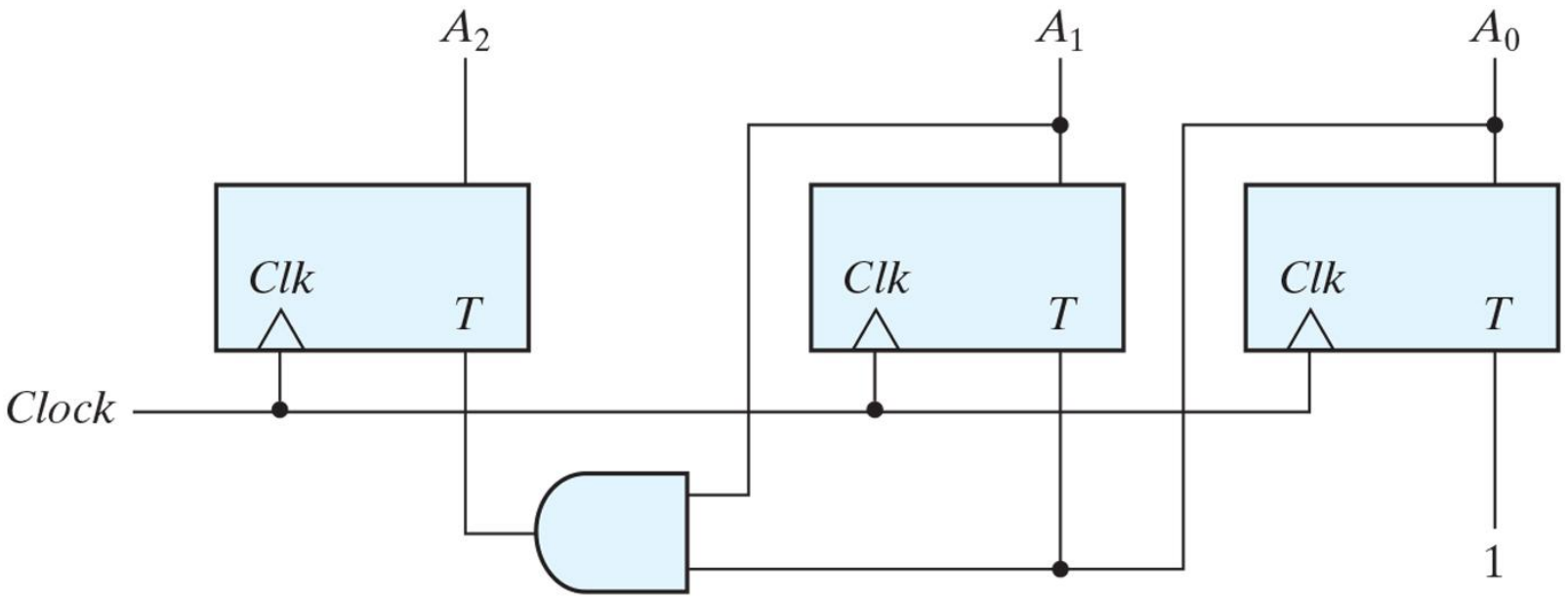

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Figure P5.7

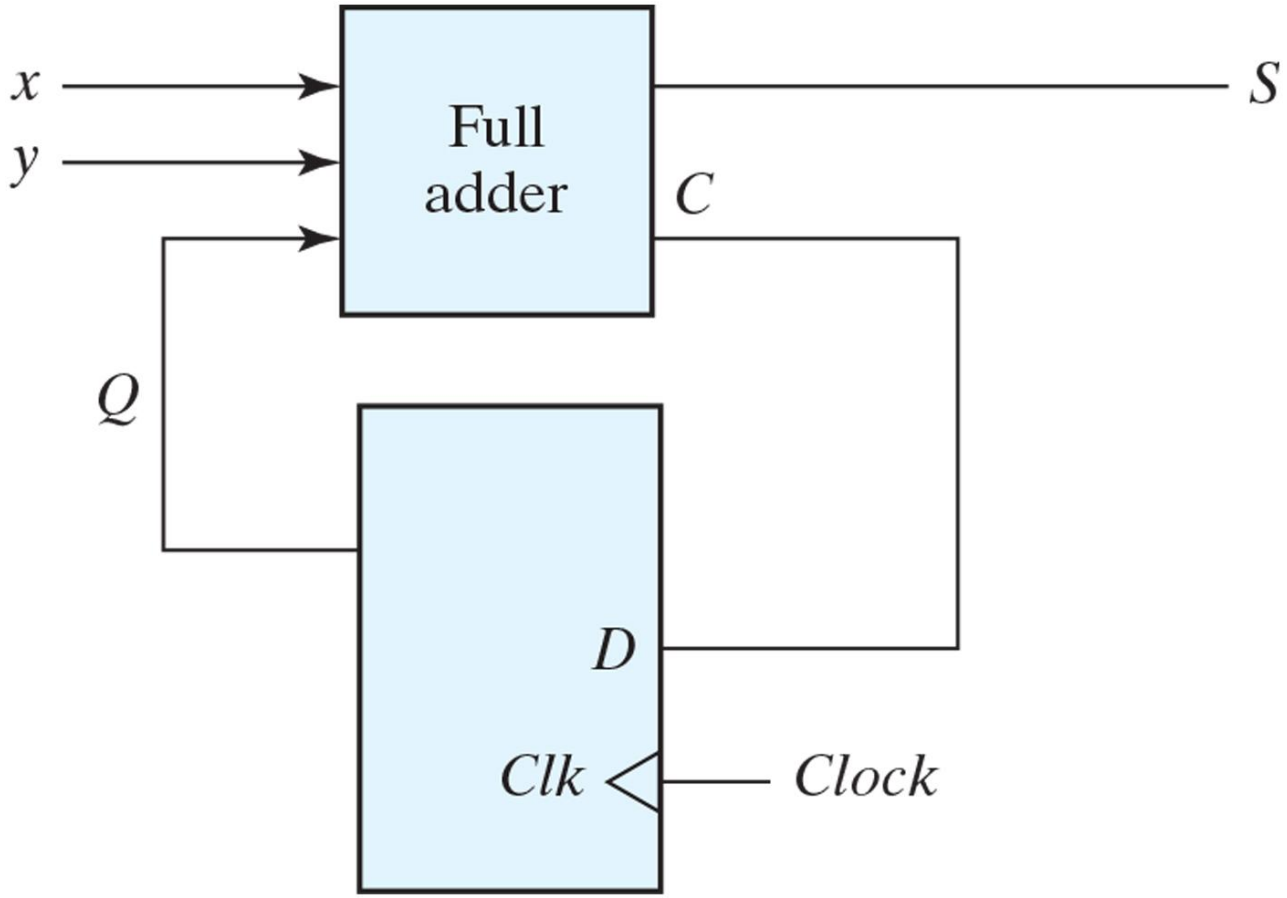

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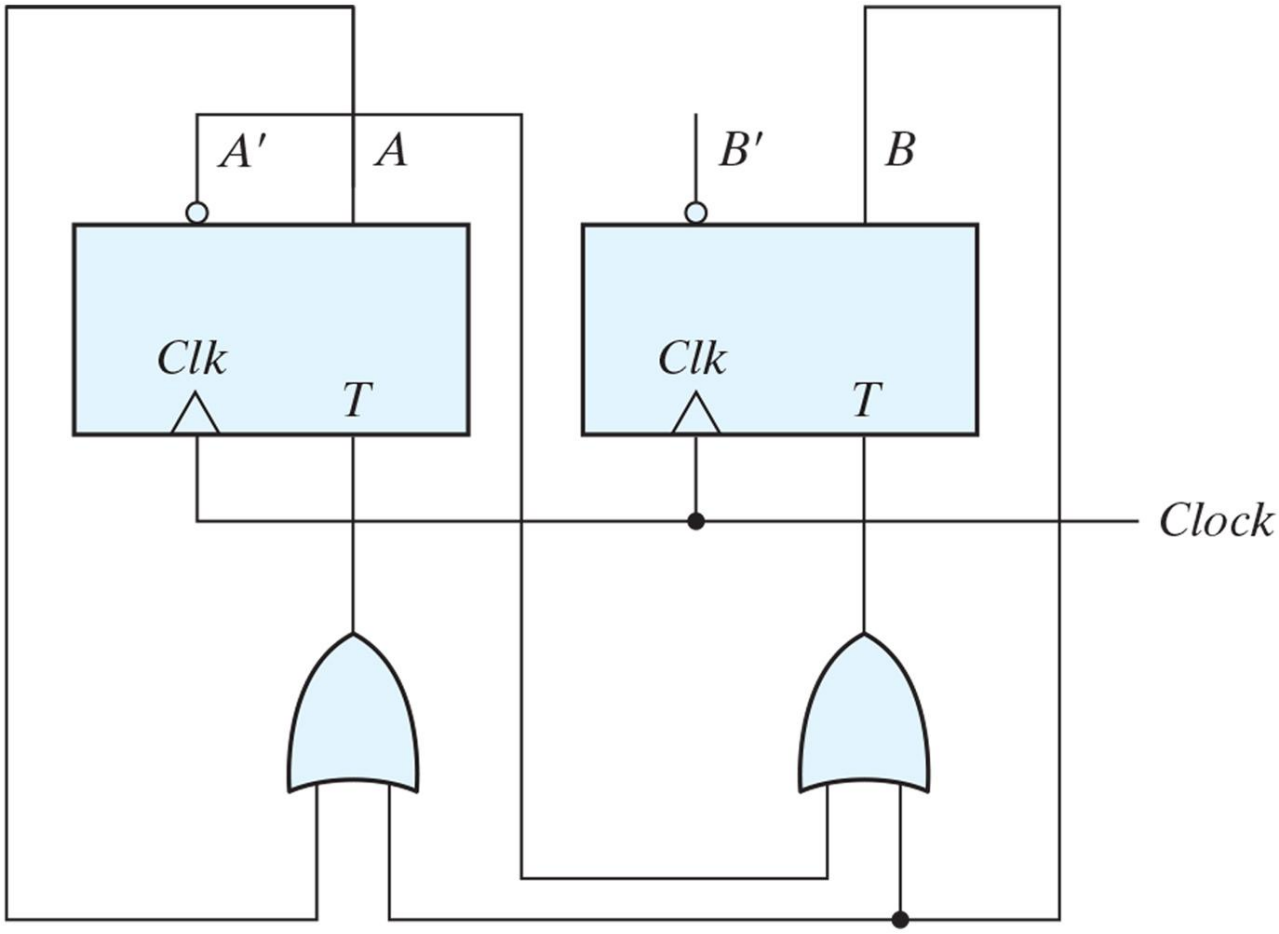
Figure P5.8



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Problem 5.12

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

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Figure P5.19

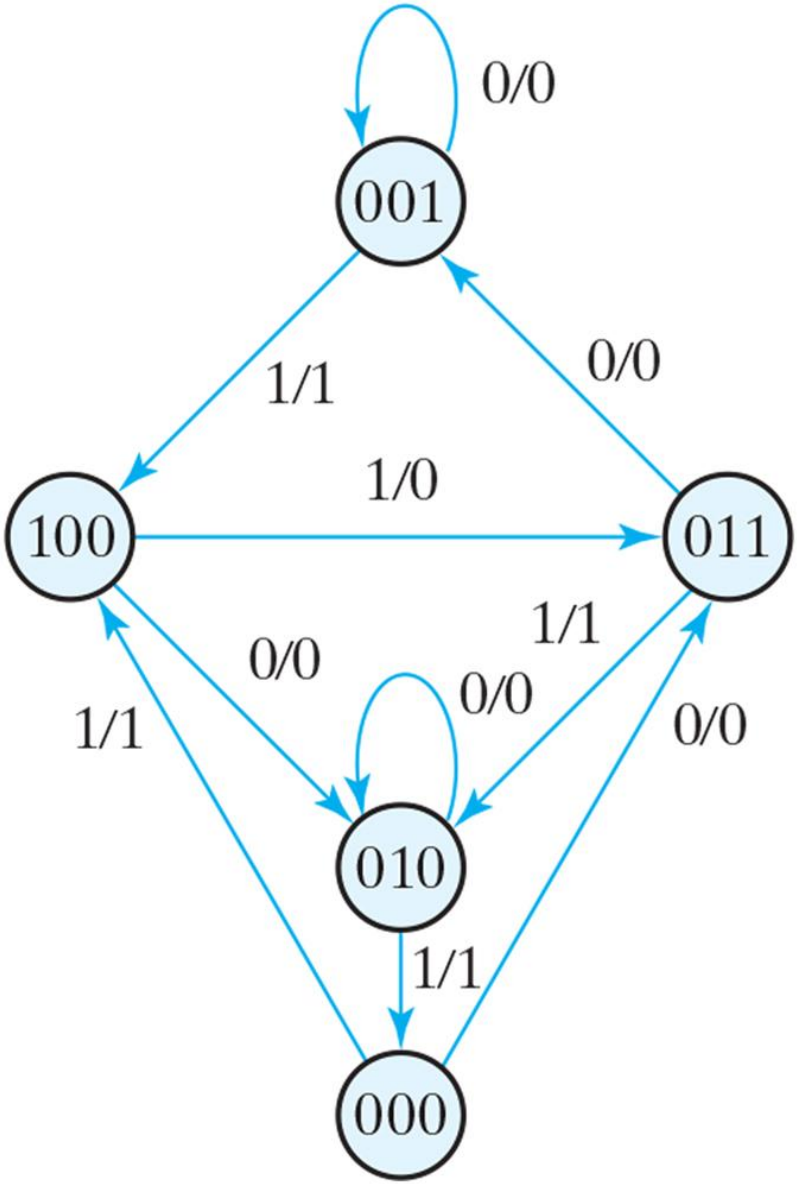

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Figure P5.32
Waveforms for Problem 5.32.

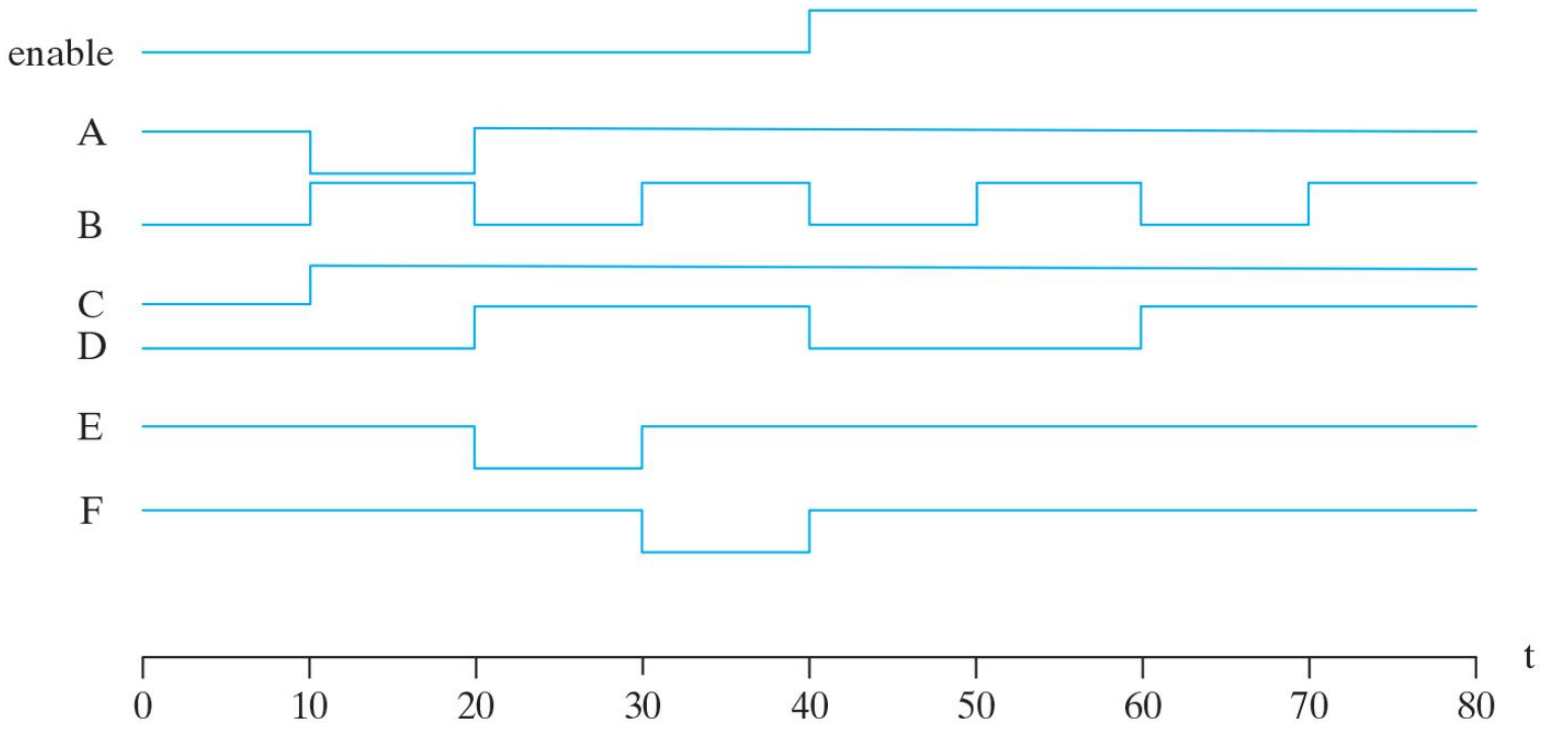

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Figure P5.48

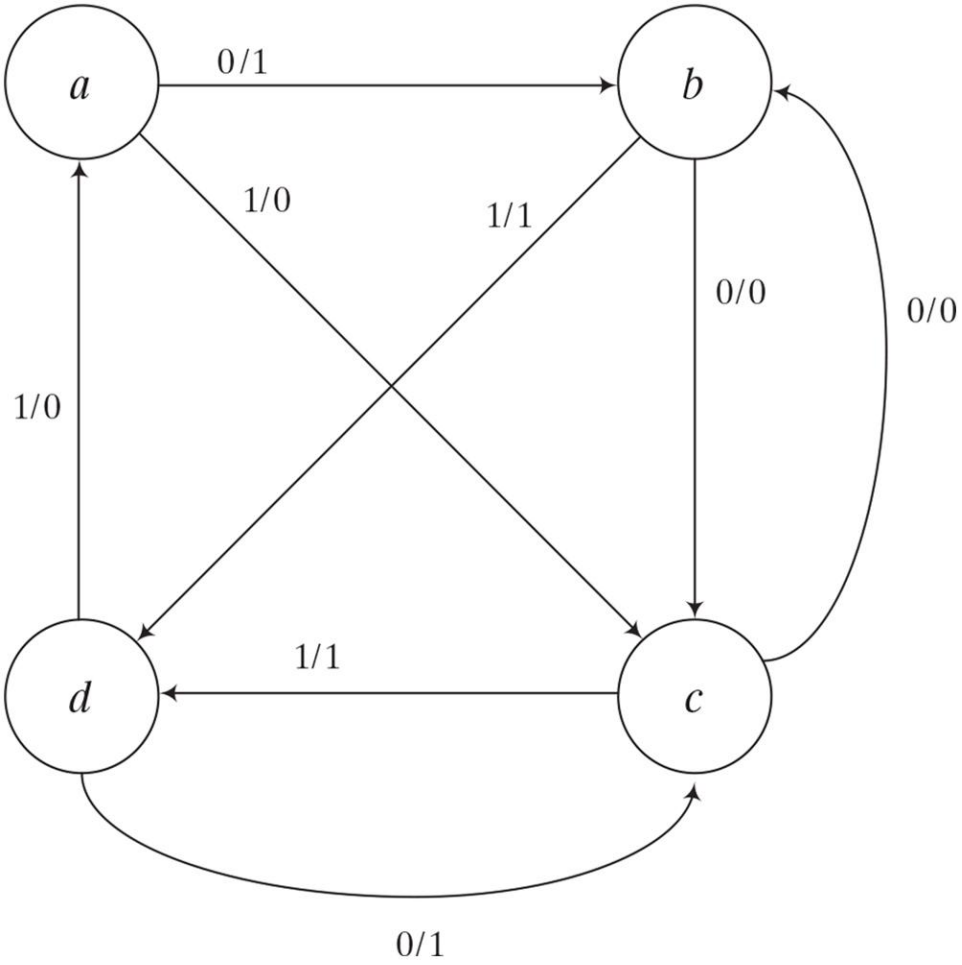

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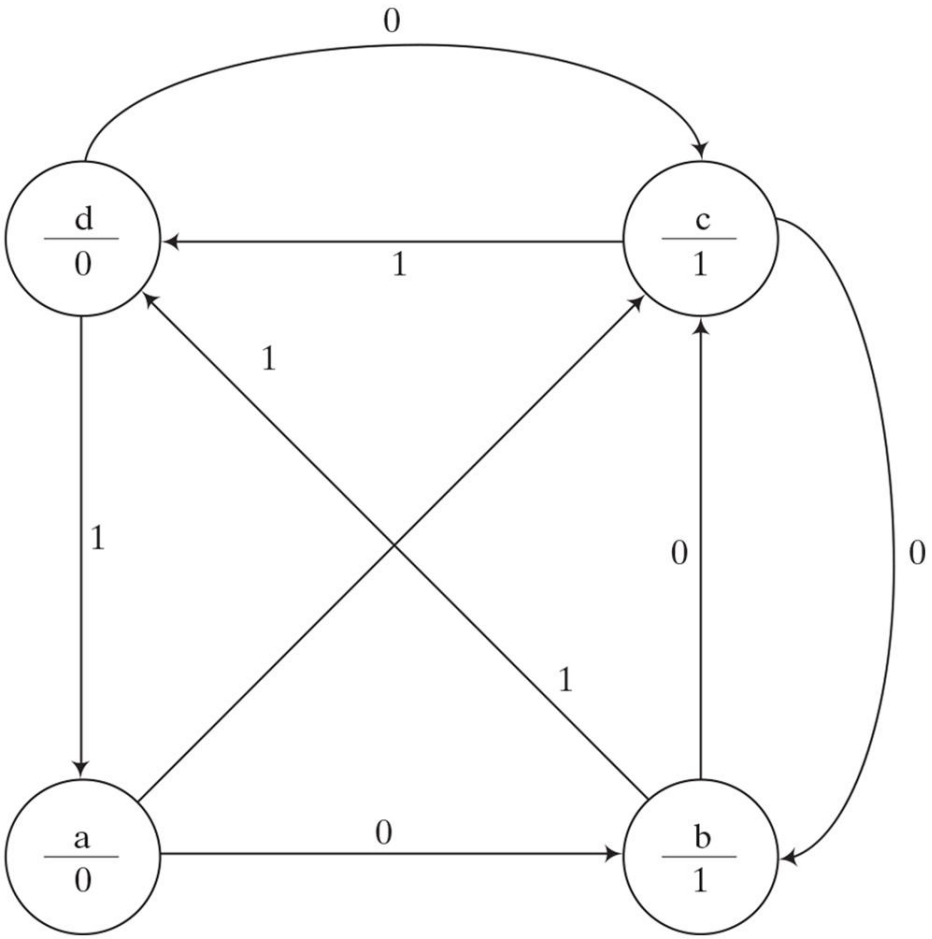
Figure P5.49



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