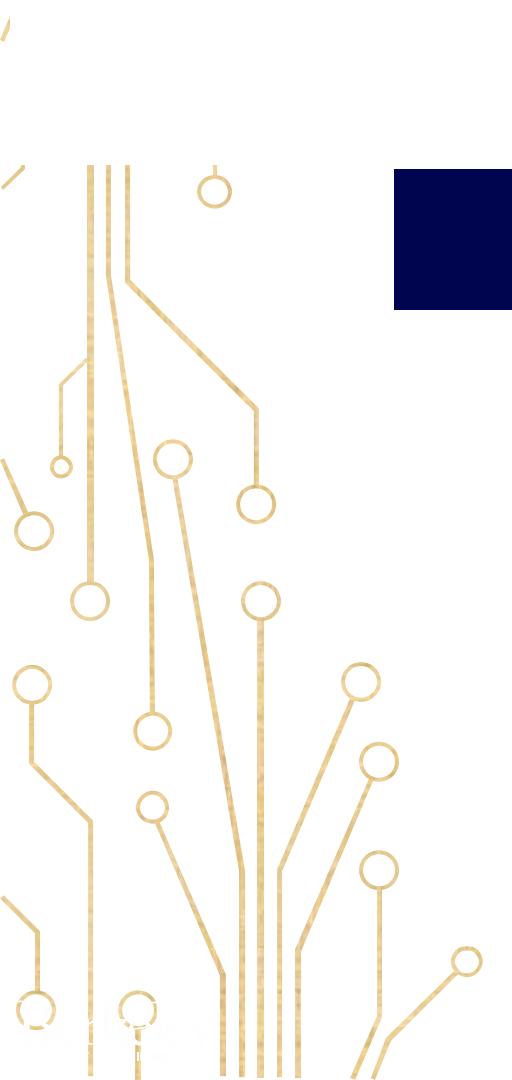
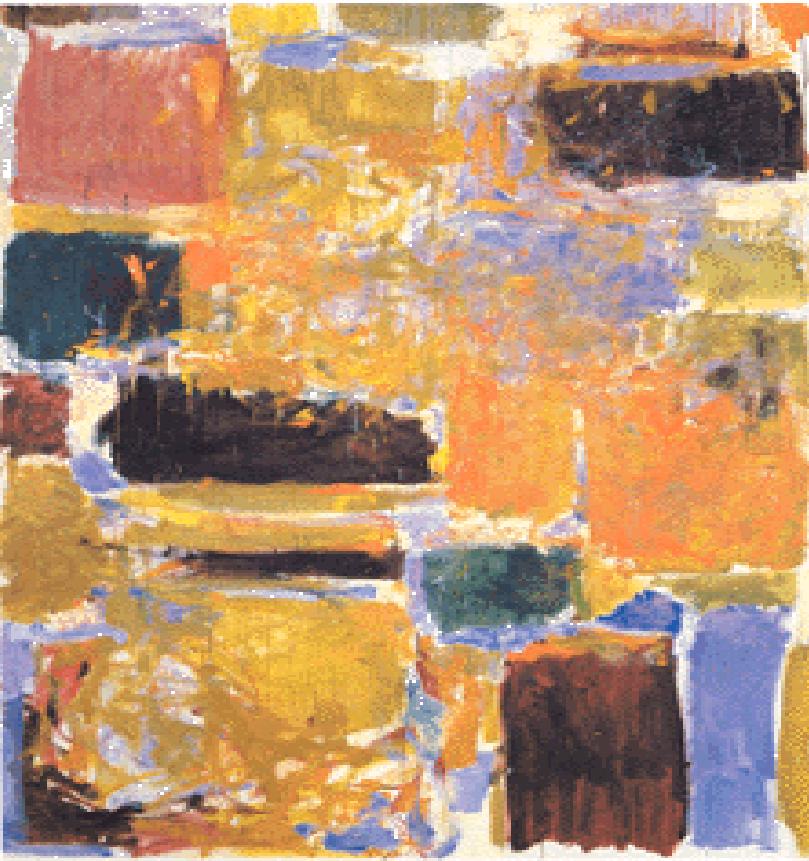




EE1007E: Introduction to Digital Design and ICs

Lecture 1 – Introduction

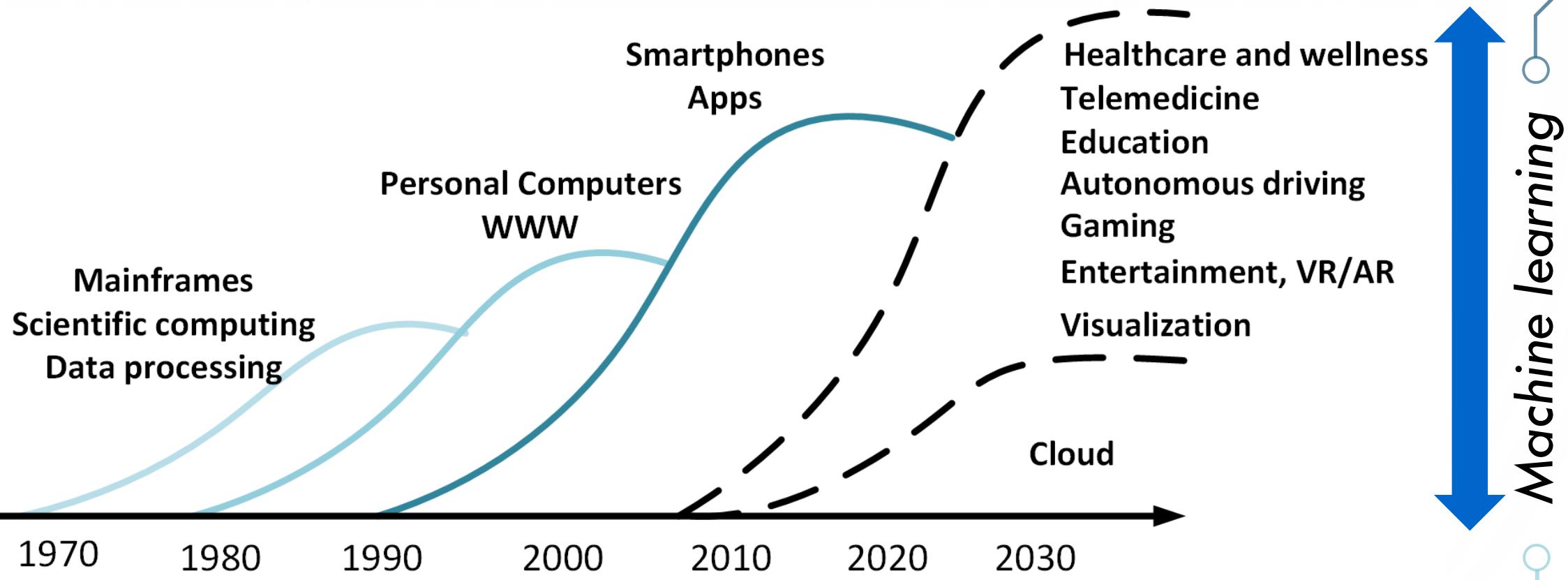




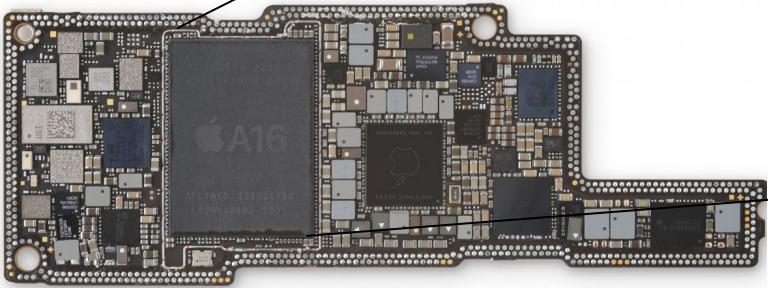
Digital Integrated Circuits and Systems

Past, Present and Future

Diversifying Applications



The Era of Customized Silicon



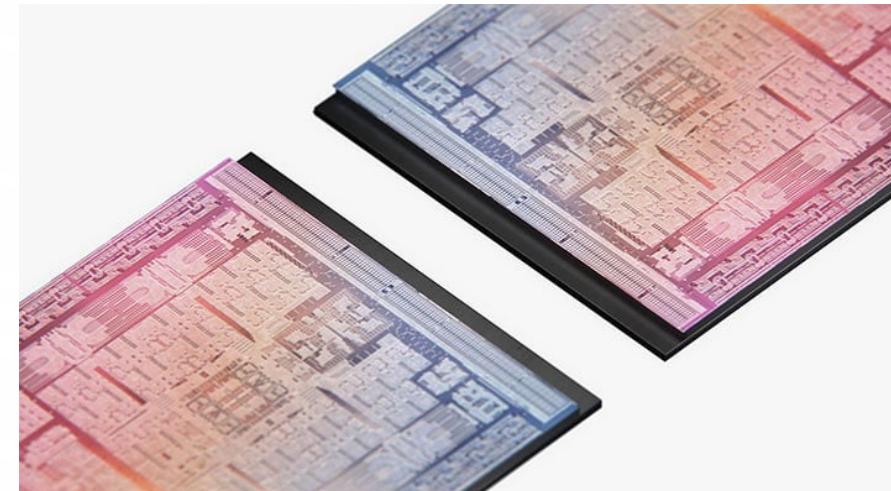
Apple iPhone 15

Source: iFixit



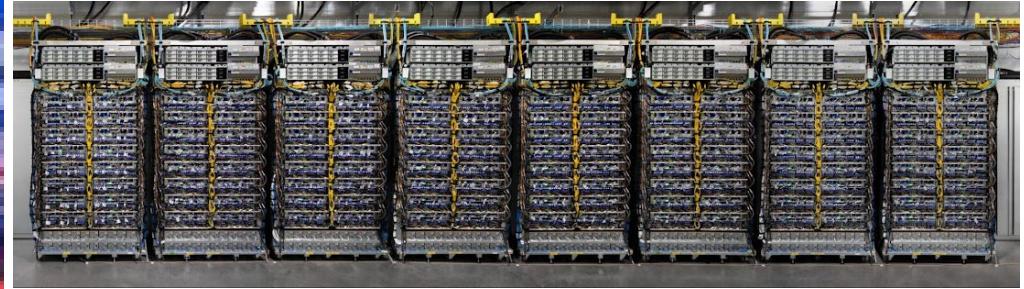
Apple A16

Source: Angstromics

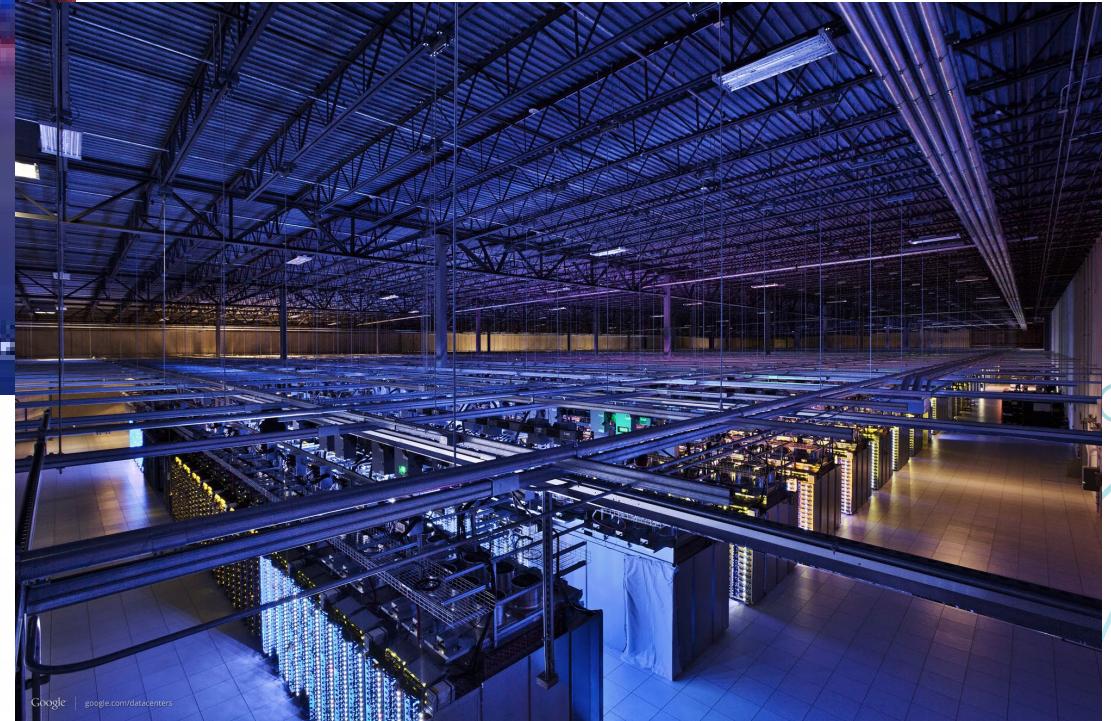


Apple M2 Ultra

Remember: My Other Computer ...



TPU v4 (Google)

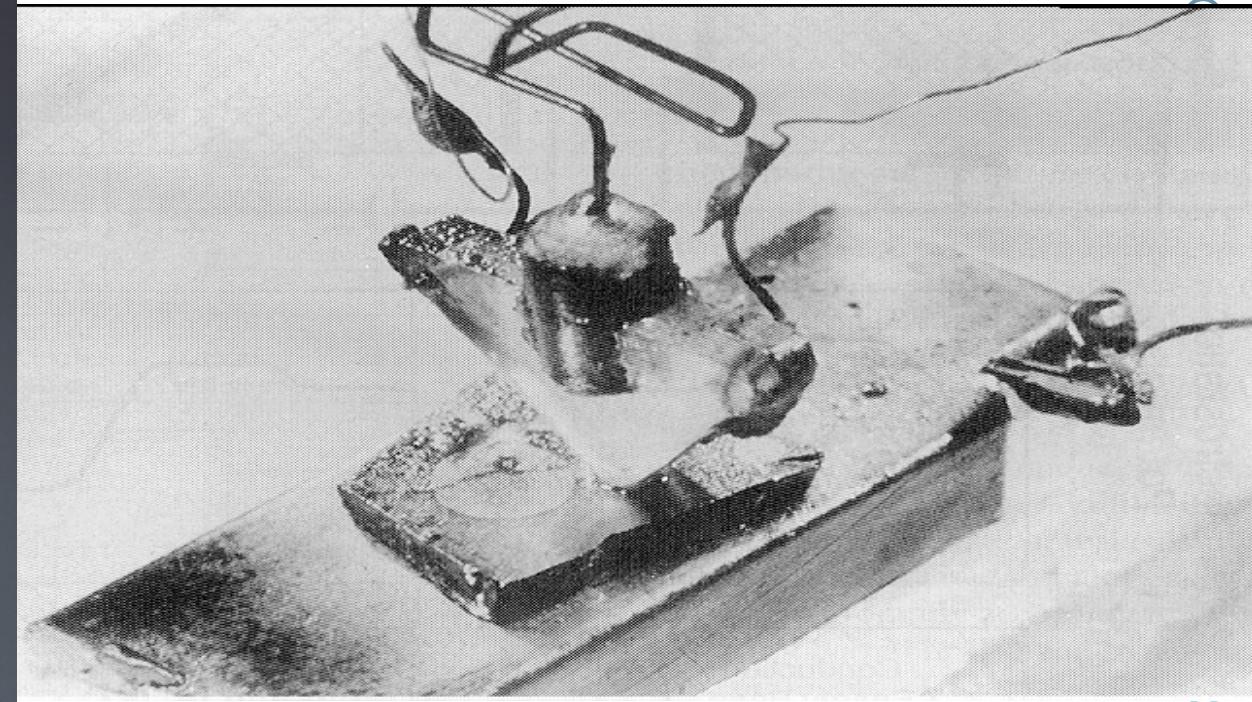
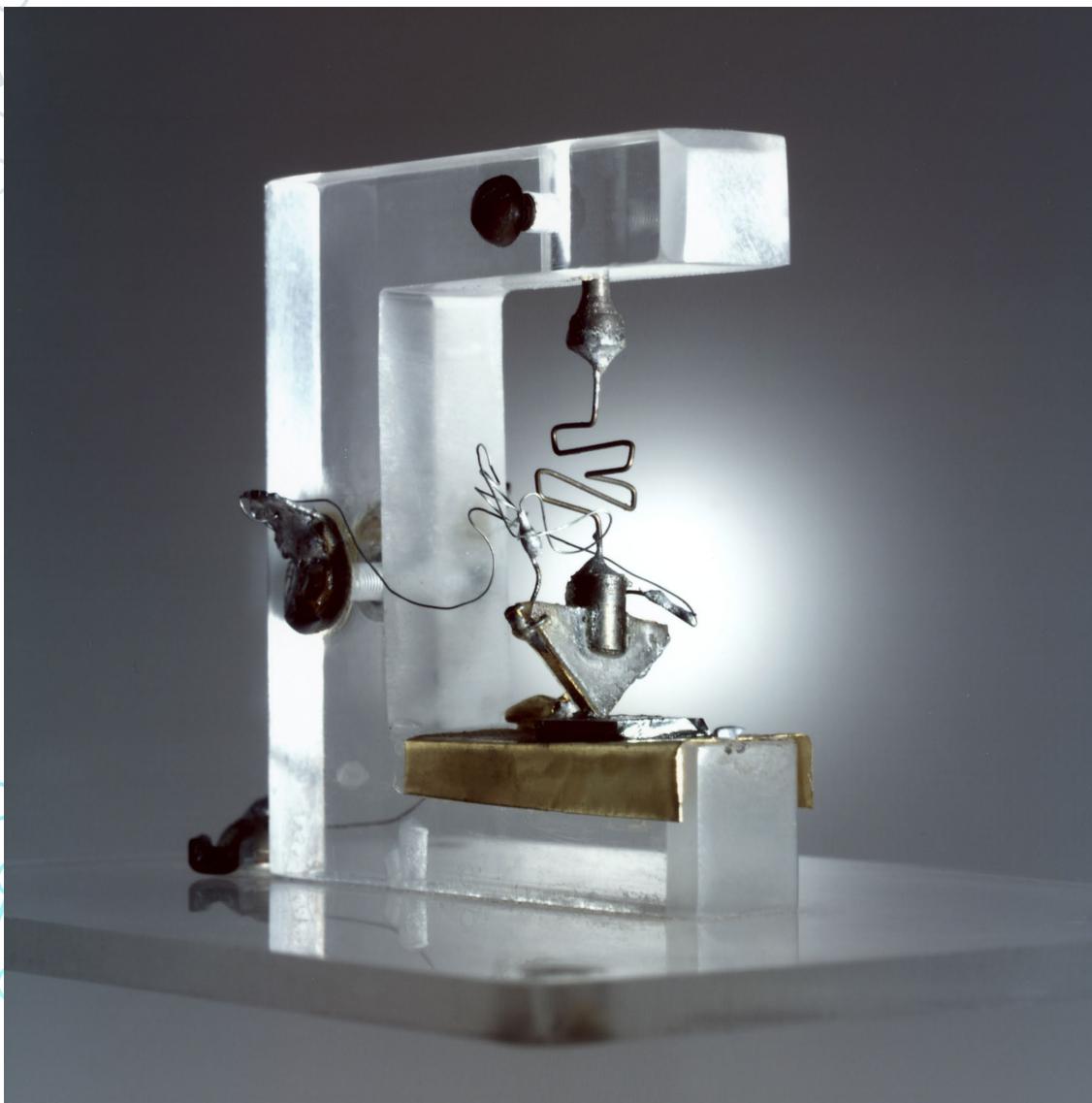


- It is being customized as well!



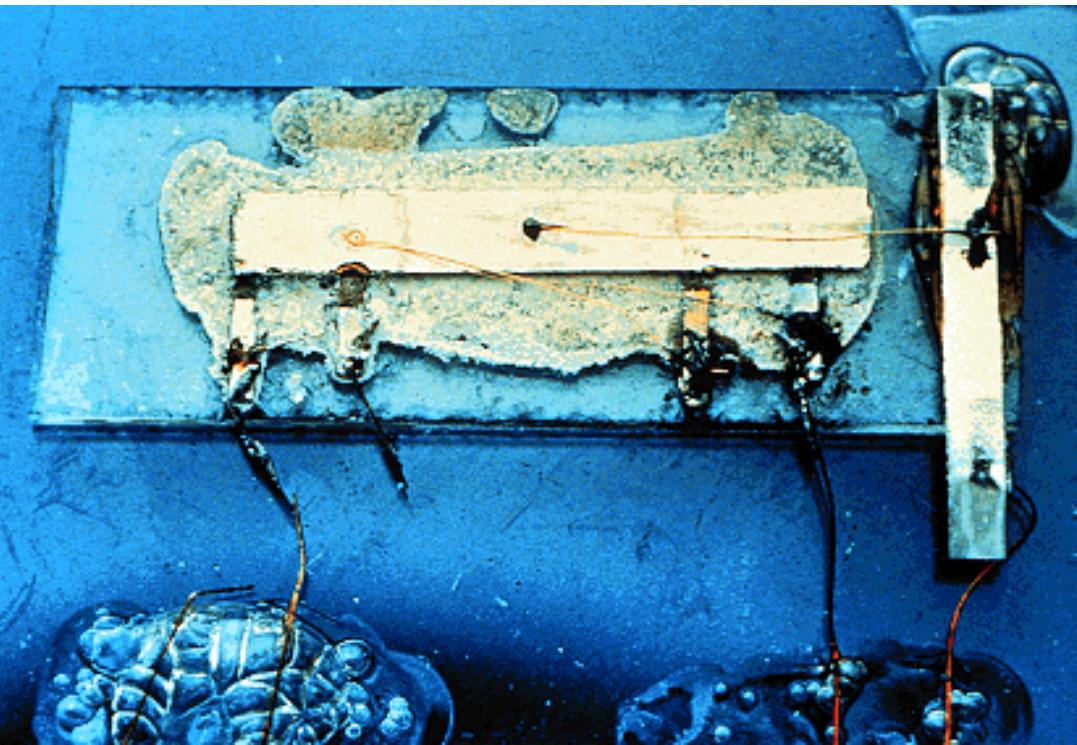
How Did All This Arise?

The Transistor Revolution



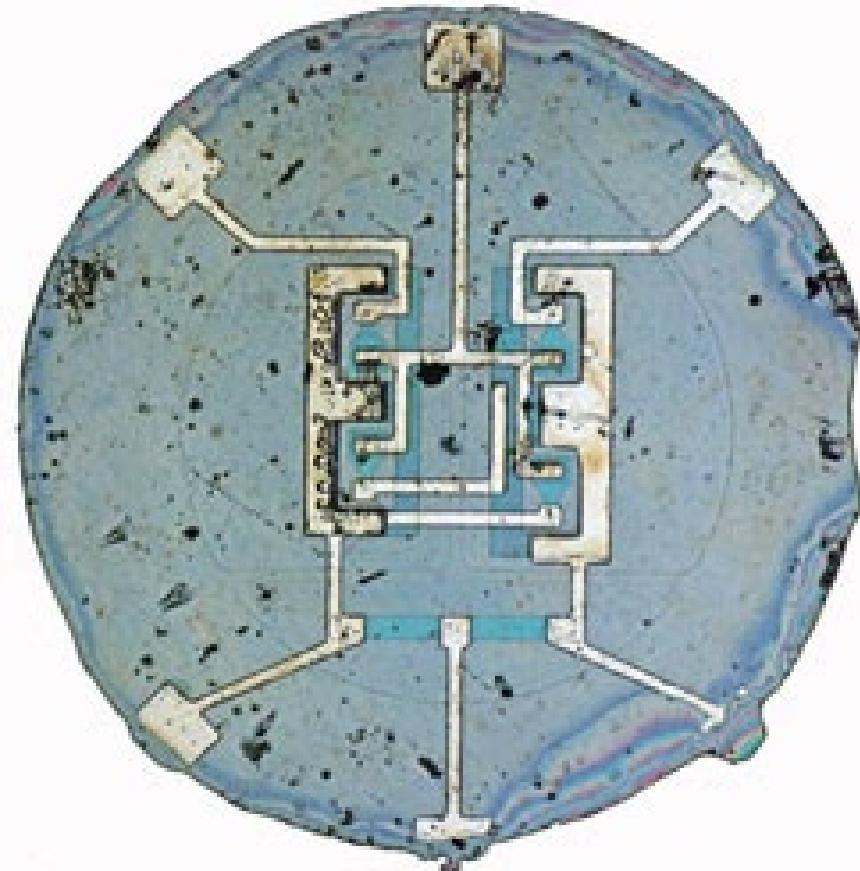
First transistor
Bell Labs, Dec 1947

First Integrated Circuits (1958-59)



Jack Kilby, Texas Instruments

Bob Noyce, Fairchild



Moore's Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 12 months.
- He made a prediction that semiconductor technology will double its effectiveness every ~~12~~ months

~~18~~

24

“The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term, this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000.”

Gordon Moore, Cramming more Components onto Integrated Circuits, (1965).

Moore's Law - 1965

Transistors

Per Die

10^{10}

10^9

10^8

10^7

10^6

10^5

10^4

10^3

10^2

10^1

10^0

1960 1965 1970 1975 1980 1985 1990 1995 2000 2005 2010

Graph from S.Chou, ISSCC'2005

"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."
Electronics, Volume 38, Number 8, April 19, 1965

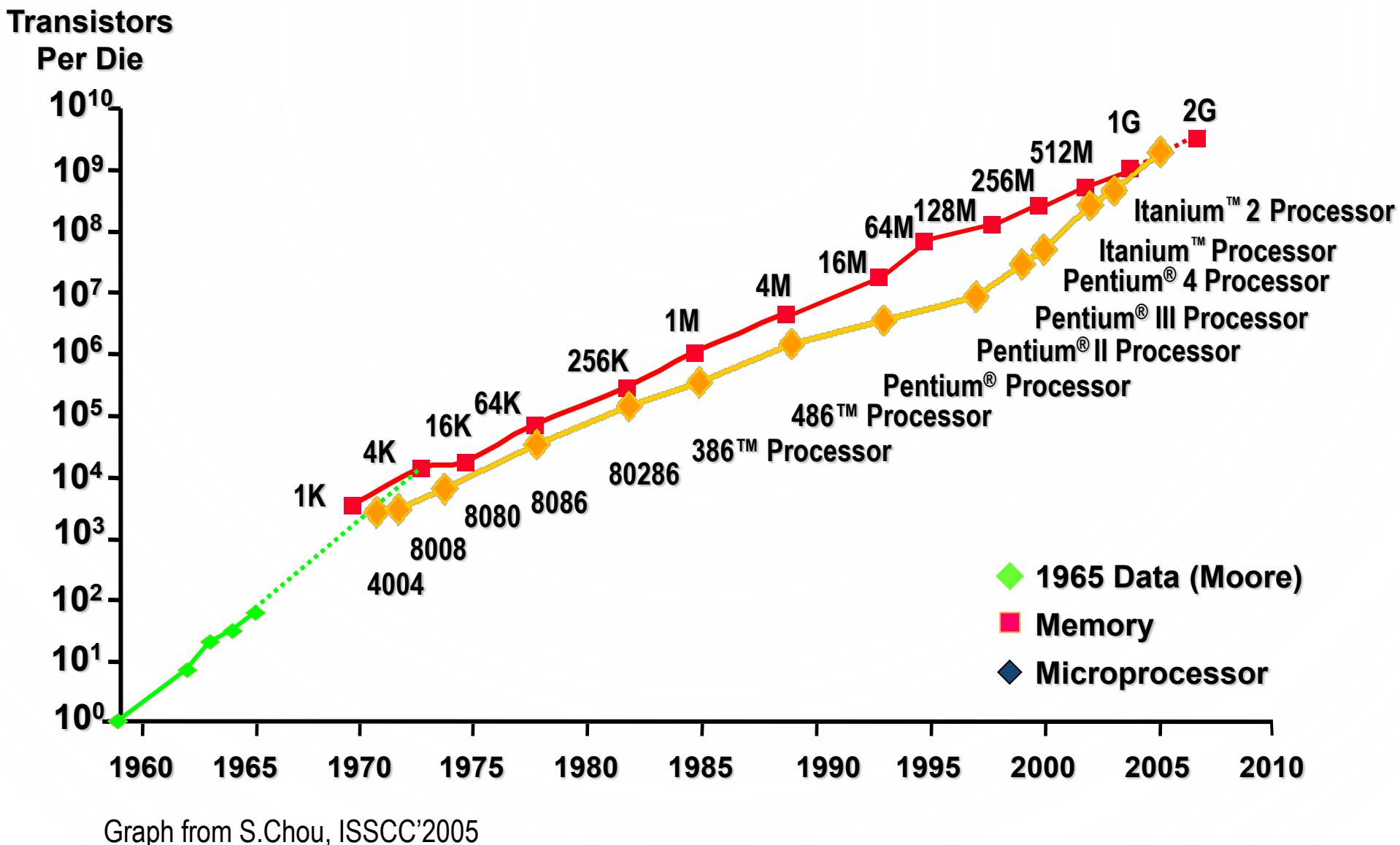
◆ 1965 Data (Moore)

Source: Intel

38



Moore's Law - 2005



Moore's Law - 2023

Transistors per Processor

Transistors in CPUs

1,000,000,000,000

100,000,000,000

10,000,000,000

1,000,000,000

100,000,000

10,000,000

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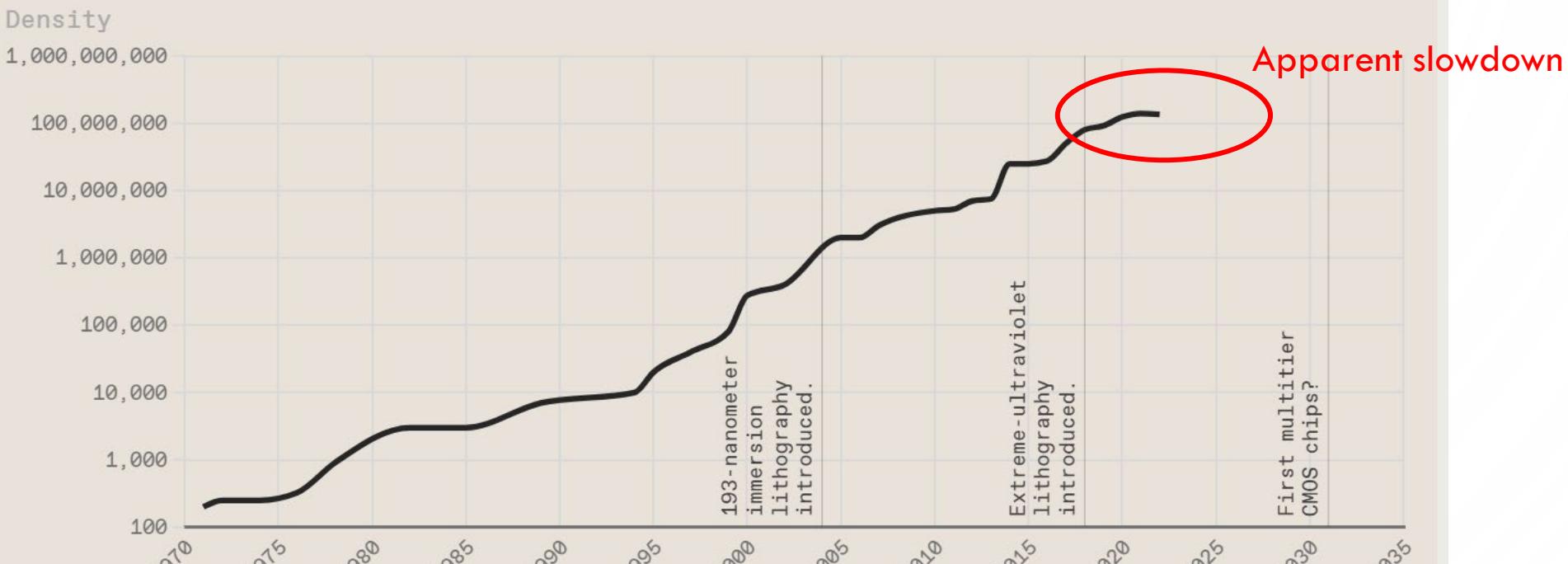
1

Transistor Density

Scaling and Density

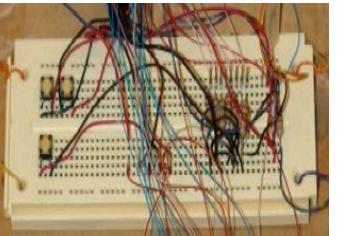
Maximum devices per mm², millions; critical dimensions, nanometers

● Contacted gate pitch, nanometers ● Metal pitch, nanometers
● Transistor density, devices per square millimeter



Sources: IEEE International Roadmap for Devices and Systems, Stanford Nanoelectronics Lab; H.-S. P. Wong, et al., data accessed 17 October 2022

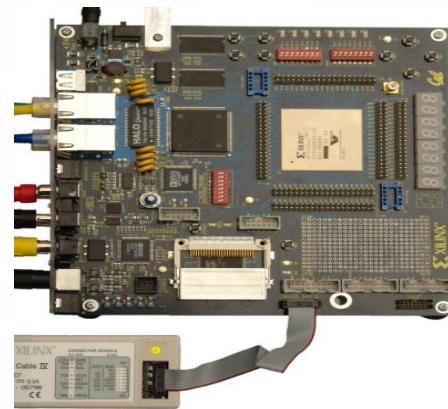
CS150/EECS151 Project Complexity



1980 Pong game
10's of logic gates



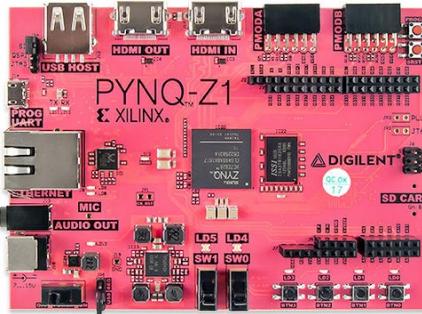
1995 MIDI synthesizer
1000's of logic gates



2000-2010 eTV tuner
10K's logic gates



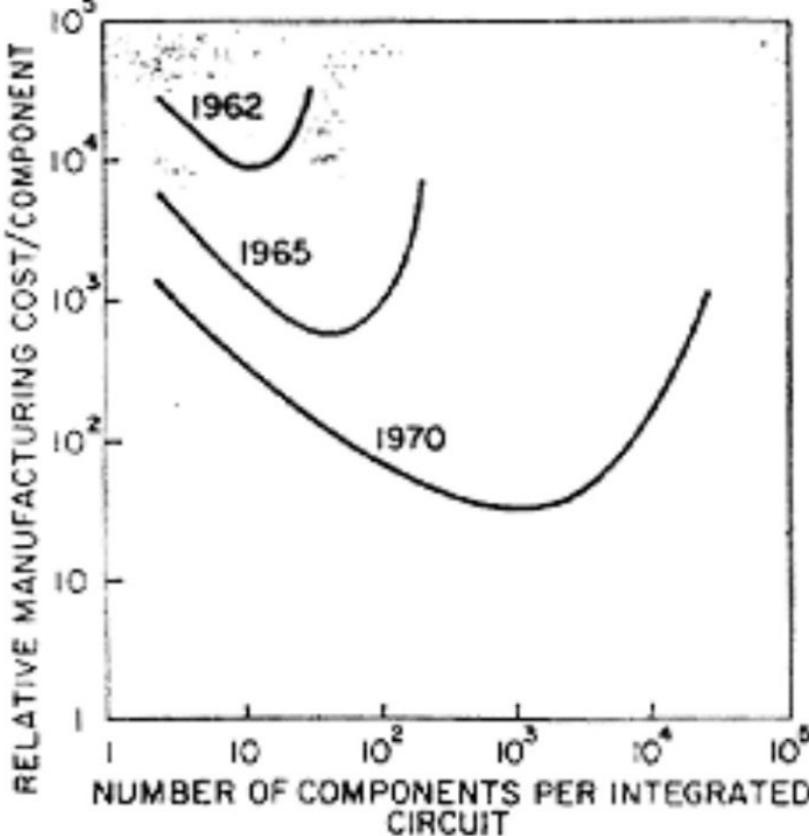
2010-2017 MIPS CPU or BYO
1M logic gates



2018 MIPS CPU
Programmable SOC: dual core ARM, 85K logic cells, 220 MACC

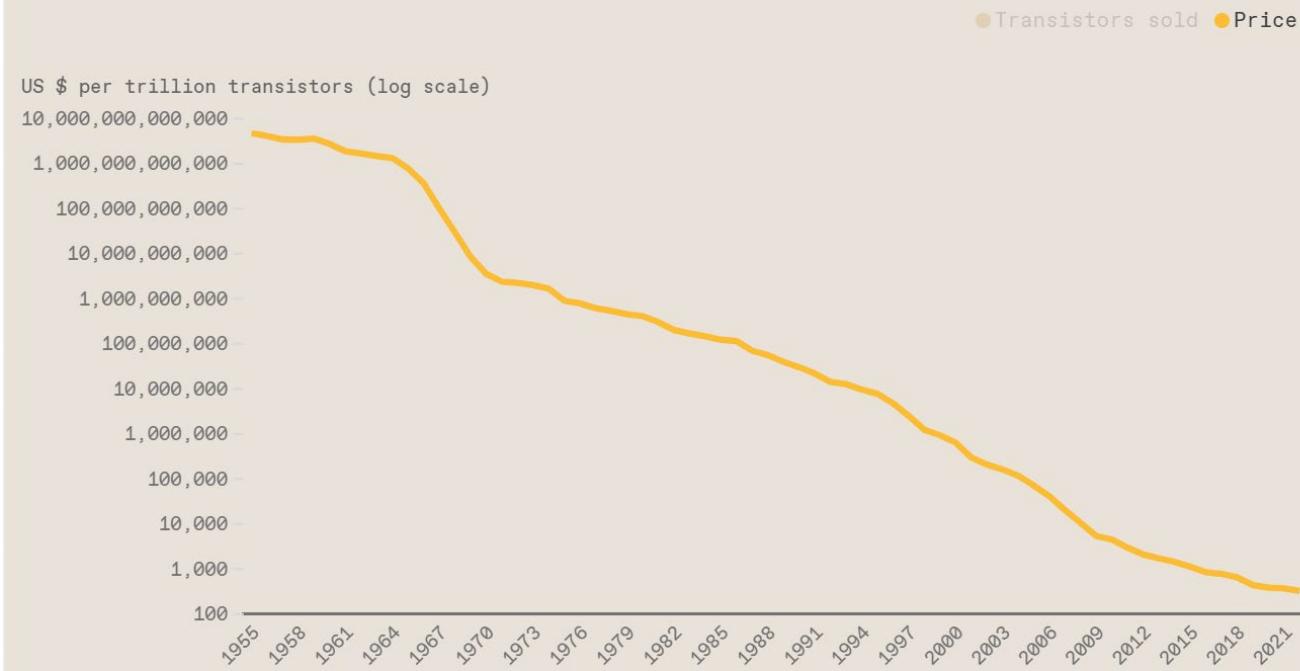
The Key: Cost

Moore's 1965 paper:



Huge Volume, Small Price

Price per trillion transistors, US \$; transistors sold per year, trillions

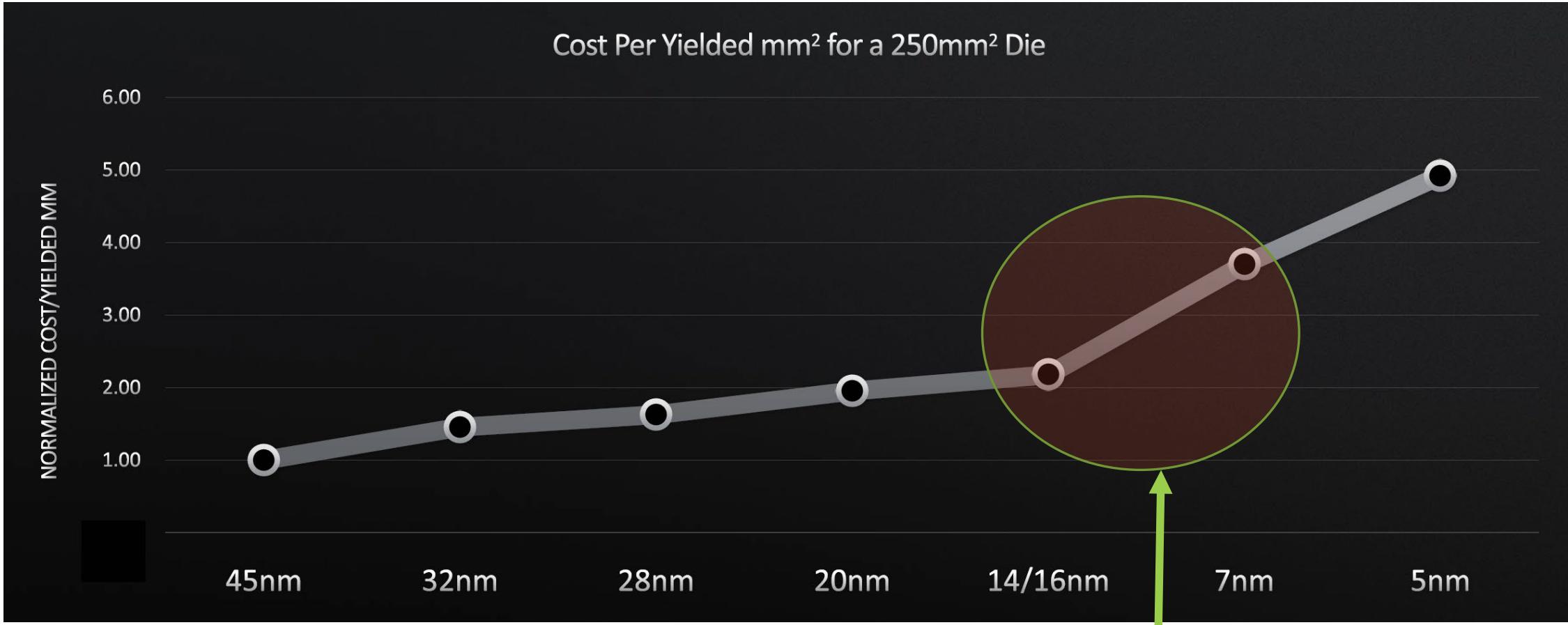


Source: TechInsights

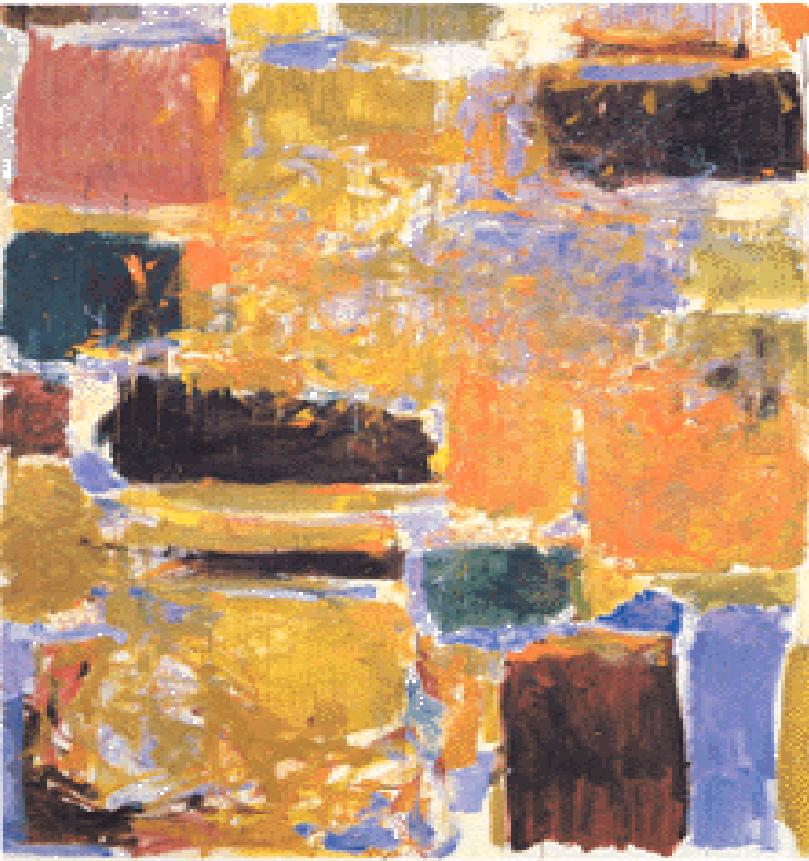
IEEE Spectrum, Nov. 2022

Moore's Law ends when cost reduction stops

Recent Cost Trend



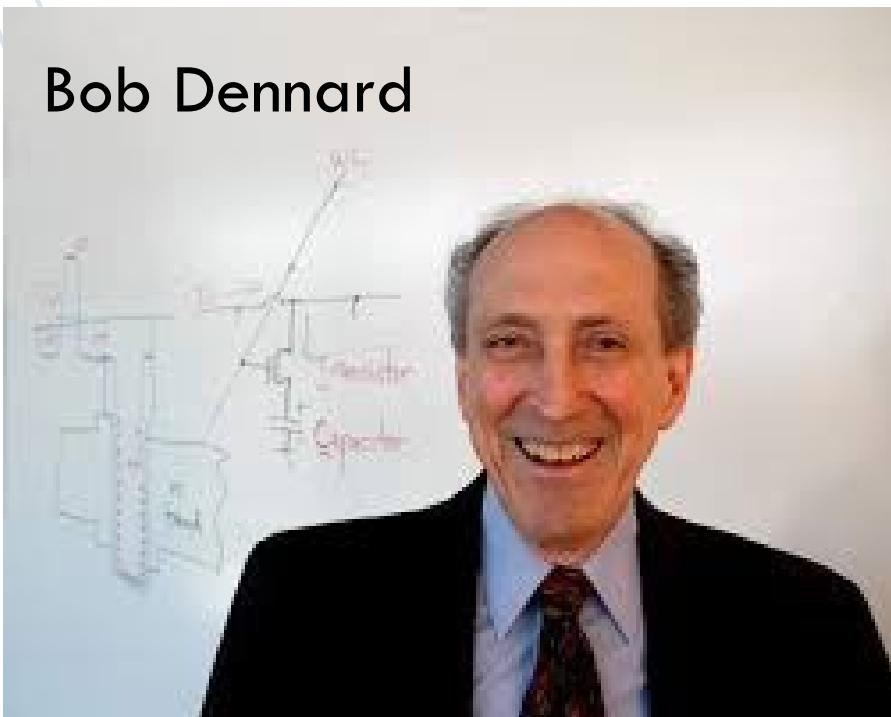
L. Su, HotChips, August 2019.



The Other Trends

Dennard Scaling (1974)

Bob Dennard



- Voltages (and currents) should be scaled proportionally to the dimensions of the transistor
- If so, delay and power should scale

$$\text{Delay} \approx C \cdot V/I_{avg}$$

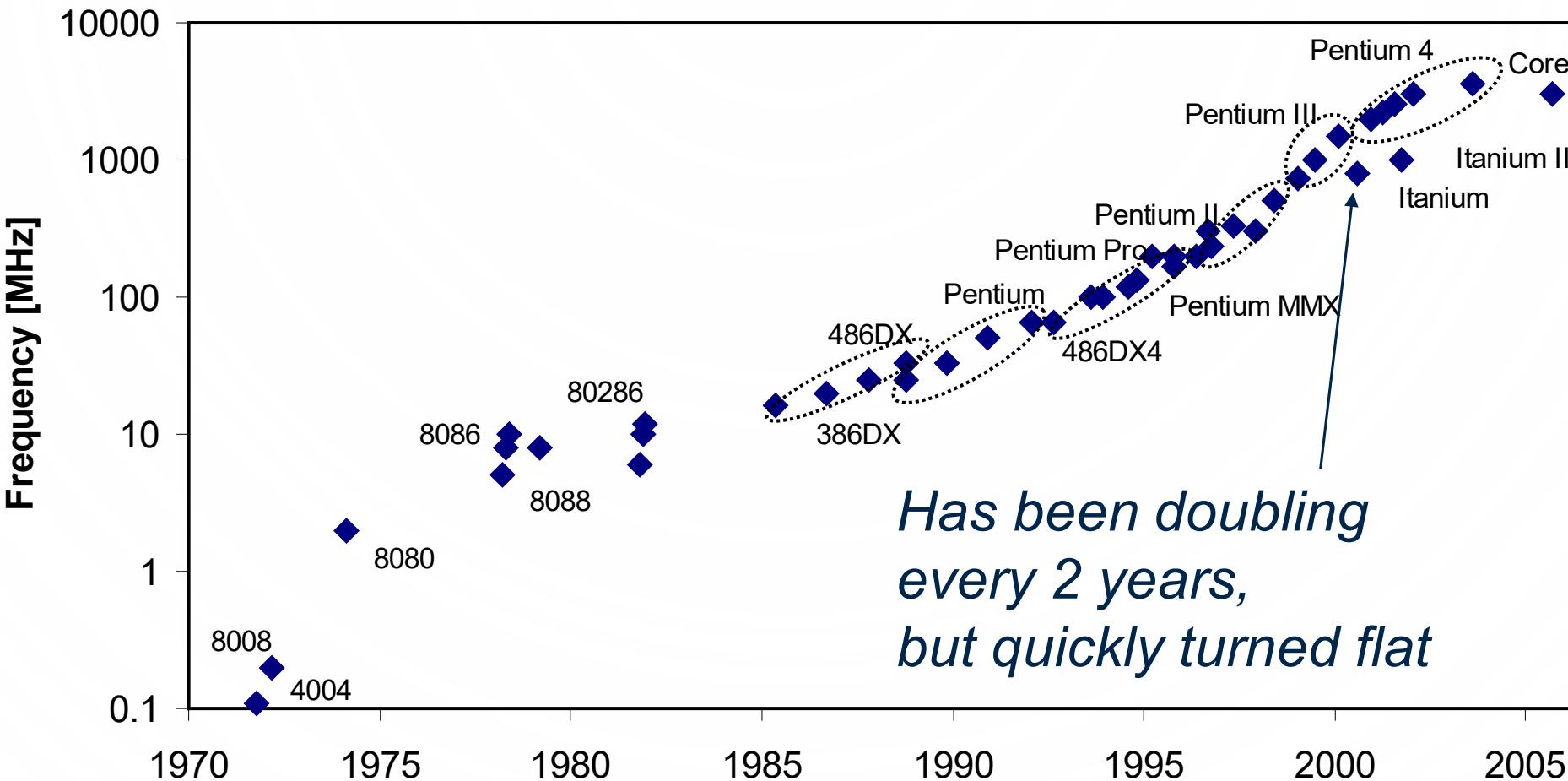
$$P \approx C \cdot V^2/\text{Delay}$$

- And, in theory, power density constant with scaling!
- We are not following Dennard's scaling since ~ 2005

R.H. Dennard, F. Gaenslen, H.-N. Yu, L. Rideout, E. Bassous, A. LeBlanc, Andre
"Design of ion-implanted MOSFET's with very small physical dimensions," IEEE Journal of Solid State Circuits. SC-9
(5), 1974.

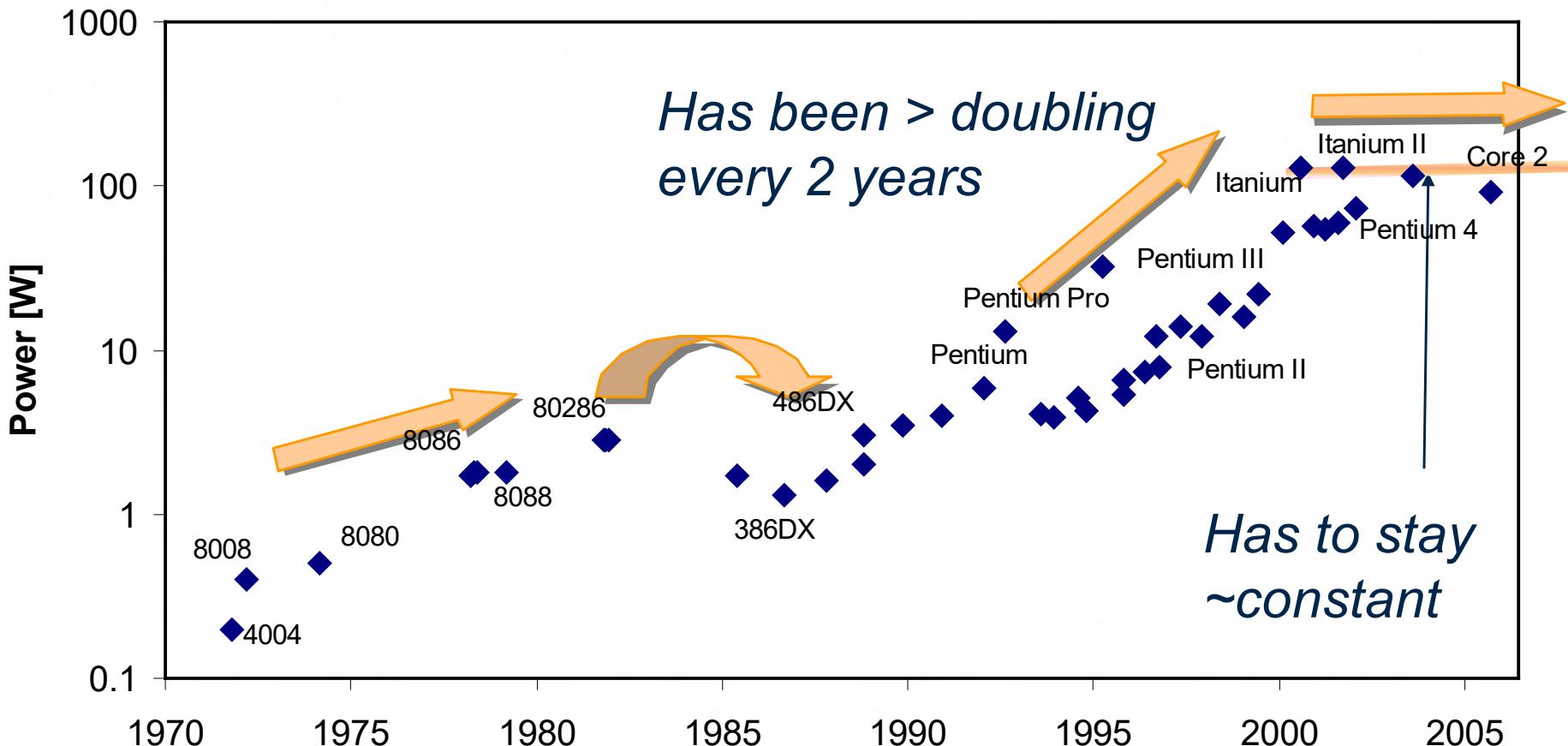
Frequency

Frequency Trends in Intel's Microprocessors



Power Dissipation

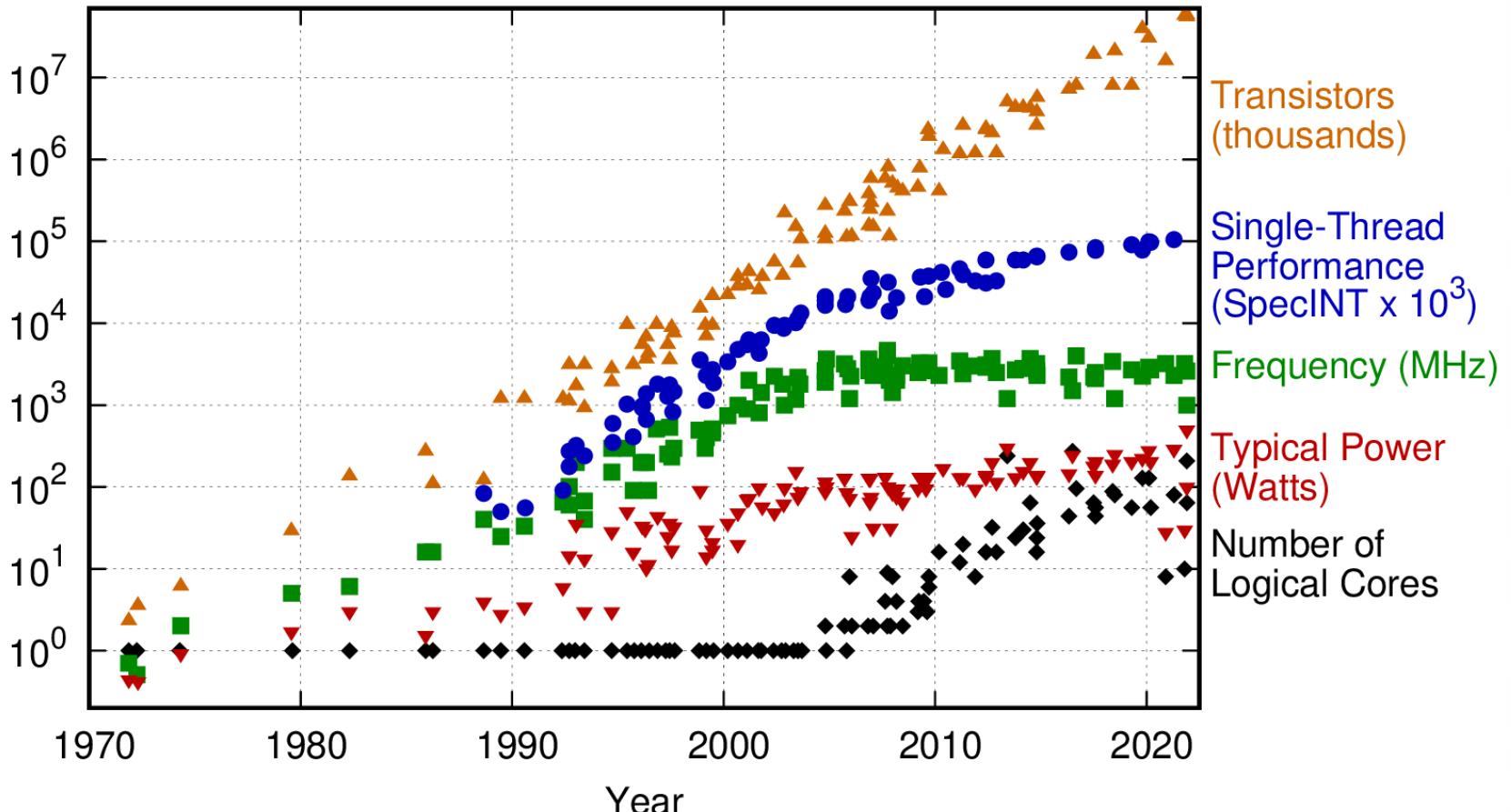
Power Trends in Intel's Microprocessors



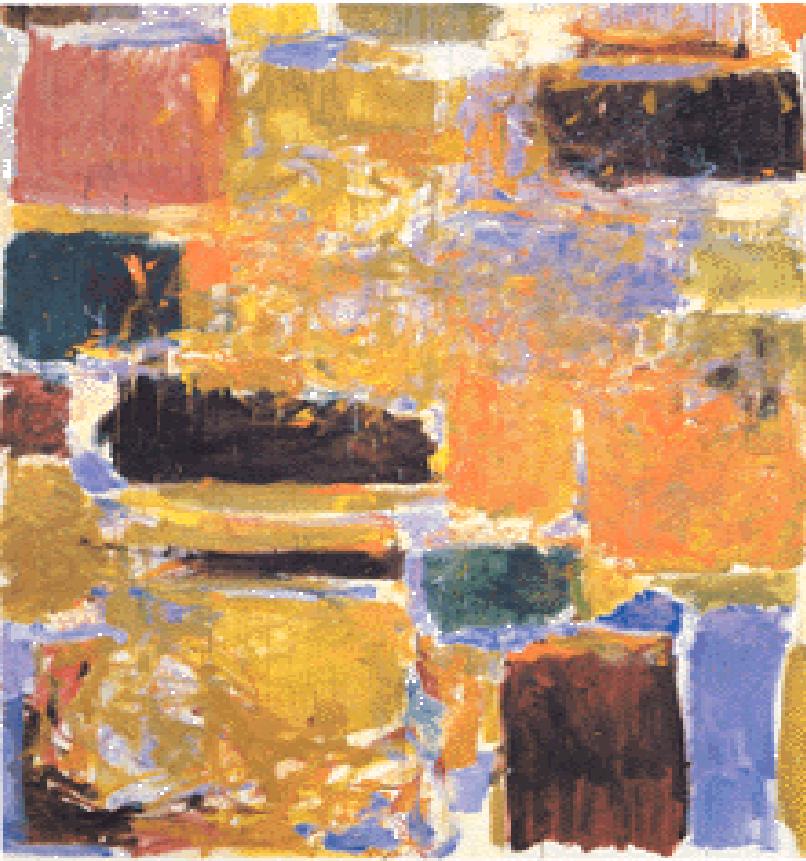
Power and Performance Trends

- What do we do next?

50 Years of Microprocessor Trend Data

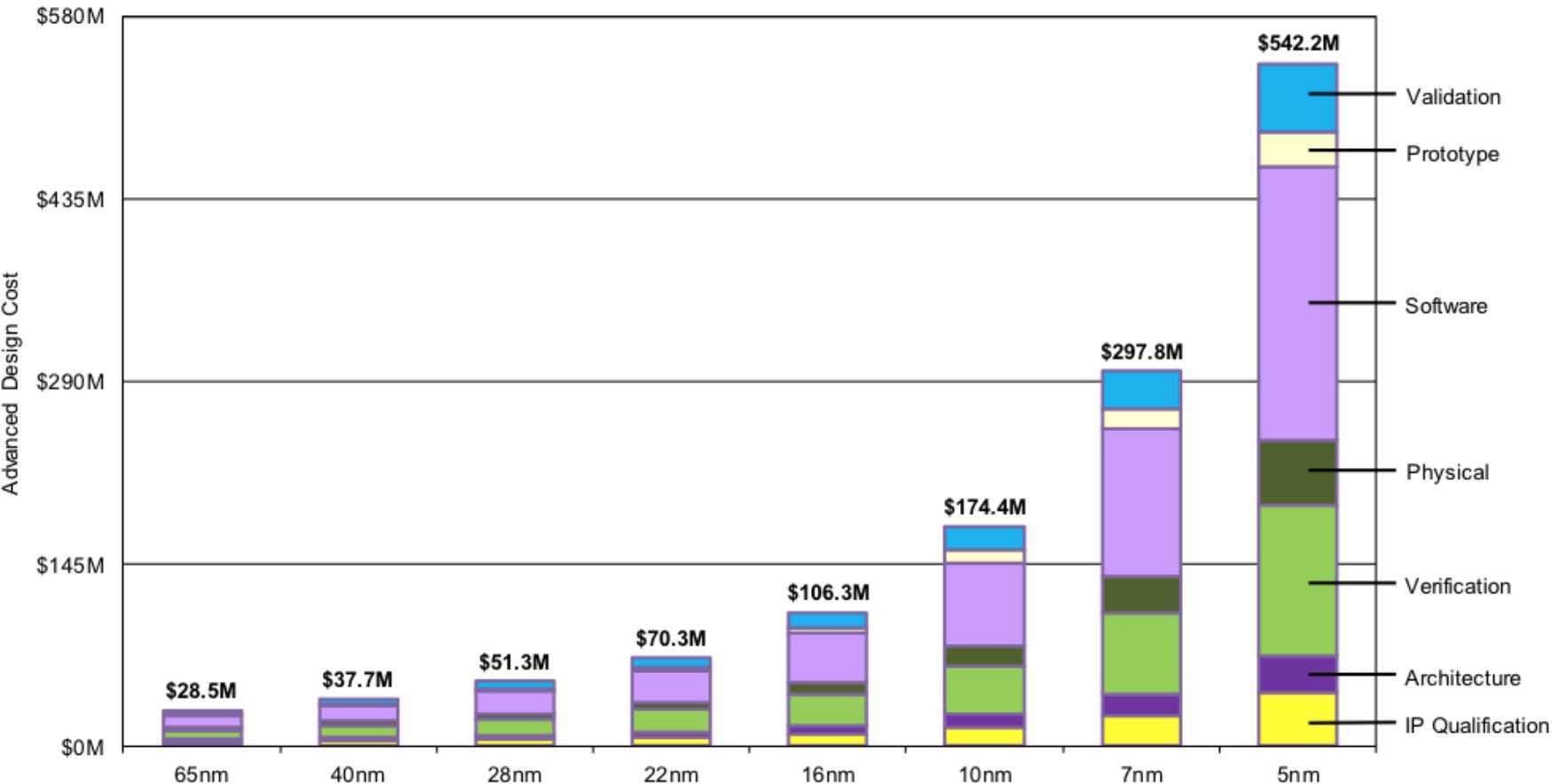


Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2021 by K. Rupp



The Other Demon: Complexity and Design Costs

Cost Of Developing New Products



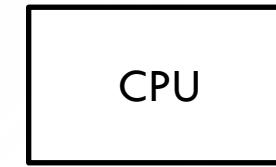
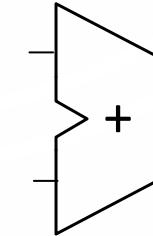
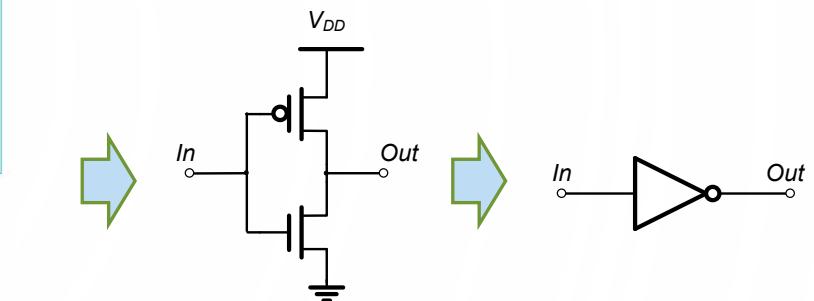
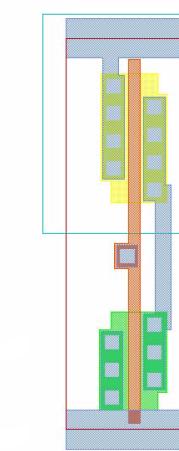
- These are non-recurring (NRE) costs, need to be amortized over the lifetime of a product
- We will attempt to dismantle this...

Solutions

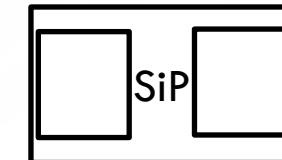
- Software faced the complexity issues as well
- Solutions: Increase abstraction level, be modular, improve reuse, rely on open source, be agile...
- Apply to hardware design!

Abstraction

- How to design a Pong game
 - Hand layout
 - Gate-level design (semi custom)
 - Describe in HDL
 - Synthesis, place and route
 - HLS, HCL
 - “Computer, design a pong game” ?



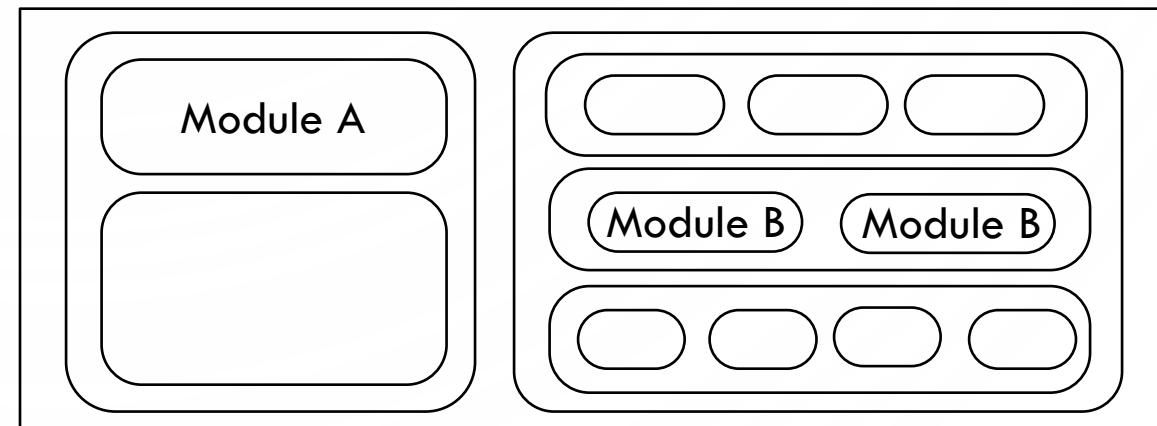
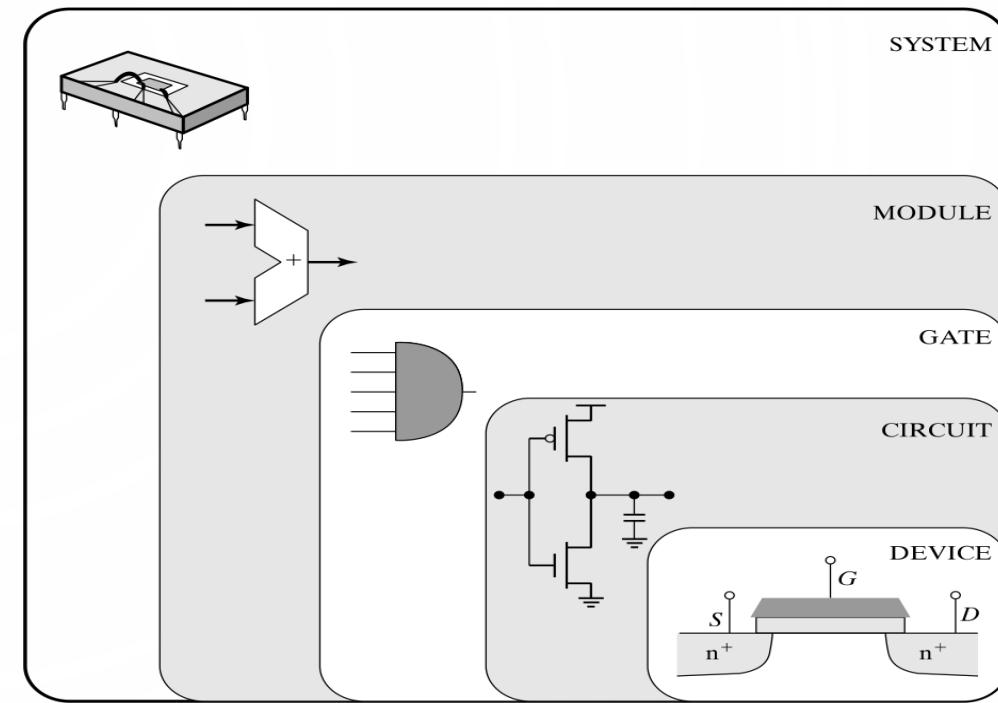
System on a Chip



System in a Package

Hierarchy in Designs – Complexity Control

- Design Abstraction
 - Hide details and reduce number of things to handle at any time
- Modular design
 - Divide and conquer
 - Simplifies implementation and debugging
- Regularity
 - Instantiate identical modules



Digital Design: What's it all about?

Given a functional description and performance, cost, & power constraints, come up with an implementation using a set of primitives.

- How do we learn to do this?
 1. Learn about the design primitives and how to use them.
 2. Learn about design representations.
 3. Learn formal methods and tools to manipulate the representations.
 4. Study design examples.
 5. Have robust approach to verification.
 6. Use trial and error - CAD tools and prototyping. Practice!
- Digital design is a bit an art as well as a science. The creative spirit is critical in combining basic elements & other components in new ways to achieve a desired function.
- However, unlike art, we have objective measures of a design:

Performance Cost Power