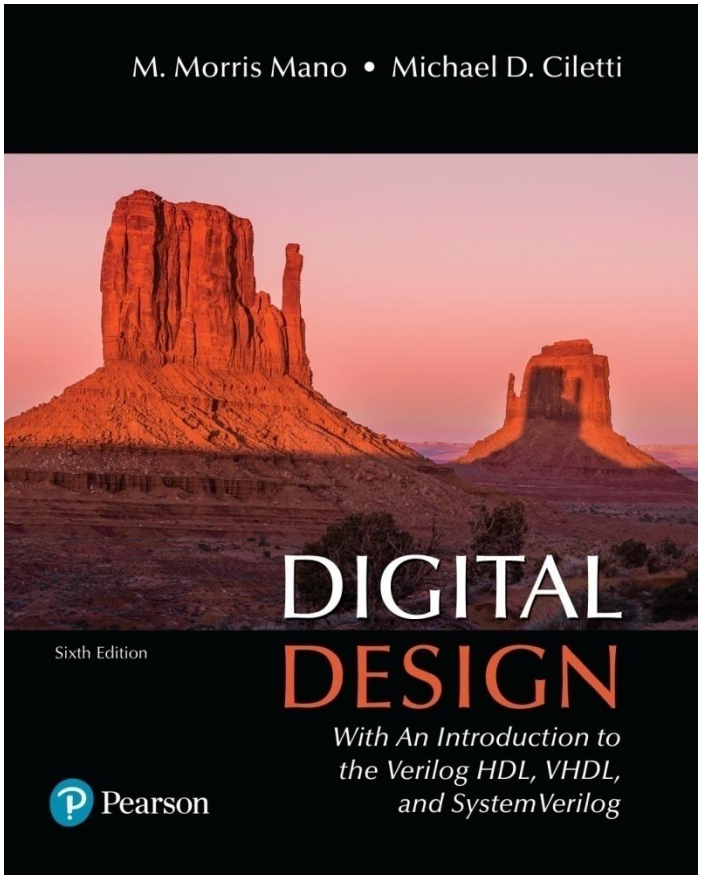
Digital Design

With an Introduction to the Verilog HDL, VHDL, and SystemVerilog

6th Edition

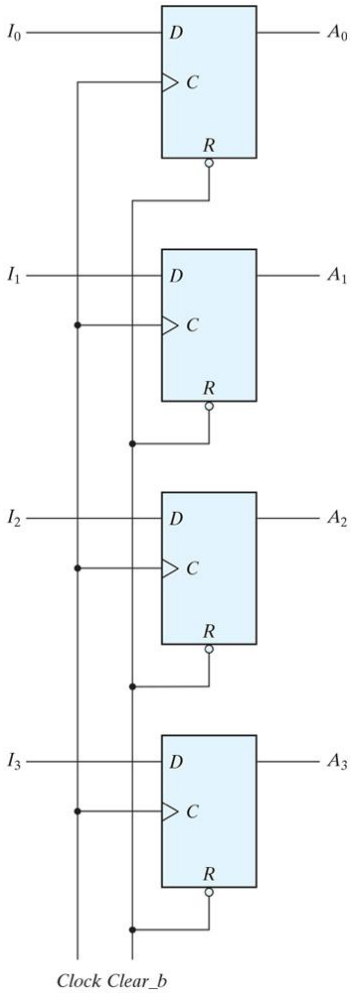


Chapter 06

Registers and Counters

Pearson

Figure 6.1
Four-bit register.



Pearson

Figure 6.2
Four-bit register with parallel load.

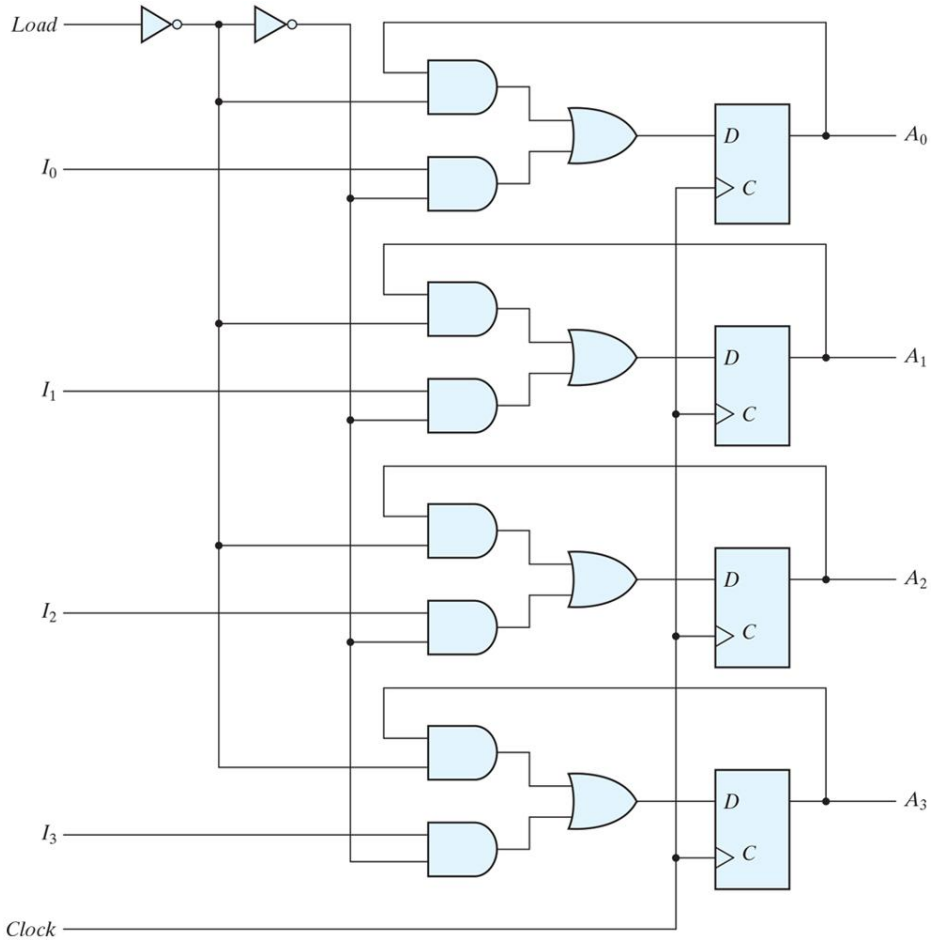


Figure 6.3
Four-bit shift register.

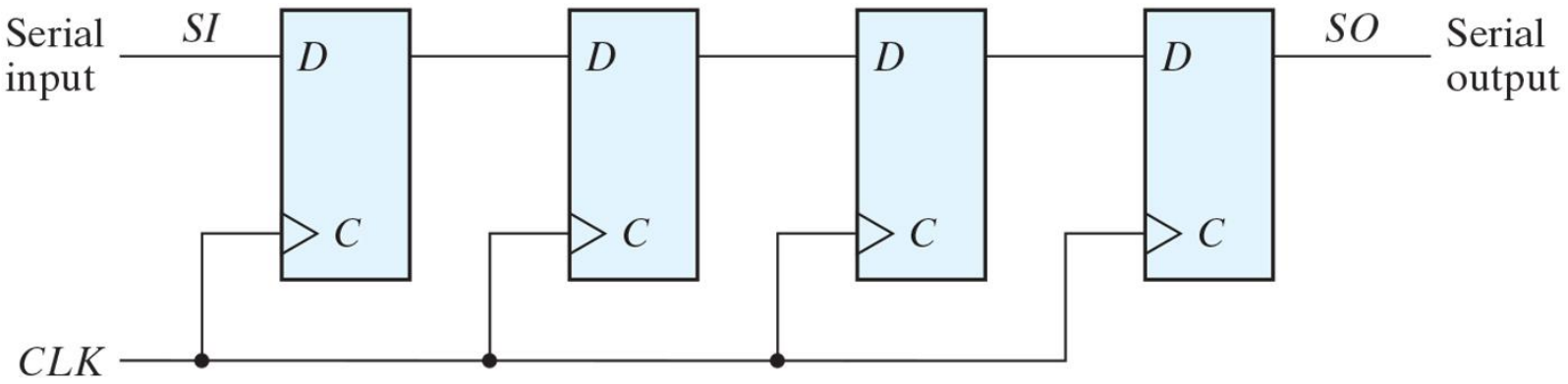


Figure PE6.1

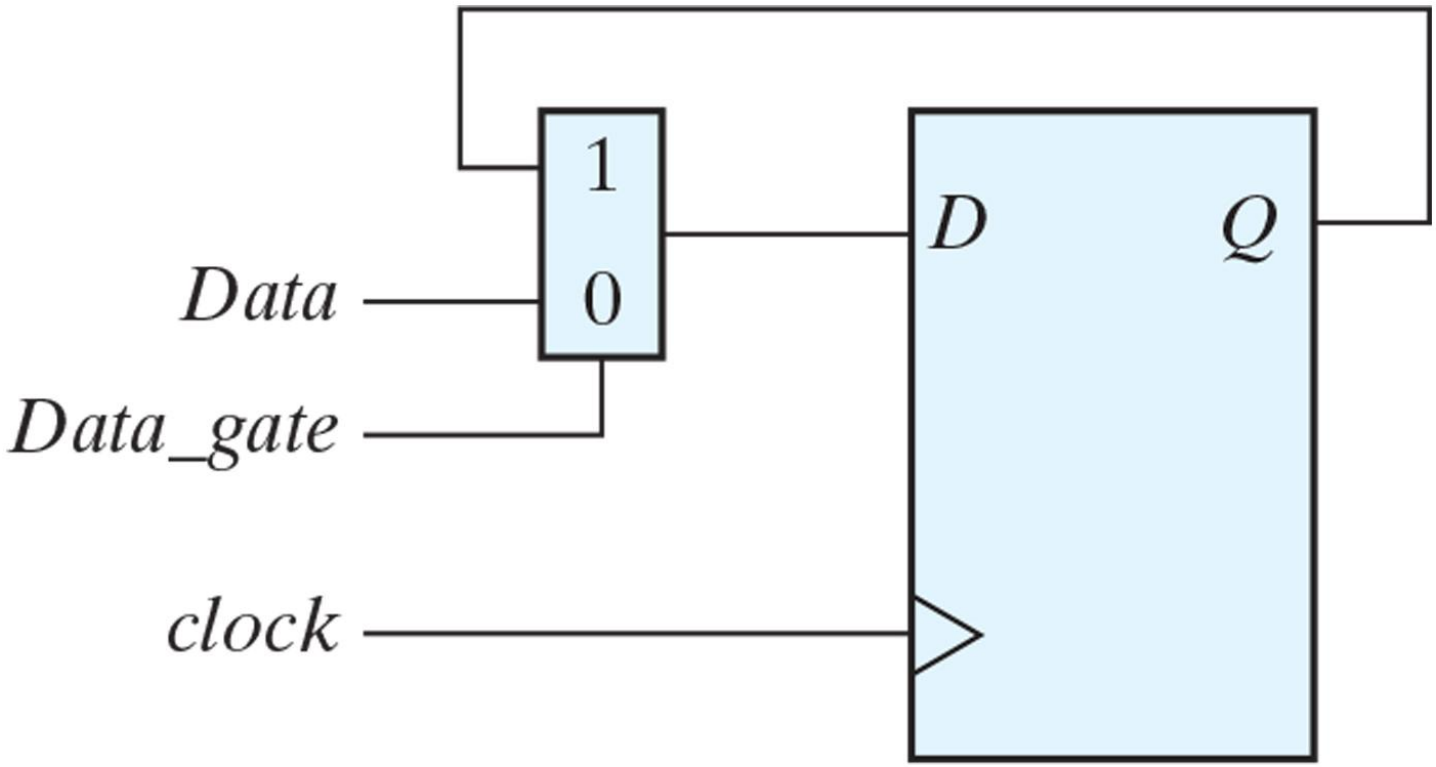


Figure 6.4
Serial transfer from register *A* to register *B*.

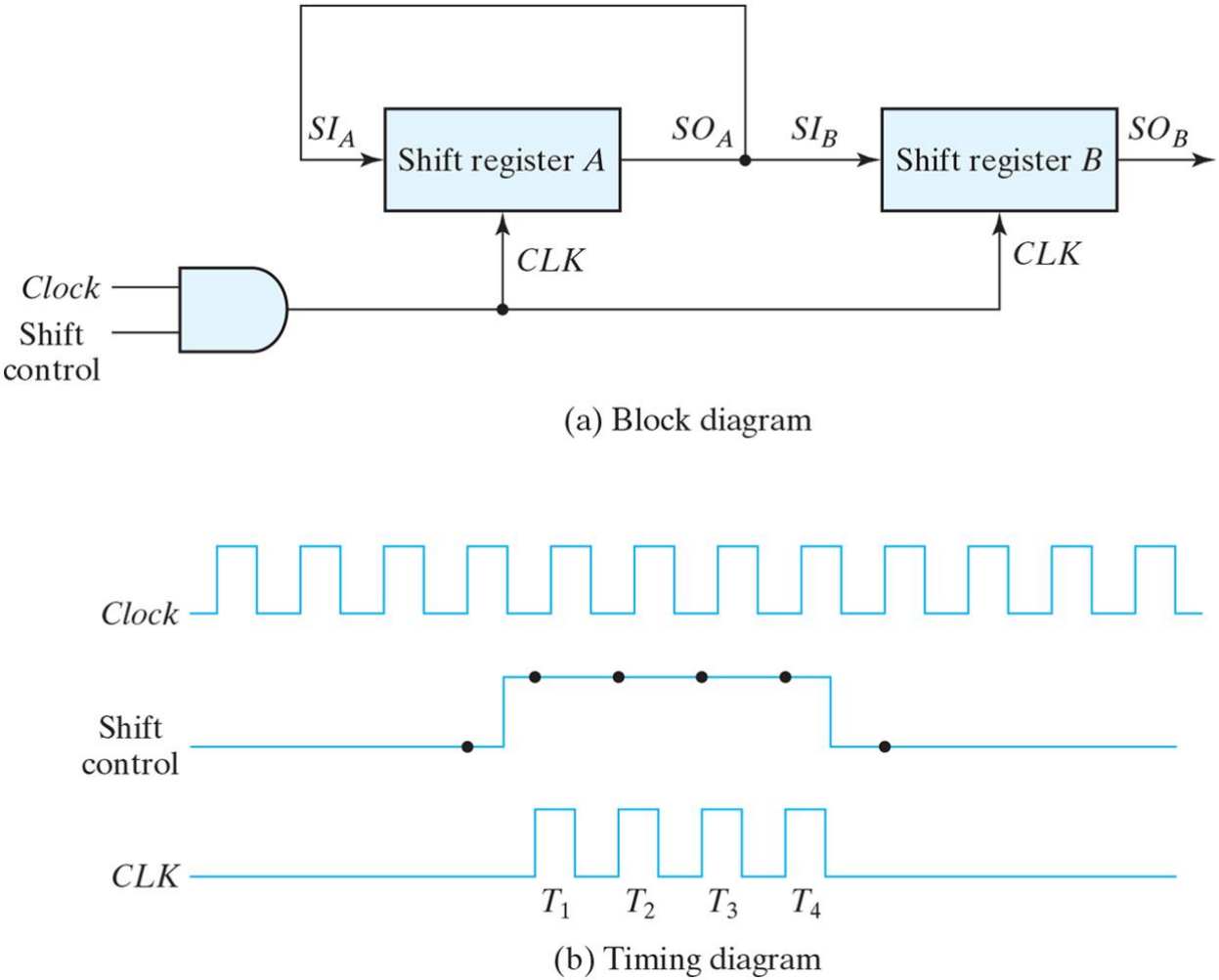


Table 6.1
Serial-Transfer Example.

Timing Pulse	Shift Register *A*				Shift Register *B*			
Initial value	1	0	1	1	0	0	1	0
After T_1	1	1	0	1	1	0	0	1
After T_2	1	1	1	0	1	1	0	0
After T_3	0	1	1	1	0	1	1	0
After T_4	1	0	1	1	1	0	1	1

Figure 6.5
Serial adder.

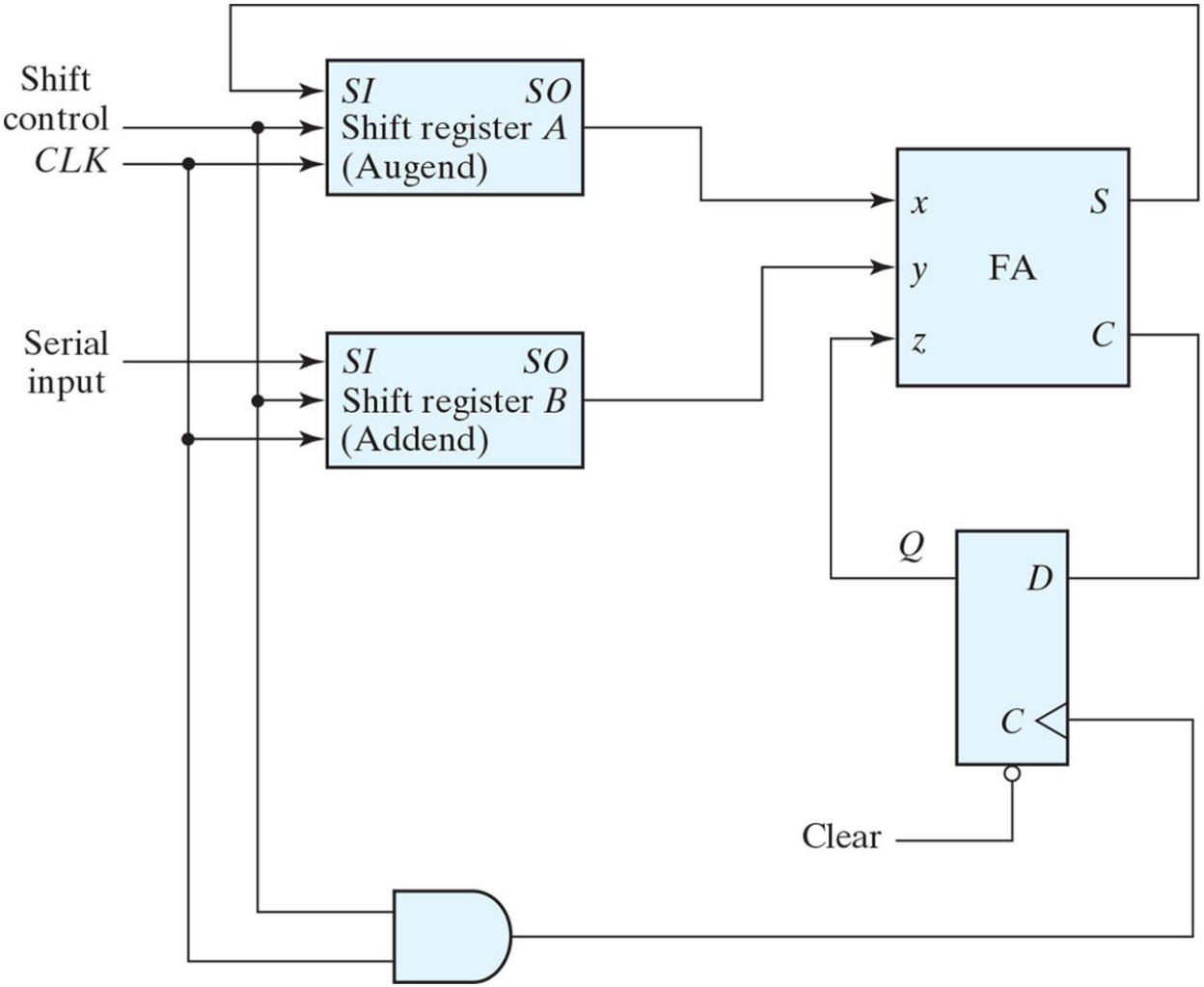


Table 6.2
State Table for Serial Adder.

Present State	Inputs		Next State	Output	Flip-Flop Inputs	
Q	x	y	Q	S	J_Q	K_Q
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

Figure 6.6
Second form of serial adder.

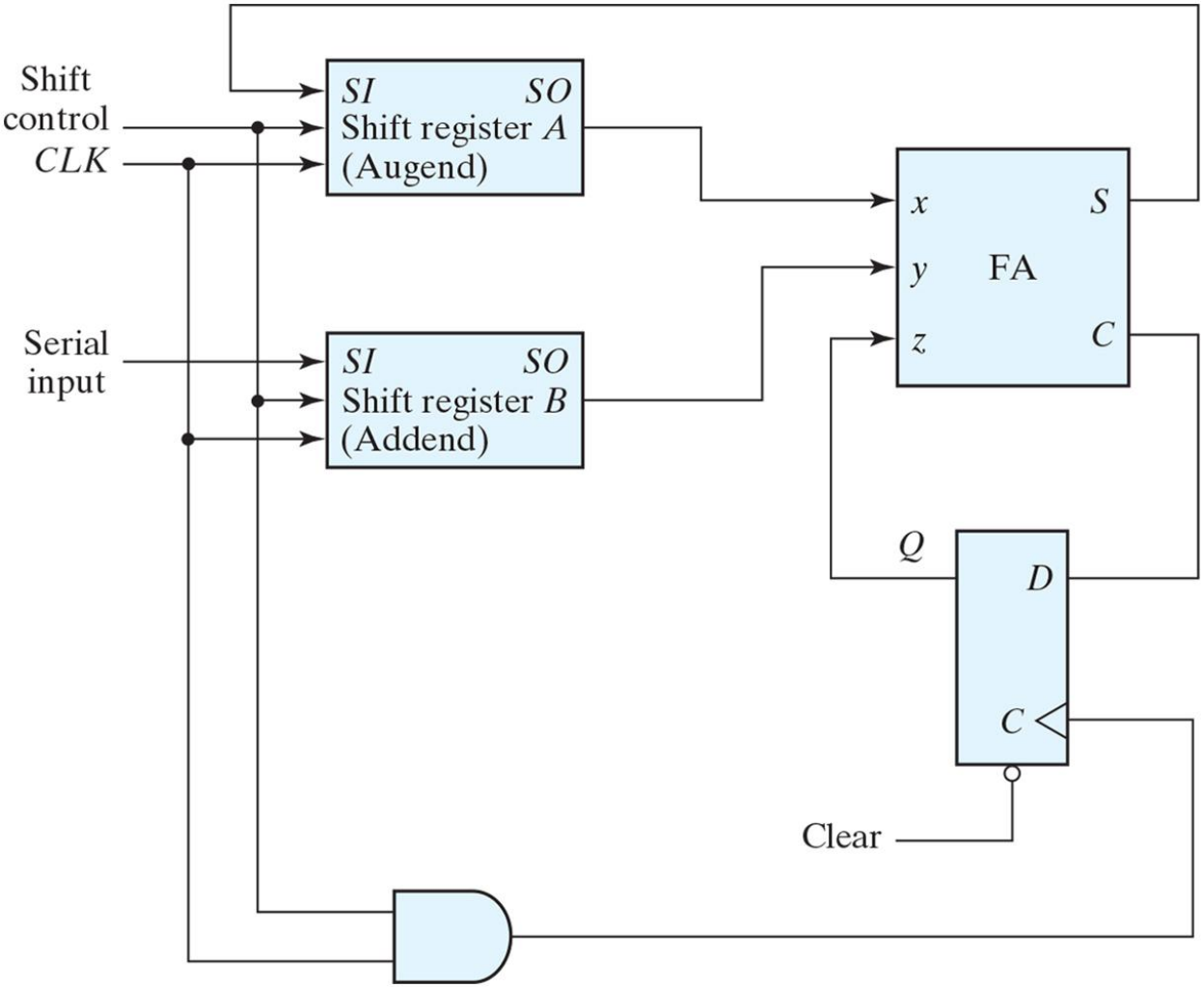


Figure 6.7
Four-bit universal shift register.

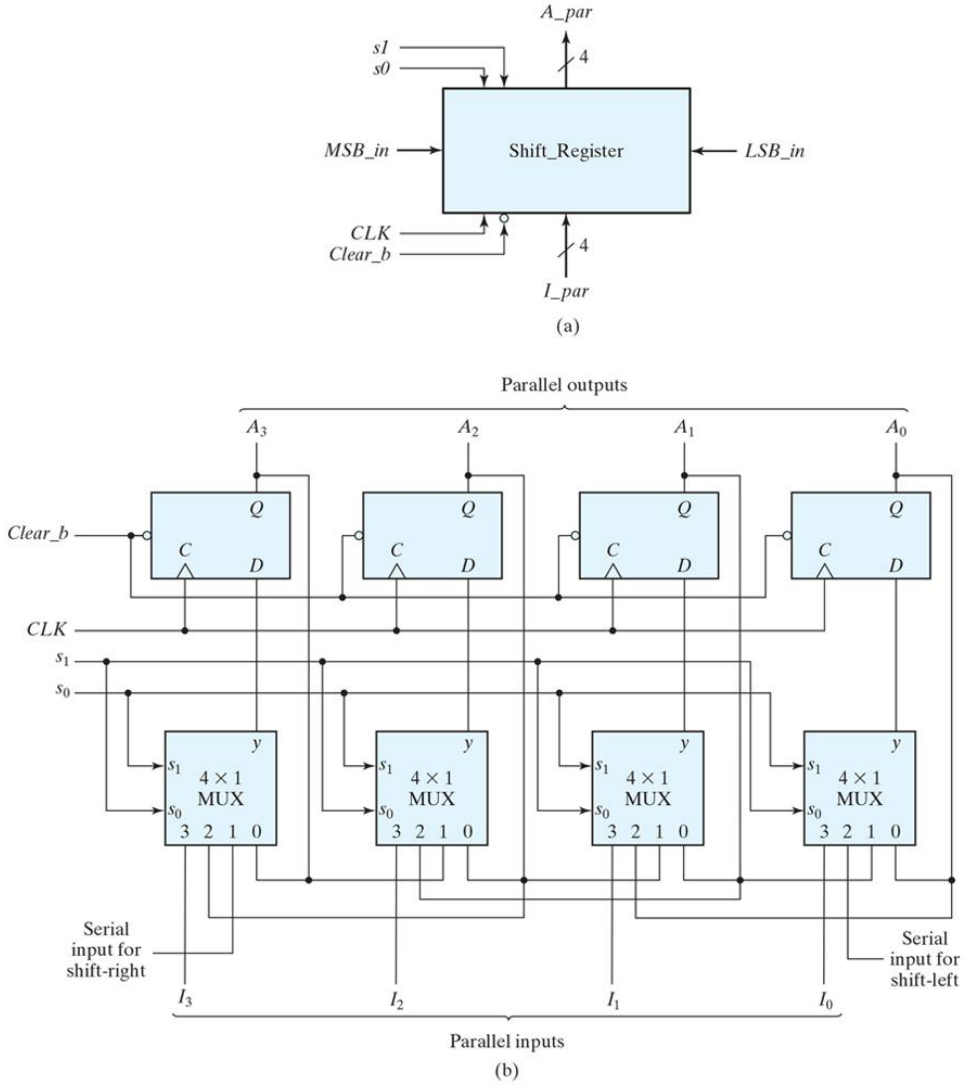
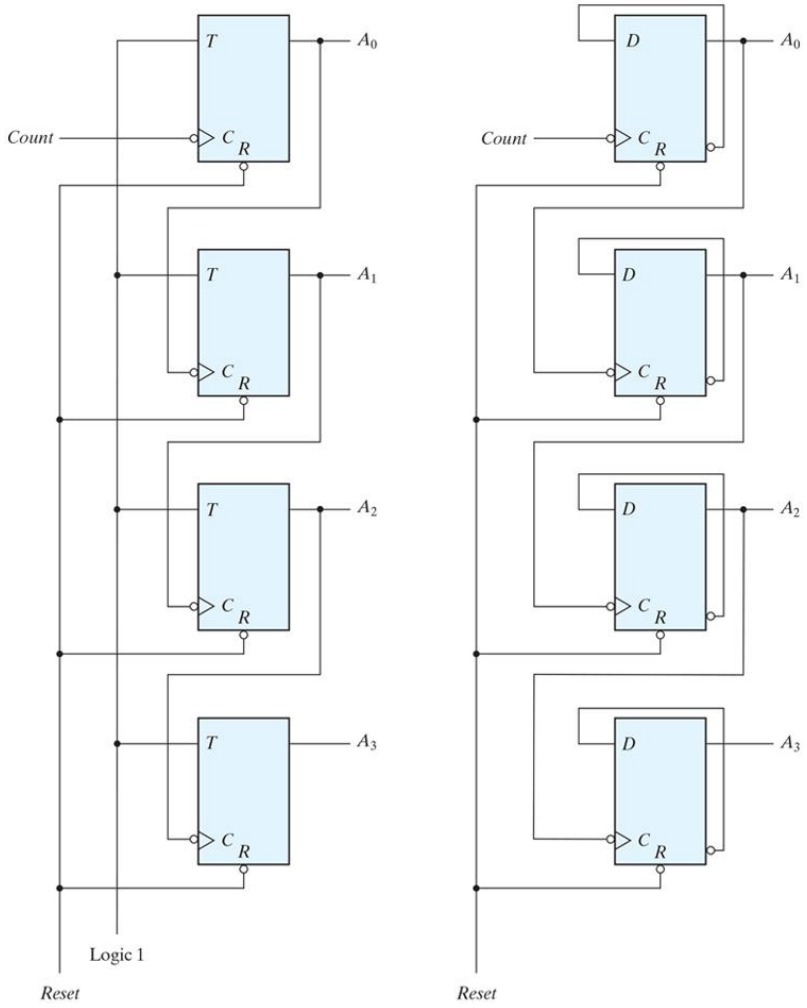


Table 6.3
Function Table for the Register of Fig. 6.7.

Mode Control		
s_1	s_0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

Figure 6.8
Four-bit binary ripple counter.



(a) With *T* flip-flops

(b) With *D* flip-flops

Pearson

Table 6.4
Binary Count Sequence.

A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0

Figure 6.9
State diagram of a decimal BCD counter.

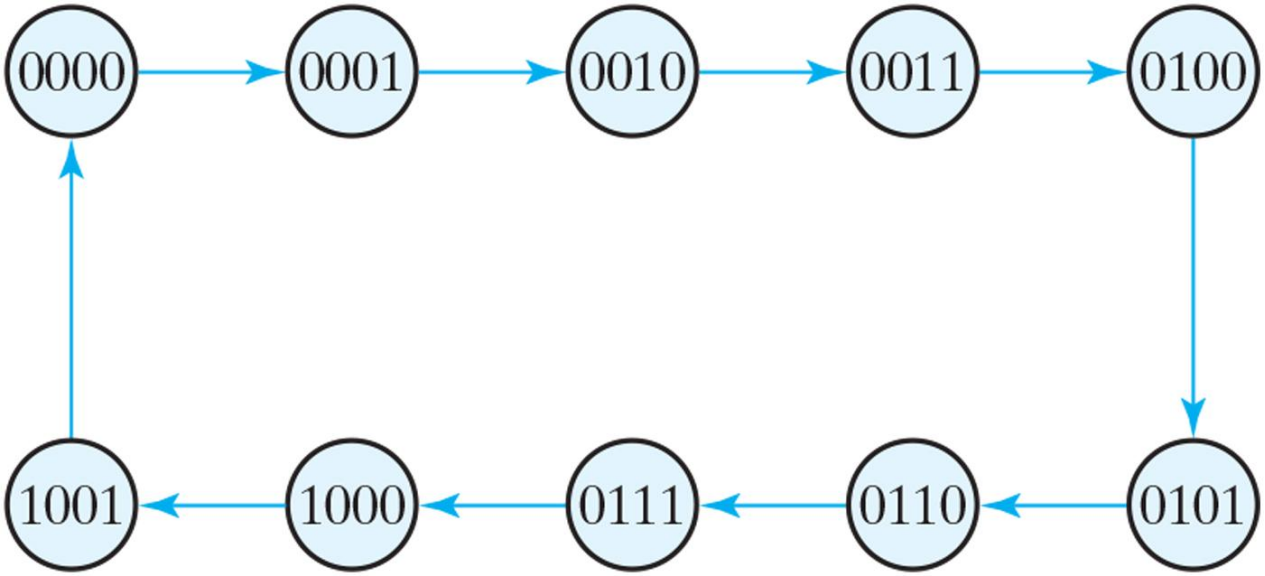


Figure 6.10
BCD ripple counter.

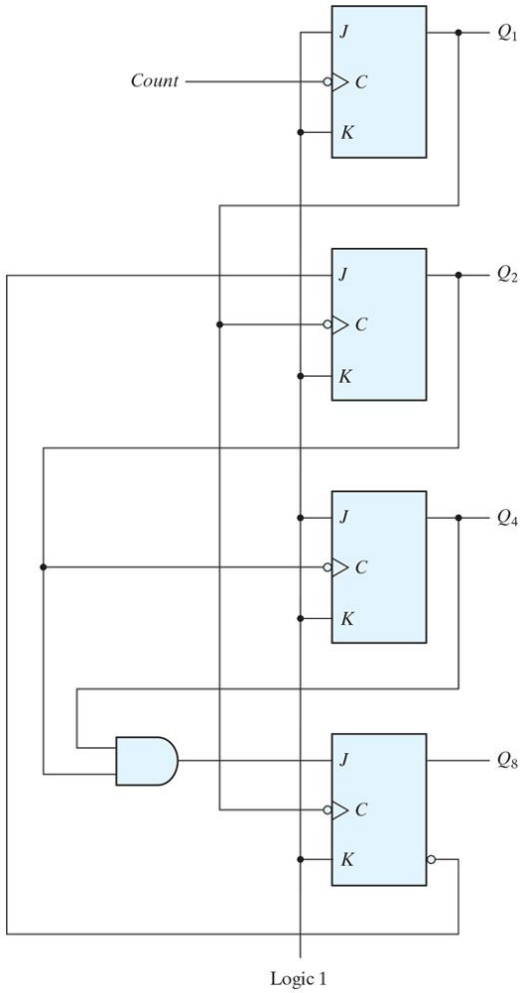


Figure 6.11
Block diagram of a three-decade decimal BCD counter.

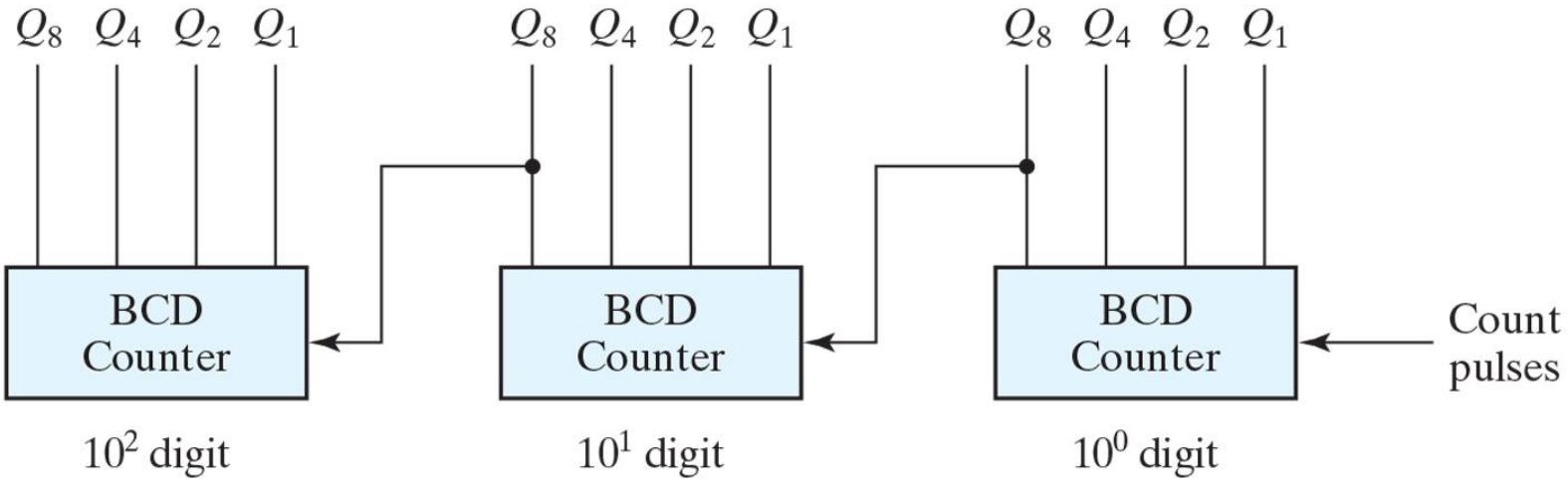


Figure 6.12
Four-bit synchronous binary counter.

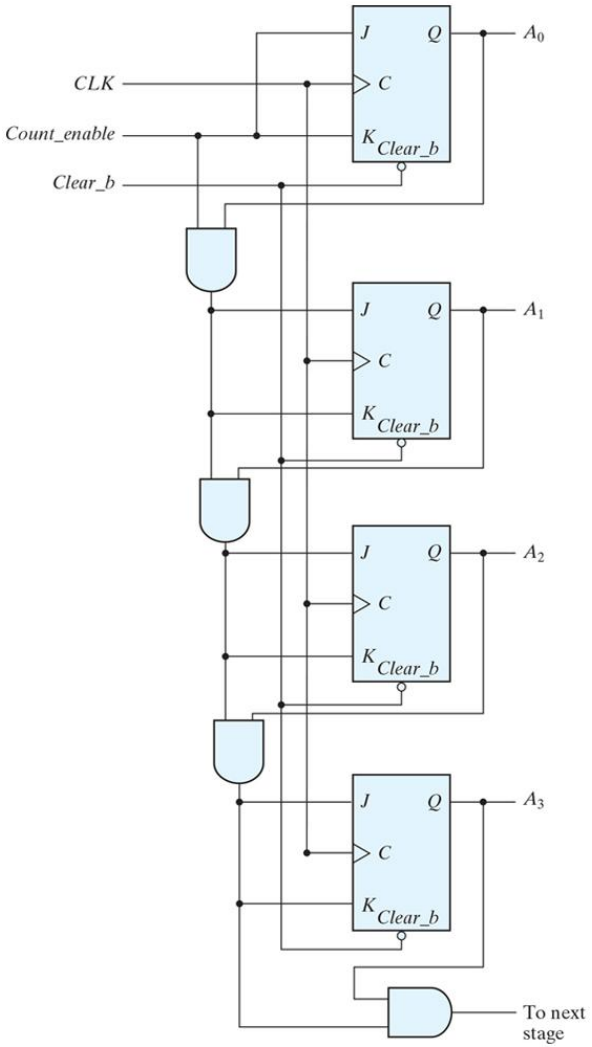


Figure 6.13
Four-bit up–down binary counter.

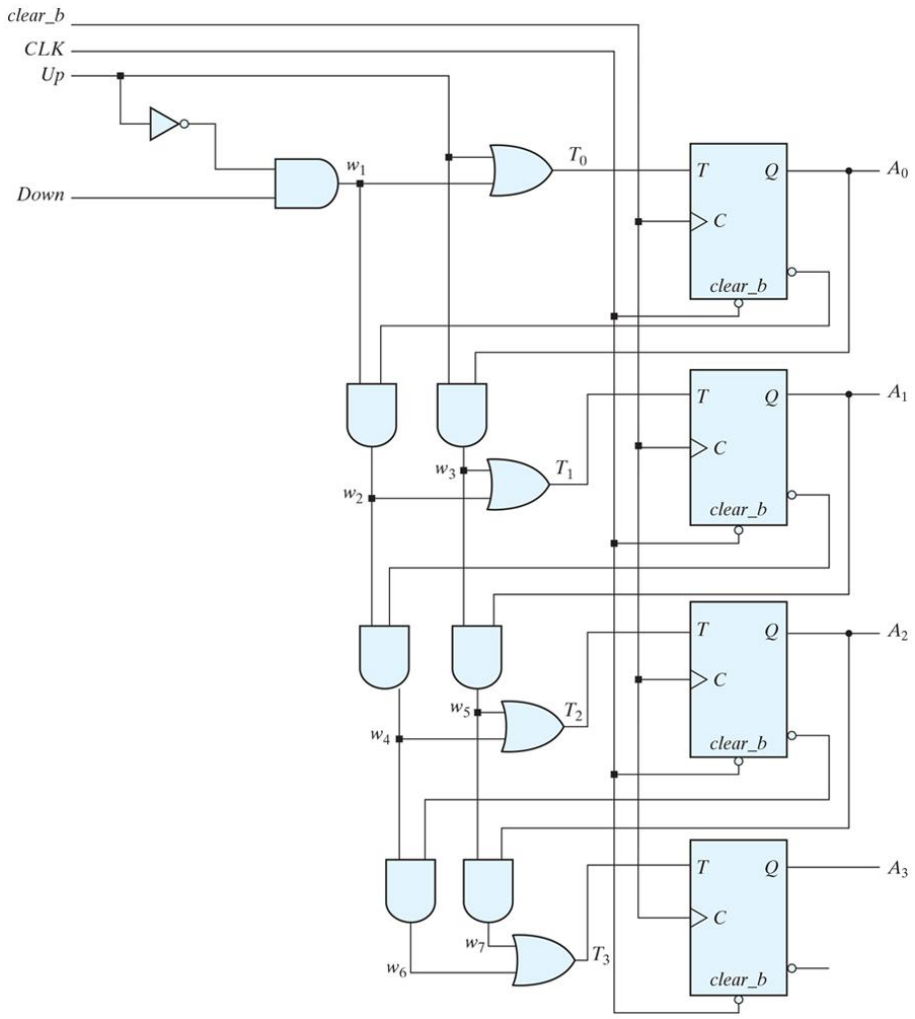


Table 6.5
State Table for BCD Counter.

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	T_{Q8}	T_Q4	T_{Q2}	T_{Q1}
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

Figure 6.14
Four-bit binary counter with parallel load.

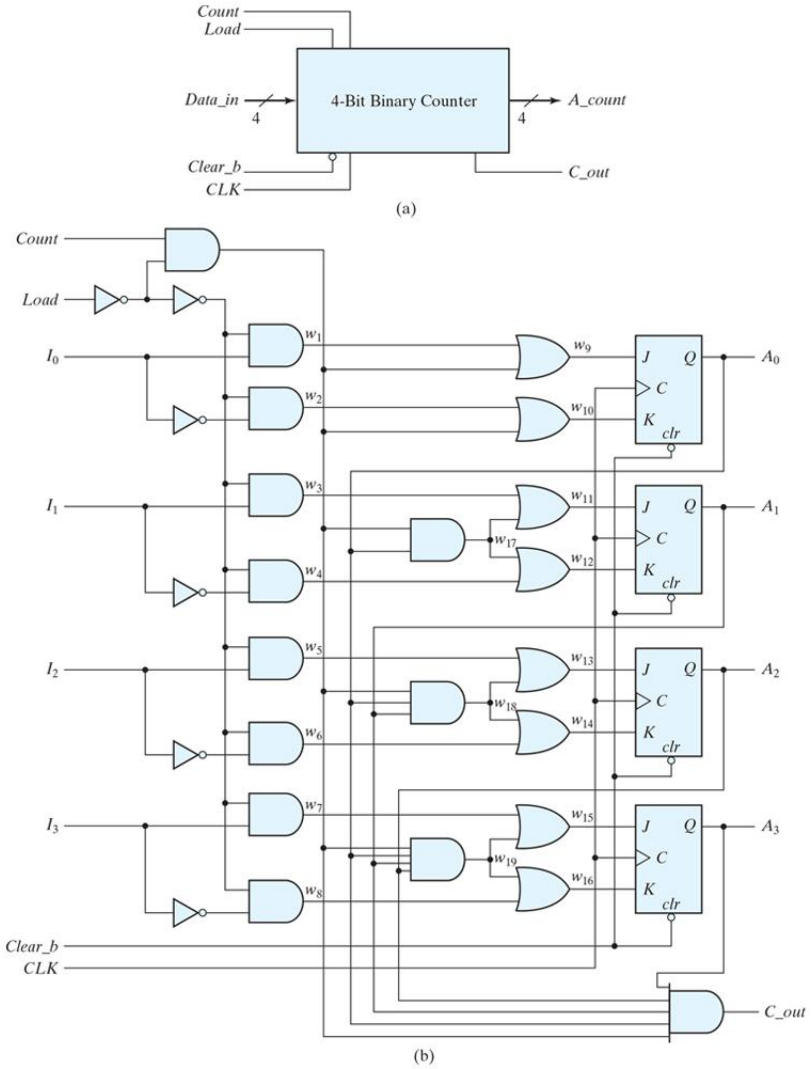


Table 6.6
Function Table for the Counter of Fig. 6.14.

Clear_b	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

Figure 6.15
Two ways to achieve a BCD counter using a counter with parallel load.

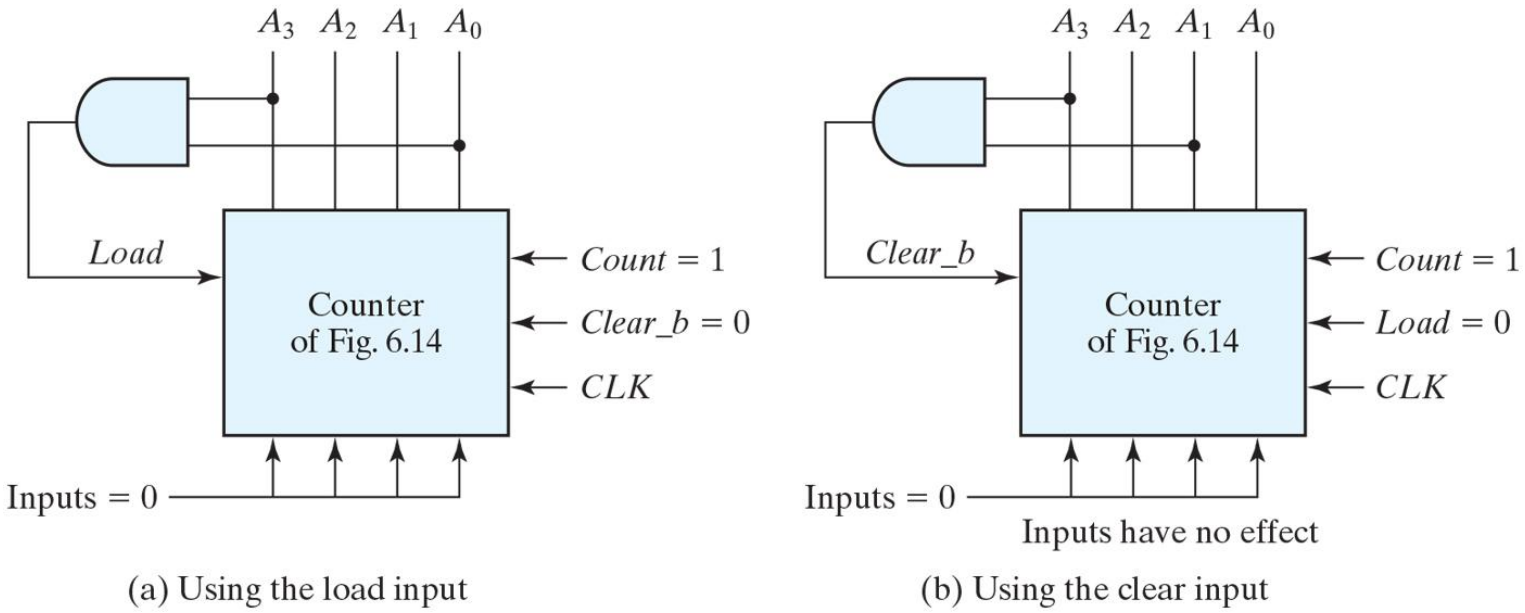
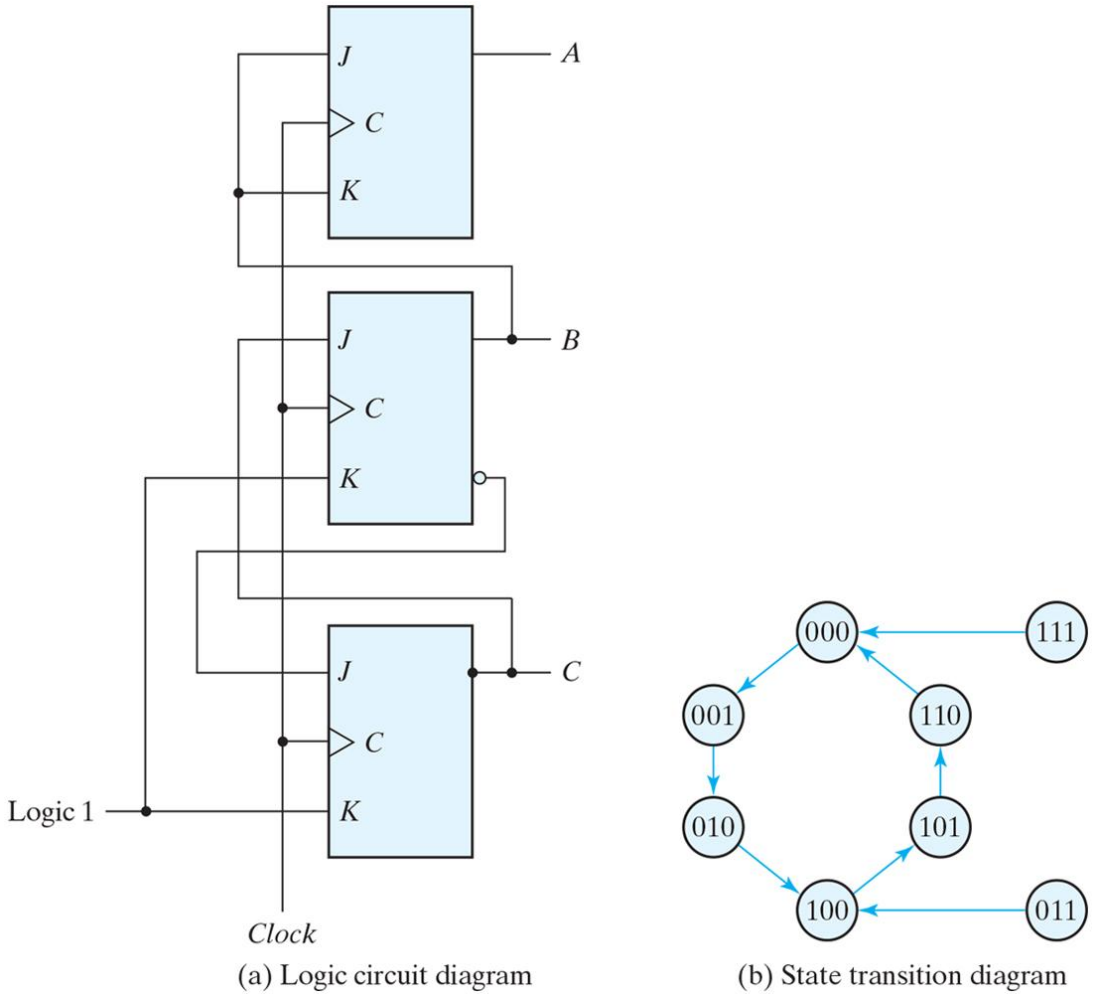


Table 6.7
State Table for Counter.

Present State			Next State			Flip-Flop Inputs					
A	*B*	*C*	*A*	*B*	*C*	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

Figure 6.16
Counter with unused states.



(a) Logic circuit diagram

(b) State transition diagram

Figure 6.17
Generation of timing signals.

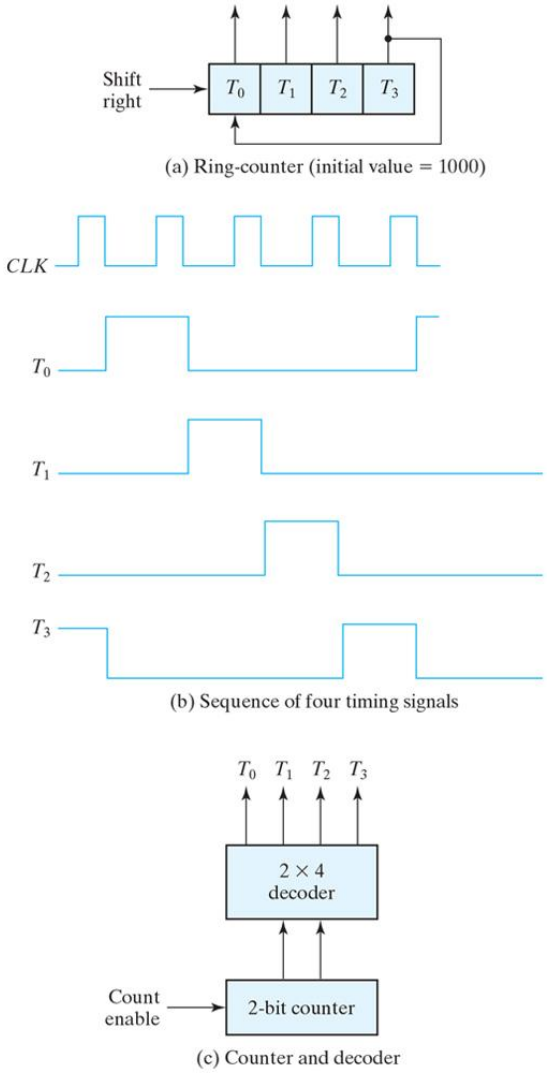
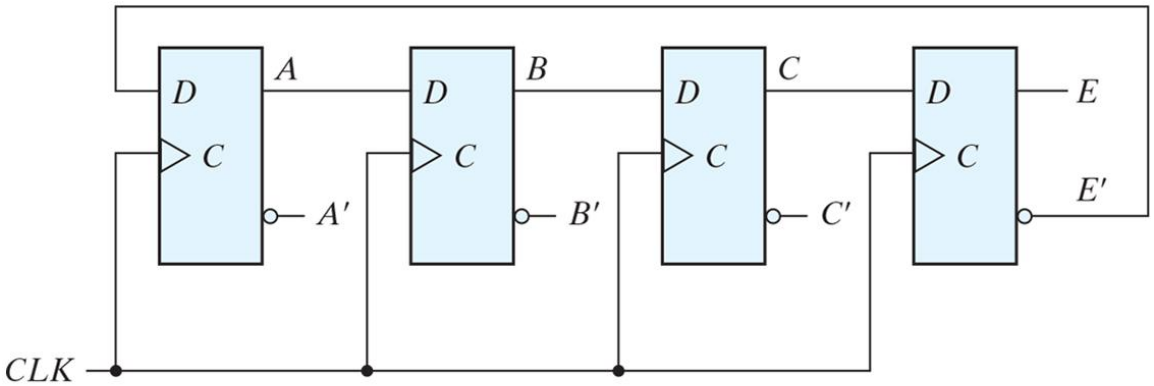


Figure 6.18
Construction of a Johnson counter.

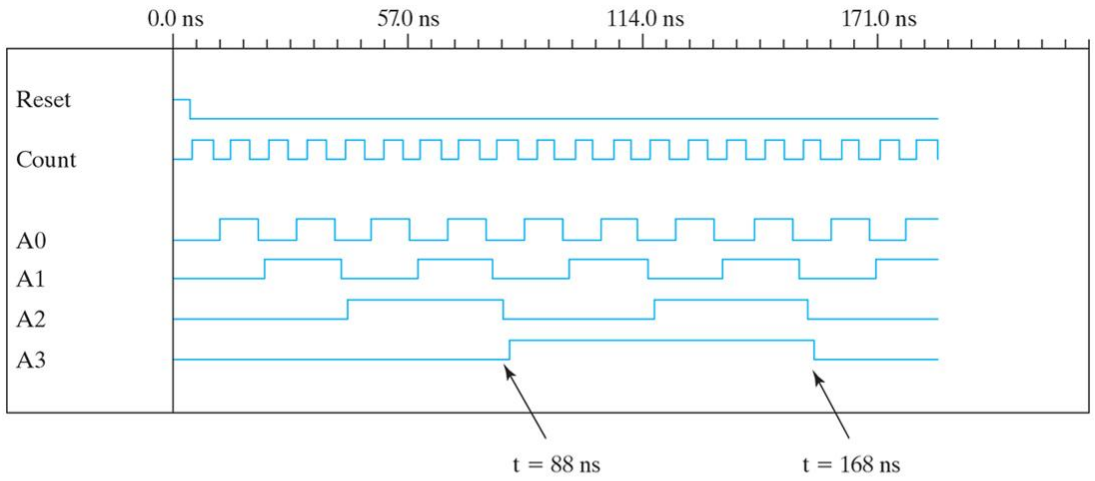


(a) Four-stage switch-tail ring counter

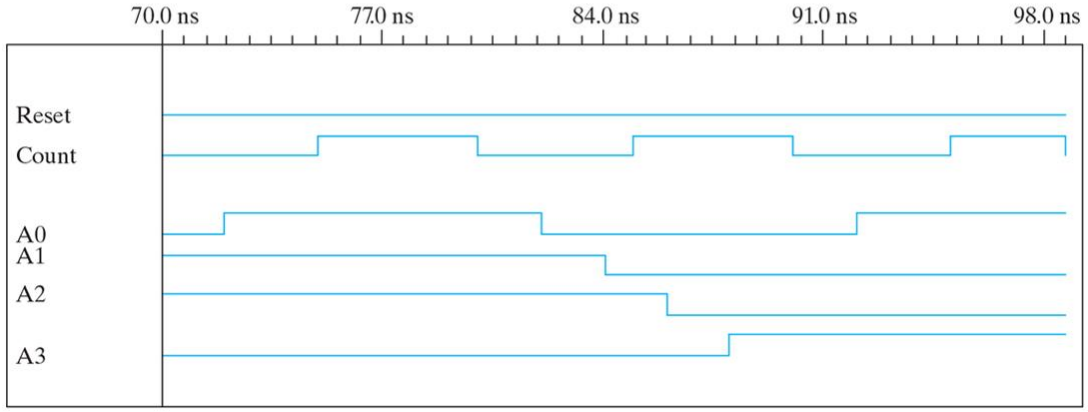
Sequence number	Flip-flop outputs				AND gate required for output
	A	*B*	*C*	*E*	
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

(b) Count sequence and required decoding

Figure 6.19
Simulation output of HDL Example 6.4.



(a) From 0 to 180 ns



(b) From 70 to 98 ns

Problem 6.7

s_1	s_0	Register Operation
0	0	No change
1	0	Complement the four outputs
0	1	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data

Figure P6.21

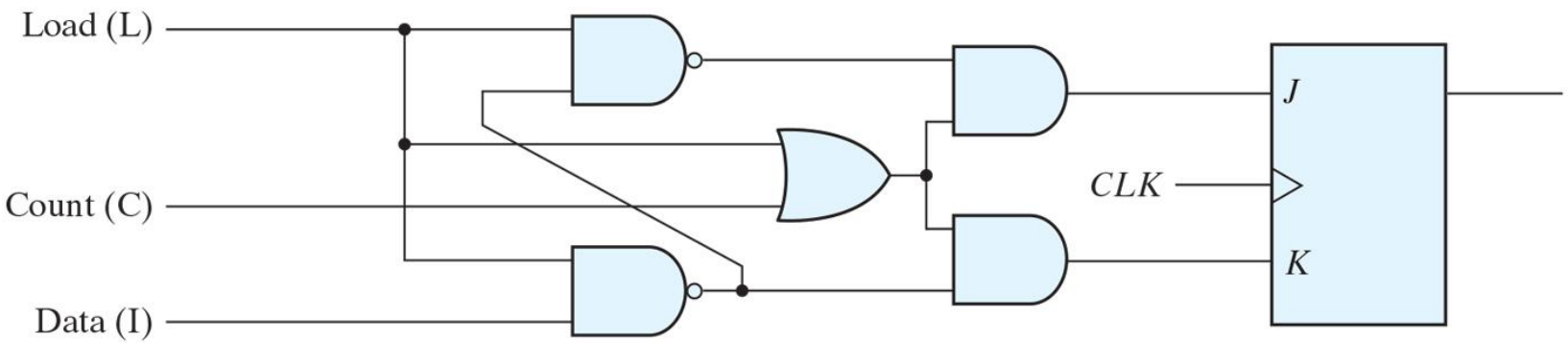


Figure P6.47
Circuit for Problem 6.47.

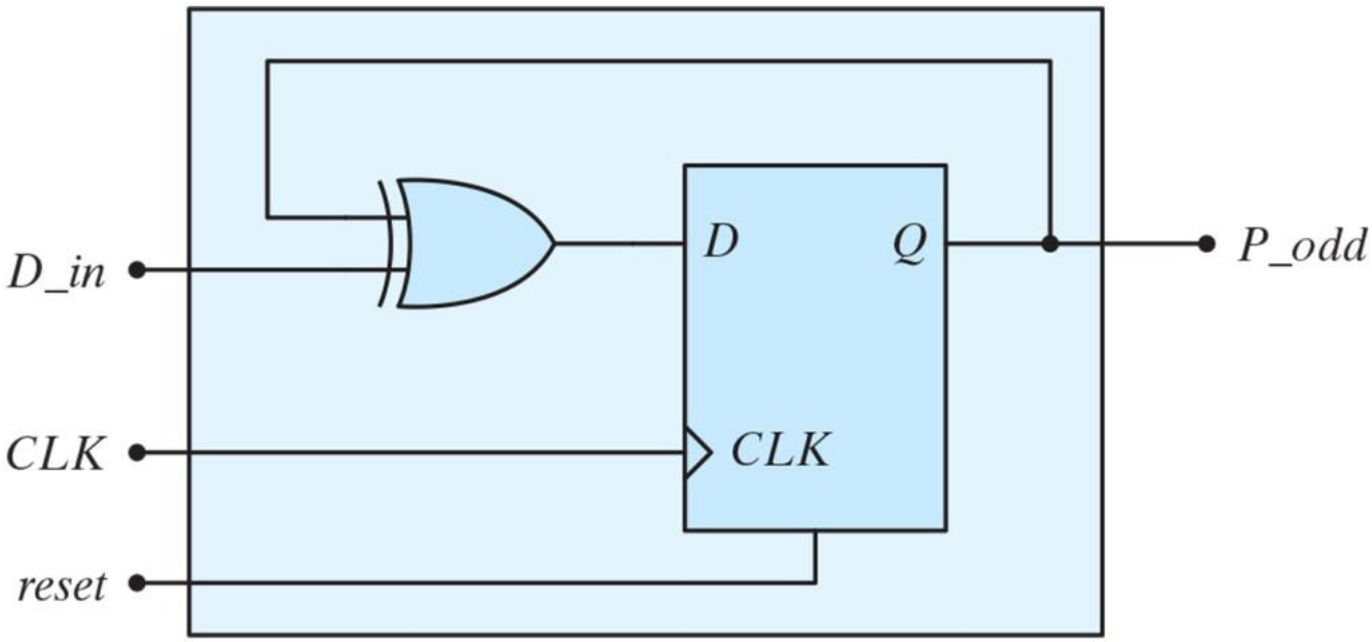


Figure P6.48
Circuit for Problem 6.48.