Today, Nov. 2nd.

Chapter 3 Gate-Level Minimization

1. 3-variable or 4-variable K-map, K-map with **don't care (X)** items
2. Implementation logical functions with **Sum of Products**, or **Products of Sum**
3. Implementation logical functions with physical gates, especially with **NAND** gates and **NOR** gates, **two-level** and **multi-level** gate implementation
4. ~~Half-Adder, Full-Adder, Look-ahead-Carry-Adder. Understand why **Carry-Look-Ahead-Adder** is faster than **Ripple-Carry-Adder**~~
5. principle of **parity check**, and its implementation with gates on page 108

Home works：

In the 5th Edition text book, go to **page 118**, please finish the following questions:

3.6 (c) (d)
3.9
3.11
3.12
3.16 (c) (d)
3.19 (b) (c)
3.21
3.22