**ECSS-E-HB-20-20A**
15 April 2016


# Space engineering

## Guidelines for electrical design and interface requirements for power supply

**ECSS Secretariat**
**ESA-ESTEC**
**Requirements & Standards Division**
**Noordwijk, The Netherlands**

**Foreword**

This Handbook is one document of the series of ECSS Documents intended to be used as supporting material for ECSS Standards in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards.

The material in this Handbook is defined in terms of description and recommendation how to organize and perform the ECSS-E-ST-20-20.

This handbook has been prepared by ECSS-E-ST-20-20 Working Group, reviewed by the ECSS Executive Secretariat and approved by the ECSS Technical Authority.

**Disclaimer**



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# Introduction

The power distribution by Latching Current Limiters, or LCLs, has been widely used in almost all European satellites for some decades as an effective way to achieve a very controlled and reliable load connection and disconnection from the satellite main bus, including power management in case of overload and load short circuit failures.

Additionally, power distribution by LCLs minimises inrush current events due to load filters charging (see section 5.7.2.3), and for this reason effectively allows the reduction of the loads filters themselves.

On the other side power distribution by LCLs has always been matter of "local" discussion and review, while no attempt has been done so far to collect all the available information in a congruent and explanatory handbook and to allow a product-oriented specification as presently done with ECSS-E-ST-20-20.

This handbook complements ECSS-E-ST-20-20, and it is directed at the same time to power system engineers, who are specifying and procuring units containing LCLs for power distribution and protection, and to power electronics design engineers, who are in charge of designing and verifying power distribution by LCLs.

For the system engineers, this document explains the detailed issues at circuit level and the impacts of the requirements for the design of LCLs.

For design engineers, this document gives insight and understanding on the rationales of the requirements on their designs.

It is important to notice that the best understanding of the topic of Power Distribution based by LCLs is achieved by the contextual reading of both the present handbook and the ECSS-E-ST-20-20.

Note that the present issue of the handbook covers electrical design and interface requirements for power distribution based on Latching Current Limiters only.

Future issues of the present handbook will cover additional power interfaces.

# 1
# Scope

In general terms, the scope of the consolidation of LCLs power distribution interface requirements in the ECSS-E-ST-20-20 and the relevant explanation in the present handbook is to allow a more recurrent approach for the specific designs offered by power unit manufacturers, at the benefit of the system integrators and of the Agency, thus ensuring:

- better quality,
- stability of performances, and
- independence of the products from specific mission targets.

A recurrent approach enables power distribution manufacturing companies to concentrate on products and a small step improvement approach that is the basis of a high quality industrial output.

In particular, the scope of the present handbook is:

- to explain the principles of operation of power distribution based on LCLs,
- to identify important issues related to LCLs, and
- to give some explanations of the requirements set up in the ECSS-E-ST-20-20 for power distribution based on LCLs, for both source and load sides.

# 2 References

| | |
|---|---|
| ECSS-S-ST-00-01 | ECSS system - Glossary of terms |
| ECSS-E-ST-20-20 | Space engineering - Electrical design and interface requirements for power supply |
| ECSS-Q-ST-30-02 | Space product assurance - Failure modes, effects (and criticality) analysis (FMEA/FMECA) |
| ECSS-Q-ST-30-11 | Space product assurance - Space product assurance, Derating – EEE components |
| ESA PSS-02-10 Vol.1 Issue 1, Nov. 1992 | Power standard |
| IEEE CFP13APE-USB (2013) | MOSFET Gate Open Failure Analysis in Power Electronics, IEEE Applied Power Electronics Conference and Exposition, Long Beach, California, 17-21 March 2013, pp. 189-196 (reported as Annex G in the present HB) |
| ESA SP-719 (2014) | Approach to design for stability a system comprising a non-ideal current source and a generic load, 10th European Space Power Conference, Noordwijkerhout, The Netherlands, 13-17 May 2014 (reported as Annex H in the present HB) |
| ESA SP-719 (2014) | LCL current control loop stability design, 10th European Space Power Conference, Noordwijkerhout, The Netherlands, 13-17 May 2014 (reported as Annex I in the present HB) |

# 3
# Terms, definitions and abbreviated terms

## 3.1 Terms from other documents

a. For the purpose of this document, the terms and definitions from ECSS-S-ST-00-01 apply, in particular for the following terms:

1. **redundancy**
2. **active redundancy**
3. **hot redundancy**
4. **cold redundancy**
5. **fault**
6. **fault tolerance**

b. For the purpose of this document, the terms and definitions from ECSS-E-ST-20-20 apply.

## 3.2 Abbreviated terms

For the purpose of this document, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

| Abbreviation | Meaning |
|---|---|
| **A** | analysis |
| **BJT** | bipolar junction transistor |
| **EOL** | end-of-life |
| **ESTEC** | European Space Technology and Research Centre |
| **I** | inspection |
| **LCL** | latching current limiter |
| **MFET** | MOS field effect transistor |
| **MOS** | metal oxide semiconductor |
| **OVP** | overvoltage protection |
| **PCDU** | power conditioning and distribution unit |
| **PDU** | power distribution unit |
| **RDSON** | drain source resistance in on state (for MFET) |
| **RLCL** | retriggerable LCL |

| Abbreviation | Meaning |
|---|---|
| **RoD** | review of design |
| **S3R** | sequential unit switching regulator |
| **SOA** | safe operating area |
| **SPFF** | single point failure free |
| **T** | test |
| **TWTA** | travelling wave tube amplifier |
| **UVP** | undervoltage protection |
| **WCA** | worst case analysis |

# 4 Explanations

## 4.1 Explanatory note

The present handbook refers to the electrical interface requirements defined in the ECSS-E-ST-20-20.

The ECSS-E-ST-20-20 requirements are referred to in this handbook by using following convention and are indicated in *italic font*:

[requirement number] feature - sub-feature.

For example:

Requirement 5.2.3.2.1a.

Clause Heading 3 title = "Current Limitation Section"

Clause Heading 4 title = "Switch element, positions"

→ *[5.2.3.2.1.a.] Current Limitation Section – Switch element, position*

See also, for more information, Annex A of ECSS-E-ST-20-20.

In addition:

- each requirement (i.e. any statement containing a "shall" in the standard) is marked with **red text**.
- each recommendation (i.e. any statement containing a "should" in the standard) is marked with **blue text**.

Keywords are highlighted in **bold**. A keyword is a word that either has a special meaning in the contest of the chapter in which it appears, or highlight a concept.

## 4.2 How to use this document

For the best utilisation of this document, it is recommended to print it together with the ECSS-E-ST-20-20 and to consult Annex A, Annex B and Annex C separately and at the same time when reading the document core.

In this way, the discussion and the rationale explanation of each individual requirement are clearer and there is the minimum risk of misunderstanding.

# 5 Power distribution by LCLs/RLCLs

## 5.1 General architecture

A generic architecture for a Latching Current Limiter, or LCL, is shown in Figure 5-1.

Note that the diagram in Figure 5-1 is given only as a reference, without losing generality, and some of the features thereby reported can be actually realised differently.

Common LCL design alternatives are discussed further in section 5.2.

Without losing in generality, the general architecture is hereby explained for the distribution by LCLs.

For the specific case of Retriggerable Latching Current Limiter, or RLCL, refer to section 5.3.

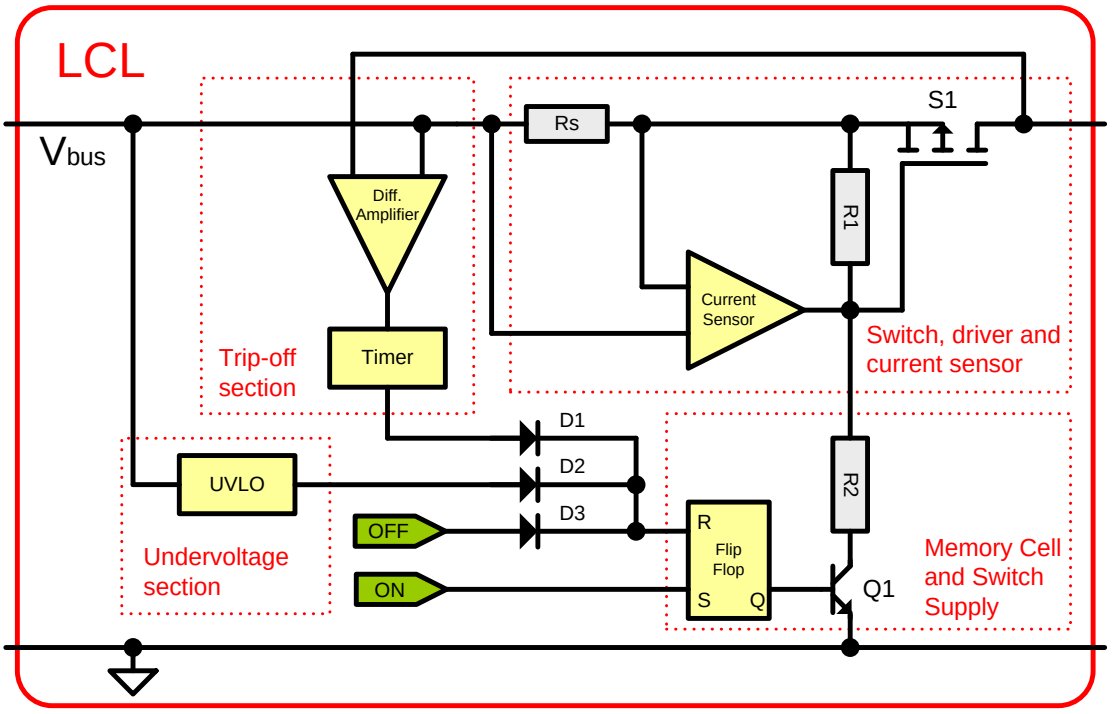



**Figure 5-1: LCL generic block diagram**

The Latching Current Limiter, or LCL, is a switch-able, latching, retriggerable over-current/overload protection placed between a power source and the relevant load.

The LCL can be commanded ON and OFF and its status is normally latched by a relevant memory cell.

Typically, an LCL presents a minimum residual resistance between power input and power output during nominal operation (i.e. when the switch is commanded closed).

In case of an overload, e.g. when the load current request exceeds a prefixed threshold, the LCL enters current limitation and a time counter is activated.

If the overload condition persists for a given time duration (called trip-off time), the time counter commands the LCL OFF.

Normally there should be an external command activation to reset the LCL into its original ON state.

Note that the LCL identifies a function: therefore it is independent from the number of power switches or MOSFETs used to implement the function itself.

The functionality of the LCL, in relation to the block diagram in Figure 5-1, is detailed in section 5.2.

## 5.2 Functionality

### 5.2.1 Overview

The basic elements of an LCL are the following:

- the section containing **the switch, the driver and the current sensor**,
- the section relevant to the **trip-off** timer,
- the section relevant to the **memory cell and switch supply** section,
- the **undervoltage protection** (UVP) section,
- the **auxiliary supply** section (not shown in Figure 5-1), and
- the **telemetry** section.

Each basic element is discussed in a dedicated section in the present chapter.

### 5.2.2 Switch, driver and current sensor

The switch is generally constituted by an enhancement MFET, either P or N channel, even though other devices could be used (for example, bipolar transistors for lower current applications).

It is called “switch” in relation to the switching capability of the LCL (e.g. it can apply or remove power from the load), but actually it operates either in ohmic “ON” mode or in linear mode according to the load current being below or above a specified threshold.

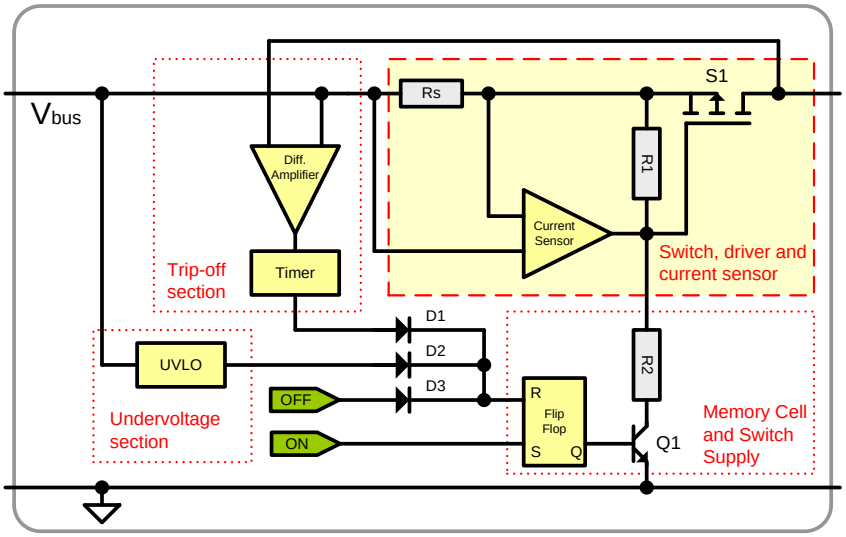



**Figure 5-2: Switch, driver and current sensor**

It is to point out that the **switch** and the **current sensing resistor** (or sensing element), is not placed on the power line connected to ground: this is a **mandatory** feature if the LCL power output is distributed outside the unit containing the LCL itself (as it happens on the main bus protected outputs in the power system Distribution Unit or PDU). The reason is that the power output lines need to be protected versus accidental short circuit to ground due to failures in the connectors, in the harness, or in the supplied load.

*[5.2.3.2.1.a] Current limitation section – Switch element, position*

*[5.2.3.3.1.a] Current limitation section – Current sensing element, position*

The relevant **switch driver** is usually inherently included in the same circuit implementing the **current sensing** feature: when the LCL is commanded ON, the switch is normally in ohmic "ON" mode and presents either a low ohmic characteristic (for MFETs, ON channel resistance, or $R_{DSON}$) or anyhow a low voltage drop (as in the case of a BJT switch).

*[5.4.5.1.1.a], [5.4.5.1.1.b], [5.4.5.1.1.c] Voltage drop – Voltage drop*

In case of an overload, it is necessary that the switch is **quickly** brought outside ohmic "ON" mode condition and into linear one, in order to reduce the relevant surge current conditions (causing also relevant system EMC conducted and radiated disturbances) and the switch power/thermal stress.

The speed of response is function of the MFET gate charge and it is a figure of merit of the current sensing circuit.

*[5.4.1.1.1.a], [5.4.1.1.1.b], [5.4.1.1.1.c], [5.4.1.1.1.d], [5.4.1.1.1.e], [5.4.1.1.1.f] Overall requirements - Current overshoot*

The current sensor is in charge of regulating the current in overload situation, by modulating the gate voltage of the switch: the accuracy of the gate voltage is function of the current sensing circuit and the relevant reference voltages used in the design.

*[5.2.1.1.1.a], [5.2.1.1.1.b] HLCL/LCL class – HLCL/LCL class*

*[5.2.2.1.1.a] RLCL class – RLCL class*

*[5.2.3.1.1.a] Current limitation section - Range*

In case more than one MOSFET is used, it is important to have a dedicated current control per MOSFET to ensure current sharing in limitation.

If two or more MOSFETs are used in parallel with one single limiter, each MOSFET should be able to handle the total limitation current.

The current sensor is also sometimes used to derive a current telemetry signal, which is normally referred to ground.

An important observation is that the LCL/RLCL needs to contain a provision to circulate (free-wheel) the current circulating in the load (or harness) inductance, when the LCL/RLCL is either commanded OFF or it opens the line after an overload.

This is normally achieved by placing an anti-parallel diode to the output of the LCL itself.

*[5.2.7.7.1.a] Conditions at start-up/switch-off – switch-off*

## 5.2.3 Trip-off section

### 5.2.3.1 Overview

The LCL trip-off section is in charge to start the "counting" of the overload condition duration, and to set the LCL status to OFF after the relevant trip-off time has elapsed.

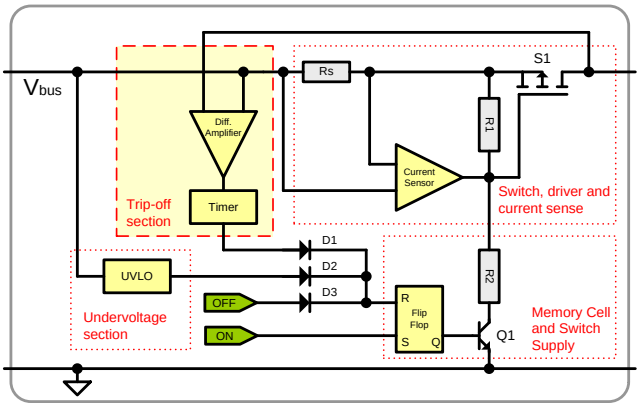



**Figure 5-3: Trip-off section**

*[5.2.1.1.1.a], [5.2.1.1.1.b] LCL/HLCL class – LCL/HLCL class*

NOTE Specifically minimum and maximum trip-off time.

*[5.2.2.1.1.a] RLCL class – RLCL class*

NOTE Specifically minimum and maximum trip-off time.

*[5.2.4.1.1.a] Trip-OFF section - Range*

It can be triggered by a signal coming from the current sense section, which identifies that the current limitation has been entered as a consequence of an overload, or by the differential reading of the voltage across the switch (as shown in Figure 5-1).

When the differential voltage across the switch is over a prefixed threshold, a timer is started to count the trip-off time.

The timer is usually implemented by means of a simple resistive-capacitive (RC) element in combination with a comparator, or a digital counter/comparator.

If the timer is implemented by a RC low-pass filter, the voltage across the capacitor mimics the temperature developed at the junction of the LCL MFET switch under current limiting conditions.

To understand this concept, it is useful to think of the electrical equivalence of a thermal network (see following Table 5-1 and Figure 5-4).

**Table 5-1: Thermal electrical network equivalence**

| Electrical domain | | **Thermal domain** | |
|---|---|---|---|
| Current | A | Power | W |
| Voltage | V | Temperature | °C |
| Resistance | Ohm | Thermal Resistance | °C/W |
| Capacity | F | Thermal Capacity | J/°C |

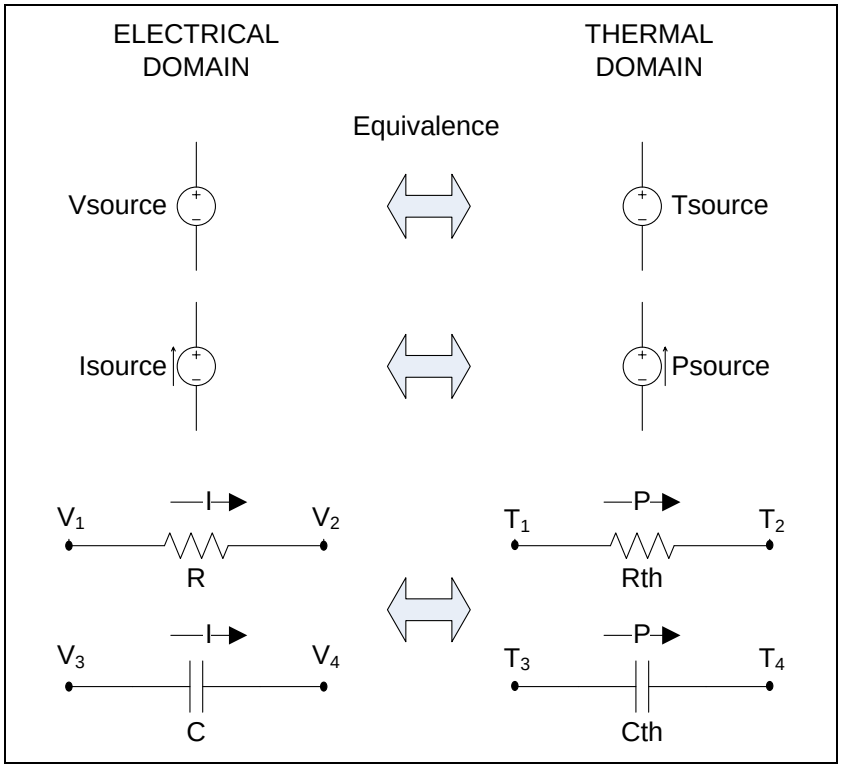



**Figure 5-4: Thermal electrical network equivalence**

When the timer predefined trip-off time duration is elapsed, the LCL is switched OFF.

A time diagram illustrating the qualitative current profile of an overload event is shown in Figure 5-5.

We can identify two different modes of operation for the current limitation:

a. the first current limitation mode occurs when an LCL is enabled with a command and then starts to charge the input filter capacitance in the load (Figure 5-6, right). In this case a negligible overshoot in the current profile can be expected and achieved.

b. the second case (Figure 5-6, left) is when the LCL is enabled and a sudden overload like a short circuit occurs (in this case, a larger current overshoot can occur).

The specification and understanding of these two cases are important to clarify when compatibility tests and analyses are made on real hardware at equipment level.

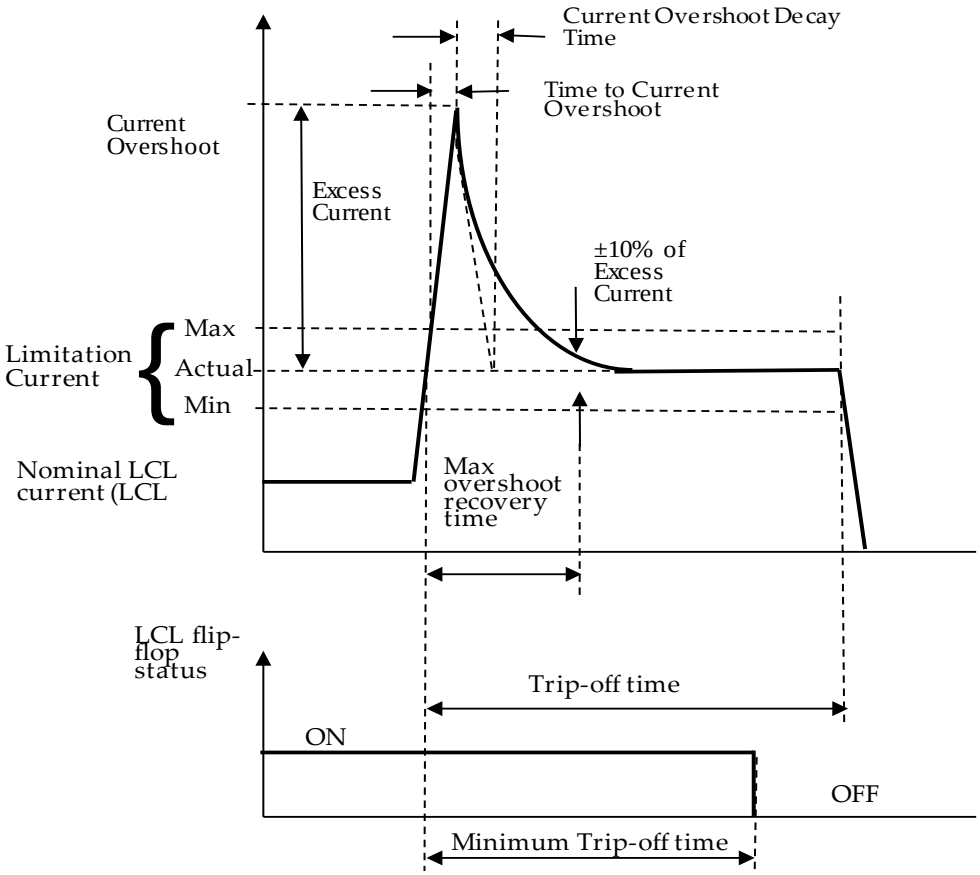



**Figure 5-5: LCL overload timing diagram**

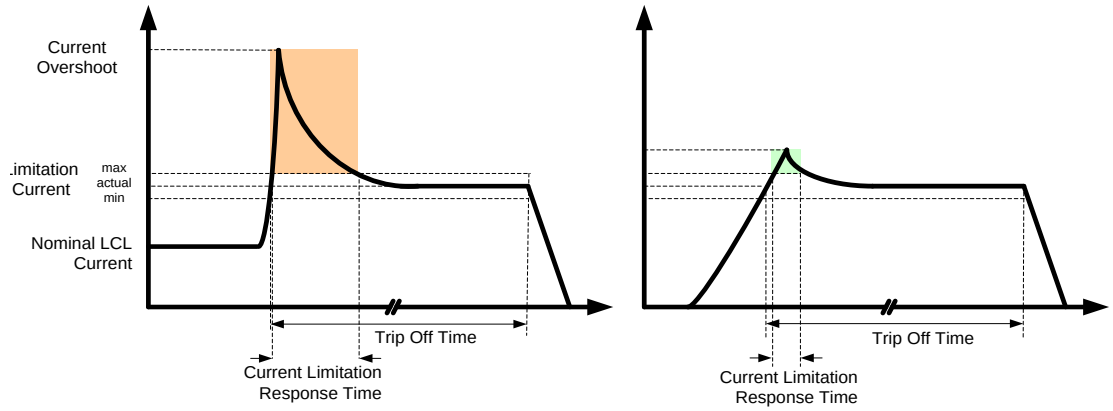



**Figure 5-6: Comparison between nominal turn ON (right) and overload caused by a short circuit (left)**

With respect to Figure 5-5, the minimum trip-off time is evaluated with respect to the flipping action of the relevant LCL memory cell (state flip-flop) and not with respect to the actual decay of the current from limitation value to zero: in fact, and depending on the adopted design solution, there can be a non-negligible delay before the LCL delivered current decays to zero and after the LCL memory cell has been commanded OFF by the relevant trip-off section.

This specific issue needs indeed a careful consideration during LCL design phase.

#### 5.2.3.2 Verification

In case the trip-off is triggered by the differential voltage across the switch it should be verified that the switch dissipation/temperature is acceptable when the LCL is in limitation but the differential voltage threshold $V_{diff}$ is not crossed (considering the worst case threshold value).

In this case the switch can continuously dissipate $V_{diff\_max}$ x $I_{limitation\_max}$.

### 5.2.4 Memory cell and switch supply section

The memory cell and switch supply section contains the "memory" of the LCL, which is by definition a latching function and therefore is characterised by two states (ON and OFF).

The circuit implementing this section is also designed to provide a predefined LCL status at start-up (e.g. when the bus voltage is ramped up).

The predefined LCL status at start-up should be OFF (while it is ON for a RLCL – see section 5.3).

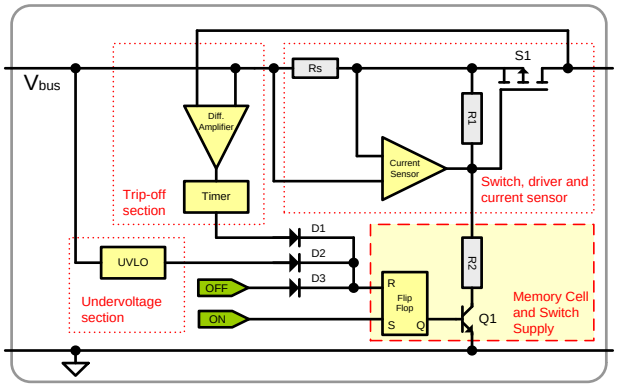



**Figure 5-7 : Memory cell and switch supply section**

The memory cell usually provides the signal enabling the supply of the switch, current sensor and switch driver that normally are referred at the hot side for the reasons explained in section 5.2.2.

The design of the switch supply is done in a way that the rate of rise (respectively fall) of the output current is within the specified limits during power up after command ON application (respectively power down after command OFF application).

The reasons to limit the current slope are essentially for reducing EMC interference (both conducted and radiated) and to have clear, reproducible conditions to ensure that no unwanted status change is caused by LCL activation or deactivation (especially after satellite integration).

*[5.4.2.1.1.a] Start-up / switch-off requirements - Start-up current rate*

*[5.4.2.2.1.a] Start-up / switch-off requirements - Switch-off current rate*

Increasing component densities and number of layers on PCBs make cross talk issues more and more difficult to deal with. Cross talk can occur between tracks when high dv/dt or di/dt are present and the distance between tracks is small. Typically, the design of the PCB should guarantee that power tracks, driver and current sense section tracks and sensitive signal tracks are sufficiently separated, such as any unwanted behaviour (such as spurious protection activation) is avoided.

### 5.2.5 Undervoltage protection section

The undervoltage protection section, or UVP, is provided to avoid the LCL from being switched ON when the MB voltage is below a critical threshold, and to switch it OFF in case of an abnormal low value of the MB voltage.

By switching the LCL OFF, the load is disconnected from the bus automatically: in this case, the bus itself can restore its nominal value in case the reason for the undervoltage events is a power deficit between the source capability and the load demand.

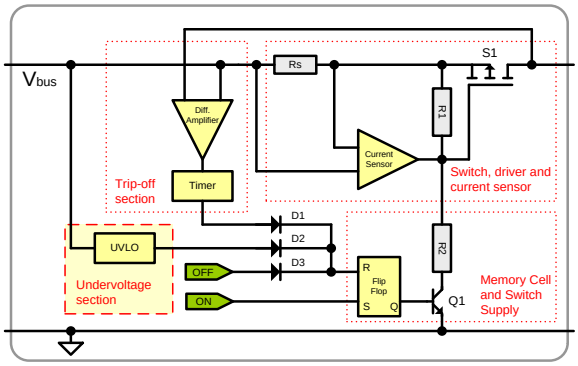



**Figure 5-8 : Undervoltage protection section**

Usually, when LCLs are used in the main bus power distribution, the UVP feature is used as the last resort to recover the bus to its nominal range (while higher main bus voltage thresholds for load shedding are usually managed by the on-board computer and software).

It is to point out that the UVP is also needed to ensure that no load enters unpredictable operation or reaction due to abnormally low power supply voltage.

*[5.2.5.1.1.a] Undervoltage protection section - provision*

The normal functioning of the LCL UVP is to operate on the relevant memory cell, e.g. to command the LCL in OFF state, in a way that an external command is needed to switch it ON again.

This is the normal implementation to avoid an uncontrolled "hiccup" mode of operation due to bus overload conditions: if the UVP is not latching, and a bus overload occurs, the bus voltage decreases, the UVP disables the LCL and therefore removes the overload, the bus voltage increases to its nominal range, the UVP becomes inactive and the overload condition reappears, etc.

*[5.4.3.1.1.a] UV protection - Switch-off threshold, regulated bus*

*[5.4.3.2.1.a] UV protection - Switch-off threshold, unregulated bus*

*[5.4.4.1.1.a] Switch-on capability - Enable ON threshold Voltage, regulated bus*

*[5.4.4.2.1.a] Switch-on capability - Enable ON threshold Voltage, unregulated bus*

The specified ranges for UVP switch-off threshold and LCL enable ON threshold voltages are intended as the envelope that the standard product of a power subsystem manufacturer need to be able to offer. The actual threshold values are normally established based on the specific mission needs.

For unregulated bus case, it is definitively necessary to provide the UVP with hysteresis to avoid uncontrolled "hiccup" mode for RLCLs or for LCLs that are not latched OFF after a trip-off event, while on a regulated bus the normal configuration is just to switch-off the LCL once the switch-off threshold is reached (and therefore it might not be necessary to implement a relevant hysteresis).

*[5.2.5.2.1.a], [5.2.5.2.1.b] Undervoltage protection section - unregulated bus case*

*[5.4.3.5.1.a] UV protection – UV protection hysteresis*

To avoid that the UVP is triggered by noise or by bus voltage transients, some noise immunity is implemented. The specified noise immunity value is usually not critical.

The generic UVP timing diagram, explaining the relevant noise immunity requirements and UVP operation, is given in Figure 5-9.

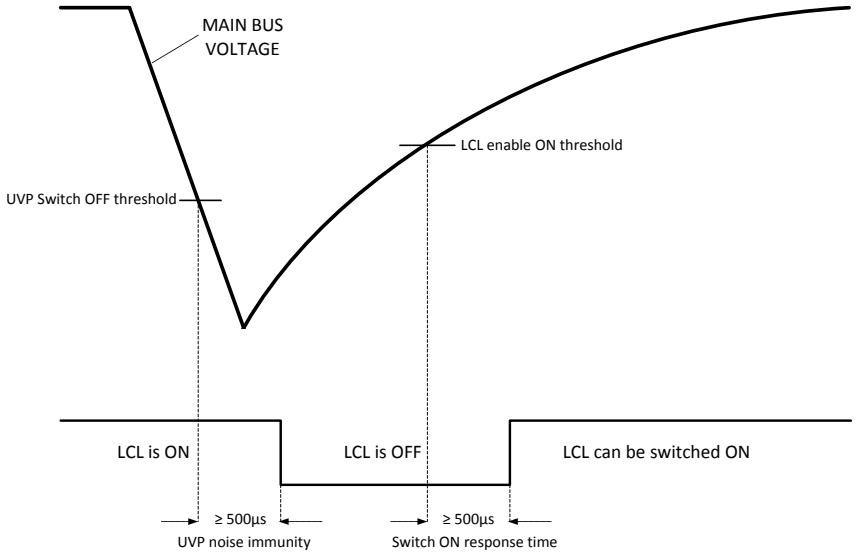



**Figure 5-9, UVP timing diagram**

In any case, the UVP activation timing is also of importance. A minimum activation delay is necessary at least for regulated buses, to avoid spurious switch-off in case of transients. In addition, at bus recovery, some noise immunity is also considered. The behaviour of the system is analysed considering that some LCL could have been tripped OFF by UVP and others not (depending on the bus transient).

*[5.4.3.3.1.a] UV protection - UV protection noise immunity*

*[5.4.3.4.1.a] UV protection - UV protection noise immunity, verification*

*[5.4.4.3.1.a] Switch-on capability – Switch-on response time, value*

*[5.4.4.4.1.a] Switch-on capability – Switch-on response time, verification*

The UVP feature is sometimes proposed as a **centralised** function (i.e. serving many LCLs) in addition or opposed to a **distributed** function, (i.e. local to each individual LCL).

In this case, a centralised UVP detector sends a command OFF to a number of LCLs.

If centralised, the UVP needs to be implemented as a Single Point Failure Free (SPFF) feature, e.g. no single failure should cause the deactivation of all the served LCLs. The reason is that even a non-permanent failure could happen in a critical operational time of the spacecraft and induce a heavy or catastrophic consequence. This is why cold redundant circuits are generally not preferred for this function.

*[5.2.5.3.1.a] Undervoltage protection section - Centralised protection*

The centralised UVP protection is more critical and risky than the decentralised one, and the relevant advantage in terms of components used must be traded against all necessary redundancies and features like majority voting circuits.

## 5.2.6 Auxiliary supply section

The auxiliary supply section (not shown in Figure 5-1) is dedicated to the supply of the LCL functions.

Some of the LCL functions (typically, the current sensor and switch driver) are usually self-supplied by the bus voltage, at least for voltages up to 50V.

The other functions normally require one or more supply lines that can be **locally** derived from the LCL power input lines by means of dedicated power supplies, or could be **centralised**, e.g. serving many LCLs (even though centralisation normally increase the chances of common failure paths and therefore it could be less appealing).

In this case, the auxiliary power supplies (in active redundancy) are normally implemented as a Single Point Failure Free (SPFF) feature, e.g. no single failure causes the deactivation of all the served LCLs.

## 5.2.7 Telemetry section

### 5.2.7.1 Status telemetry

The LCL status is an important telemetry information: combined with the current telemetry (see section 5.2.7.2), it can be used to determine if failures are present in the power subsystem or in the load, and allow debugging and isolation of failures in flight.

The detailed explanation of the proposed ECSS-E-ST-20-20 requirements is presented in section 5.7.3.5: the proper definition of what the status signal represents allows the complete understanding of possible failure modes and allows a straight forward fault detection and recovery by the satellite operator.

### 5.2.7.2 Current telemetry

#### 5.2.7.2.1 Overview

The current telemetry provides a low-level signal proportional to the current flowing on the hot distribution line of the LCL/RLCL.

The current telemetry is provided for main bus distribution, in order to give the satellite operator the information of the consumption of the relevant load.

*[5.2.8.2.1.a] Telemetry section - Current telemetry*

The current telemetry normally provides a full-scale reading up to the LCL/RLCL nominal limitation current, is linear and comes with a specified accuracy.

*[5.2.8.3.1.a] Telemetry section - Current telemetry, full scale reading*

*[5.2.8.4.1.a] Telemetry section - Current telemetry, linearity and accuracy*

The current telemetry meets a maximum offset specification and it is possible to read down to zero current without affecting the relevant accuracy.

*[5.2.8.5.1.a] Telemetry section - Current telemetry, offset*

*[5.2.8.6.1.a] Telemetry section - Current telemetry, reading at zero current*

The capability of the current telemetry to read down to zero current can be easily implemented by allowing a positive telemetry output offset (in case of a single telemetry circuit supplied by a single line with respect to ground). This solution has the advantage to remove the systematic telemetry error at low current due to the typical telemetry circuits output offset voltage (for example, due to operational amplifiers).

#### 5.2.7.2.2 Verification

Current TM performances are verified by analysis and test, on a minimum number of points.

*[5.2.8.7.1.a] Telemetry section - Current telemetry, verification*

## 5.3 Retriggerable Latching Current Limiter case

The Retriggerable Latching Current Limiter, or RLCL, is an LCL including additional features.

It is basically an LCL not provided with an OFF command, which is set in any case in ON condition during start-up, and performing an automatic start-up, repeated switch-on sequence after an overload occurred, as long as the overload is present; in case the overload is removed, the RLCL automatically ends up in ON conditions, e.g. delivering power to the load.

The RLCL is normally used for supplying essential satellite loads, e.g. the ones that are essential for mission success (e.g. receivers and decoders).

An example of RLCL timing diagram is given in Figure 5-10.

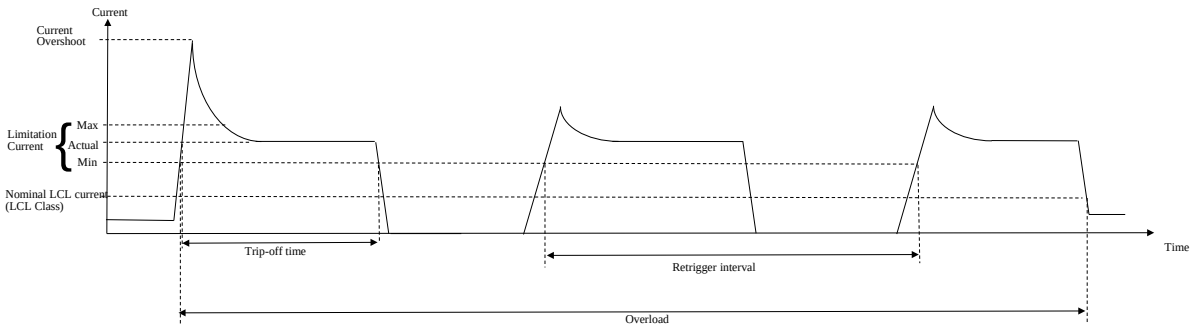



**Figure 5-10: RLCL overload timing diagram**

The RLCL retrigger rate in overload conditions is determined by design to respect the required stress limitations (derating) on the relevant RLCL switch; the RLCL retriggerability can be disabled under special circumstances should the load be acknowledged as definitively failed.

In any case, to allow the isolation of essential loads that can present an overload and malfunction, causing not allowable perturbations at spacecraft level, it is convenient to allow the possibility of enable or disable the retrigger function of an RLCL.

*[5.2.6.2.1.a] Telecommand section feature - Retrigger function*

The RLCL is normally configured as explained in chapter 5.1 for the LCL and provided with the same other LCL functionalities explained in chapter 5.2.

At start-up, the RLCL is ON.

*[5.2.7.1.1.a] Conditions at start-up/switch-off - Auto ON*

At start-up, the RLCL retrigger status is ENABLED.

*[5.2.6.3.1.a] Telecommand section feature - retrigger ENABLE*

When the RLCL is used to supplying essential satellite loads, it is of the utmost importance that it is made robust to any possibility of being commanded to an OFF condition due to spurious event (EMC, ESD, SEE nature), and also that the status of its retriggerable condition (ENABLE by default) cannot be disabled by any spurious event.

Since it is almost impossible to prove the absence of such spurious events in the final satellite configuration (space segment element), it is necessary to require an autonomous recovery from spurious OFF status and/or retriggerable DISABLE condition in any case.

*[5.2.18.1.1.a] Noise immunity feature - RLCL spurious switch-off*

*[5.2.18.2.1.a] Noise immunity - RLCL spurious effects*

Note that the practical verification that no spurious perturbation can command OFF the LCL/RLCL *[5.2.16.1.1.a]* is necessarily limited to few environmental conditions with defined test set-up, while spurious OFF can appear due to other conditions expected in satellite real-life.

In practice, we try to minimise the occurrence of spurious OFF but we cannot exclude it, and that is the reason for *[5.2.18.1.1.a].*

## 5.4 Heater Latching Current Limiter case

The Heater (group) Latching Current Limiter, or HLCL, is an LCL that is dedicated to the supply and the protection of a group of heaters, as shown in Figure 5-11.

Note that the heater switches can be placed either on the hot or in the return line.

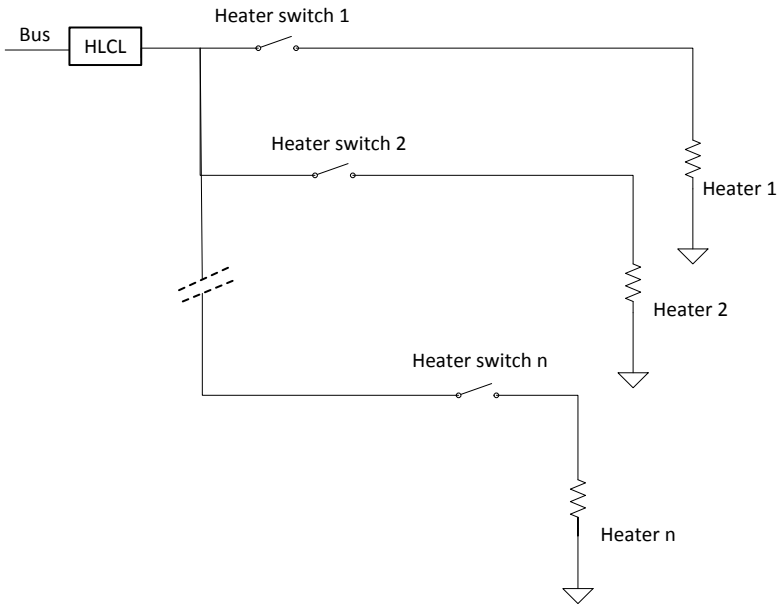



**Figure 5-11: HLCL application**

The HLCL has the same functionality of a generic LCL, but its performances are relaxed because the nature of the load is resistive. That is why in the ECSS-E-ST-20-20C the HLCL classes differ from the LCL ones, and not all the requirements valid to the LCLs are also applicable to the HLCLs.

*[5.2.1.1.1.b] LCL/HLCL class – LCL/HLCL class*

The maximum load capacitance expected for a HLCL line is only due to parasitic effects and not to actual capacitors components.

*[5.5.2.2.1b] Load characteristic – Maximum Capacitance*

The maximum inductance expected in a HLCL line is only due to harness and parasitic effects.

*[5.5.2.1.1b] Load characteristic – Maximum Inductance*

## 5.5 Reference power bus specification

To ensure the development of recurrent power distribution LCL/RLCLs for a number of applications, it is essential to define the envelope of the applicable power bus specifications (see ECSS-E-ST-20-20 clause 5.1 and Table 5-1).

For each nominal or abnormal bus specification reference characteristic, ECSS-E-ST-20-20 identifies the applicable functional response of the power distribution by LCLs/RLCLs (e.g. if it has to work nominally, survive or fulfil specific requirements).

*Power distribution nominal operation in nominal conditions [5.1.a]*

*Power distribution survival operation in abnormal conditions [5.1.b]*

*Power distribution survival operation in abnormal conditions, unregulated bus case [5.1.c]*

*Power distribution trip-off up to maximum abnormal DC bus voltage limits [5.1.d]*

The rationale for the requirements follows the generic rule that nominal functionality and performance need to be respected under nominal use, while only survival needs to be respected under abnormal interface conditions.

## 5.6 Performance, state of the art

A short briefing of the actual state of the art LCL performance is given in Table 5-2, in relation to the critical LCL requirements mentioned so far. These figures are not strict requirements, but rather a picture of what is currently achieved in the industry.

**Table 5-2, LCLs, state of the art performances**

| Characteristic | Performance (end-of-life) | Remark |
|---|---|---|
| *Voltage drop* | 0,5 % to 1 % of Vbus | The original source of voltage drop requirements is the standard ESA PSS-02-10 |
| *Current Limitation Response time* | 10 µs | For a maximum main bus voltage of 50 V.<br>Read the detailed discussion in section 5.6 |
| *Current limitation section - range* | ± 10 % | EOL accuracy |
| *Trip-off section - range* | ± 20 % | EOL accuracy |
| *Size and Mass* | Module of Power Distribution<br>28 V bus, 16 LCLs 5 A each or 32 LCLs 1,5 A each:<br>0,6 kg (all auxiliary supplies and bus undervoltage protection included )<br>- 1800 mm² / 37,5 g / LCL 5 A | |

**The Voltage drop** across the LCL is typically affecting the distribution losses.

Starting from an arbitrary selection of the allowable power distribution losses per class of satellite, the standard ESA PSS-02-10 concluded on the requirement given in Table 5-2 on the basis of test results on existing designs including a margin (see ESA PSS-02-10, para 5.3.1).

The maximum LCL power loss expected by the application of the requirement is:

- 0,25V/28V = 0,89% for 28V bus
- 0,25V/50V = 0,5% for 50V bus, and
- 0,5V/120V = 0,42% for 120V bus.

Taken into consideration that an overall power loss of 2 % is normally considered for main bus distribution (e.g. it is mainly driven by the harness losses), it does not make too much sense to impose a better LCL voltage drop than what is nowadays specified.

On the other side, many RFW's are normally accepted in ESA projects for marginal out-of-spec on LCL voltage drop performances, and therefore an overall limit of max 1 % of nominal main bus voltage is considered sufficient for a reasonable performance that can be achieved without excessive effort (for a single switch, while the limit is 2 % maximum at nominal main bus voltage if there are two switches on the LCL line).

*[5.4.5.1.1.a], [5.4.5.1.1.b], [5.4.5.1.1.c] Voltage drop - Voltage drop*

The **current limitation response time** is a very critical performance for a LCL, especially when there is no appreciable resistive or resistive-inductive impedance on the line that limits the current in case of abrupt short circuit.

Unfortunately a rigorous definition of the current limitation response time was not given in the past, and for practical reasons, in the ECSS-E-ST-20-20 a more rigorous approach is given with the definition of the **time to current overshoot** and the **current overshoot recovery time**, and their relevant requirements *[5.4.1.1.1.c]* and *[5.4.1.1.1.d].*

Due to lack of a rigorous definition, the performance indicated in Table 5-2 is only indicative.

The most critical case of an overload is a short circuit appearing straight at the LCL output, either from a failure of a component, or by a short circuit at the LCL output connector, and indeed the relevant requirement *[5.4.1.1.1.a]* needs to be checked in the worst applicable conditions, as required by requirement *[5.4.1.1.1.b].*

Note that the worst case conditions identified by requirement *[5.4.1.1.1.b]* should encompass a short circuit performed with a resistance and inductance in the order of 1/100 or less than the ones present in the LCL line (inside the Distribution Unit) when the LCL is in ohmic mode. The transition to the short circuit should also happen in a time at least 1/100 of the time to current overshoot.

The response time needs to be sufficiently fast to avoid reaching dangerous stress levels on the LCL switch before the LCL enters current limitation and this thanks to the designed and parasitic resistive / resistive-inductive impedances on the LCL power lines.

Note that the current limitation response time is of importance to reduce the stress on the LCL switch, and a number of design options exist to fulfil this need.

For example, one could think to increase the bandwidth of the current regulation loop to achieve the quickest reaction time (but taking care not to affect the loop stability), or rely on inductive impedance added in series with the power line or on the inductive-resistive nature of the current sensor (with reduced bandwidth for the current regulation loop, and improved stability margins).

When trying to decrease the current limitation response time, special care has to be paid to the stability of the relevant control loop: in fact, the state of the art performance is achieved as a compromise between speed of reaction and stability (see also section 5.7.2.5).

In any case, what is important for the system where the LCL is used is to respect a maximum energy limit during abrupt overload (see area highlighted in green in Figure 5-5): if the inrush current (peak) increases, the current limitation response time has to decrease, and vice versa.

This has been translated into requirements *[5.4.1.1.1.e]* and *[5.4.1.1.1.f],* specifying respectively the **maximum overshoot charge** and the relevant analysis and/or test conditions to be applied for the verification.

Note that the test or analysis verification of *[5.4.1.1.1.e]* and *[5.4.1.1.1.f]* are not required to be performed for any load inductance specified, but for a limited set of inductance values between zero and the maximum specified.

One last remark on overload reaction time: as shown in Figure 5-12, the response of an LCL to an (abrupt) overload might differ from the one shown in Figure 5-5 due to nonlinear saturation effects of some stages of the MOSFET driver and/or the current sensor.

The concept of the current overshoot recovery time (in place of the current overshoot decay time) and the relevant requirement *[5.4.1.1.1.d]* have been introduced to be able to give a correct specification of the LCL reaction time for both cases shown in Figure 5-12 and in Figure 5-5.

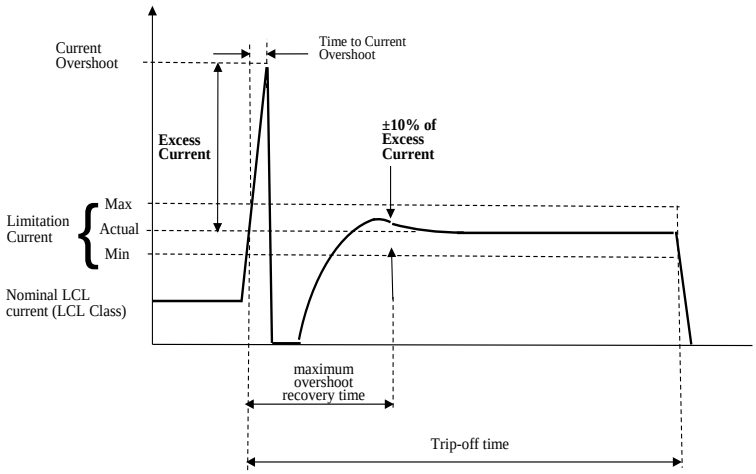



**Figure 5-12: LCL overload timing diagram, alternative behaviour**

**Current limitation section, range,** EOL accuracy is achieved by a proper selection of the current limitation circuit and the relevant components (current sensor, current loop reference, etc.). The better the accuracy is,

- the less margin can be allocated from maximum operational (nominal) current to nominal limitation current, and
- the less the LCL power switch is stressed in worst case conditions (maximum limitation current).

**Trip-off section, range,** EOL accuracy is achieved by a proper selection of the timer circuit and the relevant components.

The better the accuracy is,

- the less margin can be allocated for charging the users input filter (see clause 5.7.2.2), and
- the less the LCL power switch is stressed in worst case conditions (maximum limitation current).

It is important to note that:

- the **minimum** trip-off time duration is driven by the user (for example, we need to be sure to charge the user input filter with an adequate margin, see clause 5.7.2.2);
- the **maximum** trip-off time duration is driven by the maximum allowable stress limits on the LCL switch MFET (junction temperature): indeed the maximum trip-off time duration can be longer if the ambient/MFET temperature before the overload event is lower.

That means that the trip-off duration accuracy can indeed be relaxed if the trip-off time duration is inversely correlated to temperature. This approach can be pursued to have a more affordable and light design: in this case the design can allow the maximum exploitation of the LCL switch (thermal capability).

**Size and mass** performances quoted in Table 5-2 refer to an implementation with discrete components.

# 5.7 Critical requirements and important issues

## 5.7.1 Overview

In the present section, critical requirements and important issues are discussed, with the aim to give a rationale to the LCL interface requirements listed in the ECSS-E-ST-20-20.

In first instance, a set of critical points are discussed in relation to LCL **nominal** operation (e.g. when no failure is considered in the LCL itself – clause 5.7.2).

Then, a number of critical points are discussed in relation to the LCL **in fault condition**, and the relevant consequences and alternatives to the overall power distribution architectural design and the requirements set that are necessary in this case (clause 5.7.3).

Some RLCLs specific requirements are discussed in clause 5.7.4.

To conclude, some consideration is made on the correct application of rating/derating rules to the LCL switch (clause 5.7.5).

In any case, the reference block diagram of the power distribution by LCL is the one reported in

Figure 5-13, where the basic LCL block diagram has been complemented by the addition of the harness and a generic load (supposed to be provided with an input filter).

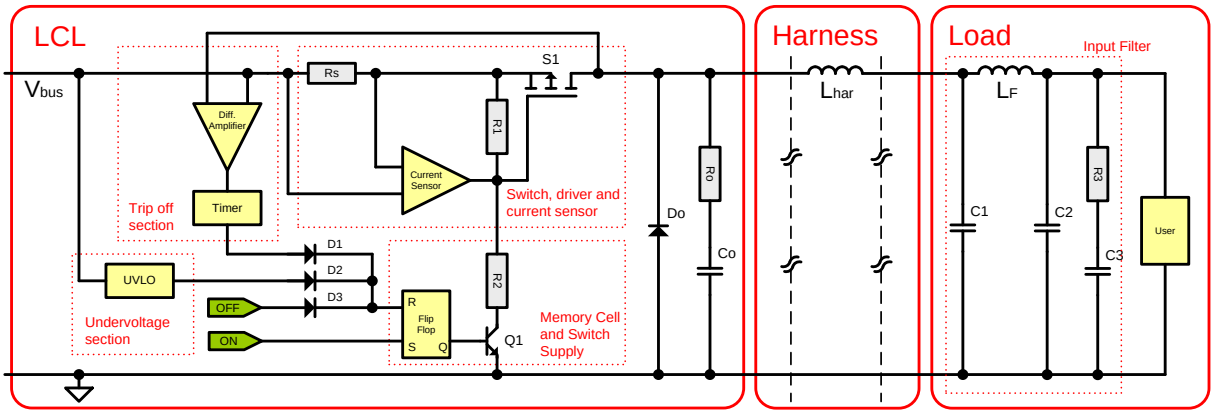



**Figure 5-13, Generic power distribution diagram by LCL.**

Note that alternative solutions to each issue are given on purpose in a **qualitative form** and with the aim to justify the defined ECSS-E-ST-20-20 requirements to be in control of the critical phenomena.

## 5.7.2 Nominal conditions (LCL fully operational)

### 5.7.2.1 LCL class attribution

#### 5.7.2.1.1 Overview

Normally, LCLs are divided in classes according to their maximum operational (nominal) or nominal limitation (trip-off) current.

Before the introduction of ECSS-E-ST-20-20, the definition of the LCL classes was usually arbitrary and defined by the prime or by the platform responsible, each time according to the specific mission

needs: usually integer current classes were specified (1A, 2A, 3A…) and fractions for lower power ranges (0,5A, 0,25A…).

#### 5.7.2.1.2 Issue

In a context of a better recurrent "product" definition, and to allow a level of standardisation which is beneficial for both customers and manufacturers, it seems more relevant to define the LCL classes according to the LCLs inherent performance limitations, and adopt this standard class definition for the widest range of applications.

It is clear that the LCL classes definition requires the indication of the relevant minimum and maximum limitation current and trip-off time, according to:

- the max allowable power stress during an overload event
- the required voltage drop
- the maximum unit temperature

#### 5.7.2.1.3 Proposed alternatives

The present LCL/RLCL/HLCL classes definition given in the ECSS-E-ST-20-20 (tables 3-1, 3-2 and 3-3) are elaborated to ensure an adequate capability to charge load input filters for most of practical applications, to enhance the chances to use single MOSFETs for LCL of lower current classes, and under environmental/application conditions that should be normally respected in all LCL practical design cases.

The LCL classes have been defined with the following purposes:

a. to ensure a sufficient number of classes for the users and prime to optimise the class current and associated harness sizing

b. to be compatible with the state of the art or with practical design for having only one MOSFET for a given class. This is achievable for low current classes to a given extent

c. to ensure for the prime and user the largest minimum trip-off time to cope with the maximum extent of input filter designs

d. to get a consistent input filter energy and sizing when changing the bus voltage level

e. to limit and standardise as much as possible the possible numerical values in the standard (e.g. current class, trip-off times).

In particular the following assumptions were made for LCL classes definition:

- Max MOSFET junction temperature Tj in permanent short circuit ≤ rated temperature
- Max MOSFET case temperature before limitation ≤ 85degC
- The MOSFET is supposed to be at LCL class current before a hard short circuit is applied
- Use the MOSFET manufacturer SOA to derive the maximum allowable trip-off time especially for trip-off time > 10ms

*[5.2.1.1.1.a], [5.2.1.1.1.b] LCL/HLCL class – LCL/HLCL class*

The following assumptions were made for RLCL classes definition:

- Max Tj in permanent short circuit ≤ Derated temperature (110 degC)
- Max MOSFET case temperature before limitation ≤ 85 degC
- The MOSFET is supposed to be at RLCL class current before a hard short circuit is applied

- Use the MOSFET manufacturer SOA to derive the maximum allowable trip-off time especially for trip-off time > 10ms

*[5.2.2.1.1.1a] RLCL class – RLCL class*

The ECSS-E-ST-20-20 (tables 3-1, 3-2 and 3-3) provide also the maximum load capacitance per class, provided according to the minimum limitation current and trip-off time, and maximum DC bus voltage value (both for regulated and unregulated bus).

*[5.5.2.2.1.a], [5.5.2.2.1.b] Load characteristic - Maximum capacitance*

An additional factor of 70% is applied, leaving a 10% margin to comply with the maximum allowed input filter charge time of 80% of LCL/RLCL class minimum trip-off time.

*[5.4.2.3.1.a] Start-up/Switch-off requirements - Load input filter charge time*

The 10% margin is the allowance for covering a specific effect affecting LCL performance, the so-called dragging effect, which is explained in Annex D.

### 5.7.2.2 Generic start-up requirements

#### 5.7.2.2.1 Overview

When the bus voltage starts up (during satellite integration phases, in LEOP or during and/or after flight contingency), the LCLs are energised at their input.

It is necessary to know the state of the LCL at the first application of the main bus or after main bus recovery, together with the definition of the relevant start-up parameters (rate of main bus rise and typical/minimum/maximum profile, etc.).

Normally, at main bus application (or re-application), the LCLs needs to be in a well-defined state.

During ECSS-E-ST-20-20 standard drafting the relevant working group decided to consider that by default all LCLs are OFF, and that all RLCLs are ON during start-up.

Additionally there are other specific cases to be taken into consideration (see clauses 5.7.2.3 and 5.7.2.4).

#### 5.7.2.2.2 Proposed alternatives

At MB application, or reapplication, the LCL and RLCL ON/OFF state needs to be unambiguously specified.

*[5.2.7.1.1.a] Conditions at start-up / switch-off – Auto ON*

*[5.2.7.2.1.a] Conditions at start-up / switch-off – Auto OFF*

*[5.2.7.4.1.a] Conditions at start-up / switch-off – LCL status at start-up*

#### 5.7.2.2.3 Verification

Requirements *[5.2.7.1.1.a]*, *[5.2.7.2.1.a]*, and *[5.2.7.4.1.a]* are verified primarily by test.

### 5.7.2.3 LCL behaviour when turned ON by command

#### 5.7.2.3.1 Overview

It is assumed that the MB is within its nominal voltage range before receiving the command.

Being the LCL equipped with current limitation and trip-off time, it can be conveniently used to reduce the inrush current to the load input filter at line switch-on.

Normally, in fact, all equipment's are required to reduce their inrush current at switch-on under specified limits (inrush current dI/dt, max current peak and surge duration, see for example Figure 5-14).

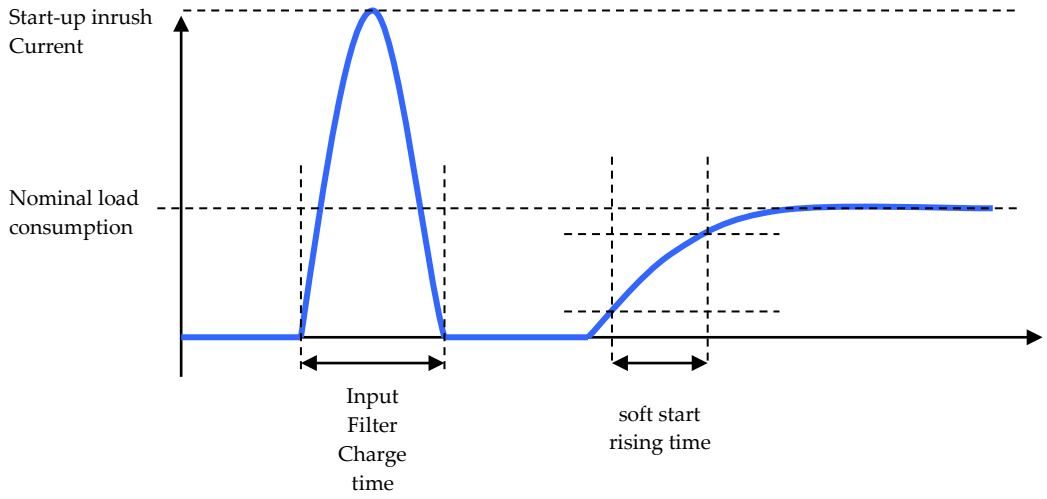



**Figure 5-14: Typical start-up current profile of a DC/DC converter attached to a voltage source and a series switch.**

The introduction of a power distribution approach by LCLs allows getting a natural resolution of the issue, since the inherent current limitation provides at switch-on a very controlled profile for all inrush parameters (see Figure 5-15).

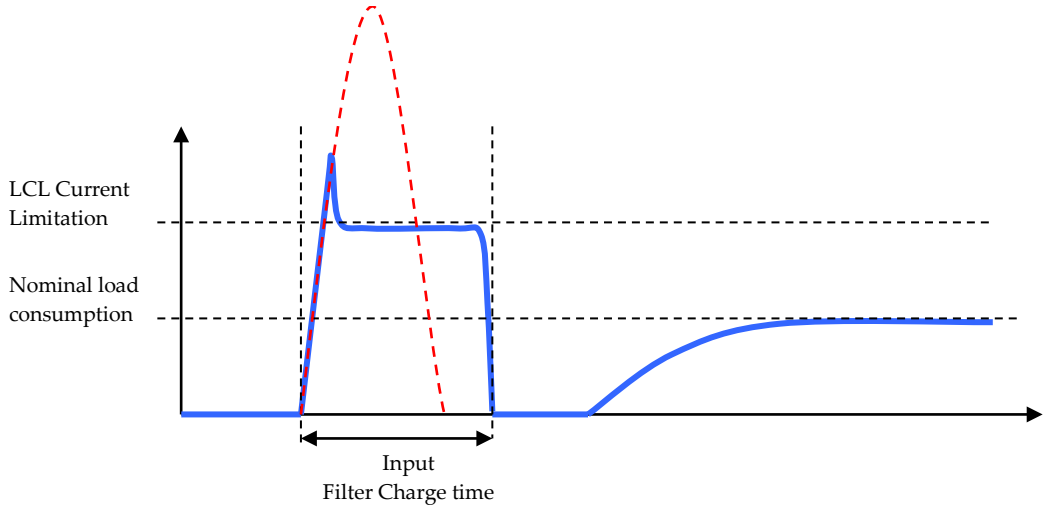



**Figure 5-15: Typical start-up current profile of a DC/DC converter attached to a LCL**

There is obviously the need to ensure that the load input filter charging is achieved within the LCL trip-off time, with an adequate margin.

*[5.3.2.3.1.a] Switch-on - Input filter charging*

*[5.4.2.3.1.a] Start-up/Switch-off requirements - Load input filter charge time*

Note that the inrush current event at switch-on is normally dominated by the input filter of the user, but on equipment provided by DC/DC converters some additional inrush charge can be produced by filters and capacitors placed at the secondary side of the converters, according to a profile depending on the converter initialisation (usually controlled by a soft start circuitry).

While the use of the LCL to reduce the inrush current event due to the load input filter charging is welcome and in fact one of the largest benefits of a power distribution by LCLs, it is better to avoid controlling the additional inrush charge due to the converter and its secondary filters and capacitors at start-up.

In fact, ECSS-E-ST-20-20 forbids using LCL/RLCL to limit inrush current due to converters and their secondary filters and capacitors.

*[5.3.2.1.1.a] Switch-on - Load behaviour 1*

*[5.3.2.2.1.a] Switch-on - Load behaviour 2*

In fact, if the LCL current limit is reached during this event, the consequences to the converter operation can be rather unpredictable because the source becomes a current generator, and the stability and transient behaviour of the converter itself can be affected.

Note that PWM DC/DC converters normally cannot work properly if supplied by sources with high impedance (as it is a current source or an LCL in limitation).

#### 5.7.2.3.2 Proposed alternatives

The load Input Filter Charge time *[5.4.2.3.1.a]* needs to be well within the LCL (minimum) trip-off time according to relevant LCL/HLCL class *[5.2.1.1.1.a]*, *[5.2.1.1.1.b]*, or RLCL class *[5.2.2.1.1.a]*, and it has to be verified under representative conditions, e.g. with a current-limiter power source with the same dynamic behaviour of the LCL.

Typically a rather large margin is used between Input Filter Charge time *[5.4.2.3.1.a]* and LCL (minimum) trip-off time, since the power distribution loads are usually not qualified using a representative model of the LCL in their supply lines, and it could happen that the first time the compatibility between the two requirements *[5.4.2.3.1.a]* and *[5.2.1.1.1.a]*/ *[5.2.1.1.1.b]* or*[5.2.2.1.1.a]*, is checked is at power system load integration level, e.g. when power system and loads are **already** developed and qualified.

Moreover in power system development (e.g. when the power distribution LCLs and the loads are developed and manufactured by different companies), it is highly recommended to verify the compatibility of Input Filter Charge time *[5.4.2.3.1.a]* and LCL (minimum) trip-off time by adopting for all critical loads a test verification that includes a representative current limited source during the relevant qualification and acceptance.

*[5.3.4.1.1.a] Load test condition – Load test condition*

By ensuring that a representative current limited source is used during the qualification of the relevant loads, there is the best confidence on the relevant compatibility, including all modes of load operation and under all environmental conditions (thermal vacuum, EMC, vibration, etc.).

This approach also allows a possible reduction of the required margin, with clear advantages in power system mass (due to the better utilisation of the LCLs capabilities).

The LCL needs to be able to start up correctly (and within applicable rating/derating limits) when an overload or short circuit is already present at its outputs.

*[5.2.7.5.1.a] Conditions at start-up / switch-off – LCL start-up on SC 1*

The *[5.2.7.5.1.a]* requirement is applicable, both in case of the LCL/HLCL being commanded ON by telecommand and when the bus voltage raises (RLCL being configured to auto-start at bus voltage application).

*[5.2.7.6.1.a] Conditions at start-up / switch-off – LCL start-up on SC 2*

After start-up events, the LCL load current is expected to stay well within the relevant class, including step load changes and other transients. The maximum current allowed for the user needs to be respected also in presence of the applicable bus voltage transients, and load conducted emissions as specified in the relevant EMC specifications.

*[5.3.1.1.1.a] Nominal feature - load behaviour*

*[5.3.1.1.1.b] Nominal feature - load behaviour*

After start-up, one important issue is the additional ripple current that a load consumes when ripple is present at the bus. For example, let us assume a 0,1 Vrms amplitude ripple on the bus. The impedance of the input filter within a load could be in the "one ohm range" at resonance even for low power applications. For 0,1 Vrms and 1 Ω, this means that a peak current of 0,14 A is added to the nominal load current and, since the LCL is a fast device, it can start limiting the current and can therefore latch off if its threshold is reached. This means that if LCLs with lower trip-off current than around 2 Ampere are to be used, a detailed analysis of this case is required including load impedance properties at different frequencies. This is particularly true for buses regulated by an S3R or when a high power pulsed payload is operating (TDMA TWTA for example). This discussion also applies for bus voltage transients that cause transient currents into the loads. Mitigation provision can consist in increasing the filter inductance at the equipment input.

#### 5.7.2.3.3 Verification

During start-up, it is not possible to predict exhaustively the complex load behaviour by analysis, especially because the relevant circuits are not yet stabilised within the recommended operation ranges.

It is therefore necessary to verify the Input Filter Charge time *[5.4.2.3.1.a]* by test, potentially in worst case operational and environmental conditions (including max loading case, under different modes of load operation, in temperature, during load EMC test campaign).

Some assessments (e.g. verification by analysis) are anyhow requested at the beginning of the load development to be able to define the correct LCL class, including the relevant trip-off time.

### 5.7.2.4 LCL behaviour when the LCL is configured to start in OFF mode

#### 5.7.2.4.1 Overview

LCLs should remain OFF at first application of the main bus or after main bus recovery.

Within the specified main bus start-up or recovery profile, it is important to identify the maximum allowable LCL input-output charge transfer (see for example Figure 5-16).

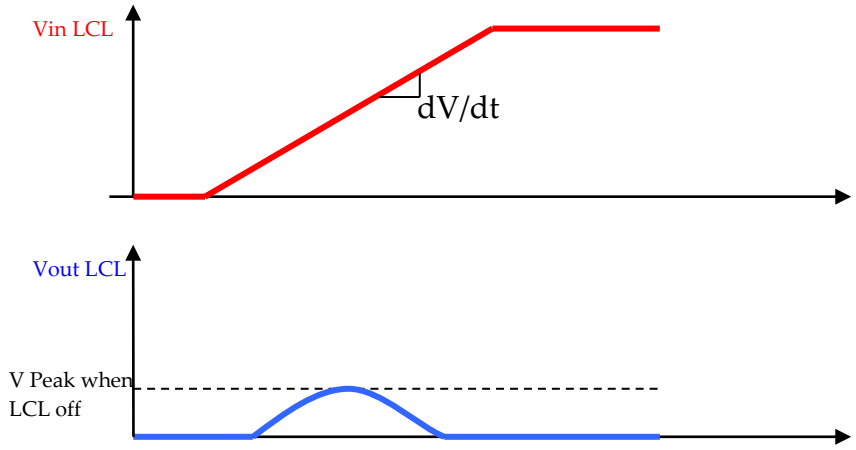



**Figure 5-16: Possible LCL output voltage when input bus voltage is rising**

The definition of the maximum allowable LCL input-output charge transfer considers that no load have an unpredictable behaviour when it is spuriously supplied during the MB start-up or recovery phase.

#### 5.7.2.4.2 Proposed alternatives

To avoid any special issue with the possible input-output LCL charge transfer during main bus recovery, the maximum allowable output voltage transient profile is specified, similarly to what is shown in Figure 5-16, and to indicate that the load remains in OFF state at the application of this transient.

*[5.4.2.4.1a] and [5.4.2.4.1b] Start-up / switch-off requirements - output, auto start OFF, amplitude*

*[5.4.2.5.1a] and [5.4.2.5.1b] Start-up / switch-off requirements - output, auto start OFF, duration*

#### 5.7.2.4.3 Verification

It is recommended to verify requirements *[5.4.2.4.1a], [5.4.2.4.1b]* and *[5.4.2.5.1a], [5.4.2.5.1b] by* analysis and/or test.

### 5.7.2.5 Stability

#### 5.7.2.5.1 Overview

The control of the current in the LCL during the limitation period is based on a regulation loop comparing the current flowing through the LCL MFET, i.e. the MFET source current, with the reference current, defining the current limitation threshold.

The current control acts on the LCL MFET gate voltage to achieve the desired effect.

If the current flowing through the LCL is lower than the reference one, the gate-source voltage is normally increased to achieve full conduction of the MFET (minimum RDSON resistance and LCL voltage drop).

If the current flowing through the LCL tends to exceed the reference one, the MFET is commanded in its linear region by the relevant control, which lowers the gate-source voltage as required.

The MFET in fact behaves like a current source at the Drain under the control of the Gate voltage.

The dynamic performances of the current control loop are typically dominated by the parasitic gate-drain and gate-source capacitance of the MFET, which are responsible for a dominant pole in the control loop when combined with the gate driver impedance.

Further dominant poles in the current regulation loop are typically caused by line inductance, especially at the output of the LCL, combined especially with parasitic MFET capacitances.

Some hints for an effective and stable LCL design are given in the paper in Annex I.

#### 5.7.2.5.2 Proposed alternatives and verification

The design of the stability of an electrical system comprising a non-ideal current source (LCL) and a generic load can become rather difficult when the possible dynamic load characteristics can vary over a wide range.

The main issue is that the stability of the non-ideal current source depends heavily on the nature of the load. A typical case is the design of a latching current limiter when a number of possible loads are considered: it soon appears very difficult to size for stability of the current limiter loop when the envelope of the possible loads is taken into account (including failure scenarios, harness contribution, common and differential mode filter design options, etc.).

The proposed approach for ensuring source-load stability is derived from the paper in Annex H and it is based on a three-step verification method and on the check of the system stability by application of source-load interface requirements control. It seems to have an undoubted advantage over the study of the current loop stability with the conventional Bode or Nyquist approach applied for each load case, especially because the load nature could not be known in detail to the designer of the LCL from the beginning, and it could be difficult, if not impossible, to practically run the analysis for all load envelope cases.

The steps for source-load stability verification are the following:

a. Fix the operating point (LCL DC output voltage), and linearise the source and load circuits around it;

b. Design the LCL checking the loop stability with the LCL output "short-circuited" on a DC voltage sink;

c. Check the ratio of source (LCL) and load impedance according to the revised Bode or other criteria.

More details are given in Annex H.

In practice, in ECSS-E-ST-20-20 some requirements are specified for the verification of the LCL stability in stand-alone configuration (to be applied during design and LCL manufacturing / production phase, both in frequency domain and in time domain), and other requirements are specified to check the compatibility of the LCL with its particular load before the relevant integration phase, so that possible source-load stability issues can be predicted and resolved in early design or procurement phases.

In detail, the LCL needs first of all to be designed to meet minimum stability margins (50° phase margin, 10dB gain margin) when loaded on a DC voltage sink.

*[5.4.6.1.1.a] Stability - Frequency domain, phase margin*

*[5.4.6.2.1.a] Stability - Frequency domain, gain margin*

When connected to a DC voltage sink, the stability of the LCL can be analysed irrespective to the LCL output impedance (it is short-circuited on the fixed LCL output voltage).

Both requirements *[5.4.6.1.1.a]* and *[5.4.6.2.1.a]* are specified to be verified by analysis and tested at design qualification level for an LCL DC input - output voltage drop of (4±1) V: this value has been chosen based on the current MOSFET technology, for which the worst –largest – parasitic capacitance range is expected at low drain-source voltages. The DC voltage drop across the LCL has been recommended to (4 ±1)V and not lower because normally the LCL current limitation in overload

conditions is expected to happen with a low voltage at the output, and the (4±1)V drop represents a reasonable worst case.

In any case, note that breaking the current limitation control loop for LCL stability verification is not trivial and an adequate break point should be selected (such that the circuit impedance at the left and at the right of the break point is very different at all frequencies, and the load conditions are not altered). For example, a reasonable break point for the LCL shown in Figure 5-17 is point A-B.

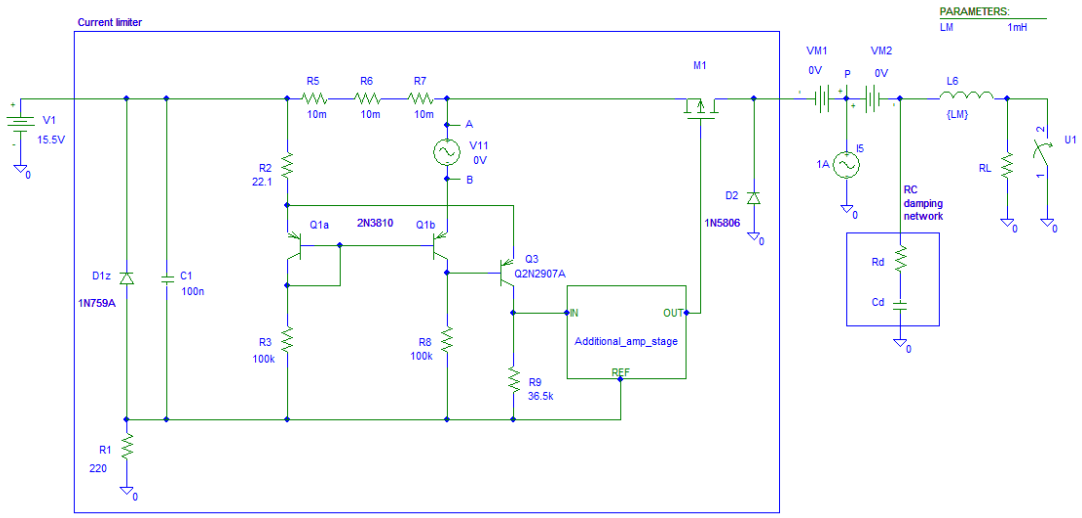



**Figure 5-17: LCL current limitation control loop example**

At LCL stand-alone level (e.g. not coupled with its specific load in the final application), it is also necessary to verify the LCL stability

a. when an overload occurs and it is connected to an inductive load within its specified range;

b. during start-up transients involving current limitation mode for any specified inductive or capacitive load.

The relevant verification can be conveniently done in time domain, using analysis to identify the worst case inductance and/or capacitance to be applied for the relevant test verification.

*[5.4.6.3.1.a], [5.4.6.3.1.b] Stability - Time domain, transient from non-limiting mode to current limitation mode.*

*[5.4.6.4.1.a], [5.4.6.4.1.b] Stability - Time domain, start-up transient to current limitation mode*

The interpretation of the requirements *[5.4.6.3.1.a]*, *[5.4.6.3.1.b]* and *[5.4.6.4.1.a]*, *[5.4.6.4.1.b]* is clarified by Figure 5-18.

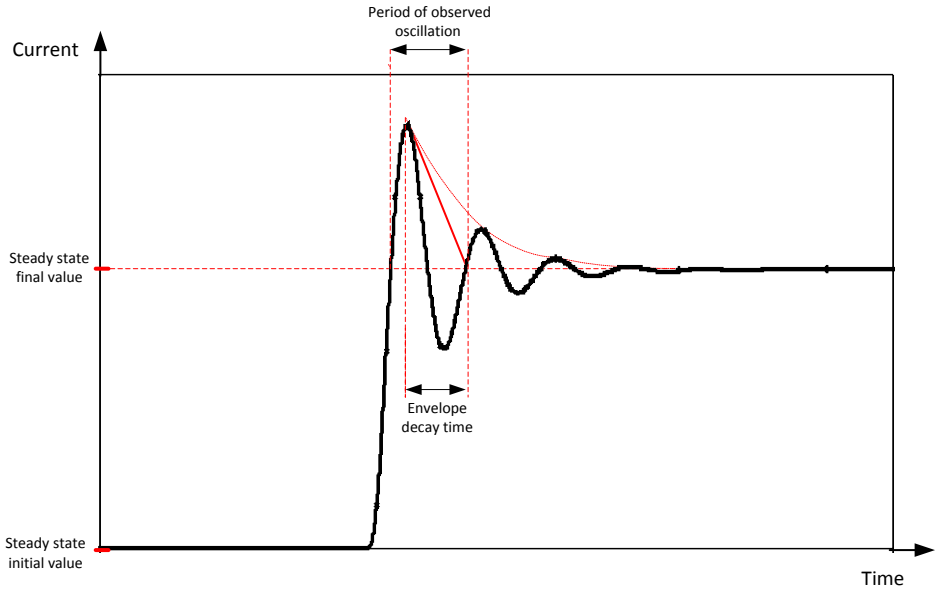



**Figure 5-18, Stability and time domain transients**

In particular, requirement *[5.4.6.3.1b]* has been derived from an assessment on the reaction of a control loop (3rd order, with one zero), characterised by a phase margin of 30° and a gain margin better than 10dB. The assessment has been performed under three different cases (e.g. with a different location of the relevant poles, zeroes and different gain).

Note that requirement *[5.4.6.3.1b]* is equivalent to say that the number of visible "oscillations" periods in the relevant time domain transient is not higher than 3-4 to be sure to have a phase margin of 30° and a gain margin better than 10dB.

Note that a valid set-up should be used for the verification of requirements *[5.4.6.4.1.a]* and *[5.4.6.4.1.b]*, as shown in Figure 5-19. In particular the critical load impedance $Z_L$* should be selected according analysis or simulation (or both), and the switch** closure time should be significantly lower than LCL reaction time.

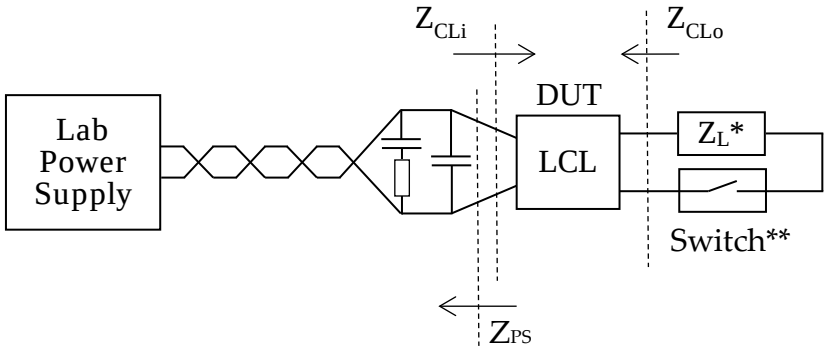



**Figure 5-19: LCL time domain measurement set-up**

Some more information on the possible set-up to be used for the test verification of requirements *[5.4.6.4.1.a]* and *[5.4.6.4.1.b]* is given in Annex E.

The overall supply impedance $Z_{PS}$ as seen from LCL input should also be negligible (e.g. 30dB or so lower) than the one presented at the input side by the LCL in limitation ($Z_{CLi}$ in).

The Switch** impedance $Z_{Switch}$ should also be negligible with respect to the one presented by the LCL in limitation at its output side ($Z_{CLo}$ in Figure 5-20).

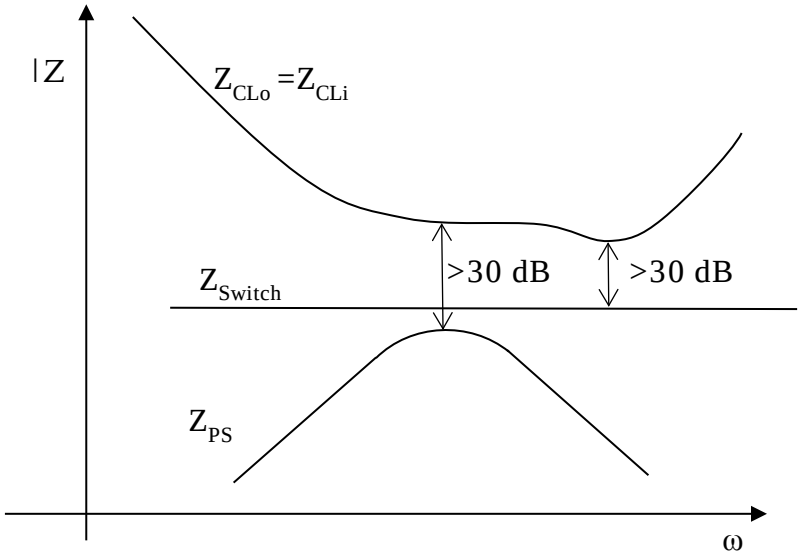



**Figure 5-20: LCL impedance versus power supply and switch impedance**

After the stability checks performed on the LCL as a stand-alone item, it is necessary to verify possible stability issues relevant to the matching of LCL output impedance – source impedance – and the load one.

First of all, the LCL output impedance is characterised:

*[5.2.17.1.1.a] Output impedance envelope (when in limitation) - Value*

*[5.2.17.2.1.a] Output impedance envelope (when in limitation) - Verification*

Note that it is recommended to verify requirement *[5.2.17.2.1.a]* by test at design qualification level for an LCL DC input - output voltage drop of (4±1)V, for the same reasons explained for requirements *[5.4.6.1.1.a]* and *[5.4.6.2.1.a]* in this chapter. The verification of requirement *[5.2.17.2.1.a]* is only recommended by test and not by analysis since the present MOSFET simulation models are normally not accurate enough to represent the devices in linear operation.

Note that the LCL output impedance envelope test at design qualification level should not be necessarily performed at final (flight) module level, but indeed

a. using an LCL model that is sufficiently representative of the actual flight product;

b. using a main bus voltage source that is representative to the one to be used in flight conditions (delivering the worst case impedance envelope of the future flight applications);

c. performing the test at least at ambient temperature.

The test set up for the LCL output impedance test should also be documented in a relevant characterisation report.

The load impedance then needs to be checked, evaluated by analysis and/or test, and provided by the load manufacturer to the system integrator.

*[5.5.2.3.1.a] Load characteristic - Load impedance envelope*

Finally, and according to the approach explained in Annex H, the source -LCL- and the load impedances need to be compared to verify if any potential stability issues are present: a minimum phase and gain margin is then verified (30° and 5 dB respectively).

*[5.5.3.1.1.a] Source-Load characteristic - Source-Load impedances phase margin*

*[5.5.3.2.1.a] Source-Load characteristic - Source-Load impedances gain margin*

Note that the verification of requirements *[5.5.3.1.1.a]* and *[5.5.3.2.1.a]* is performed at SSE or SSS level: in case of a non-compliance there is a risk that the integration of the LCL with the load results in a non-satisfactory behaviour (uncontrolled oscillations, unpredictable performance, possible components stress to be quantified).

In case of a non-compliance for requirements *[5.5.3.1.1.a]* and/or *[5.5.3.2.1.a]* it is necessary either to perform an advanced integration of the LCL with the relevant load (and verify that the overall integrated behaviour is satisfactory from functional, performance and stress point of view), or to modify either the LCL design or more likely the load one to achieve compliance.

Note that the load modification is normally to be preferred since it affects just the input filter of the equipment, and this is more easily modified than the LCL design.

### 5.7.2.6 Repetitive overload behaviour

#### 5.7.2.6.1 Overview

Especially in case of complex loads, including one or more DC/DC converters and having different modes of operation, it is virtually impossible to exclude that specific failure modes at load level do not result into a cyclic entry and exit from LCL current limitation.

For example, the user load in Figure 5-13 contains a DC/DC converter provided by local undervoltage protection.

If a failure occurs on the secondary side of the converter, causing a local overload, the LCL enters current limitation, the input voltage to the converter decreases and enables the local UVP protection. As a result, the overload disappears, and therefore the input voltage to the converter increases, releasing the UVP and enabling the converter operation again.

The depicted scenario results in the LCL entering a cyclic entry and exit from current limitation (we call it LCL in ***hic-up*** mode).

#### 5.7.2.6.2 Issue

The main issue of the LCL in hiccup mode is that the internal LCL timer can be periodically reset when the LCL exits current limitation, and for particular hiccup frequencies and duty cycles the timer could **never** command the LCL OFF.

In this case, the junction temperature of the switch can easily achieve dangerous levels (over rating, or absolute maximum limits), and there is the chance for the switch to fail in short circuit, with catastrophic consequences (main bus short, loss of mission).

*[5.2.10.1.1.a] Repetitive overload - LCL case*

*[5.2.10.2.1.a] Repetitive overload - RLCL case*

*[5.3.5.1.1.a] User UV protection at bus input side - User UV protection at bus input side*

Assuming the MFET case temperature is not modified by the application of the overload pulse or pulses until the trip-off occurs, the $Z_{thj\text{-}c}$ information given in the MFET data sheet (see Figure 5-22) is used to derive the thermal behaviour of the MFET junction temperature.

The thermal impedance of the MFET ($Z_{thj-c}$) is normally given in the datasheet in graphical form.

$Z_{thj-c}$ shows the junction to case temperature increase per watt dissipated in function of the pulse width and of the pulse repetition rate (see Figure 5-22).

In Figure 5-21, it is shown that the thermal behaviour (MFET junction temperature) is "simulated" by the voltage appearing across the capacitor of the trip-off counter, under the hypothesis to use an analogue trip-off timer: when the voltage reaches the defined trip-off level $V_{trip}$ at time $t_1$, the LCL switch is opened. The corresponding MFET junction temperature is $T_{max}$, which indeed needs to be lower than the relevant maximum rated limit (see section 5.7.5).

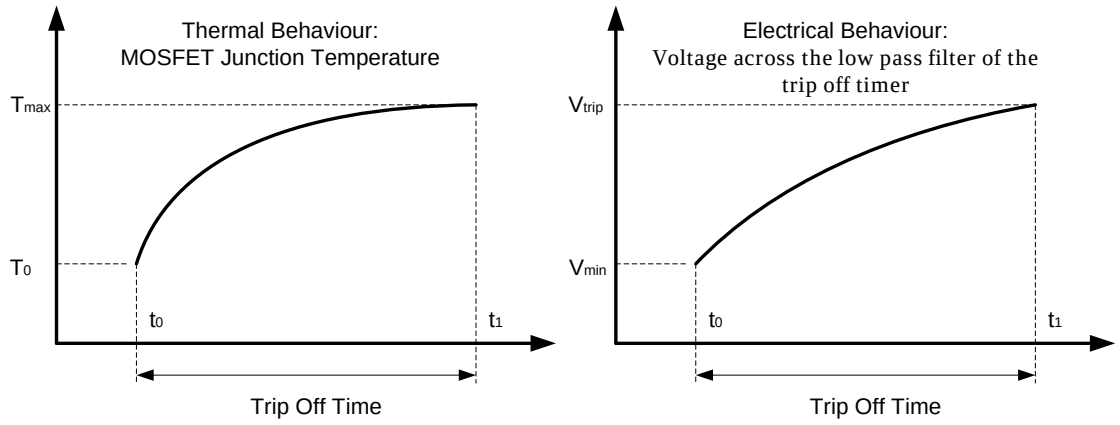



**Figure 5-21: Thermal and electrical behaviour under current limitation mode**

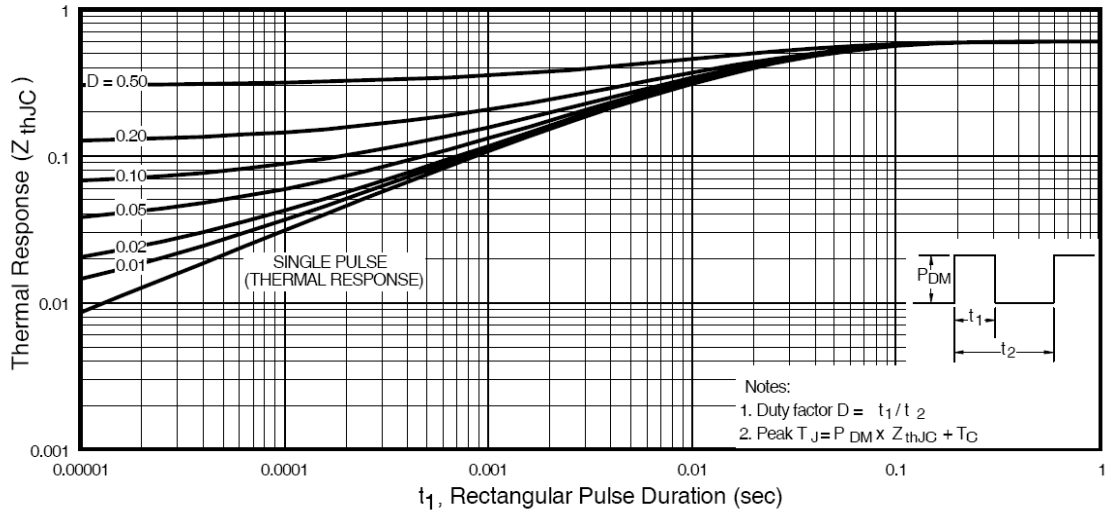



**Figure 5-22: MFET Thermal impedance, example**

Note that the MFET thermal impedance information is applied under the worst case conditions, which means at both the maximum drain-source voltage and with the MFET drain current in current limitation mode.

In case of a single overload pulse, it is possible indeed to match the two curves given in Figure 5-21 to have the correct reaction of the LCL and open the LCL switch before to reach the relevant rated temperature.

In case of repetitive overloads, the thermal and electrical behaviours under current limitation mode given in Figure 5-21 do not necessarily match, to ensure the LCL to open before reaching dangerous temperature limits on the LCL switch.

It can happen in fact that the trip-off-counter "discharge", linked to the electrical time constant of the relevant low pass filter, is faster than the decrease of the MFET junction temperature (linked to the relevant thermal capacity).

The resulting situation is shown in Figure 5-23: in spite that the overload is repetitively applied for a duration $t < t_{trip\text{-}off\text{-}time}$. the rated junction temperature $T_{j,\,max}$ is reached without trip-off.

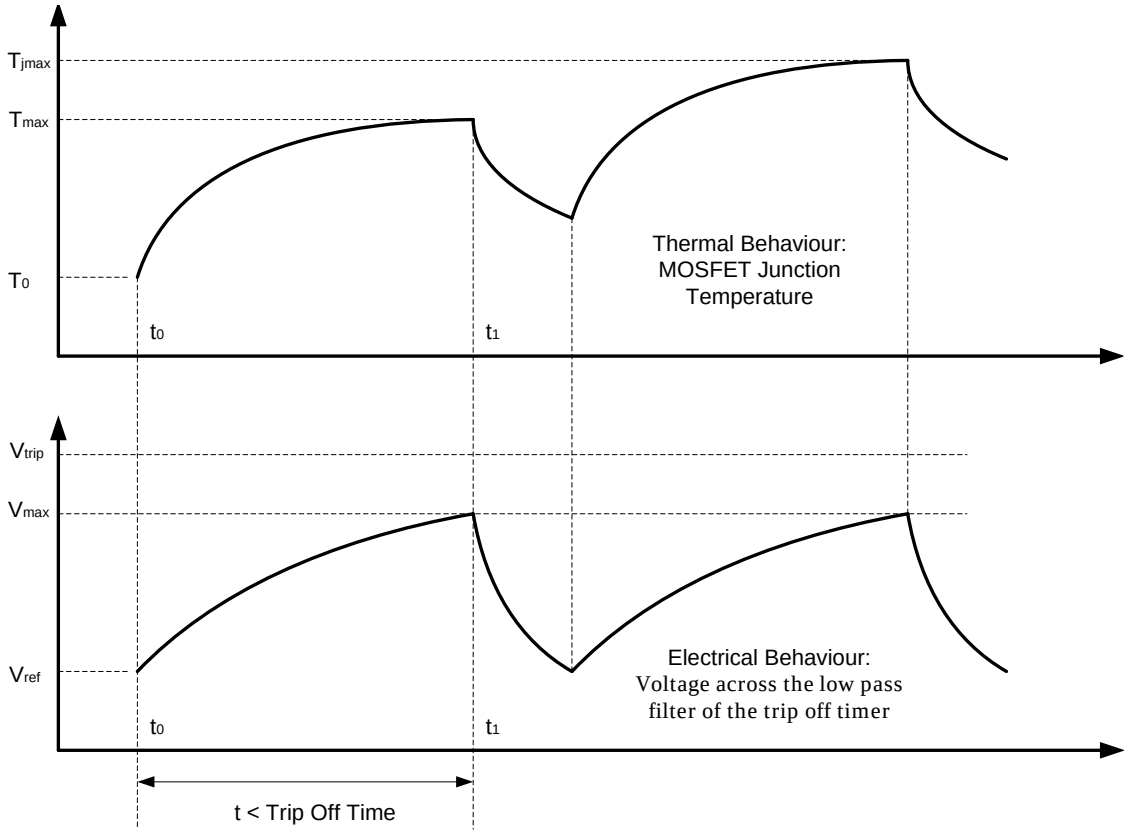



**Figure 5-23: Electrical and thermal behaviour mismatch under repetitive overload**

#### 5.7.2.6.3 Proposed alternatives

The issue of ensuring **reliable** reaction (switch-off) of the LCL under repetitive overload conditions (e.g. maintaining the switch junction temperature within rating conditions – see also section 5.7.5 -) can be resolved rather efficiently by implementing the LCL timer in the trip-off section with different time constants for counting up (e.g. during overload duration, and switch current limiting mode) and for counting down (e.g. when the switch goes back to ohmic conditions).

More in detail, the counting down time constant needs to be at least one order of magnitude lower than the count up time (it is recommended to use a ratio of about 30, to be confirmed with detailed analysis).

The ratio of 30 between the count down and count up time constant is an indicative design choice verified on typical LCL design circuit – characterised by the current limiter section shown in Figure 5-17 – under the application of a reasonable repetitive overload case – square wave, 10 KHz maximum, with different duty cycles.

*[5.2.10.1.1.a] Repetitive overload - LCL case*
*[5.2.10.2.1.a] Repetitive overload - RLCL case*

#### 5.7.2.6.4 Verification

The repetitive overload requirements *[5.2.10.1.1.a]* and *[5.2.10.2.1.a]* are expected to be verified by analysis, in worst case conditions, with most critical conditions to be verified by test at design qualification level.

It is highly recommended to spend some time to model the thermal impedance of the switch in order to have a correct prediction of the switch junction temperature for all repetitive loading cases, and to use this information to run a number of analyses for different overload repetition frequency and duty cycles.

The repetitive overload analysis verification should be done for the most critical cases, e.g. for current overload profiles for which the MOSFET junction temperature is the highest and/or for which the trip-off does not occur.

It is proposed to perform the verification with the application of a square wave overload profile (from nominal LCL/RLCL class current to short circuit) and variable duty cycle to find out the most critical cases defined above, for different application frequencies up to about 10KHz. The most critical conditions should be verified also by test verification at design qualification level.

### 5.7.2.7 Undervoltage protections at load side and interactions with LCL

#### 5.7.2.7.1 Overview

Especially in those cases where the responsibility of power source or distribution unit (including LCLs) and load belongs to different companies (and/or when the load is a recurrent item, already developed and manufactured at the time of definition of the power system), it is common to have loads provided with their internal undervoltage protection.

Typically, an undervoltage protection is introduced in the functions of an electrical user because it avoids that the equipment is supplied by a voltage that is outside its nominal operative range (if this condition is not guaranteed, abnormal modes of operation or event stress conditions could be started, with possibility of failures and failure propagation).

The undervoltage protection typically cuts the supply line to the user circuits for input voltages below a critical threshold, and allows the supply line to be restored in case of a second voltage threshold is reached by the power input line.

Normally there are two different thresholds (one for cutting, another for restoring the supply line), separated by a hysteresis.

The hysteresis of the undervoltage protection is essential to avoid high frequency ON/OFF cycles should the input voltage be around the undervoltage threshold.

The undervoltage protection reacts on the input voltage level with a delay which is necessary to avoid spurious, transient switch-off due to voltage transients due to step loads or other reasons.

#### 5.7.2.7.2 Issue

If a user is provided with its internal undervoltage protection is connected to a power bus protected by LCLs, there can be specific failure modes (at load side, on the secondary converter or in the supplied load) that result in an overload situation.

Such failures are normally identified by the relevant FMECA analysis, but the user could not appreciate the consequence of the overload at system level if the interface with the LCL is not evaluated in the context.

In case of an overload, the LCL reacts by entering current limitation, and as a result the input voltage to the user decreases.

If the input voltage to the user decreases below the user undervoltage protection threshold, this causes the power supply cut-off, the overload disappears and the voltage at the user input increases again.

The result is a spurious current limitation/saturation LCL cycle and a user undervoltage protection activation and deactivation, with abnormal bus perturbations, EMC disturbances and possible failure propagation due to thermal stress on the LCL switch (see also section 5.7.2.6).

#### 5.7.2.7.3 Proposed alternatives

In general terms, and for the issues explained in the section 5.7.2.7.2, it is advisable to evaluate carefully the effects of undervoltage protections on user's side if a power distribution by LCLs is used.

It is difficult to generalise the possible problems that can arise from the interaction source-load in this case, the best advice is indeed to analyse the possible issues as part of the FMECA.

*[5.3.5.1.1.a] User UV protection at bus input side - User UV protection at bus input side*

Note that off-the-shelf units developed for power distribution based on fuses are normally provided with undervoltage protection.

In any case, to be in control of the possible thermal stresses on the LCL switch, it is necessary to **apply** the **requirements** applicable to the **repetitive overload** issue (see section 5.7.2.6).

*[5.2.10.1.1.a] Repetitive overload - LCL case*
*[5.2.10.2.1.a] Repetitive overload - RLCL case*

Additionally, it is necessary to confirm the correct behaviour of the power distribution chain not only in nominal mode, but also in case of a failure.

In fact, the effects of the disturbances generated by the spurious current limitation/saturation LCL cycle and a user undervoltage protection activation and deactivation need to be assessed at system level (note that the relevant current emission is likely to exceed the normal conducted emission limits, both in frequency and time domain).

It is not obvious to conclude that any LCL "hiccup" mode in this respect results in a switch-off after a given time (in fact, there is always a minimum overload duty cycle, and maximum overload period that do not result in LCL switch-off).

In the Figure 5-24 two possible different situations are shown.

The first one (a) is an overload situation that results in LCL switch-off after certain number of cycles, the second one (b) is the worst case condition, when the overload appears with the condition that does not result in LCL switch-off (a minimum duty cycle $\delta T_2$ and a maximum period $T_2$), since the voltage of the trip-Off timer never reach the reference value.

In both cases it is necessary to assess the increase of the MFET junction temperature $T_j$.

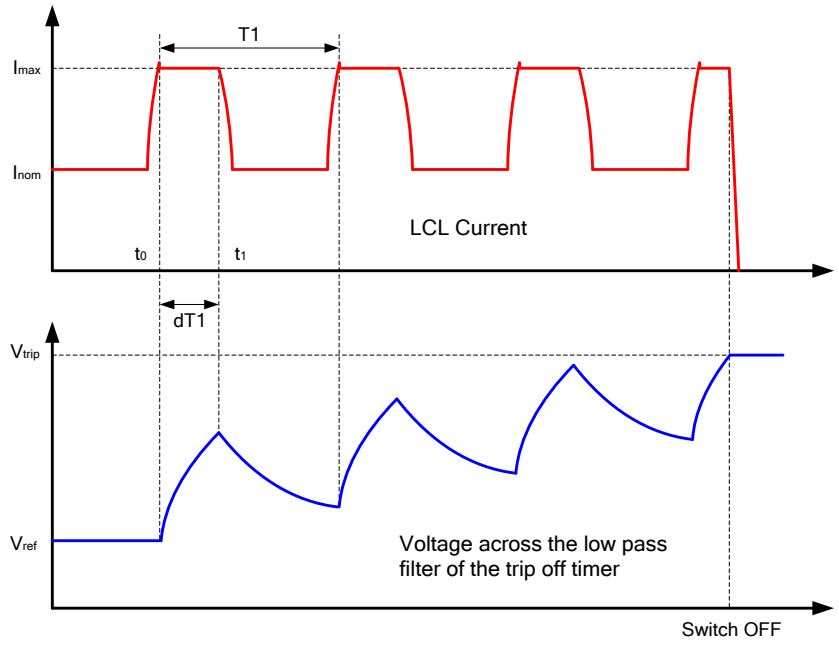
In fact, if the design is not done according to the requirements discussed in section 5.7.2.6, $T_j$ can reach in both cases a very high value, which can destroy the LCL switch and the whole circuitry because of failure propagation.

So, either the effects of the phenomenon are clearly analysed in worst case and tested under a reduced set of critical conditions, or evidently a non-measurable risk is taken, and it is then better to revise the presence of undervoltage protection on the user side.

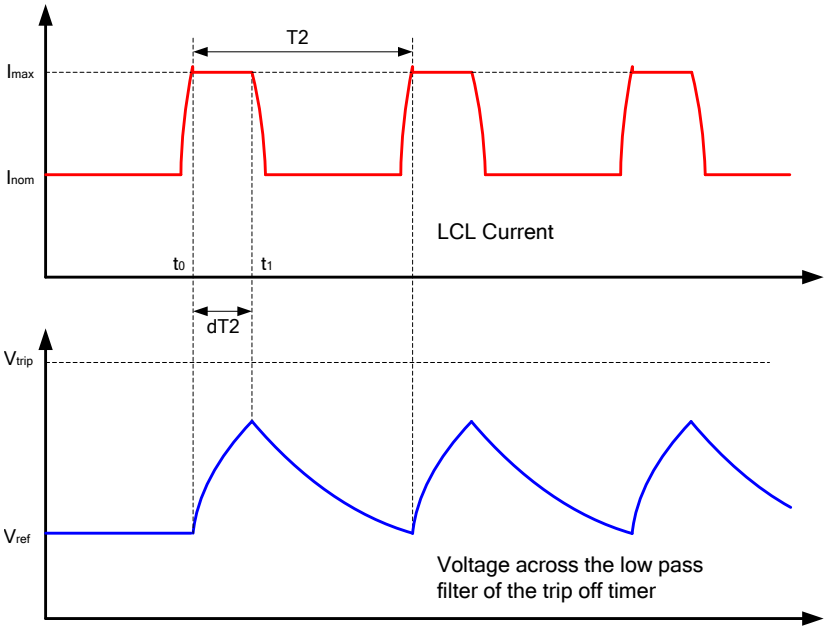
A potential solution can also be an additional feature of the LCL design that causes the immediate trip-off in case the LCL enters current limitation for two consecutive time periods, whatever the time period duration is.

Indeed, this function resolves the present problem but it is considered too risky to be adopted: in fact, it requires a perfect screening of start-up conditions, where it could be very likely to enter/exit current limitation during input filter charging or converters start-up.

A potential LCL switch-off during start-up, under specific circumstances, indeed cannot be accepted.




**a)**




**b)**

**Figure 5-24: LCL Behaviour under repetitive overload and UVP activation.**

#### 5.7.2.7.4 Verification

As mentioned in section 5.7.2.7, it is recommended to analyse undervoltage protection of loads and interaction with LCLs in worst case.

Analysis should entail emission and susceptibility checks both on source and load side, to ensure that no spurious change of operational status, power quality, telemetry or other signal corruption can result.

Analyses conditions should be applied in order to maximise as much as possible emission and susceptibility patterns.

### 5.7.2.8 Series connection of LCLs

#### 5.7.2.8.1 Overview

In some cases it can be needed to distribute power inside a piece of equipment via secondary LCLs in order to protect the different loads of the equipment in the event of a short-circuit to ground, or overload in one of the loads as shown in Figure 5-25.

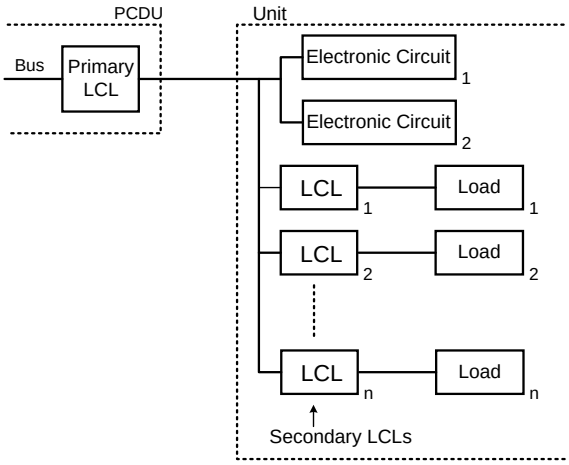



**Figure 5-25: Complex payload with an internal distribution system**

Different loads can be connected to a single power line from the bus: for example, a DC/DC converter powering a digital/analogue load, a pure resistive load (e.g. heaters), a load powered at bus voltage (not needing DC/DC conversion), etc.

We define *primary LCL* as the one placed in the Distribution Unit (for example PCDU), while *secondary LCLs* are the ones distributing the power within the equipment (normally placed in the equipment, not in the Distribution Unit).

It should be noted that secondary LCLs might not follow the scheme explained in section 5.2.

In some cases, only the current limiting function and/or the switching capability is implemented and not the rest of the features.

#### 5.7.2.8.2 Issues

- **Interactions between primary and secondary LCL**

  If we consider just the current limiting function (without protections, trip-off time, intermediate decoupling capacitors, etc.) there is no problem in placing two current limiters in series. There is no theoretical reason why two independent current limitation loops can interact and lead to an

instability. It should be noted that LCLs do not store energy and hence, oscillations due to this interaction are not likely.

From a preliminary check, it was not possible to find a situation where oscillations occur between primary and secondary LCLs. Checked scenarios included having very fast and very slow current limiters, current limiters with the same or very different current thresholds, taking into consideration inductive/capacitive loads, harness inductance, etc. Oscillations between current limiters were not found in any of these scenarios.

However, this could be different when other protection circuits (e.g. UVP) come into play (see relevant bullet discussion in this section).

- **LCL versus switches**

  Switches are typically used for thermal control, pyro circuits, etc. Typically, an LCL feeds a group of (ON/OFF) switches controlled by the satellite on-board computer. The switches could be placed on the hot line or on the return line. The advantage of a hot line switch is that any short circuit to the ground can be isolated.

  More in detail, in case many switches are connected on the hot line to the same LCL (as it is the case for the switches commanding ON/OFF different heaters on a same group), the rest of the heater group can still be used in case one of the heaters loads fails in short circuit to ground.

  Conversely, having a heater switch in the return line allows lower Rdson MFETs to be used (N instead of P-channel types), but the whole group of heaters (protected by LCL) is lost in case of a heater short circuit to ground.

  When the arrangement of Figure 5-26 is implemented, the MFET used as a switch could enter (dissipative) linear mode. If there is a short-circuit in the load, the primary LCL enters into limitation ($I_{LIM}$). This forces the gate voltage of the switch ($V_{GS}$) to have the necessary value to drive this exact current level. Hence, the MFET in the switch is not saturated but in linear mode, with substantial current ($I_{LIM}$) and non-negligible voltage difference between drain and source ($V_{DS}$). Thus, the thermal design is implemented to cope with this failure.

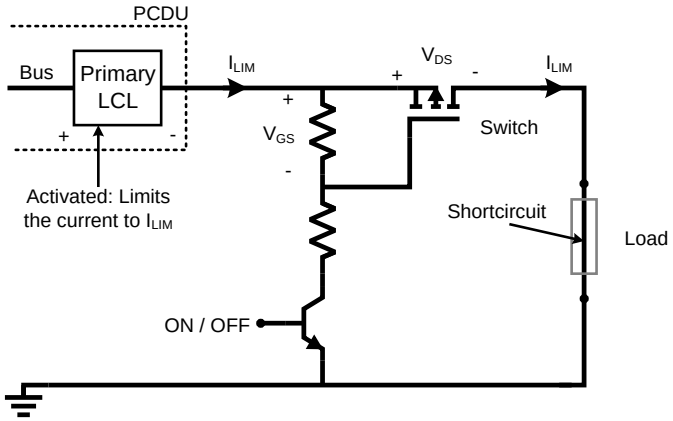



**Figure 5-26: LCL followed by a switch**

- **Undervoltage protection**

  As previously mentioned, if no other functions besides current limitation are implemented in the LCL, it is not likely that interactions between the primary and the secondary LCL occur.

  However, if UVP is implemented, hiccup modes can occur as in the general case.

  Figure 5-25 represents a generic complex load that comprises several internal sub-loads.

Some of them are fed through LCLs but there can be other electronic circuits directly powered from the Distribution Unit LCL.

If there is a failure on some of the un-protected electronics leading to an overload (not a short-circuit), the primary LCL can start limiting the current hence lowering the input voltage of the complex payload. If the internal LCLs have input UVP protections, they could switch off and the current could go down. The overload case could therefore disappear and the primary LCL could stop limiting the current. The system then re-starts and comes back to the previous condition. As a consequence, the system enters in a hiccup mode with unpredictable consequences.

This interaction could also occur between the secondary LCLs and their relevant loads. This case is similar to the one depicted in section 5.7.2.7. Note that the secondary LCLs prevent the voltage coming from the Distribution Unit to go down. Hence, in this case there is no interaction between the primary LCL and the secondary LCLs.

#### 5.7.2.8.3 Proposed alternatives

If all the internal circuits of the unit are fed through secondary LCLs as shown in Figure 5-27, the hiccup mode between primary and secondary LCLs is completely avoided under the assumption that the secondary LCLs, if provided with UVP at their input, has not have internal failure modes resulting into primary LCL limitation.

Note that these assumptions are normally verified.

In such case, there are three options:

- No UVP is needed
- There is UVP in secondary LCL or
- There is UVP in secondary load.

In case secondary LCL and relevant load contain UVP, see the discussion presented in the section 5.7.2.8.2.

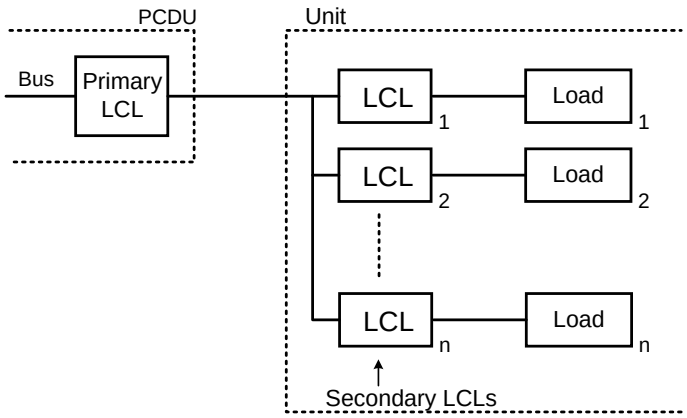



**Figure 5-27: Complex load with cascaded LCLs**

The selection of the secondary UVP (UVPsec) needs to be carefully designed according to the nature of the load and to the defined primary UVP (UVPprim), which is normally defined as a "general" default to be in control of bus behaviour but could be modified in special cases.

- di/dt control

If di/dt control is implemented in primary LCL there is no need to implement additional di/dt in secondary LCLs in case the secondary LCLs are configured ON at the start-up (see chapter 5.7.2.2).

If the secondary LCLs are used later as switches while the primary LCL stays ON then naturally di/dt control is also required for the secondary LCLs.

- Trip-off time

The LCL classes are defined in each case applying a pre-defined set of values. As a consequence, the total sum of the current limits for the secondary LCLs could be higher or lower than the primary LCL limit.

Two possibilities arise:

- If $I_{lim\text{-}sec\_i} + \Sigma I_{\text{-}sec\_j}$ (j=0..n-1)< $I_{lim\text{-}prim}$ (with margin to be defined) the primary LCL does not enter into limitation. Hence, there is no need to respect any special relation between trip-off time of primary and secondary LCLs.
- If $I_{lim\text{-}sec\_i} + \Sigma I_{\text{-}sec\_j}$ (j=0..n-1)≥ $I_{lim\text{-}prim}$ the primary LCL can enter into limitation, for example during start-up when secondary filters are charged.

  If the secondary trip-off time is longer than the primary one, the primary LCL can trip-off preventing the load form starting properly. Hence, it is necessary to ensure that $t_{trip\text{-}off(sec)} < t_{trip\text{-}off(prim)}$. In this situation the margin between the trip-off time of the primary LCL and the secondary LCLs should be high enough (for example 50%) to ensure that limitation on secondary side does not latch up the primary LCL. At the same time it needs to be guaranteed that the input filter of the load (if applicable) is charged completely within the trip-off time of the secondary LCL. This margin could be lower if the same manufacturer provides the secondary LCL and the load itself.

**Requirements**

In general, it is always better to apply the design rule If $I_{lim\text{-}sec\_i} + \Sigma I_{\text{-}sec\_j}$ (j=0..n-1)< $I_{lim\text{-}prim}$ to avoid any interaction between the primary LCL and the secondary ones.

In req. *[5.5.5.1.1.a]* $I_{lim\text{-}prim}$ has been replaced with $I_{class}$ to have some additional margin

*[5.5.5.1.1.a] Internal load input current limitation - Internal load input current limitation*

In case the rule above cannot be applied, or there is a late realisation in the design/procurement process that the condition $I_{lim\text{-}sec\_i} + \Sigma I_{\text{-}sec\_j}$ (j=0..n-1)< $I_{lim\text{-}prim}$ is not fulfilled, it is necessary to apply the second rule, e.g. if $I_{lim\text{-}sec\_i} + \Sigma I_{\text{-}sec\_j}$ (j=0..n-1)≥ $I_{lim\text{-}prim}$ then $t_{trip\text{-}off(sec)} < t_{trip\text{-}off(prim)}$.

### 5.7.2.9 Parallel connection of LCLs

#### 5.7.2.9.1 Overview

Parallel connection of LCLs is another possibility that can be found in some cases because of several reasons.

Very powerful loads could need more than one LCL to supply the total nominal current, and in this case one option is to put two or more current limiters in parallel. This solution could be interesting to make extensive use of a recurrent LCL instead of developing a new one for a specific load.

#### 5.7.2.9.2 Issues

Redundancy is another reason why LCLs could be connected in parallel. Figure 5-28 shows three typical scenarios.

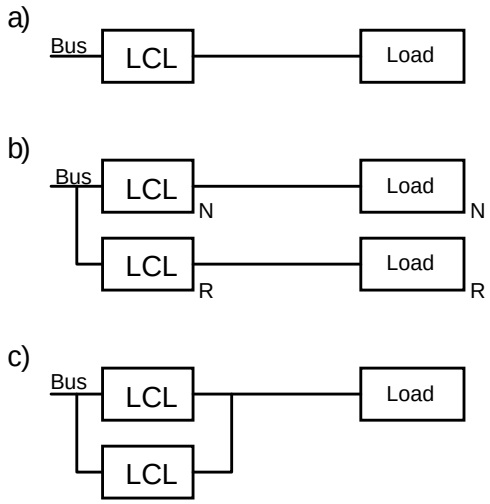
In Figure 5-28a) a load is supplied by a single LCL. This is usually done when the load needs no redundancy or higher power LCLs than the ones already available as recurrent items.

Figure 5-28b) shows a nominal + redundant load supplied through two (nominal + redundant) LCLs.

Finally, Figure 5-28c) shows a single payload fed by two LCLs connected in parallel.

Note that the parallel LCL configuration is justified by the need of having a higher current capability, and not by redundancy needs.

As it is explained in the ECSS-E-ST-20-20 scope, paralleling of LCLs to increase power supply line reliability is not reasonable, since it does not appreciably change the reliability of the overall function (LCL plus load). In fact, a typical reliability figure of the LCL (limited to the loss of its switch-on capability) is 20 FIT or less. If the load to be connected to the LCL line has a substantial higher failure rate than this, it does not make a lot of sense to duplicate the LCL to supply that load.




a) single string case
b) nominal + redundant case
c) parallel LCLs

**Figure 5-28: LCL connections**

#### 5.7.2.9.3 Proposed alternatives

After concluding that the parallel LCL connection makes sense only for increasing power of the line, a number of requirements are established in ECSS-E-ST-20-20 to ensure that

- the LCLs can be effectively put in parallel,
- their current sharing and the trip-off time is correctly assessed (to avoid premature tripping off with respect to expected thresholds)
- the relevant command is shared and
- that the current telemetry is expected to provide the sum of the currents through each one of them.

Note that the overall limitation current of two (or more) LCLs in parallel is usually smaller than the sum of the individual LCLs limitation currents.

*[5.2.12.1.1.a] Parallel connection - LCLs in parallel*

*[5.2.12.2.1.a] Parallel connection - LCLs in parallel and current sharing*

*[5.2.12.3.1.a] Parallel connection - LCLs in parallel and trip-off*

*[5.2.12.4.1.a] Parallel connection - LCLs in parallel and ON/OFF command*

*[5.2.12.5.1.a] Parallel connection - LCLs in parallel and current telemetry*

It is important to highlight that the requirements *[5.2.12.1.a.]* to *[5.2.12.5.1.a]* above refer to parallel connection of LCLs performed during the development phase by the Distribution Unit or in any case by the power distribution function manufacturer.

There is also the possibility to put LCLs in parallel by the system integrator (when the Distribution Unit or the power distribution function are already manufactured), but this is not recommended for a number of reasons:

- there might be differences on the timing of the parallel LCLs commands, and therefore load input filter charging might not see a correct current sharing on all the LCLs in parallel;
- the LCLs in parallel might have differences in actual current limitation and trip-off time characteristic, in a way that is not trivial to account for ensuring a predictable behaviour of the interface (especially if LCLs of different classes are parallelised);
- the actual current sharing of the LCLs in parallel in nominal operation (for currents up to the individual class current, and also above) might not be easily assessed;
- the status information of the LCLs in parallel might not be reliable (one, or more, of the LCLs in parallel might confirm ON status also if they are in OFF state);
- It is necessary to guarantee that an LCL in OFF conditions can accept an output voltage up to its input voltage.

In summary, it is possible to parallel LCLs belonging to a unit already manufactured, but a number of additional precautions and assessments are required.

#### 5.7.2.9.4 Verification

Requirements *[5.2.12.1.1.a]* should be verified by review of design, and the other requirements relevant to LCLs in parallel (*[5.2.12.2.1.a]* to *[5.2.12.5.1.a]*) should be generally verified by analysis and test.

Test verification can be necessary to ensure that indeed the parallel LCL configuration is functional with all LCLs in parallel active.

### 5.7.2.10 Reverse current tolerance

#### 5.7.2.10.1 Overview

Some loads (e.g. reaction wheels, solar array drive electronics, motors, and magnetic rods) can re-inject current into the bus under specific circumstances.

In these cases it is necessary that the LCL design is able to withstand the relevant condition.

Practical case: the power injected on the bus by a reaction wheel assembly can reach 100 W peaks, with 10 Wh energy to be discharged.

#### 5.7.2.10.2 Proposed alternatives

It is clear that the capability to withstand reverse current imposed by the load does not apply to all LCL application cases, and therefore the relevant requirement is in fact a recommendation.

*[5.2.11.1.1.a] Reverse current tolerance - Reverse current tolerance*

In case requirement *[5.2.11.1.1.a]* is complied, the reverse current peak tolerance needs to be at least equal to the LCL class current, with a decay time of 10 minutes maximum based on actual practical case information.

*[5.4.1.2.1.a] Overall requirements - Reverse Current Tolerance*

Note that a recurrent LCL product definition and design could consider the reverse current tolerance requirements *[5.2.11.1.1.a], [5.4.1.2.1.a]* since it could be difficult to demonstrate the relevant compliance if some ad-hoc measures are not taken during the design phase.

## 5.7.3 Fault conditions (partially or fully failed LCL)

### 5.7.3.1 Introduction

In this section, we deal with requirements stemming from abnormal (fault) conditions happening in the LCL itself.

### 5.7.3.2 dI/dt control and current limitation

#### 5.7.3.2.1 Overview

The control of dI/dt at LCL switch-on and switch-off is a mandatory feature to be implemented in the design to be in control of EMC performances, and avoid critical conditions at system level related to potential spurious switch-off, equipment mode changes, self-susceptibility problems when issuing ON or OFF commands.

Normally, the dI/dt control is implemented in the LCL in the switch, driver and current sense section, and it could be combined or not with the current limiter control.

#### 5.7.3.2.2 Issue

Depending on the load nature, after a single failure in the LCL, dI/dt control could not be effective anymore to respect the relevant requirement, and therefore the critical control of EMC performances discussed above may **not** be guaranteed.

One peculiar case is the loss of the current limitation by the LCL, without losing its switching capability: normally a number of failure modes can be identified in the LCL, which causes this situation.

In case the LCL current limitation is lost, but not its switching capability,

a. it is very likely that on specific loads the dI/dt control is affected, and

b. the current at start-up is not limited to the designed limitation threshold.

Actually, the loss of the current limitation could be the cause of uncontrolled dI/dt: consider that the supplied user interface includes an input filter, as shown in Figure 5-13.

If the LCL current limitation is lost, at switch-on the LCL reacts as a normal switch, and the user input filter is then charged on a **voltage** source.

The inrush current profile in this case is indeed much different than the one produced with a fully functional LCL.

In particular, the inrush current is very likely much higher than nominal if LCL current limitation is lost, especially if the inductor of the user input filter is partially or totally saturated during the inrush event.

#### 5.7.3.2.3 Proposed alternatives

From the analysis performed in section 5.7.3.2.2, it is easy to conclude that it is useful to ensure dI/dt control at source side (at start-up and at switch-off).

*[5.4.2.1.1.a] Start-up / switch-off requirements - Start-up current rate*

*[5.4.2.2.1.a] Start-up / switch-off requirements - Switch-off current rate*

It might not be difficult to implement the LCL in a way that the dI/dt requirement is fulfilled also in case of single internal failures (including loss of current limitation).

Of course, the loss of start-up dI/dt control for sudden failures of the switch, driver or for a sudden overload cannot be avoided, but these conditions need just to be accepted (they could happen only ***once*** after a failure).

In any case, it is necessary to place some requirement on load (user) side to ensure that the start-up transient that could result if LCL current limitation is lost is within specified limits.

The issues in this case are:

- high inrush current peaks, that can stress the MFET switch and/or the capacitors in the user input filter, or other parts, over their rated value;
- abnormal main bus disturbance (to be kept under control).

To be sure that there is no effect on power distribution functionality even after a failure of the current limitation feature of the LCL (when its switching capability is maintained), the proposed approach is to specify for the user that the maximum inrush current on a sudden switch-on event **on a voltage source** is within a specified value (this value being compatible with component stresses and required main bus disturbance limits)

*[5.5.4.1.1.a] Start-up Surge Input Current - Start-up Surge Input Current*

Note that it is not practical to require the LCL to comply with single point failure free current limitation (it requires doubling the switch, driver and current section – see Figure 5-13).

#### 5.7.3.2.4 Verification

In general, the verification of all proposed requirements *[5.4.2.1.1.a]*, *[5.4.2.2.1.a]* and *[5.5.4.1.1.a]* is performed by both analysis and test.

Analysis is necessary because all the relevant requirements are design drivers for the LCL and the load input filter: the relevant analyses are necessary iterations to be able to define the electrical design of both source and load.

Test verification is necessary to confirm analyses outputs and to ensure that EMC self-compatibility is adequate.

Note that for specific cases the requirements can be verified by simple RoD (in case that the supplied loads are of exclusive resistive or resistive-inductive nature, like heaters or similar).

### 5.7.3.3 Additional switching capability

#### 5.7.3.3.1 Overview

On the power distribution architecture based on LCL, the question is normally placed if a second switching element is added to the LCL switch itself.

This section identifies issues and alternatives relevant to the presence or the absence of the secondary switch.

#### 5.7.3.3.2 Issue

As usual, let us take into consideration Figure 5-13.

- **Case 1, no additional switching capability**

This is the case depicted in Figure 5-13, in which there is no additional switching element other that the switch S1 in the LCL.

In case of any failure resulting in a low-ohmic, saturated switch, in short circuit or with a permanent low voltage drop across it, the load is in any case energised.

For dissipative failures across the MFET switch, see section 5.7.3.4.

Since there is one failure already in the LCL, there is no need to take into account contingent (failure) situations for the load.

In any case, it is not possible to remove the power supply from the load, meaning that the load consumption is in any case part of the power budget.

This fact has direct implications on the power budget, or in the specific load requirements:

If the following conditions are met:

a. all of the load operational modes imply a non-negligible power consumption, and

b. the load operational modes cannot be directly commanded by an autonomous, on board load shedding routine to be triggered by abnormal bus load consumption

the power budget needs to cover the LCL switch failure by considering the actual MB maximum load, plus eventually the unwanted load connected to the failed LCL.

The relevant requirement on power budget is important especially for safe or contingency modes of operation of the satellite (e.g. when normally all non-essential loads are commanded OFF to save power).

In general, it is advisable that an autonomous, on board load shedding routine acts directly on the load operational mode through specific telecommand and not on the LCL switch (unfortunately this being usually the baseline).

If the load operational mode, activated at start-up, is a stand-by one for which a negligible power consumption is expected, there is no special need for putting constraints on the power budget.

- **Case 2, additional switching capability**

In this case, let us consider that an additional switch S2, with independent ON/OFF capability with respect to the LCL, is present either on the power system (LCL) side (Figure 5-29) or on the load side (Figure 5-30).

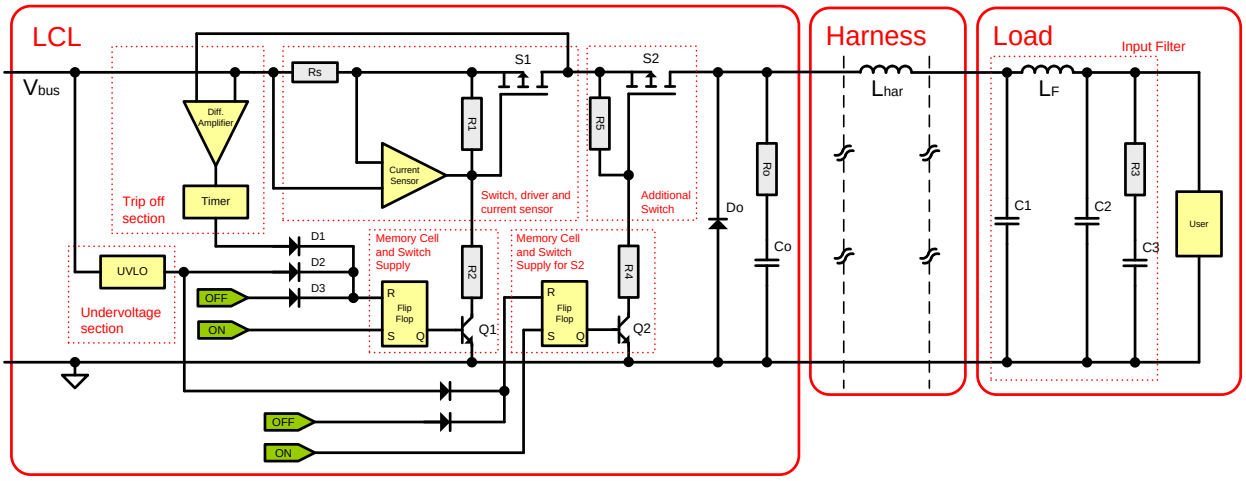



**Figure 5-29: Additional switch on power system (LCL) side**

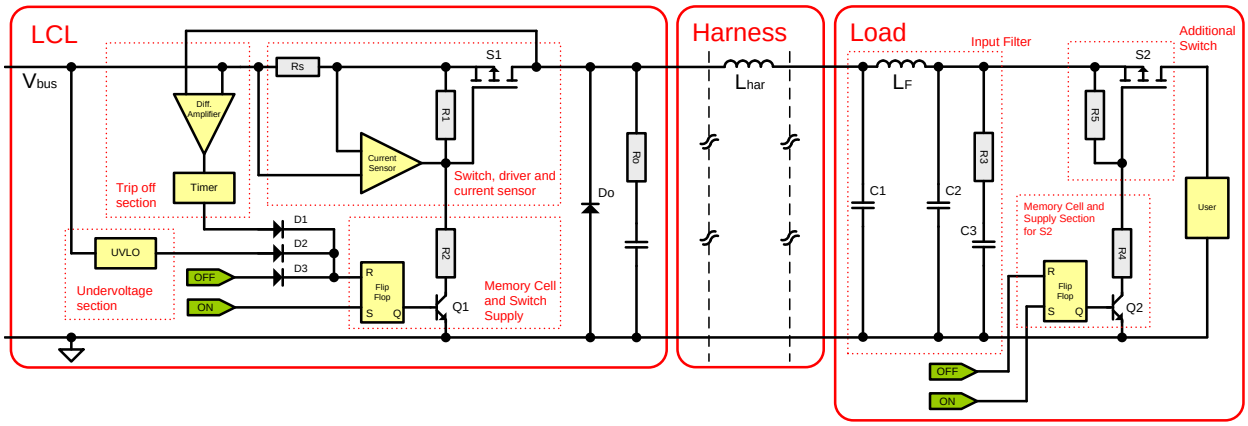



**Figure 5-30: Additional switch on load side**

Normally, if no specific constraints exist (like the re-use of off-the-shelf payloads) it is **preferred** that the additional switch is available **on the power system (LCL) side**, to save all the dedicated ON/OFF command lines and relevant harness and connectors that on the contrary are needed.

Note that this being the supply line for the load, the switch on the load side requires dedicated ON/OFF interface and it is not possible to use the available digital TM/TC interface (for example, serial CAN bus, MIL 1553, etc.).

Irrespective to the location of the additional switch, it is necessary to ensure that the additional switch can in any case be opened when the LCL switch is commanded ON (or fails ON or in short circuit).

The reason is to ensure that no unwanted load is connected to the main bus after a single failure (e.g. not to impose constraints on the power budget).

Even if an additional switch is given, it is important to be sure that there is the possibility to have an automatic, quick load removal in case of a bus overload event.

It is therefore a **good recommendation** to let the (LCL) **UVP act both on the LCL switch and on the additional switch** (to be provided by an independent memory cell), so that the load shedding can be performed in any case, even if the LCL switch fails in continuous ON or in short circuit condition.

Note that the situation leading to a load shedding in this case could not depend on a failure (it could be an operator error, or a satellite abnormal attitude due to other reasons), e.g. it is necessarily a second failure case (we normally are required to implement SPFF design).

#### 5.7.3.3.3 Proposed alternatives

From the discussion made in the previous section 5.7.3.3.2, there are two main alternatives:

- **Case 1, no additional load switch (no contingency ON/OFF capability)**

This is very likely the option that minimises the overall power management and distribution architecture. Reference is Figure 5-13.

It is especially interesting (e.g. it does not require to put constraints on the power budget) for users having a low stand-by consumption modes.

*[5.2.13.1.1.a] Switching options - No additional switching capability*

*[5.2.13.2.1.a] Switching options - No additional switching capability, negligible load power consumption modes*

- **Case 2, additional load switch (contingent ON/OFF capability)**

This option is more likely to be adopted for those loads already available as off-the-shelf items and provided with a switch on the power line (for example, such loads are normally developed for power distribution architectures based on overload protections by fuses), or when the conditions a. and b. of section 5.7.3.3.2 apply, and one does not want to put specific constraints on the power budget.

*[5.2.13.3.1.a], [5.2.13.3.1.b] Switching options - Additional switching capability*

*[5.2.13.4.1.a] Switching options - Additional switching capability, location of additional switch*

In case the additional switch is implemented on the power system (LCL) side to avoid relevant commanding line, harness and connectors, it is a **good recommendation** to let the (LCL) **UVP act both on the LCL switch and on the additional switch** (to be provided by an independent memory cell), so that the load shedding can be performed autonomously and quickly in any case, even if the LCL switch fails in continuous ON or in short circuit condition.

*[5.2.13.5.1.a] Switching options - Additional switching capability - UV protection acting on additional switch*

#### 5.7.3.3.4 Verification, method and operative conditions

The requirements relevant to additional switching capability *[5.2.13.3.1.a]*, *[5.2.13.4.1.a]* and *[5.2.13.5.1.a]* are normally easy to verify by simple RoD.

The verification of the requirement *[5.2.13.2.1.a]* is accomplished by review of design (made by the unit manufacturer), after an analysis performed by the system integrator (with some assessment related to what can be considered "negligible" with respect to overall satellite power budget, to be evaluated for each critical mission phase and especially for power contingency modes; other assessment is also required to ensure that the expected load state at power application is confirmed also in case of sudden LCL switch failure or similar, with any applicable dI/dt and dV/dt conditions).

Additionally, the correct load initialisation and power consumption at start-up, with the most representative cases of dI/dt and dV/dt is verified by test.

### 5.7.3.4 LCL switch, dissipative failures

#### 5.7.3.4.1 Issue

Normally, the LCL switch is concerned by appreciable power dissipation in overload conditions (e.g. in current limitation and during trip-off time), while in normal conditions (e.g. low-ohmic switch operation) the switch power dissipation is rather limited, also due to the stringent requirements on LCL maximum voltage drop.

*[5.4.5.1.1.a], [5.4.5.1.1.b], [5.4.5.1.1.c] Voltage drop – Voltage drop*

The situation is different when LCL switch dissipative failures are taken into account.

Postulating that the LCL switch is a MFET, and that the only notable failure condition of interest is an equivalent Drain to Gate short circuit condition (according to annex G of ECSS-Q-ST-30-02), we can predict a maximum dissipation $P_d$ of

$$P_d = V_{DS} * I_D = (V_{GS,\,Th} + 1/G_{fs} * I_D) * I_D$$

where

- $V_{GS,\,th}$ is the MFET Gate-source threshold voltage (typically 2V to 4V)
- $G_{fs}$ is the MFET transconductance (typically ranging from 15S to 45S)
- $I_D$ is the drain current

The expected dissipation in function of load current is shown in Figure 5-31.

The expected voltage drop in function of load current is shown in Figure 5-32.

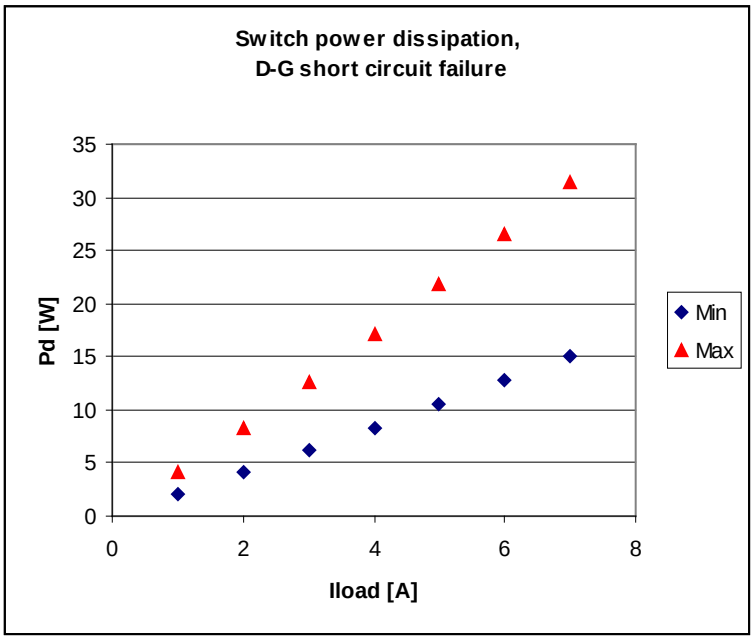



**Figure 5-31: Switch power dissipation in event of D-G short circuit failure**

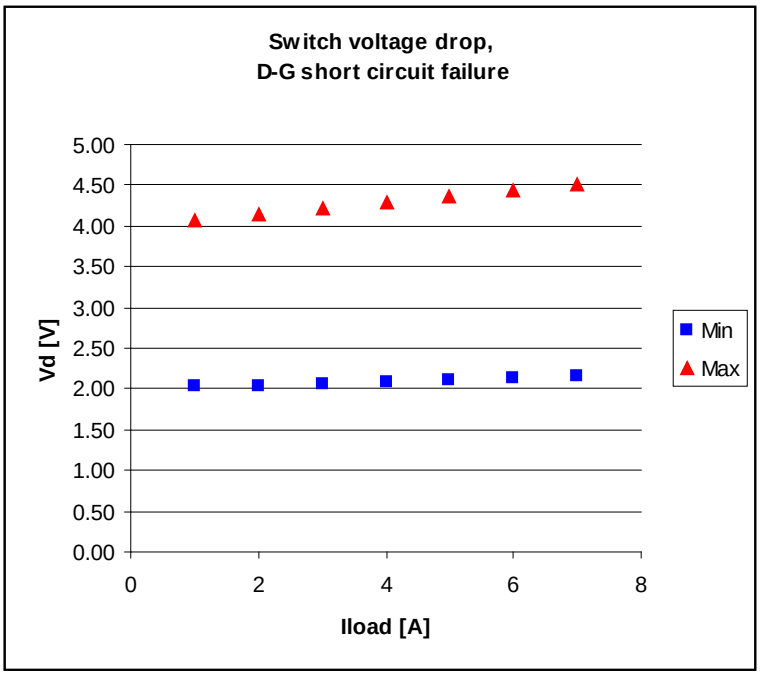



**Figure 5-32: Switch voltage drop in event of D-G short circuit failure**

It appears that

- already with load currents of few Amps, the dissipative failure of the switch could create critical local hot spots, unless the LCL switches are mounted on thermal conductive supports to minimise the relevant thermal resistance to the unit baseplate;
- especially for low main bus voltage cases (28V), the voltage drop across the LCL can become important, but not such to necessarily activate the potential undervoltage protection at load side.

In reality it appears that the worst case with respect to LCL (MFET) switch dissipation is gate open failure condition (bonding wire in open circuit), which could be higher than what considered as assumption, possibly increasing the voltage across the failed MFET up to twice (or more) the relevant threshold voltage $V_{GS,\,Th}$.

For a more precise evaluation of the possible worst condition of a dissipative failure across the LCL MOSFET it is recommended therefore to contact the relevant MOSFET manufacturer.

The assessment contained in this handbook remains in any case valid as well as the requirements related to MOSFET switch dissipative failures contained in the ECSS-E-ST-20-20.

For more details on MOSFET dissipative failures, see the paper in Annex G.

#### 5.7.3.4.2 Proposed alternatives

Three options are proposed in alternative

a. In case the LCL switch fails in a dissipative failure and in case no other protection removes the failure, all the surrounding components should be within derating, to ensure that no failure propagation takes place due to the relatively high dissipation.

b. In case the LCL switch fails in a dissipative failure and in case the "on board system" removes the failure by reducing the load or commanding OFF additional switch, all the surrounding components should be within rating during the on board system reaction time.

c. In case the LCL switch fails in a dissipative failure and in case the option 1 and 2 above are not fulfilled, a protection should be embedded in the LCL or the Distribution Unit.

For surrounding components, it is intended those components relevant to other functions surrounding the failed LCL switch.

The switch dissipative failure can be managed as a steady state condition, or as a transient condition.

*[5.2.14.1.1.a] LCL Switch dissipative failure - Steady state condition*

*[5.2.14.2.1.a] LCL Switch dissipative failure - Transient condition*

*[5.2.14.3.1.a] LCL Switch dissipative failure - Local protection*

Note that the steady state solution (option a) could appear more attractive because it could not require special additional functions with respect to the power distribution "nominal" design, but in fact this could not be true because implicitly it requires a very good thermal path from the LCL switch to the relevant unit baseplate.

Another option (which is not translated into an alternative requirement) makes use of a duplication of the MOSFET switches in the LCL: in case of a dissipative failure in one of the paralleled MOSFETs, the majority of current flows on the other MOSFET(s).

The drawback of this solution is that the LCL should never commanded in OFF state after the dissipative failure, on the contrary the good MOSFET stops conducting and the failed one dissipates abnormal power levels. The LCL control circuit need then to be modified to enter ON state, or refuse OFF command, in case one MOSFET is failed in dissipative conditions.

The "transient" solutions (options b or c) can allow a "minimum" power distribution LCL mass (no special need of thermal conductive paths from LCL switch to baseplate) but they need either an additional switch and/or an automatic detection and a change of the load to a low consumption mode).

For example, an over temperature protection can be used to command the additional switch in OFF or to command the relevant load in a low stand-by power condition (see section 5.7.3.3).

In any case, the load needs to be under control for the actual supply voltage resulting from the dissipative failure: either it should still work nominally, or it should enter a safe mode of operation (stand-by mode or similar).

*[5.3.3.1.1.a] LCL Switch dissipative failure - Steady state condition, load*

#### 5.7.3.4.3 Verification, method and operative conditions

It seems reasonable to verify all of the requirements *[5.2.14.1.1.a]*, *[5.2.14.2.1.a]*, *[5.2.14.3.1.a]* and *[5.3.3.1.1.a]* by analysis in worst case conditions.

Requirements *[5.2.14.3.1.a]* and *[5.3.3.1.1.a]* should also be verified by test to ensure that the hardware is compliant and that the expected performance and functionality is present on the flight equipment.

Req. *[5.3.3.1.1.a]* refers to the load capability when the relevant input voltage is reduced (due to linear failure in the LCL/RLCL switch). It is no problem to perform the relevant verification by test.

Req. *[5.2.14.3.1a]* refers to the need of a dedicated protection when dissipative failure cannot be tolerated (continuously or in a transient). The verification that the protection reacts correctly can be performed by test either by stimulus injection or by simulating the LCL switch dissipative failure. This can be conveniently performed at design qualification level.

### 5.7.3.5 LCL Status telemetry

#### 5.7.3.5.1 Overview

In order to monitor the status of the LCL, it is important to select proper signals for the telemetry.

The LCL switch can be:

- in overload conditions (e.g. in current limitation and during trip-off time),
- in normal conditions (saturation);
- in open circuit condition;
- in linear dissipative failure.

Sometimes only the voltage drop (*[5.4.5.1.1.a]*, *[5.4.5.1.1.b]*, *[5.4.5.1.1.c]*) is read and, if it exceeds the maximum value in nominal conditions, this means that the LCL is in current limitation mode.

But the voltage drop can exceed the maximum value not only in LCL current limiting conditions, but also in case of MFET dissipative failure and in case of not-nominal LCL output voltage.

Therefore more than one signal is needed for a correct LCL status telemetry.

#### 5.7.3.5.2 Proposed alternatives

A way to overcome the problem is to check different signals depending on the status of the ON/OFF command:

- if the LCL is commanded ON, then check the Drain-Source voltage of the LCL MFET;
- if the LCL is commanded OFF, then check the current telemetry.

Another way can be also to check, when the LCL is commanded ON, if the voltage at the output of the LCL is or not in nominal conditions.

In any case it is important to confirm that the LCL output voltage is within its nominal range to a specified accuracy.

*[5.2.8.1.1.a] Telemetry section - LCL status*

It is also important to be sure that the status information can be trusted, independently from possible failures of the LCL command interface.

*[5.2.9.1.1.a] Status section - LCL status under failed conditions*

The reason for requirement *[5.2.9.1.1.a]* is to avoid any failure propagation from the command interface circuitry of the LCL/RLCL/HLCL to the status circuitry.

Knowing why an LCL tripped off can also be useful. In order to do so, an additional memory cell could be needed. Its role is to provide additional telemetry in case of a trip-off event. The returned signal should allow the user to determine what caused the trip-off, whether it is a spurious off command (unwanted or noise) or an overcurrent.

This can allow better failure detection and recovery in flight.

The relevant requirement has not been added to the ECSS-E-ST-20-20 because it is very likely to impact the cost of recurrent distribution by LCLs/RLCLs; in any case it can be considered for specific critical lines/applications.

#### 5.7.3.5.3 Verification

Requirement *[5.2.9.1.1.a]* should be verified by analysis (in worst case, to be sure that the status telemetry signal is indeed able to discriminate that the MFET D-G voltage, or the LCL output voltage, are indeed within their applicable nominal range when the LCL is ON).

### 5.7.3.6 Start-up with an internal LCL failure

#### 5.7.3.6.1 Issue 1: Start-up after a command, bus power-up or automatic switch-on

When an internal failure of the LCL occurred resulting in the trip-off of the LCL, it is important to protect the power bus if the operator or an automatic restart circuit or routine attempts to turn it on again, or at the next occurrence of bus power-up.

**Proposed alternatives**

To safeguard the power bus, the internal LCL components blocking failure propagation should still meet de-rating after any internal failure causing it to trip-off.

*[5.2.7.3.1.a] Conditions at start-up/switch-off - LCL Start-up with an internal failure*

**Verification**

Requirement *[5.2.7.3.1.a]* is verified by analysis.

#### 5.7.3.6.2 Issue 2: Start-up with loss of current limitation

Refer to section 5.7.3.2.

## 5.7.4 RLCL specific requirements

### 5.7.4.1 RLCL retrigger enable/disable

#### 5.7.4.1.1 Overview

The RLCLs are normally used to supply essential spacecraft loads (for example decoders, receivers, reconfiguration modules within CDM), and as such they are supposed to provide continuously power to the load after start-up.

In case of a load malfunction implying an overload, they enter current limitation mode for the given trip-off time duration, switch off and attempt a re-start after a given time duration as explained in detail in chapter 5.3.

It could be practical or even necessary to stop the repeated switch-on sequence after an overload occurred, because of thermal and/or EMC reasons and also for possible adverse consequences on the satellite functionality or performance that could be triggered by anomalous behaviour of the failed load (for example, a repeated pattern of output signals from failed essential load triggering FDIR actions on the spacecraft).

It is therefore important to foresee the disabling of the RLCLs retrigger function that is normally enabled by default.

*[5.2.6.2.1.a] Telecommand section feature - Retrigger function*

*[5.2.6.3.1.a] Telecommand section feature - Retrigger ENABLE*

#### 5.7.4.1.2 Proposed alternatives

Due to the criticality and the possible extreme consequences of a spurious, or unwanted disabling of the RLCLs retrigger function (loss of an essential load not caused by failures), some measures should be put in place to be sure that

a. No on-board automatism can disable the retrigger function, being this command ensured only by ground commands;
*[5.2.6.4.1.a] Telecommand section- Retrigger DISABLE*

b. The RLCLs retrigger disable cannot be caused by noise, EMC, ESD, SEE or other unexpected reasons with exception of hardware failures.
*[5.2.16.1.1.a] Noise immunity - General*
*[5.2.16.2.1.a], [5.2.16.2.1.b] Noise immunity – Verification*
*[5.2.18.1.1.a] Noise immunity - RLCL spurious switch-off*
*[5.2.18.2.1.a] Noise immunity - RLCL spurious effects*

In particular, according to the requirement *[5.2.18.2.1.a.]*, some solid approach should be implemented to ensure the robustness "by design" of the RLCL against unexpected retrigger disable.

One design implementation possibility is described in Annex F.

The idea is to "force" the memory cell responsible for the RLCL retrigger status to deliver indeed an enabled signal as long as the number of RLCL retriggering cycles have not reached a minimum number of counts: in this way it is almost impossible for spurious glitches of any nature to disable the retrigger function, or not being able to recover the RLCL to ON conditions after a spurious switch-off thanks to the retrigger function itself.

Another possibility is to configure the retrigger disable circuit as a mono-stable feature: if an external command is received periodically within maximum time intervals, then the retrigger disable is maintained, on the contrary the retrigger restarts autonomously.

Note the relevant implementation is not in conflict with requirement *[5.2.6.4.1.a] Telecommand section feature - Retrigger DISABLE*: in fact a single command could be issued from ground to start an on board routine (or circuit) in charge to refresh the retrigger disable periodically and achieve the de-activation of the relevant RLCL.

## 5.7.5 Applicable rating/derating rules

One recurrent issue when designing and using power distribution by LCLs is the uncertainty over the correct application of rating/derating rules with respect to the switch stress (in terms of power and temperature) during an overload event.

**Prerequisites.**

According to ECSS-Q-ST-30-11 (clause 3.2, definition 3.2.3), "derating" is defined as follows:

*"Intentional reduction in a parameter rating of a component in order to increase its useful life in terms of drift and reliability"*

On the other side, circuits that are requested to operate in protection or fail-safe mode in order to prevent failure propagation are required to meet derating (ECSS-Q-ST-30-11, req. 5.3.2h):

*"Where components are required to operate in protection mode or in fail-safe mode in order to prevent failure propagation (e.g. short-circuit protection), the components concerned shall meet the derating requirements and application rules when performing the protection or fail-safe function under the worst failure case (i.e. highest stress applied to the components that can last throughout the mission)."*

The third useful information is given by ECSS-Q-ST-30-11, req. 5.4.2a and 5.4.2b:

*"a. If ratings are provided for transients or surge conditions, the same derating figures as for steady state equivalent parameters shall be used.*

*b. If ratings are not provided for transient or surge conditions, then it shall be assured that the transient or surge values are below the steady state specified maximum ratings."*

**Discussion.**

Since the LCL is in fail-safe or protection mode when an overload occurs, and this is an abnormal and transient situation by design, the requirements 5.3.2h, 5.4.2a and 5.4.2b of ECSS-Q-ST-30-11 are applicable.

In case of an anomaly (overload at user's side), the overload situation is only applied for a limited time, and there is **no need** to respect **static** derating rules under these conditions.

The correct interpretation is therefore that the conditions as per 5.4.2a or 5.4.2b of ECSS-Q-ST-30-11 should be applied, intending that the "derating" should be either applied to the specified rated transient or surge condition as per the load ratio defined in the standard for the corresponding steady state equivalent parameter (5.4.2a), or to respect the steady state specified maximum ratings if the information is not available on the applicable switch requirement specification (5.4.2b).

More specifically, during the **worst case** overload transient, req.5.4.2a is typically applied to the switch power application (see relevant maximum safe operating area, for which an example is given in Figure 5-33), while req. 5.4.2b is applied to the switch junction temperature.

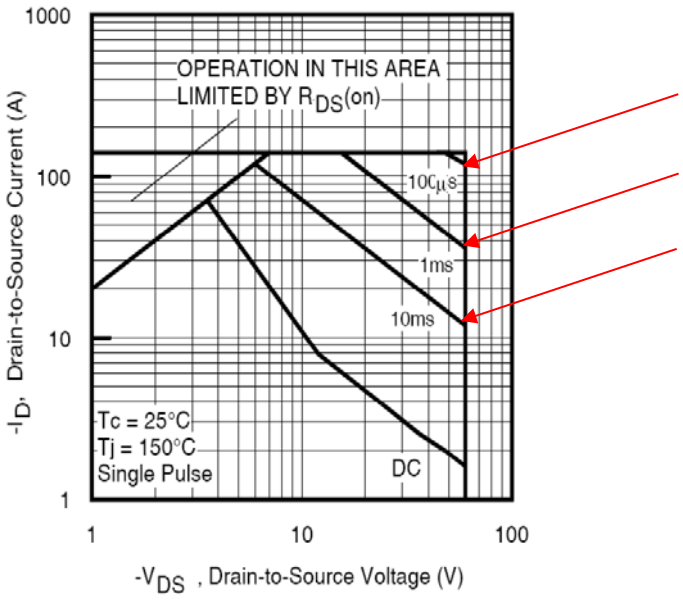



**Figure 5-33: Maximum safe operating area, example (red arrows indicate power limit in transient application)**

Normally, for space-grade MFETs switches, the rated junction temperature is specified to 150 degC, while the derating rule, to be applied on static or steady-state conditions, requires to comply to 110 degC or Tjmax – 40 degC , whichever is lower (see ECSS-Q-ST-30-11, clause 6.29.2).

Note that the compliance to the rated junction temperature during the transient overload case should be guaranteed in any case with **some margin** under **worst case** conditions, taking into account all uncertainties on switch temperature evaluation.

*[5.2.3.4.1.a] Current limitation section - Current limitation, LCL rating*

When charging load input filters, the LCL switch should meet derating limits, especially when the LCL ON/OFF cycles are very frequent or repeated with high duty cycle within the satellite lifetime and for additional reliability.

Note in any case that that during load input filter charging the temperature is lower than the rating limit because during charge the load voltage is not permanently at 0V and the load Input Filter Charge time is necessary smaller than the min trip-off time.

In case of repetitive overload, following the logic explained in this chapter, it should be clear which rule to apply.

If the repetition of overload is within **limited** time duration after a failure, rating can be applied.

If in the contrary the overload repetition is **not** within limited time duration after a failure, derating should be applied.

*[5.2.10.1.1.a] Repetitive overload - LCL case*

*[5.2.10.2.1.a] Repetitive overload - RLCL case*

Consequently, for RLCLs, the relevant components stay under derating when the RLCL is in limitation mode.

*[5.2.3.5.1.a] Current limitation section - Current limitation - RLCL derating*

### 5.7.6 Load input filter damping

The damping of input filter of units connected to the spacecraft power bus is highly recommended to avoid any stability issues or power bus oscillations when the unit is submitted to voltage ripple in the range of the resonant frequency of input filter, typically in the range 1 kHz to tens of kHz.

Although the subject of input filter damping is not linked with the performances of the LCL function, it has been judged important to formalise some recommendations, this being part of the power interface in the distribution function.

The following recommendations and best practices should be followed:

a. Unit input filters inserted in the power line should be properly damped.

b. The damping should be calculated in the worst case, considering at least (but not limited to):

   1. Input voltage range,
   2. Unit power consumption,
   3. Source impedance (including or excluding LISN),
   4. Components incertitude,
   5. Load impedance (regulators, PWM converters…).

c. As a good practice, the damping factor $\zeta$ should not be lower than 0,4 (equivalent 2nd order filter) in flight conditions; in ground condition (test conditions, wider input voltage range…) the damping factor should not be lower than 0,3.

d. These recommendations should apply for differential and common mode filters.

These recommendations are justified as follows:

a. $\zeta = 0,4$ (equivalent 2nd order system) corresponds to:

   1. 36% amplification in frequency response
   2. 25% overshoot in step response
   3. a control loop with 40° phase margin.

b. Damping factor of 0,4 is a still poor performance but the experience shows that most input filters of high consuming units are underdamped.
The main reason is that increasing the damping requires to select a the "damping" capacitor much bigger that the useful capacitor.
In addition, power DC/DC converters have a negative load impedance which degrades the damping. Putting strong requirements (like 0,7) would be not realistic. The figure of 0,4 is an acceptable compromise.

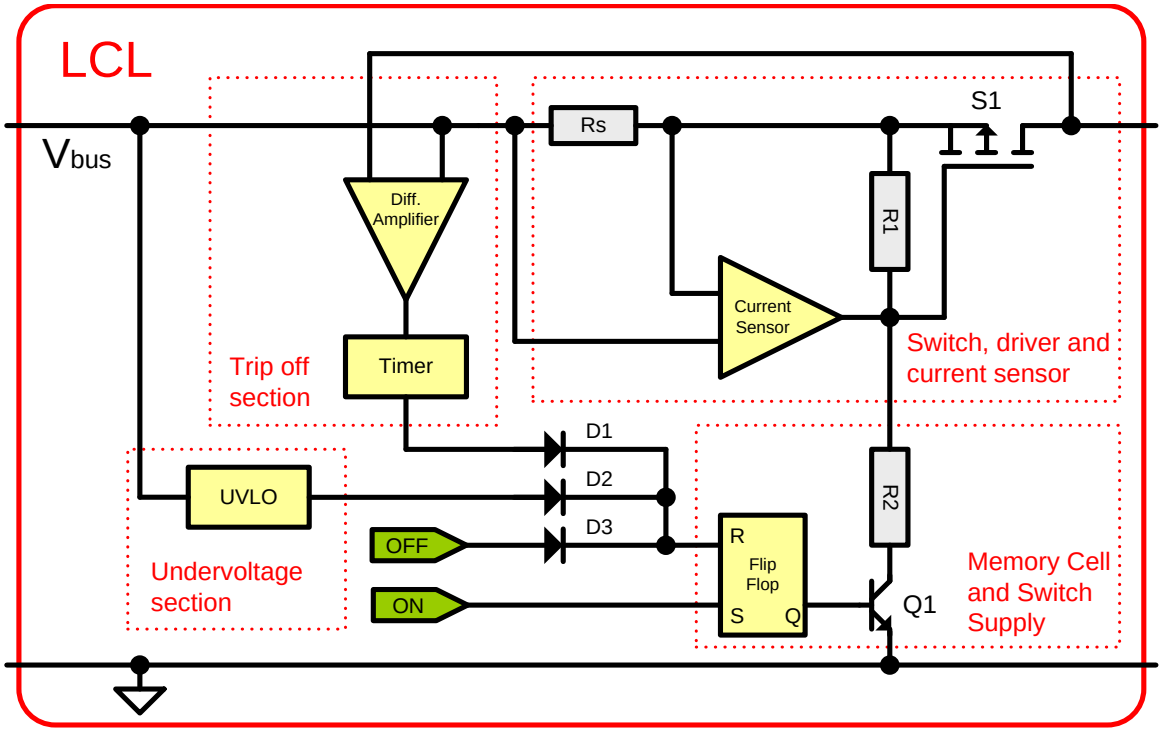
c. In ground conditions the input voltage can be lower than the min spec. value (soft start of the EGSE).

d. For high power units, designers often prefer large capacitors and small inductors in LC filters for keeping the efficiency high. Values for L can be as low as some μH. The line inductance, modelled by the LISN is not negligible anymore with respect to the LC components, and it can change significantly the damping and the resonant frequency.

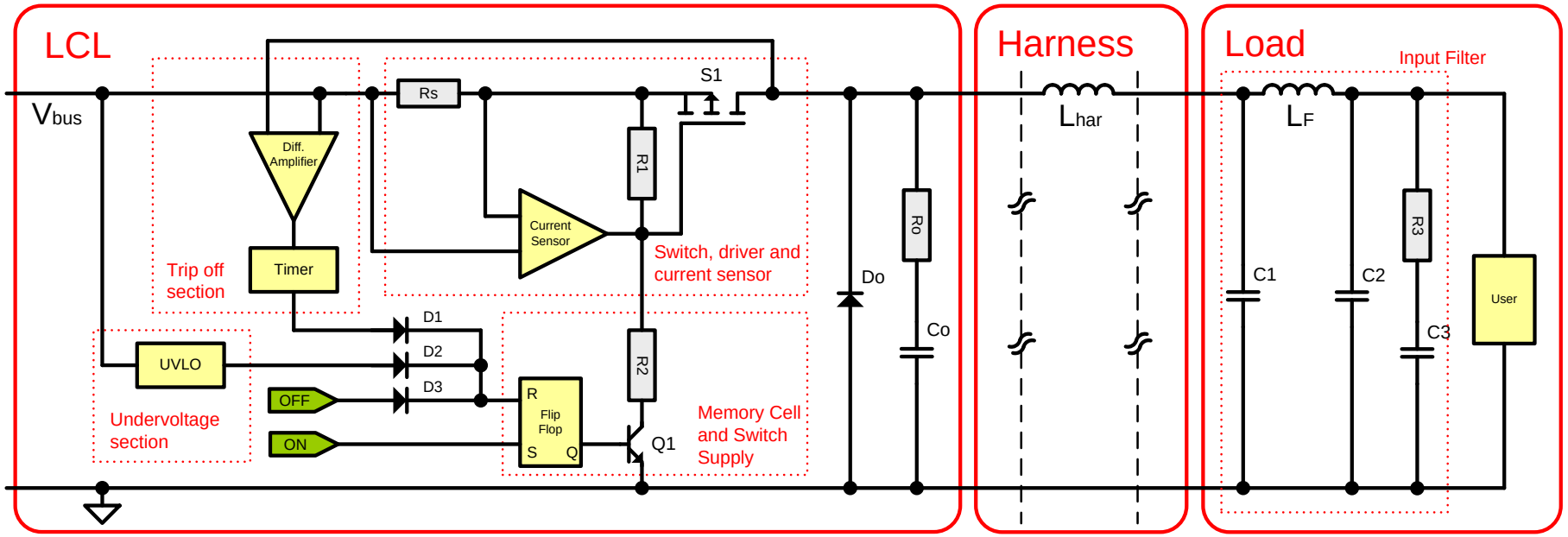
e. Load impedance is roughly:

   1. A current generator (infinite resistance) for a linear regulator.
   2. A negative resistance for a switching converter.
   This negative resistance is worse when its absolute value is low.
   This occurs at low input voltage and at max load current.
   3. Damping components should be sized to withstand AC voltage/current conditions experienced in orbit and on ground (EMC tests).
   Damping components stress is generally very low in normal operation (no noise).
   However, EMC tests and especially the 1Vrms injection, can stress the damping network.
   This is particularly true if the damping factor is low (amplification of the ripple).
   4. The common mode filter is small and has a high resonant frequency (10's or 100's of KHz) and may interact with the switching of its harmonics, and also generate ringing on the transitions. So, there is some interest to damp it.

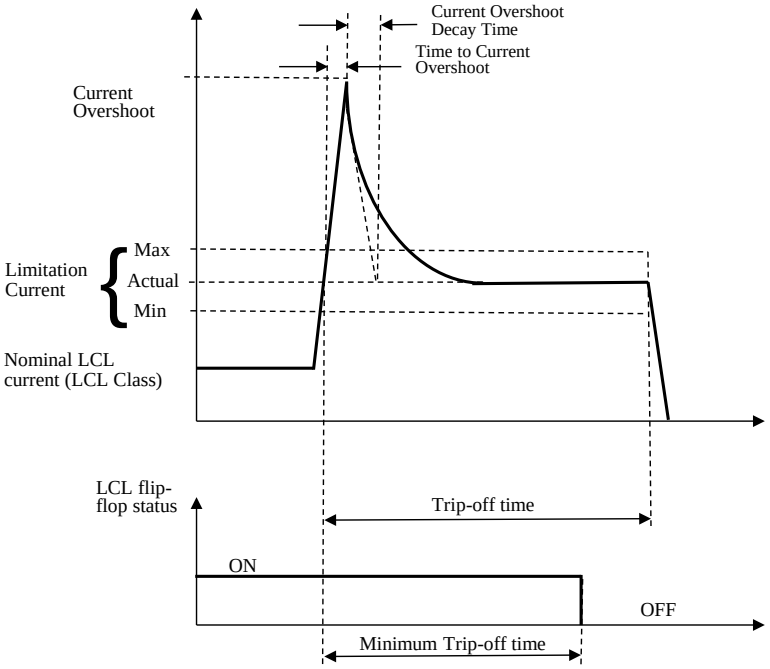
# Annex A
# LCL generic block diagram



# Annex B
# Generic Power Distribution diagram by LCLs



# Annex C
# LCL timing diagram



# Annex D
# Dragging effect

The current delivered by the LCL in limitation mode is known to depend on the impedance of the load attached at LCL output.

For a zero load impedance (pure short-circuit), the LCL output current, called $i_o$, is equal to the intended limitation current, called $i_{source}$. For any load impedance $Z_L$, the LCL output current is given (in linear condition) by the next formula, where $Z_{SC}$ is the output impedance of the LCL (Annex H).

$$\frac{i_o}{i_{source}} = \frac{1}{1+\frac{Z_L}{Z_{SC}}} \qquad [D\text{-}1]$$

The LCL current control loop design is meant for reaching a steady-state current limitation being DC value of the intended limitation current $i_{source}$, whatever the (steady-state) LCL output voltage is.

Such a property is verified if $Z_{SC}$ tends to infinity when the frequency tends to zero. Accordingly, the LCL output impedance typically features a capacitive profile beneath a threshold frequency, as illustrated on Figure D-1.

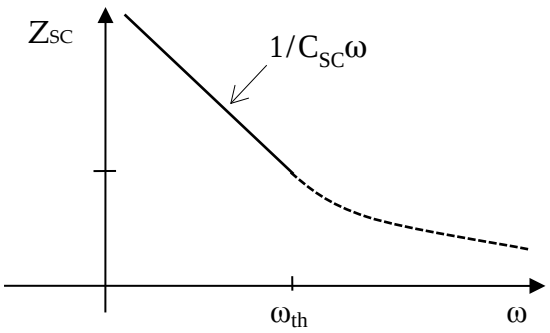



**Figure D-1: Typical LCL output impedance profile**

Let us concentrate on frequencies below the above-mentioned threshold, and assume that the load impedance is a capacitance $C_L$. This concerns typically the charge of a payload input filter (with serial inductance negligible below the threshold frequency). Eq. [D-1] could now be rewritten as follows.

$$\frac{i_o}{i_{source}} = \frac{1}{1+\frac{C_{SC}}{C_L}} \quad [D\text{-}2]$$

Obviously, if $C_L$ is in the same order of magnitude (or smaller than) $C_{SC}$, the LCL output current $i_o$, i.e. the output capacitance charge current, is a fraction of the expected limitation current $i_{source}$. This is the dragging effect.

**The dragging effect is defined as the drift of the actual LCL output current from the expected limitation current because of the non-zero load impedance.**

With reference to Eq. [D-1], the dragging effect is negligible, in a given frequency window, on the next condition.

$$\left|\frac{Z_L}{Z_{SC}}\right| << 1 \quad [D\text{-}3]$$

The dragging effect is typically significant with load having impedance increasing with decreasing frequency, i.e. with capacitive load, in which case the condition for negligible dragging effect could be rewritten with reference to Eq. [D-2]as follows:

$$\frac{C_{SC}}{C_L} << 1 \quad [D\text{-}4]$$

The dragging effect is significant on the next condition:

$$\frac{C_{SC}}{C_L} >> 1 \quad [D\text{-}5]$$

Hence, the dragging effect is all the more likely to happen that the load capacitance is small.

In case of significant dragging effect, the output capacitance charge no longer occurs at constant current but at constant dV/dt. Indeed, dividing the load capacitance by 2 entails dividing the LCL output current by 2.

As such, the dragging effect is not problematic as long as it is negligible for the maximum load capacitance. The maximum load capacitance is indeed driven by the allowable fraction of the LCL trip-off time needed to charge the load filter capacitance up to the bus voltage. Allowing a significant dragging effect in such case could therefore result in the trip-off time being reached when the capacitance is charged because the actual charge current $i_o$ would be lower than the intended limitation called $i_{source}$.

To assess the dragging effect on a given LCL design (with capacitive output impedance at low frequency), it is therefore necessary and sufficient to check the next condition for the maximum load capacitance (for a more precise assessment, refer to Eq. [D-2]).

$$\frac{C_{SC}}{C_{L\,max}} << 1 \quad [D\text{-}6]$$

An intuitive explanation could be given for the lagging effect with reference to the simple LCL design according to Figure D-2

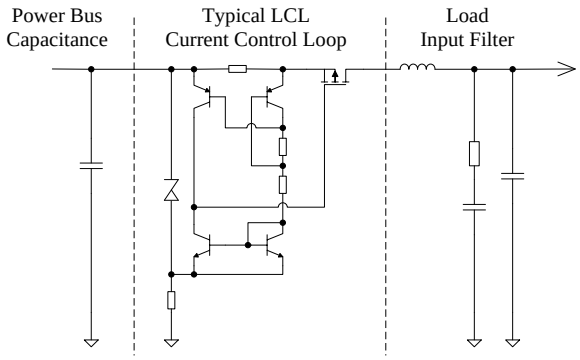



**Figure D-2:Typical LCL design**

When charging the load filter capacitance, a constant dV/dt is expected at LCL output. Consider now the drain to gate impedance (the drain to source impedance plays also a role but less critical). That impedance being typically a capacitance, the dV/dt signal at the drain results in current injection onto the gate, which generates a bias in the measurement of the LCL current by the current mirror onto the shunt. Accordingly, the charge current of the load filter settles to a lower value than the one applicable a constant output voltage (short-circuit case).

Note finally that the dragging effect is amplified by any (R)C filter added across drain and gate of the MOSFET for LCL current control loop stabilisation purpose.

# Annex E
# LCL Transient Mode Stability Verification

A critical test for LCL stability is when an LCL is switched on into an input filter that acts like an inductive load while the LCL has to stabilize the current at its current limitation level.

A very useful test is therefore to measure the LCL output voltage and current when the LCL is commanded on into an "inductive" input filter with sufficient capacitance to be charged to ensure the LCL enters and stay in limitation for sufficient time, up to e.g. 50% of its trip-off time.

Such transient mode verification has the advantage to pass through all practical values of node voltages and also verifies the large signal performance. Another reason to focus on the switch-on transition is that switching ON/OFF of equipment is a nominal performance of the LCL while any kind of current regulation in case of an equipment overload is only in case of a failure. For the switch-on transient verification the following simple test circuit can be applied (Figure E-1):

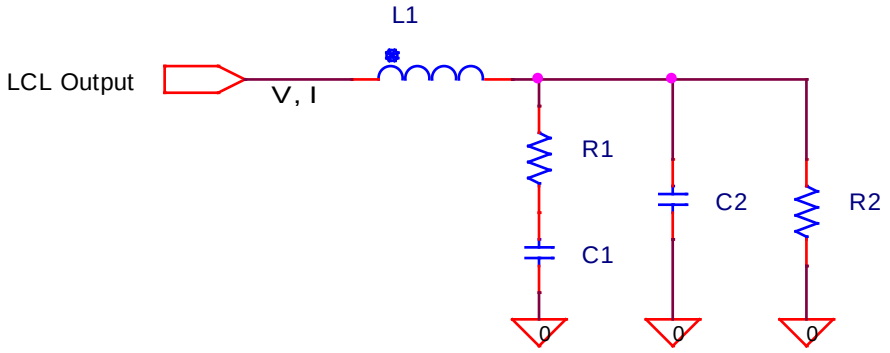



**Figure E-1: Test circuit**

The basic idea of the test circuit design is to have a well damped input filter that due to capacitive loading requires the LCL to enter current limitation while the LCL current regulation loop sees it as an inductive element.

The component values can be determined in the following way:

- C1 + C2 < 100 % max load capacitance as per ECSS-E-ST-20-20 table 3.1 and 3.2
- C1 = ~2 x C2
- L1 = ~10 µH to 300 µH (e.g. to be applied in 3 steps like 10 µH, 50 µH, 300 µH))
- R1 = to ensure proper damping of the resonance effect of L1 and C2 (max amplitude at resonance peak < 6dB)
- R2 >> Vbus/Ilim (for discharge after switch-off)

It is of great importance to ensure that the applied inductors can maintain full inductance value at maximum applied class current to avoid inductor saturation. The recommended three steps of inductor values are selected based on experience with criticality of applied LCL design.

The results of the test can look as shown in the following Figure E-2, with plots of LCL output voltage and current.

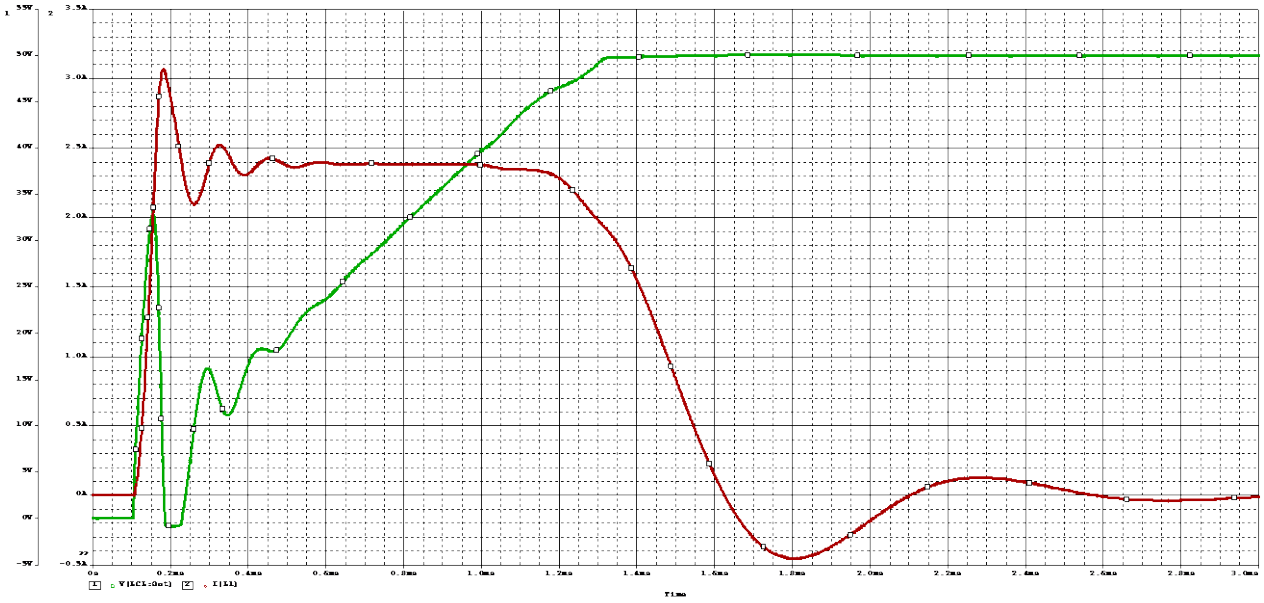


**Figure E-2: Possible test results**

Applied test example: 50 volt class 2A LCL switch-on into: L= 500 µH, C1=40 µF, C2=10 µF, R1=5R

As the LCL has to regulate the current into an inductive element the output voltage rises fast to accelerate the current up to limitation and hereafter settle to follow the voltage rise of the capacitors. The related current regulation stability can be assessed from the LCL output current waveform.

# Annex F
# Reliable RLCL retrigger disable approach

An approach is proposed, as shown in Figure 1, for a reliable RLCL retrigger disable.

Figure F-1 shows the time diagram of the RLCL output current (Iout) and voltage (Vout), the state of the LCL function in the RLCL ("LCL" state), together with three conditions (condition 1,2,3) determining if the RLCL retrigger disable can be performed or not.

The RLCL retrigger disable cannot be performed if any of the three conditions is true:

- **Condition 1**: Vout higher than a specific threshold Vth,
- **Condition 2**: number of retrigger cycles less or equal than a predefined number N,
- **Condition 3**: no sufficient delay time (Delay) passed from the latest ON-> OFF edge of the state of the LCL function("LCL" state).

To be effective against spurious de-activation (by noise, ESD, SEE or whatever else), the de-activation of the RLCL retrigger disable function under the conditions 1,2,3 should be achieved by overriding or making the relevant memory cell ineffective and not just by disabling the relevant command.

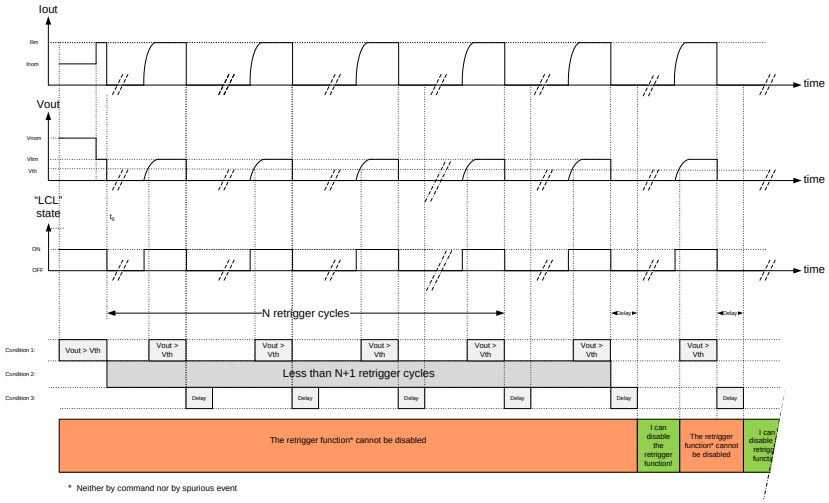



**Figure F-1 : Reliable RLCL retrigger disable approach**

**Implementation**

**Conditions 1** and **3** are easily achieved, it is a matter to "block" the retriggerable EN/DIS memory cell in a way that the proper triggering enable signal is in any case active if Vout > Vth (including the required delay): for example, ensure that the re-triggering enable signal is active low and shunting the supply voltage to the relevant retriggerable EN/DIS memory cell if Vout > Vth (including the required delay).

**Condition 2** can be achieved by "blocking" the retriggerable EN/DIS memory cell in a way that the proper triggering enable signal is in any case active if count of n events is not elapsed. The counting can be made by checking Vout /Vth crossings. The memory cell "block" can be achieved by indicated above in the example for conditions 1 and 3.

**Advantages**

- No cross –strapping of M&R chains.
- It allows to disable the retrigger function (after a certain number of retrigger cycles, with a command to be sent when the RLCL output is low – easy to do if the ratio RLCL retrigger period / trip-off time is large – at the moment the ratio is around 20s/20ms=1000).
- Immunity to spurious de-activation of retrigger function both when RLCL output is nominal (impossible by design) and after an overload or spurious de-activation of "LCL" memory cell (for n retrigger cycles).
- Same (single) glitch cannot cause the spurious de-activation of "LCL" memory cell and the retriggerable EN/DIS memory cell (reason for the introduction of "delay").
- Relatively easy to implement.

# Annex G
# APEC 2013 paper "MOSFET Gate Open Failure Analysis in Power Electronics"

## MOSFET Gate Open Failure Analysis In Power Electronics

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***Abstract*—The compliance to the fault tolerant operation requirement for power electronics is commonly assessed with reference to fault models applicable at component level. For switching MOSFET, the fault models include the short-circuit and open-circuit failures, implicitly assuming that the Gate open failure is equivalent to a switch open or short failure. MOSFET Gate open failure, also called floating Gate failure, may however entail a Drain to Source channel conduction with non-zero impedance and the subsequent power dissipation in the failed device may prove critical because of the thermal failure propagation risk. The present paper is dedicated to that question. It is shown that a power MOSFET with floating Gate is driven by leakage current from whatever initial conduction status either into a steady-state dissipative status or into run-away due to thermal instability. The analysis is confirmed by practical tests. As a conclusion, provisions to mitigate the MOSFET Gate open failure are proposed to be implemented at MOSFET level and/or at converter design level.**

### I. Introduction

Fault tolerant operation of power converters is generic for space, aeronautical and military applications and is currently gaining traction for commercial applications [1] [2]. In this context, many works are dedicated to power switch failure mitigation, however restraining their attention for power switches to the open or short failure [3] to [11].

Fewer works have been dedicated to the floating Gate transistor fault. Attention has initially been paid to such failure for low power integrated circuit [12] to [14]. In [15], a design provision based on redundant structures is proposed such that the bond wire lift-off of power semiconductors does not result in an uncontrolled failure mode. In [16], the issue of Gate open circuit failures is illustrated by SEM (Scanning Electron Microscope) picture and a methodology is proposed to analyse such failed parts.

These works concentrate onto the analysis of failed parts. They however leave open the question to which extent the Gate open failure may yield thermal dissipation, making it difficult to assess the risk of thermal failure propagation.

The present work is dedicated to that question. With reference to [17] and [18], it is examined in which conditions the floating Gate MOSFET is exposed to thermal instability yielding run-away. When these conditions are not met, floating Gate MOSFET behaviour is demonstrated to be driven into steady-state dissipative status.

The paper is organized as follows.

Chapter II addresses the thermal run-away issue. It is shown that the temperature sensitivity of the MOSFET transfer characteristics plays a critical role in the thermal instability behaviour depending whether the MOSFET is connected to a voltage source or to a current source. Chapter III is then dedicated to the Gate open failure cases which do not end up in thermal run-away. A theoretical analysis corroborated by experimental results demonstrates that the power dissipation level converges to some steady-state value driven by the Gate leakage. As a synthesis, possible die behaviour scenarios which ensue the Gate open failure are sketched in Chapter IV, whereas provisions to mitigate the consequences of the failure are considered in Chapter V.

### II. MOSFET Thermal Instability

#### A. *Transfer Characteristics*

The transfer characteristics of a MOSFET designate its Gate voltage to Drain current diagram. For power switching MOSFET, we know that the optimization of the transconductance and of the ON serial resistance result in a positive temperature coefficient of the transfer characteristics in a relatively large current range [18]. Accordingly, power MOSFET's typically present transfer characteristics as shown on Fig. 1 (both axes linear).

The transfer characteristics diagram is drawn at given Drain to Source voltage and temperatures. It features the threshold voltage $V_{th}$ and the zero temperature coefficient point ($V_0$, $I_0$). The temperature coefficient of the threshold voltage is negative. Note that the transfer characteristics also increase with the Drain voltage, i.e. the coefficient linking a delta Drain voltage to a delta Drain current is positive.

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# Annex H
# ESPC 2014 paper “Approach to design for stability a system comprising a non-ideal current source and a generic load”

## APPROACH TO DESIGN FOR STABILITY A SYSTEM COMPRISING A NON-IDEAL CURRENT SOURCE AND A GENERIC LOAD

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**ABSTRACT**

A systematic approach is presented, allowing the verification of the stability of a system comprising a non-ideal current source and a generic load. The proposed approach is based on a three-step verification method, and on the check of the stability of the system by application of source-load interface requirements control. It allows to verify that the combination of the non-ideal current source connected to specific loads results in a stable system without the need of performing intrusive verifications (e.g. accessing and opening the control loop for each load case). The approach seems specifically useful in relation to power distribution systems based on latching or fold-back current limiters, which are widely used in European space power industry.

**1. INTRODUCTION**

The design of the stability of an electrical system comprising a non-ideal current source and a generic load might become rather difficult when the possible dynamic load characteristics can vary over a wide range.

The main issue is that the stability of the non-ideal current source depends heavily on the nature of the load. A typical case is the design of a latching current limiter when a number of possible loads are considered: it soon appears very difficult to size for stability of the current limiter loop when the envelope of the possible loads is taken into account (including failure scenarios, harness contribution, common an differential mode filter design options, etc).

The proposed approach is based on a three-step verification method, and on the check of the system stability by application of source-load interface requirements control. It seems to have an undoubted advantage over the study of the current loop stability with the conventional Bode or Nyquist approach applied for each load case, especially because the load nature might not be known in detail to the designer of the current source from the beginning, and it might be difficult, if not impossible, to practically run the analysis for all load envelope cases.

**2. ASSUMPTIONS**

The proposed approach should be valid in any case when small signal stability has a sense, e.g. if one can linearize the system under analysis around a given operational point. It is anyhow necessary to run the approach for a number of possible operating points, if the linearised system (the relevant poles and zeroes of the transfer functions of interest) depends from the selected operating point. For example, if the current source is based on the current provided at the drain of a power MOSFET, it is known that the relevant trans-conductance DC gain, and gate to source, source to drain, and gate to drain capacitances are function of the DC operating point (current and voltage). As a consequence, the control loop built around the power MOSFET has to be studied for a number of applicable operating points to be sure that stability is ensured for each one of them.

**3. DESCRIPTION OF PROPOSED APPROACH**

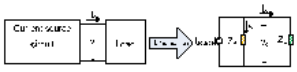

*Figure 1. Linearising the non-ideal current source*

First of all, let us identify all DC currents and voltages with capital letters (e.g. $I_0$, $I_1$, $V_1$, $V_2$, etc) while variations around the operating point are identified with small cap letters (e.g. $i_0$, $i_1$, $v_1$, $v_2$, etc).

Let us give a look to Fig.1.

The (linearised!) current source circuit is described with a Norton equivalent network, comprising an ideal current source ($i_{source}$) with a impedance ($Z_{dc}$) in parallel. It is possible in any case to describe a linear (or linearised network) in this way, also if a relevant control loop is present and/or if dependent voltage or current sources are present in the current source circuit.

Note that the $i_{source}$ is not related to the DC current source $I_0$: according to the Mayer-Norton's theorem ([2], [3]), the current source $i_{source}$ represents the current variations given by the relevant circuit in short-circuit conditions and the impedance $Z_{dc}$ represents the differential impedance read at the terminals of the current source circuit when all independent voltage or

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Approach to design for stability.pdf

# Annex I
# ESPC 2014 paper “LCL current control loop stability design”

## LCL CURRENT CONTROL LOOP STABILITY DESIGN

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**ABSTRACT**

Latching Current Limiters include a control loop meant at limiting the current in case of downstream failure. Such current control loop consists typically of a simple proportional feedback gain from a current measurement shunt resistance and may result in very limited phase margin for specified operating conditions. The present paper investigates the combination of a proportional and derivative feedback to mitigate the lack of stability margin, providing a comprehensive overview on designing Latching Current Limiters for stability. For illustration purpose, a LCL based on radiation hardened ITAR free components is considered. A breadboard has been manufactured and the reported phase margin measurements demonstrate performances in line with the analytic results.

### 1. INTRODUCTION

The electrical power within a spacecraft is distributed to the on board users by means of electrical lines drawn from the centralized power bus. Such distribution lines must be protected against overconsumption or short-circuit to cope with possible failures at user level. For earth observation or scientific spacecraft, the protection is typically based on so-called LCL (Latching Current Limiter) including a serial power PMOS in the distribution line with the capability to actively limit the current to a given reference for a limited time period and to subsequently switch OFF the power line. Originally designated as SSPC (Solid State Power Controller), LCL have been introduced in the early eighties to cope with the drawbacks of protection based on fuses and electromechanical relays, in particular the lack of inrush current control combined with the limited current switching capabilities of relay [1]. So far however, few references are found in the bibliography dealing with current control stability of LCL or SSPC, presumably owing to issues related to the non-ideal behaviour of the MOSFET used as actuator. In [2], the design of a SSPC in hybrid technology is reported mainly dealing with temperature elevation associated to the linear operation of the MOSFET. The question of the closed loop stability is raised in [3] underlining that it depends on the impedance of the bus user, especially when it is inductive, and recommending to validate the control performances of the SSPC with the actual load. Finally, in [4], the stability of the current loop is managed by an impedance network connected at the output of the LCL. While a number of test results with non-resistive load are reported, [4] remains nonetheless mainly empirical. The objective of the present paper is to provide an analytical tool supporting the understanding of the stability issue. The concerned LCL model is identified in § 2, being one of the typical designs used so far in ESA spacecraft. The model of the MOSFET used in the LCL is detailed in § 3, covering both static and dynamic parameters. The theoretical open loop gain of the LCL current control is presented accordingly in § 4, and the stakes of proportional and derivative feedback gains are discussed in § 5 and § 6 respectively. In § 7, the stability rationale previously introduced leads to the LCL output impedance diagram drawn as a function of frequency. It is shown that such a frequency plot allows dealing with the compatibility issue between LCL and downstream impedance in terms of stability. § 8 embodies the analytical study within an ITAR free radiation hardened design for which the closed loop stability is verified by simulations and measurements. The measurements performed on a breadboard are reported in § 9 and demonstrate performances in line with theoretical results and simulations. Conclusions are finally drawn in § 10.

### 2. LCL MODEL

The basic LCL model taken into account for the analytical study is presented on Fig. 1, restricted to the current limitation loop.

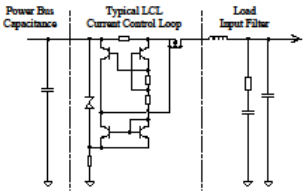


*Figure 1 Typical LCL current control loop*

Its topology is the one of LCL’s currently used on a number of ESA spacecraft for earth observation or scientific experiments. It consists in a closed loop

LCL Current Control Loop Stability Design.p

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