Signal and Bus operation Description

1. Vcc — +5 volt supply
   GND — Ground reference and negative supply

2. Device Control Signals

A1-A3	These three inputs select one of the 8 bits in the state register to be updated.
AØ	The data input to the state bit selected by A1-A3. The state to which the addressed state bit is set by an operation will select the register to be accessed by that operation. Also the /READ input. A low on this input enables the IWM to send the register selected by the state onto the data bus.
DØ-D7	The bidirectional data bus .
/DEV	Active low device enable. The falling edge of /DEV latches information on AØ-A3. The rising edge of the logical function (Q3 OR /DEV) qualifies write register data.
FCLK	Clock input for the serial data logic; either 7 or 8 MHz.
Q3	2.Ø Mhz clock input used to qualify the timing of the serial data being written out in the synchronous mode.
/RESET	Active low system reset input. When asserted, this signal places all IWM outputs in their inactive state, and sets the state and the modes to their defaults.

3. Inputs (2)

RDDATA	The serial data input. The falling transition of each pulse is synchronized by the IWM.
SENSE	An input to the IWM that can be polled via the status register.

4. Outputs (8)

WRDATA	The serial data output. A transition occurs on this output for each one bit.
/ENBL1 , /ENBL2	Programmable buffered output lines. No more than one enable may be low at any time. If an enable is low than Motor-On is true. If the 1-second on board timer is enabled then the selected one will stay low for about 1 second after it is programmed high.
/WRREQ	This signal is a programmable buffered output line.
PHASEØ-3	These are programmable output lines. A true TTL logic "1" (2.4 volts) can be maintained even while driving two darlington inputs in parallel.