

Lab 02 - First Verilog

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In this lab, you've learned how to do an initial and simple design in Verilog to learn the Vivado tooling and process involved in RTL/FPGA design.

Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

Lab Summary

In this lab, we learned how to create a Vivado project and add test.v, top.v, and constraint.xdc files to connect a switch to an led. We wrote basic code. We learned how to simulate and look at the simulation waveform. We ran the synthesis and implementation to place and route the connections. We generated a bitstream to make the circuit on the FPGA. Then we connected the Basys3 to see a physical representation of the code.

Lab Questions

1 - Describe the stages of building a Verilog project in Vivado.

First, download the files needed for the project and add them to Vivado. Then find the board that is used. Make sure the project summary is correct. Write the code following assignment instructions. Run Behavioral Simulation to check that everything is working as expected and to debug. Once it runs with no errors, click Run Synthesis to create the netlist. Then Run Implementation to connect the hardware specifics. Then Generate Bitstream to connect various parts of the FPGA. Then Open Hardware Manager to connect to the Basys3 to see a physical representation of the code.

2 - What is the value in looking at the elaborated design schematic?

Looking at the elaborated design schematic allows you to see how the code is connecting different components. You can visually see what is happening in the FPGA.

3 - Why should we simulate our designs frequently? What does the simulation do?

We should simulate our designs because it can show where something is wrong and needs to be fixed. You should do it frequently because if you make an error early on, it can be extremely difficult to find later. The simulation shows what is actually happening in the code.

Code Submission

Upload a .zip of all your code or a public repository on GitHub.

<https://github.com/elawler0575/ECE-230L-Team01/tree/main/Lab2>