Packet-Based Router Verification Using UVM

1. Introduction

Routers are key components in communication systems, directing packets to appropriate destinations. A packet-based router typically includes inputs like address and payload, and multiple output channels. Verifying such systems ensures reliable packet delivery under different traffic scenarios. This project uses UVM to verify the functionality of a packet router.

2. Objective

To verify a SystemVerilog-based packet router using Universal Verification Methodology (UVM), validating its routing logic, error detection, and data integrity under randomized input conditions.

3. Router Interface and Design

The router has an 8-bit input (`data_in`), a packet validation signal (`pkt_valid`), and 3 output channels, each with data and valid flags. The address encoded in the data determines the output path.

The router_if interface encapsulates all communication ports used in testbench connectivity.

4. Verification Methodology

UVM (Universal Verification Methodology) offers a structured approach to functional verification. The testbench consists of the following components:

- `router_xtn`: sequence item defining address, length, and payload
- `router_seq`: generates randomized sequences of packets
- `router_driver`: applies sequences to the DUT via the interface
- `router_monitor`: samples transactions and forwards them
- `router_scoreboard`: checks correctness of output
- `router_coverage`: tracks coverage on addresses and lengths
- `router_agent`, `router_env`, and `router_test`: integrate all components and start the test

A virtual interface connects the testbench components to the DUT.

5. Results

The router handled random packet sequences and routed them based on address. Functional coverage confirmed all combinations of address and length were exercised.

6. Conclusion

The router was successfully verified using UVM, demonstrating correct routing, packet delivery, and control signal generation across all valid scenarios.

7. Tools Used

- SystemVerilog
- UVM Library
- QuestaSim/VCS
- Makefile Scripts for simulation automation

8. References

1. UVM Class Reference Manual
2. SystemVerilog IEEE 1800 Standard
3. Online tutorials and router design guides